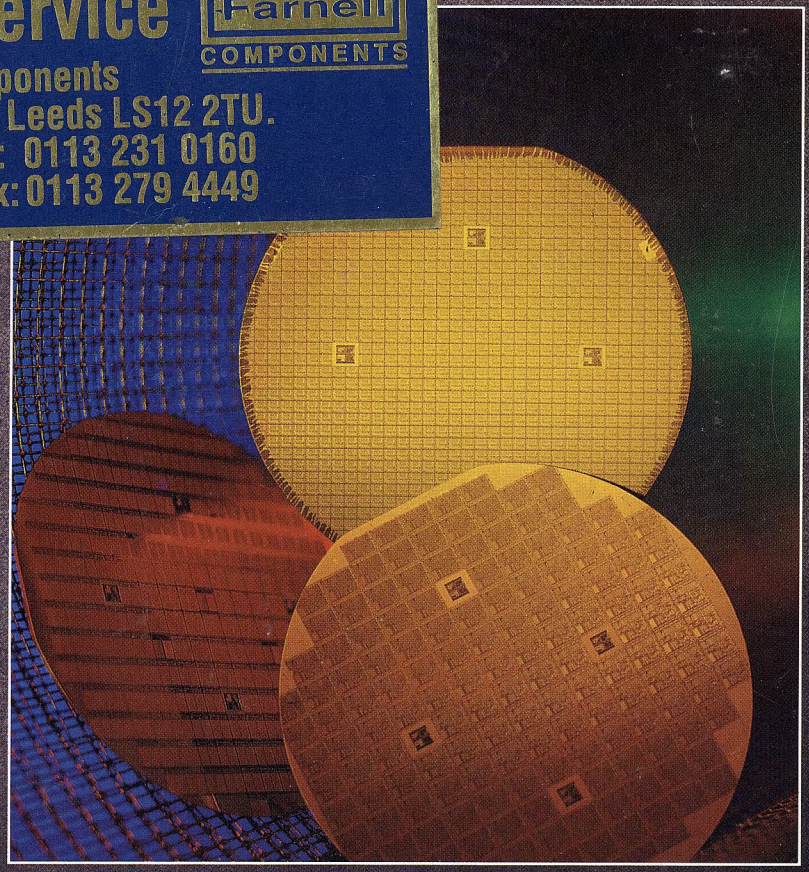

Data Acquisition

1994

HARRIS SEMICONDUCTOR

New Data Acquisition Products

A/D CONVERTERS

HI5810
12-BIT, 40mW SAMPLING A/D CONVERTER

(Page 5-52)

- CONVERSION TIME 10µs
- INL ..... ±2.0 LSB
- DNL ..... ±2.0 LSB
- 5.0V POWER SUPPLY
- LOW COST

HI5813
12-BIT, 3.3V SAMPLING A/D CONVERTER

(Page 5-79)

- CONVERSION TIME 30µs
- INL ..... ±2.5 LSB
- DNL ..... ±2.0 LSB
- POWER CONSUMPTION 3.3mW
- LOW COST

HI1276
8-BIT, 500MSPS A/D CONVERTER

(Page 6-54)

- INL ..... ±0.7 LSB
- DNL ..... ±0.5 LSB
- POWER CONSUMPTION 2.8W
- SINAD (100MHz) 37dB
- ECL LOGIC COMPATIBLE

HI1166
8-BIT, 250MSPS A/D CONVERTER

(Page 6-43)

- INL ..... ±0.5 LSB
- DNL ..... ±0.5 LSB
- POWER CONSUMPTION 1.4W
- SINAD (60MHz) 37dB
- ECL LOGIC COMPATIBLE

HI1175
8-BIT VIDEO A/D CONVERTER

(Page 7-3)

- SAMPLING RATE 20MSPS
- INL ..... ±1.3 LSB
- DNL ..... ±0.5 LSB
- POWER CONSUMPTION 60mW
- SINAD (3.85MHz) 43dB
- TTL LOGIC COMPATIBLE

HI1176
8-BIT VIDEO A/D CONVERTER

(Page 7-12)

- SAMPLING RATE 20MSPS
- INL ..... ±1.3 LSB
- DNL ..... ±0.5 LSB
- POWER CONSUMPTION 60mW
- SINAD (3.85MHz) 43dB
- TTL LOGIC COMPATIBLE
- INTERNAL SYNC CLAMP

HI7190
24-BIT SIGMA-DELTA A/D CONVERTER

(Page 4-3)

- THROUGHPUT 2kHz-10Hz
- INL ..... 0.0007% FSR
- POWER CONSUMPTION 30mW
- INTERNAL PGIA
- 20 PIN PACKAGES AVAILABLE
- SERIAL BUS INTERFACE

New Data Acquisition Products (Continued)

A/D CONVERTERS

HI1396
8-BIT, 125MSPS A/D CONVERTER

(Page 6-72)

- INL ..... ±0.5 LSB
- DNL ..... ±0.5 LSB
- SINAD (32MHz) 40dB
- POWER CONSUMPTION 870mW
- ECL LOGIC COMPATIBLE

HI1386
8-BIT, 75MSPS A/D CONVERTER

(Page 6-64)

- INL ..... ±0.5 LSB
- DNL ..... ±0.5 LSB
- SINAD 19MHz) 40dB
- POWER CONSUMPTION 580mW
- ECL LOGIC COMPATIBLE

HI5800
12-BIT 3MSPS SAMPLING A/D CONVERTER

(Page 7-23)

- SAMPLE RATE 3MSPS
- INL ..... ±0.7 LSB
- DNL ..... ±0.5 LSB
- POWER CONSUMPTION 1.8W
- INTERNAL SAMPLE AND HOLD AND REFERENCE

D/A CONVERTERS

HI20201
10-BIT 160MSPS D/A CONVERTER

(Page 8-65)

- THROUGHPUT 160MHz
- INL ..... ±1.0 LSB
- DNL ..... ±0.5 LSB
- POWER CONSUMPTION 420mW
- ECL COMPATIBLE INPUTS

HI20203
8-BIT 160MSPS D/A CONVERTER

(Page 8-65)

- THROUGHPUT 160MHz
- INL ..... ±1.0 LSB
- DNL ..... ±0.5 LSB
- POWER CONSUMPTION 420mW
- ECL COMPATIBLE INPUTS

HI1171
8-BIT 40MSPS VIDEO D/A CONVERTER

(Page 8-57)

- THROUGHPUT 40MHz
- INL ..... ±1.0 LSB
- DNL ..... ±0.5 LSB
- POWER CONSUMPTION 80mW
- TTL COMPATIBLE INPUTS

New Data Acquisition Products (Continued)

SWITCHES AND MUXs

DG401, DG403, DG405
HIGH SPEED DUAL SWITCHES

(Page 9-42)

- ON-RESISTANCE 45Ω
- FAST SWITCHING
  - ON 150ns
  - OFF 60ns
- ULTRA LOW POWER ..... <35µW
- PDIP AND SOIC PACKAGES

DG411, DG412, DG413
PRECISION QUAD SPST SWITCHES

(Page 9-44)

- ON-RESISTANCE 35Ω
- FAST SWITCHING
  - ON 175ns
  - OFF 145ns
- ULTRA LOW POWER ..... <35µW
- SINGLE SUPPLY CAPABILITY

DG441, DG442
QUAD SPST SWITCHES

(Page 9-53)

- ON-RESISTANCE 85Ω
- FAST SWITCHING
  - ON 250ns
  - OFF (DG441) 120ns
- LOW POWER ..... <1.6mW
- INTERNAL VOLTAGE REFERENCE
- UPGRADE FOR DG201A, DG202

DG444, DG445
LOW COST QUAD SPST SWITCHES

(Page 9-63)

- ON-RESISTANCE 85Ω
- FAST SWITCHING
  - ON 250ns
  - OFF (DG444) 120ns
- ULTRA LOW POWER ..... <35µW
- UPGRADE FOR DG211, DG212

MULTIPLEXERS

DG406, DG407
16 CH/8 CH DIFFERENTIAL MULTIPLEXERS

(Page 10-15)

- ON-RESISTANCE 100Ω
- FAST SWITCHING
  - TRANSITION 300ns
  - OFF 150ns
- LOW POWER ..... <0.5mW
- UPGRADE FOR DG506A, DG507A

DG408, DG409
8 CH/4 CH DIFFERENTIAL MULTIPLEXERS

(Page 10-17)

- ON-RESISTANCE 100Ω
- FAST SWITCHING
  - TRANSITION 250ns
  - OFF 150ns
- LOW POWER ..... <2.25mW
- UPGRADE FOR DG508A, DG509A

DG458, DG459
FAULT PROTECTED MULTIPLEXERS

(Page 10-31)

- ANALOG RANGE ..... ±10V
- ON-RESISTANCE 1.5KΩ
- OVERVOLTAGE PROTECTION ..... UP TO ±35V
- TTL AND CMOS COMPATIBLE INPUTS
- PINOUT COMPATIBLE WITH DG508A/DG509A

New Data Acquisition Products (Continued)

INTERFACE

HIN230, HIN241
RS-232, +5.0V TRANSCEIVERS

(Page 11-3)

HARRIS PART NUMBER	POWER SUPPLY	NO. OF RS-232 DRIVERS	NO. OF RS-232 RECEIVERS	NO. OF EXTERNAL 1µF CAPACITORS	SHUTDOWN	TRI-STATE	NO. OF PINS/ PACKAGE
HIN230	+5.0V	5	0	4	YES	NO	20
HIN231	+5.0V and 7.5V to +13.2V	2	2	2	NO	NO	16
HIN232	+5.0V	2	2	4	NO	NO	16
HIN234	+5.0V	4	0	4	NO	NO	16
HIN236	+5.0V	4	3	4	YES	YES	24
HIN237	+5.0V	4	3	4	NO	NO	24
HIN238	+5.0V	4	4	4	NO	NO	24
HIN239	+5.0V and 7.5V to +13.2V	3	5	2	NO	YES	24
HIN240	+5.0V	5	5	4	YES	YES	44
HIN241	+5.0V	4	5	4	YES	YES	28

$5.00

HARRIS SEMICONDUCTOR

THE NEW HARRIS SEMICONDUCTOR

In December 1988, Harris Semiconductor acquired the General Electriic Solid State division, thereby adding former GE, RCA, and Intersil devices to the Harris Semiconductor line.

This Data Acquisition Databook represents the full line of Harris Semiconductor Data Acquisition products for commercial applications and supersedes all previously published Harris Data Acquisition databooks under the Harris, GE, RCA or Intersil names. For a complete listing of all Harris Semiconductor products, please refer to the Product Selection Guide (PSG-201S; ordering information below).

For complete, current and detailed technical specifications on any Harris devices please contact the nearest Harris sales, representative or distributor office; or direct literature requests to:

Harris Semiconductor Literature Department
P.O. Box 883, MS CB1-28
Melbourne, FL 32901
TEL: 1-800-442-7747
FAX: (407) 724-3937

See Section 18 for Data Sheets Available on AnswerFAX

See Technical Assistance Listing on Page viii

U.S. HEADQUARTERS
Harris Semiconductor
1301 Woody Burke Road
Melbourne, Florida 32901
TEL: (407) 724-3000

EUROPEAN HEADQUARTERS
Harris Semiconductor
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: 32.2.724.21.11

SOUTH ASIA
Harris Semiconductor H.K. Ltd
13/F Fourseas Building
208-212 Nathan Road
Tsimshatsui, Kowloon
Hong Kong
TEL: 852-723-6339

NORTH ASIA
Harris K.K.
Shinjuku NS Bldg. Box 6153
2-4-1 Nishi-Shinjuku
Shinjuku-ku, Tokyo 163-08 Japan
TEL: 81-3-3345-8911

Harris Semiconductor products are sold by description only. All specifications in this product guide are applicable only to packaged products; specifications for die are available upon request. Harris reserves the right to make changes in circuit design, specifications and other information at any time without prior notice. Accordingly, the reader is cautioned to verify that information in this publication is current before placing orders. Reference to products of other manufacturers are solely for convenience of comparison and do not imply total equivalency of design, performance, or otherwise.

DATA ACQUISITION PRODUCTS

FOR COMMERCIAL AND INDUSTRIAL APPLICATIONS

TECHNICAL ASSISTANCE

For technical assistance on the Harris products listed in this databook, please contact the Field Applications Engineering staff available at one of the following Harris Sales Offices:

UNITED STATES		
CALIFORNIA	Costa Mesa	714-433-0600
	San Jose	408-985-7322
	Woodland Hills	818-992-0686
FLORIDA	Melbourne	407-724-3576
GEORGIA	Duluth	404-476-2035
ILLINOIS	Schaumburg	708-240-3480
MASSACHUSETTS	Burlington	617-221-1850
NEW JERSEY	Voorhees	609-751-3425
NEW YORK	Great Neck	516-829-9441
TEXAS	Dallas	214-733-0800
INTERNATIONAL		
FRANCE	Paris	33-1-346-54046
GERMANY	Munich	49-8-963-8130
HONG KONG	Kowloon	852-723-6339
ITALY	Milano	39-2-262-0761
JAPAN	Tokyo	81-33-345-8911
KOREA	Seoul	82-2-551-0931
SINGAPORE	Singapore	65-291-0203
UNITED KINGDOM	Camberley	44-2-766-86886

For literature requests, please contact Harris at 1-800-442-7747 (1-800-4HARRIS)

DATA ACQUISITION 1

GENERAL INFORMATION

ALPHA NUMERIC PRODUCT INDEX

NOTE: Bold Type Designates a New Product from Harris.

ALPHA NUMERIC PRODUCT INDEX (Continued)

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ALPHA NUMERIC PRODUCT INDEX (Continued)

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PRODUCT INDEX BY FAMILY

NOTE: Bold Type Designates a New Product from Harris.

PRODUCT INDEX BY FAMILY (Continued)

NOTE: Bold Type Designates a New Product from Harris.

PRODUCT INDEX BY FAMILY (Continued)

NOTE: Bold Type Designates a New Product from Harris.

PRODUCT INDEX BY FAMILY (Continued)

NOTE: Bold Type Designates a New Product from Harris.

PRODUCT INDEX BY FAMILY (Continued)

NOTE: Bold Type Designates a New Product from Harris.

LINEAR AND TELECOM PRODUCTS

COMPARATORS DATA SHEETS

CA139, CA239, CA339, LM339	Quad Voltage Comparators for Industrial, Commercial and Military Applications
CA3098	Programmable Schmitt Trigger - with Memory Dual Input Precision Level Detectors
CA3290	BiMOS Dual Voltage Comparator with MOSFET Input, Bipolar Output
HA-4900, HA-4902, HA-4905	Precision Quad Comparator
HFA-0003, HFA-0003L	**Ultra High Speed Comparator**

DIFFERENTIAL AMPLIFIERS DATA SHEETS

CA3028, CA3053	Differential/Cascode Amplifiers for Commercial and Industrial Equipment from DC to 120MHz
CA3049, CA3102	Dual High Frequency Differential Amplifiers For Low Power Applications Up 500MHz
CA3054	Transistor Array - Dual Independent Differential Amp for Low Power Applications from DC to 120MHz

OPERATIONAL AMPLIFIERS DATA SHEETS

CA124, CA224, CA324, LM324*, LM2902*	Quad Operational Amplifiers for Commercial, Industrial, and Military Applications
CA158, CA258, CA358, CA2904, LM358*, LM2904*	Dual Operational Amplifiers for Commercial Industrial, and Military Applications
CA741, CA1458, CA1558, LM741*, LM1458*, LM1558*	High Gain Single and Dual Operational Amplifiers for Military, Industrial and Commercial Applications
CA3020	Multipurpose Wide-Band Power Amps Military, Industrial and Commercial Equipment at Frequency Up to 8MHz
CA3060	Operational Transconductance Amplifier Arrays
CA3078	Micropower Operational Amplifier
CA3080	Operational Transconductance Amplifier (OTA)
CA3094	Programmable Power Switch/Amplifier for Control and General Purpose Applications
CA3100	Wideband Operational Amplifier
CA3130	BiMOS Operational Amplifier with MOSFET Input/CMOS Output
CA3140	BiMOS Operational Amplifier with MOSFET Input/Bipolar Output
CA3160	BiMOS Operational Amplifiers with MOSFET Input/CMOS Output
CA3193	BiCMOS Precision Operational Amplifiers
CA3240	Dual BiMOS Operational Amplifier with MOSFET Input/Bipolar Output
CA3260	BiMOS Operational Amplifier with MOSFET Input/CMOS Output
CA3280	Dual Variable Operational Amplifier

NOTE: Bold Type Designates a New Product from Harris.

OPERATIONAL AMPLIFIERS DATA SHEETS (Continued)

CA3420	Low Supply Voltage, Low Input Current BiMOS Operational Amplifiers
CA3440	Nanopower BiMOS Operational Amplifier
CA3450	Video Line Driver, High Speed Operational Amplifier
CA5130	BiMOS Microprocessor Operational Amplifier with MOSFET Input/CMOS Output
CA5160	BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output
CA5260	BiMOS Microprocessor Operational Amplifiers with MOSFET Input/CMOS Output
CA5420	Low Supply Voltage, Low Input Current BiMOS Operational Amplifier
CA5470	Quad Microprocessor BiMOS-E Operational Amplifiers with MOSFET Input/Bipolar Output
HA-2400, HA-2404, HA-2405	PRAM Four Channel Programmable Amplifiers
HA-2406	Digitally Selectable Four Channel Operational Amplifier
HA-2444	**Selectable, Four Channel Video Operational Amplifier**
HA-2500, HA-2502, HA-2505	Precision High Slew Rate Operational Amplifiers
HA-2510, HA-2512, HA-2515	High Slew Rate Operational Amplifiers
HA-2520, HA-2522, HA-2525	Uncompensated High Slew Rate Operational Amplifiers
HA-2529	Uncompensated, High Slew Rate High Output Current, Operational Amplifier
HA-2539	Very High Slew Rate Wideband Operational Amplifier
HA-2540	Wideband, Fast Settling Operational Amplifier
HA-2541	Wideband, Fast Settling, Unity Gain Stable, Operational Amplifier
HA-2542	Wideband, High Slew Rate, High Output Current Operational Amplifier
HA-2544	Video Operational Amplifier
HA-2548	Precision, High Slew Rate, Wideband Operational Amplifier
HA-2600, HA-2602, HA-2605	Wideband, High Impedance Operational Amplifiers
HA-2620, HA-2622, HA-2625	Very Wideband, Uncompensated Operational Amplifiers
HA-2640, HA-2645	High Voltage Operational Amplifiers
HA-2705	Low Power, High Performance Operational Amplifier
HA-2839	**Very High Slew Rate Wideband Operational Amplifier**
HA-2840	**Very High Slew Rate Wideband Operational Amplifier**
HA-2841	**Wideband, Fast Settling, Unity Gain Stable, Video Operational Amplifier**
HA-2842	**Wideband, High Slew Rate, High Output Current, Video Operational Amplifier**
HA-2850	**Low Power, High Slew Rate Wideband Operational Amplifier**

NOTE: Bold Type Designates a New Product from Harris.

OPERATIONAL AMPLIFIERS DATA SHEETS (Continued)

HA-4741	Quad Operational Amplifier
HA-5002	Monolithic, Wideband, High Slew Rate, High Output Current Buffer
HA-5004	100MHz Current Feedback Amplifier
HA-5020	**100MHz Current Feedback Video Amplifier**
HA5022, HA5024	**Dual, Quad 100MHz Video Current Feedback Amplifier with Disable**
HA5023, HA5025	**Dual, Quad 100MHz Video Current Feedback Amplifier**
HA-5033	Video Buffer
HA-5101, HA-5111	Low Noise, High Performance Operational Amplifiers
HA-5102, HA-5104, HA-5112, HA-5114	Low Noise, High Performance Operational Amplifiers
HA-5127	Ultra-Low Noise Precision Operational Amplifier
HA-5130, HA-5135	Precision Operational Amplifiers
HA-5134	Precision Quad Operational Amplifier
HA-5137	Ultra-Low Noise Precision Wideband Operational Amplifier
HA-5142, HA-5144	Dual/Quad Ultra-Low Power Operational Amplifiers
HA-5147	Ultra-Low Noise Precision High Slew Rate Wideband Operational Amplifier
HA-5160, HA-5162	Wideband, JFET Input High Slew Rate, Uncompensated, Operational Amplifiers
HA-5170	Precision JFET Input Operational Amplifier
HA-5177	Ultra-Low Offset Voltage Operational Amplifier
HA-5190, HA-5195	Wideband, Fast Settling Operational Amplifiers
HA-5221, HA-5222	Low Noise, Wideband Precision Operational Amplifiers
HA5232, HA5234	**Precision Dual and Quad Operational Amplifiers**
HFA-0001	Ultra High Slew Rate Operational Amplifier
HFA-0002	Low Noise Wideband Operational Amplifier
HFA-0005	High Slew Rate Operational Amplifier
HFA1100, HFA1120	**Ultra High-Speed Current Feedback Amplifiers**
HFA1105, HFA1106, HFA1135, HFA1145	**High-Speed, Low Power, Current Feedback Operational Amplifiers**
HFA1110	**750MHz Low Distortion Unity Gain, Closed Loop Buffer**
HFA1112	**Ultra High-Speed Closed Loop Buffer Amplifier**
HFA1113	**High-Speed, Output Clamping Closed Loop Buffer**
HFA1130	**Output Clamping, Ultra High-Speed Current Feedback Amplifier**
ICL7611, ICL7612	ICL76XX Series Low Power CMOS Operational Amplifiers
ICL7621, ICL7641, ICL7642	ICL76XX Series Low Power CMOS Operational Amplifiers
ICL7650S	Super Chopper-Stabilized Operational Amplifier

NOTE: Bold Type Designates a New Product from Harris.

SAMPLE AND HOLD AMPLIFIER DATA SHEETS

HA-2420, HA-2425	Fast Sample and Hold Amplifiers
HA-5320	High Speed Precision Monolithic Sample and Hold Amplifier
HA-5330	Very High Speed Precision Monolithic Sample and Hold Amplifier
HA-5340	High Speed, Low Distortion, Precision Monolithic Sample and Hold Amplifier
HA5350, HA5351	**Ultra Fast (50ns) Sample and Hold Amplifiers**
HA5352	**Ultra Fast (50ns) Dual Sample and Hold Amplifier**

SPECIAL ANALOG CIRCUITS DATA SHEETS

CA555, LM555	Timers for Timing Delays and Oscillator Applications in Commercial, Industrial and Military Equipment
CA1391, CA1394	TV Horizontal Processors
CA3089	FM IF System
CA3126	TV Chroma Processor
CA3189	FM IF System
CA3194	Single Chip PAL Luminance/Chroma Processor
CA3217	Single Chip TV Chroma/Luminance Processor
CA3256	BiMOS Analog Video Switch and Amplifier
CD22402	Sync Generator for TV Applications and Video Processing Systems
HA-2546	Wideband Two Quadrant Analog Multiplier
HA-2547	Wideband Two Quadrant Analog Multiplier
HA-2556	**Wideband Four Quadrant Voltage Output Analog Multiplier**
HA-2557	**Wideband Four Quadrant Current Output Analog Multiplier**
HA7210	**Low Power Crystal Oscillator**
HFA5250	**Ultra High-Speed Monolithic Pin Driver**
ICL8013	Four Quadrant Analog Multiplier
ICL8038	Precision Waveform Generator/Voltage Controlled Oscillator
ICL8048, ICL8049	Log/Antilog Amplifiers
ICM7242	Long Range Fixed Timer
ICM7555, ICM7556	General Purpose Timers

TELECOMMUNICATIONS DATA SHEETS

CD22100	CMOS 4 x 4 Crosspoint Switch with Control Memory High-Voltage Type (20V Rating)
CD22101, CD22102	CMOS 4 x 4 x 2 Crosspoint Switch with Control Memory
CD22103A	CMOS HDB3 (High Density Bipolar 3) Transcoder for 2.048/8.448 Mb/s Transmission Applications
CD22202, CD22203	5V Low Power DTMF Receiver

NOTE: Bold Type Designates a New Product from Harris.

TELECOMMUNICATIONS DATA SHEETS (Continued)

CD22204	5V Low Power Subscriber DTMF Receiver
CD22301	Monolithic Pan Repeater
CD22354A, CD22357A	CMOS Single-Chip, Full-Feature PCM CODEC
CD22M3493	**12 x 8 x 1 BIMOS-E Crosspoint Switch**
CD22M3494	**16 x 8 x 1 BIMOS-E Crosspoint Switch**
CD22859	Monolithic Silicon COS/MOS Dual-Tone Multifrequency Tone Generator
CD74HC22106, CD74HCT22106	QMOS 8 x 8 x 1 Crosspoint Switch with Memory Control
HC-5502B	**SLIC Subscriber Line Interface Circuit**
HC-5504B	**SLIC Subscriber Line Interface Circuit**
HC-5504DLC	SLIC Subscriber Line Interface Circuit
HC-5509A1	**SLIC Subscriber Line Interface Circuit**
HC-5509B	**SLIC Subscriber Line Interface Circuit**
HC-5524	SLIC Subscriber Line Interface Circuit
HC-5560	PCM Transcoder
HC-55536	Continuous Variable Slope Delta-Demodulator (CVSD)
HC-55564	Continuously Variable Slope Delta-Modulator (CVSD)

TRANSISTOR ARRAY DATA SHEETS

CA3018	General Purpose Transistor Arrays
CA3039	Diode Array
CA3045, CA3046	General Purpose N-P-N Transistor Arrays
CA3081, CA3082	General Purpose High Current N-P-N Transistor Arrays
CA3083	General Purpose High Current N-P-N Transistor Array
CA3086	General Purpose N-P-N Transistor Array
CA3096	N-P-N/P-N-P Transistor Array
CA3127	High Frequency N-P-N Transistor Array
CA3141	High-Voltage Diode Array For Commercial, Industrial & Military Applications
CA3146, CA3183	High-Voltage Transistor Arrays
CA3227, CA3246	High-Frequency N-P-N Transistor Arrays For Low-Power Applications at Frequencies Up to 1.5GHz
HFA3046, HFA3096, HFA3127, HFA3128	**Ultra High Frequency Transistor Array**

NOTE: Bold Type Designates a New Product from Harris.

DIGITAL SIGNAL PROCESSING PRODUCTS

MULTIPLIERS

HMA510	16 x 16-Bit CMOS Parallel Multiplier Accumulator
HMA510/883	16 x 16-Bit CMOS Parallel Multiplier Accumulator
HMU16/HMU17	16 x 16-Bit CMOS Parallel Multipliers
HMU16/883	16 x 16-Bit CMOS Parallel Multiplier
HMU17/883	16 x 16-Bit CMOS Parallel Multiplier

ONE DIMENSIONAL FILTERS

HSP43168	Dual FIR Filter
HSP43168/883	Dual FIR Filter
HSP43216	Halfband Filter
HSP43220	Decimating Digital Filter
HSP43220/883	Decimating Digital Filter
HSP43481	Digital Filter
HSP43481/883	Digital Filter
HSP43881	Digital Filter
HSP43881/883	Digital Filter
HSP43891	Digital Filter
HSP43891/883	Digital Filter

TWO DIMENSIONAL FILTERS

HSP48901	3 x 3 Image Filter
HSP48908	Two Dimensional Convolver
HSP48908/833	Two Dimensional Convolver

SIGNAL SYNTHESIZERS

HSP45102	12-Bit Numerically Controlled Oscillator
HSP45106	16-Bit Numerically Controlled Oscillator
HSP45106/883	16-Bit Numerically Controlled Oscillator
HSP45116	Numerically Controlled Oscillator/Modulator
HSP45116/883	Numerically Controlled Oscillator/Modulator
HSP50016	Digital Down Converter

DIGITAL SIGNAL PROCESSING PRODUCTS (Continued)

SPECIAL FUNCTION

HSP45240	Address Sequencer
HSP45240/883	Address Sequencer
HSP45256	Binary Correlator
HSP45256/833	Binary Correlator
HSP48410	Histogrammer/Accumulating Buffer
HSP9501	Programmable Data Buffer
HSP9520/9521, ISP9520/9521	Multilevel Pipeline Register

DEVELOPMENT TOOLS

DECI • MATE	Harris HSP43220 Decimating Digital Filter Development Software
HSP-EVAL	DSP Evaluation Platform
HSP45116-DB	HSP46116 Daughter Board

/883 Data Sheet Format -In the interest of conserving space, data sheets for /883 qualified products have been printed without the Pinouts, Pin Description, Waveforms, AC Test Load Circuit and Design Information sections. The information sections can be obtained from the corresponding portion of the commercial data sheet.

DATA ACQUISITION 2

A/D CONVERTERS - DISPLAY

NOTE: Bold Type Designates a New Product from Harris.

ANALOG TO DIGITAL CONVERTERS WITH DISPLAY OUTPUTS

DEVICE (NOTES 2, 3)	SUFFIX CODES	DISPLAY TYPE	DISPLAY DRIVE	CONVERSION TYPE	CONVERSION TIME µSEC	TECHNOLOGY	RANGE MIN	LINEARITY COUNTS	FEATURES
3 DIGIT WITH LED DRIVERS									
CA3162A	E	BCD	Common Anode	Integrating	10,250	Bipolar-JI	+999mV to -99mV	±1	BCD to 7 Segment Converter, 2 Chip Set Makes a Complete DPM. Analog to Digital Converter, 3 Digit Output, "EEE": Positive Over-Range Indication, "-": Negative Over-Range Display.
CA3162	E, EX	BCD	Common Anode	Integrating		Bipolar-JI	+999mV to -99mV	±1	
$3^1/_2$ DIGIT WITH LED/LCD DRIVERS									
HI7131	CM44	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	High Common Mode Front End No Overrange Hangover
HI7131	CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	
HI7133	CM44	LED	Common Anode	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	High Common Mode Front End No Overrange Hangover
HI7133	CPL	LED	Common Anode	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	
ICL7106	CM44	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	Low Cost, MQFP
ICL7106	CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	
ICL7106R	CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	Low Cost, PDIP Reversed Leads
ICL7107	CM44	LED	Common Anode	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	Low Cost, MQFP
ICL7107	CPL	LED	Common Anode	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	
ICL7107R	CPL	LED	Common Anode	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	Low Cost, PDIP Reversed Leads
ICL7116	CM44	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	ICL7106 with Display Hold Function, MQFP
ICL7116	CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	

ANALOG TO DIGITAL CONVERTERS WITH DISPLAY OUTPUTS (Continued)

DEVICE (NOTES 2, 3)	SUFFIX CODES	DISPLAY TYPE	DISPLAY DRIVE	CONVERSION TYPE	CONVERSION TIME µSEC	TECHNOLOGY	RANGE MIN	LINEARITY COUNTS	FEATURES
ICL7117	CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	ICL7107 with Display Hold Function
ICL7136	CM44	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	Low Power Version of ICL7106, MQFP
ICL7136	CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	
ICL7136R	CPL	LCD	Direct Drive	Auto-Zero Integrating	333 Typ	CMOS-JI	±0.2V	±1	Low Power Version of ICL7106 Reversed Leads
ICL7137	CPL	LED	Common Anode	Auto-Zero	333 Typ	CMOS-JI	±0.2V	±1	Low Power Version of ICL7107
$3^3/_4$ DIGIT WITH LCD DRIVERS									
ICL7139	CPL	LCD	Duplex	Auto Zero	400	CMOS-JI	±0.4V	±1	13 Ranges, Autoranging Multimeter, AC Internal
ICL7149	CM44	LCD	Duplex	Auto-Zero Integrating	400	CMOS-JI	±0.4V	±1	18 Ranges, Autoranging Multimeter, AC External, MQFP
ICL7149	CPL	LCD	Duplex	Auto-Zero Integrating	400	CMOS-JI	±0.4V	±1	
$4^1/_2$ DIGIT WITH LCD DRIVERS									
ICL7129	CM44	LCD	Triplexed	Auto-Zero Integrating	500	CMOS-JI	±0.2V	±1 Typ	10µV Resolution. 1X, 10X Range Selection, MQFP
ICL7129	CPL	LCD	Triplexed	Auto-Zero Integrating	500	CMOS-JI	±0.2V	±1 Typ	
ICL7129R	CPL	LCD	Triplexed	Auto-Zero Integrating	500	CMOS-JI	±0.2V	±1 Typ	10µV Resolution. 1X, 10X Range Selection, PDIP Reversed Leads

CA3162

December 1993

A/D Converter for 3-Digit Display

Features

- Dual Slope A/D Conversion
- Multiplexed BCD Display
- Ultra Stable Internal Band Gap Voltage Reference
- Capable of Reading 99mV Below Ground with Single Supply
- Differential Input
- Internal Timing - No External Clock Required
- Choice of Low Speed (4Hz) or High Speed (96Hz) Conversion Rate
- "Hold" Inhibits Conversion but Maintains Delay
- Overrange Indication
  - "EEE" for Reading Greater than +999mV, "-" for Reading More Negative than -99mV When Used With CA3161E
- BCD-to-Seven-Segment Decoder/Driver
- Extended Temperature Range Version Available

Description

The CA3162E and CA3162AE are I^2L monolithic A/D converters that provide a 3 digit multiplexed BCD output. They are used with the CA3161E BCD-to-Seven-Segment Decoder/Driver* and a minimum of external parts to implement a complete 3 digit display. The CA3162AE is identical to the CA3162E except for an extended operating temperature range.

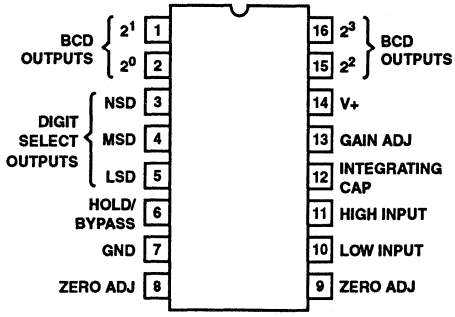
* The CA3161E is described in Display Drivers section of this data book.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3162E	0°C to +70°C	16 Lead Plastic DIP
CA3162AE	-40°C to +85°C	16 Lead Plastic DIP

Pinout

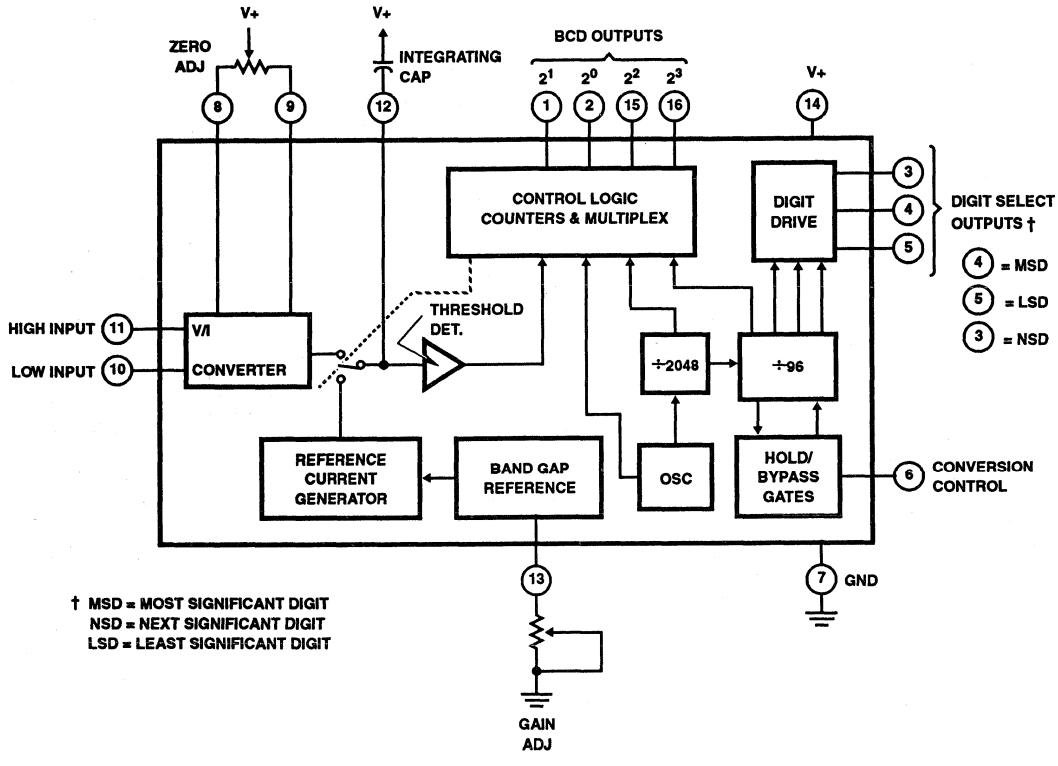
CA3162 (PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1080.1

Functional Block Diagram



Absolute Maximum Ratings

DC Supply Voltage (Between Pins 7 & 14) . . . . . +7V
Input Voltage (Pin 10 or 11 to Ground) . . . . . ±15V
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package . . . . . 90°C/W
Operating Temperature Range
CA3162E . . . . . 0 to +75°C
CA3162AE . . . . . -40°C to +85°C
Maximum Power Dissipation
Plastic DIP Package 0.67W
Junction Temperature . . . . . +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V+ = 5V, Zero Pot Centered, Gain Pot = 2.4kΩ Unless Otherwise Specified

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range, V+		4.5	5	5.5	V
Supply Current, I+	100kΩ to V+ on Pins 3, 4, 5	-	-	17	mA
Input Impedance, Z_I		-	100	-	MΩ
Input Bias Current, I_{IB}	Pins 10 and 11	-	-80	-	nA
Unadjusted Zero Offset	V_{11}-V_{10} = 0V, Read Decoded Output	-12	-	+12	mV
Unadjusted Gain	V_{11}-V_{10} = 900mV, Read Decoded Output	846	-	954	mV
Linearity	Notes 1 and 2	-1	-	+1	Count
Conversion Rate					
Slow Mode	Pin 6 = Open or GND	-	4	-	Hz
Fast Mode	Pin 6 = 5V	-	96	-	Hz
Conversion Control Voltage (Hold Mode) at Pin 6		0.8	1.2	1.6	V
Common Mode Input Voltage Range, V_{ICR}	Notes 3, 4	-0.2	-	+0.2	V
BCD Sink Current at Pins 1, 2, 15, 16	V_{BCD} ≥ 0.5V, at Logic Zero State	0.4	1.6	-	mA
Digit Select Sink Current at Pins 3, 4, 5	V_{DIGIT} Select = 4V at Logic Zero State	1.6	2.5	-	mA
Zero Temperature Coefficient	V_I = 0V, Zero Pot Centered	-	10	-	µV/°V
Gain Temperature Coefficient	V_I = 900mV, Gain Pot = 2.4kΩ	-	0.005	-	%/°C

NOTES:

1. Apply zero volts across V_{11} to V_{10}. Adjust zero potentiometer to give 000mV reading. Apply 900mV to input and adjust gain potentiometer to give 900mV reading.
2. Linearity is measured as a difference from a straight line drawn through zero and positive full scale. Limits do not include ±0.5 count bit digitizing error.
3. For applications where low input pin 10 is not operated at pin 7 potential, a return path of not more than 100kΩ resistance must be provided for input bias currents.
4. The common mode input voltage above ground cannot exceed +0.2V if the full input signal range of 999mV is required at pin 11. That is, pin 11 may not operate higher than 1.2V positive with respect to ground or 0.2V negative with respect to ground. If the maximum input signal is less than 999mV, the common mode input voltage may be raised accordingly.

Timing Diagram

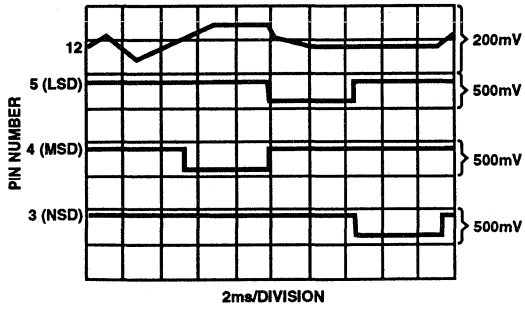


FIGURE 1. HIGH SPEED MODE

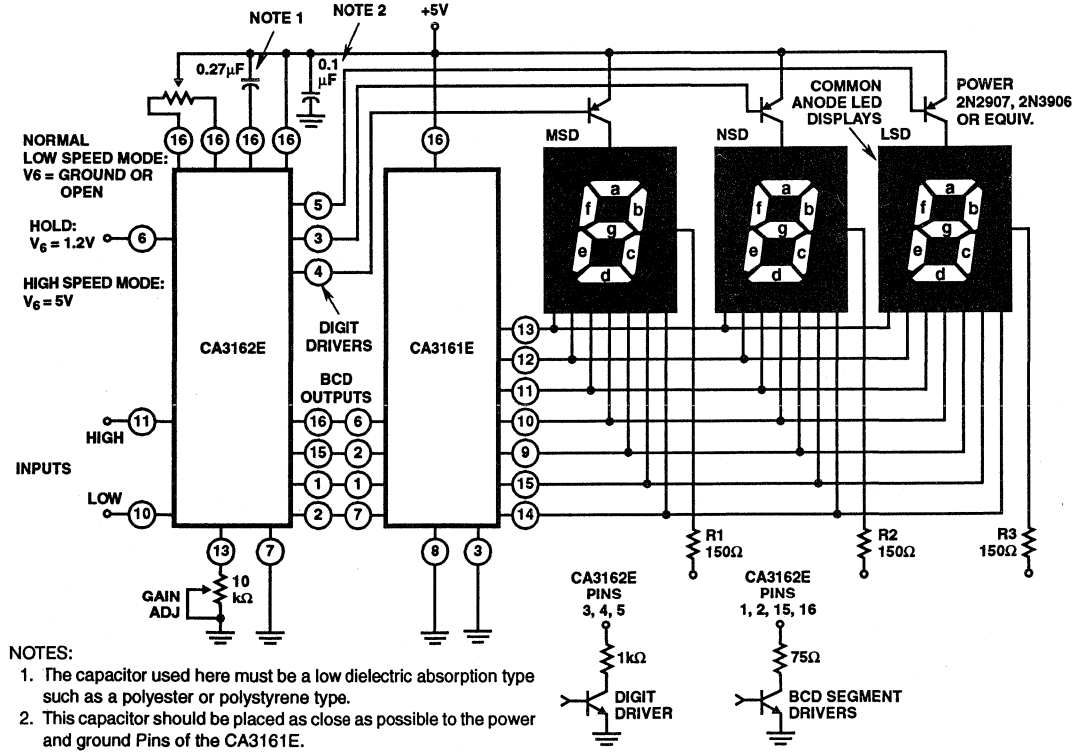
Detailed Description

The Functional Block Diagram of the CA3162E shows the V/I converter and reference current generator, which is the heart of the system. The V/I converter converts the input voltage applied between pins 10 and 11 to a current that charges the integrating capacitor on pin 12 for a predetermined time interval. At the end of the charging interval, the V/I converter is disconnected from the integrating capacitor, and a band gap reference constant current source of opposite polarity is connected. The number of clock counts that elapse before the charge is restored to its original value is a direct measure of the signal induced current. The restoration is sensed by the comparator, which in turn latches the counter. The count is then multiplexed to the BCD outputs.

The timing for the CA3162E is supplied by a 786Hz ring oscillator, and the input at pin 6 determines the sampling rate. A 5V input provides a high speed sampling rate (96Hz), and grounding or floating pin 6 provides a low speed (4Hz) sampling rate. When pin 6 is fixed at +1.2V (by placing a 12K resistor between pin 6 and the +5V supply) a "hold" feature is available. While the CA3162E is in the hold mode, sampling continues at 4Hz but the display data are latched to the last reading prior to the application of the 1.2V. Removal of the 1.2V restores continuous display changes. Note, however, that the sampling rate remains at 4Hz.

Figure 1 shows the timing of sampling and digit select pulses for the high speed mode. Note that the basic A/D conversion process requires approximately 5ms in both modes.

The "EEE" or "---" displays indicate that the range of the system has been exceeded in the positive or negative direction, respectively. Negative voltages to -99mV are displayed with the minus sign in the MSD. The BCD code is 1010 for a negative overrange (---) and 1011 for a positive overrange (EEE).



NOTES:

1. The capacitor used here must be a low dielectric absorption type such as a polyester or polystyrene type.
2. This capacitor should be placed as close as possible to the power and ground Pins of the CA3161E.

FIGURE 2. BASIC DIGITAL READOUT SYSTEM USING THE CA3162E AND THE CA3161E

CA3162E Liquid Crystal Display (LCD) Application

Figure 3 shows the CA3162E in a typical LCD application. LCDs may be used in favor of LED displays in applications requiring lower power dissipation, such as battery-operated equipment, or when visibility in high-ambient-light conditions is desired.

Multiplexing of LCD digits is not practical, since LCDs must be driven by an AC signal and the average voltage across each segment is zero. Three CD4056B liquid-crystal decoder/drivers are therefore used. Each CD4056B contains an input latch so that the BCD data for each digit may be latched into the decoder using the inverted digit-select outputs of the CA3162E as strobes.

The capacitors on the outputs of inverters G3 and G4 filter out the decode spikes on the MSD and NSD signals. The capacitors and pull-up resistors connected to the MSD, NSD and LSD outputs are there to shorten the digit drive signal thereby providing proper timing for the CD4056B latches.

Inverters G1 and G2 are used as an astable multivibrator to provide the AC drive to the LCD backplane. Inverters G3, G4 and G5 are the digit-select inverters and require pull-up resistors to interface the open-collector outputs of the CA3162E to CMOS logic. The BCD outputs of the CA3162E may be connected directly to the corresponding CD4056B inputs (using pull-up resistors). In this arrangement, the CD4056B decodes the negative sign (-) as an "L" and the positive overload indicator (E) as an "H".

The circuit as shown in Figure 3 using G7, G8 and G9 will decode the negative sign (-) as a negative sign (-), and the positive overload indicator (E) as "H".

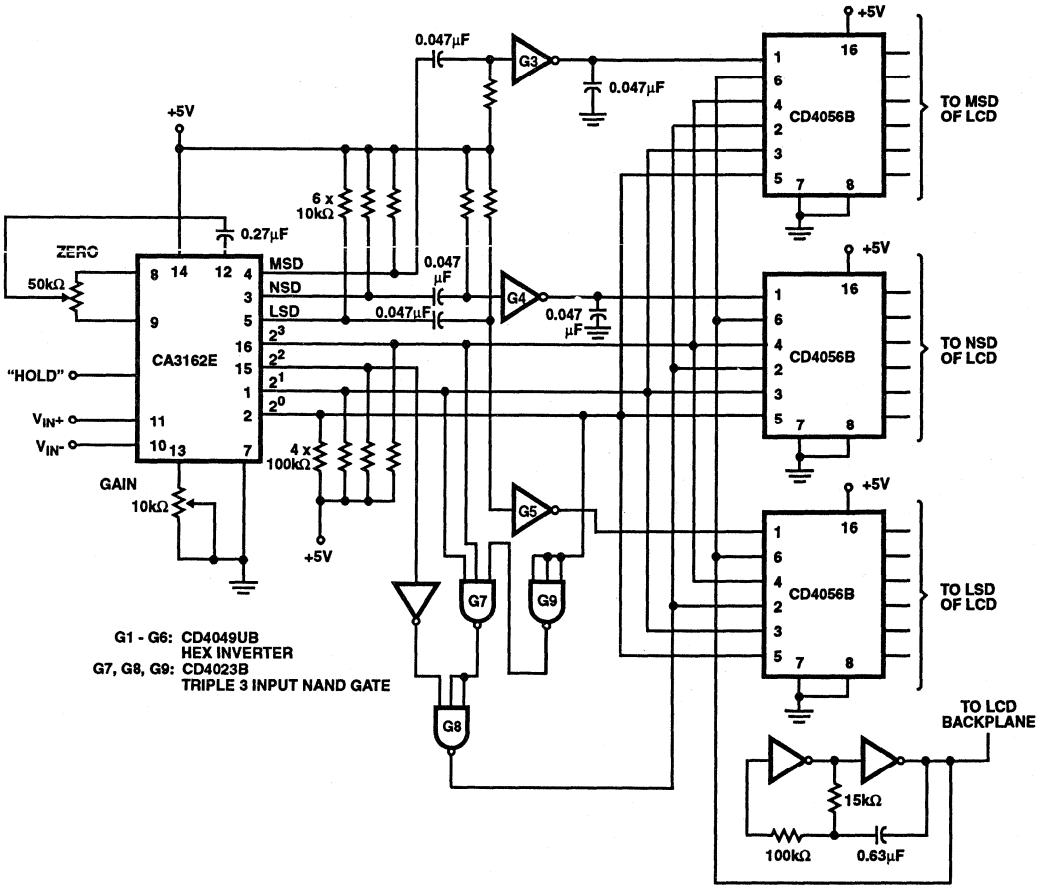


FIGURE 3. TYPICAL LCD APPLICATION

CA3162E Common-Cathode, LED Display Application

Figure 4 shows the CA3162E connected to a CD4511B decode/driver to operate a common-cathode LED display. Unlike the CA3161E, the CD4511B remains blank for all BCD codes greater than nine. After 999mV the display blanks rather than displaying EEE, as with the CA3161E. When displaying negative voltage, the first digit remains blank, instead of (-), and during a negative or positive overrange the display blanks.

The additional logic shown within the dotted area of Figure 4 restores the negative sign (-), allowing the display of negative numbers as low as -99mV. Negative overrange is indicated by a negative sign (-) in the MSD position. The rest of the display is blanked. During a positive overrange, only segment b of the MSD is displayed. One inverter from the CD4049B is used to operate the decimal points. By connecting the inverter input to either the MSD or NSD line either DP1 or DP2 will be displayed.

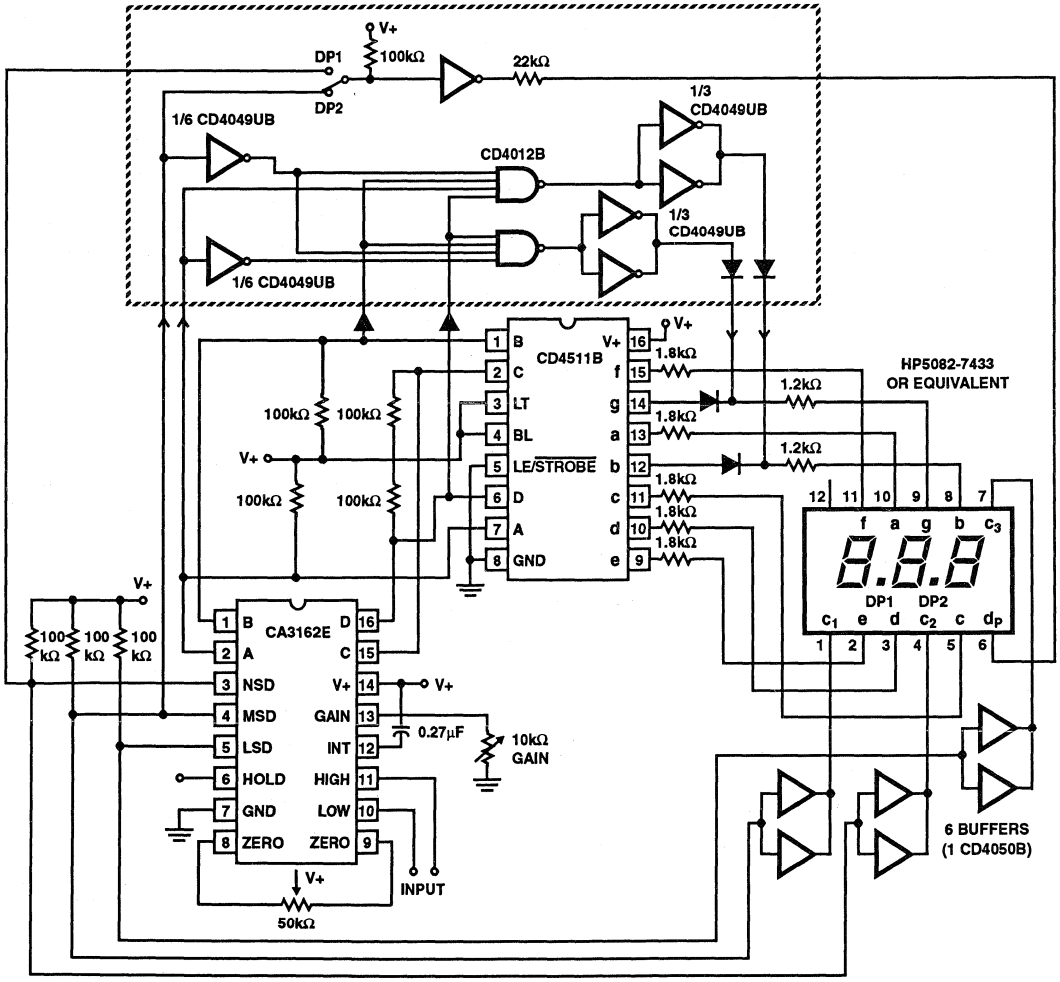


FIGURE 4. TYPICAL COMMON-CATHODE LED APPLICATION

Die Characteristics

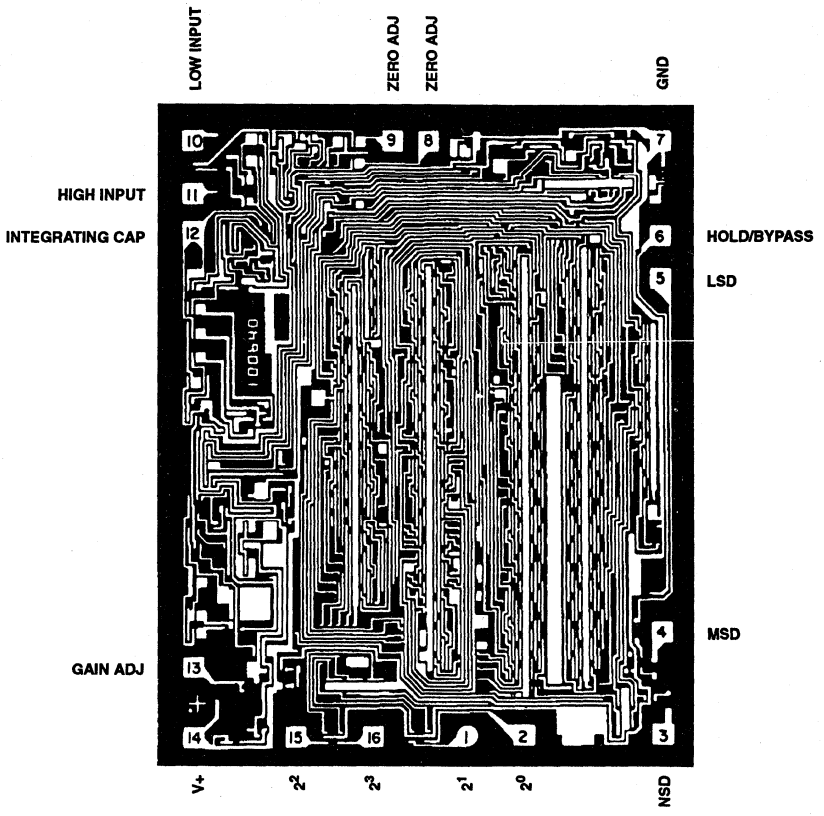
DIE DIMENSIONS:
101 x 124 x 20 ± 1mils

METALLIZATION:
Type: Al
Thickness: 17.5kÅ ± 2.5kÅ

GLASSIVATION:
Type: 3% PSG
Thickness: 13kÅ ± 2.5kÅ

Metallization Mask Layout

CA3162, CA3162A



HARRIS SEMICONDUCTOR

HI7131, HI7133

$3^1/_2$ Digit Low Power, High CMRR LCD/LED Display Type A/D Converter

December 1993

Features

- 120dB CMRR Equal to ±0.01 Count/V of Common Mode Voltage Error
- Fast Recovery from Input Overrange Results "Correct First-Reading" After Overload
- Guaranteed 0000 Reading for 0V Input
- True Polarity at Zero for Precise Null Detection
- 1pA Input Current, Typical
- True Differential Input and Reference
- Single or Dual Supply Operation Capability
- Direct LCD Display Drive - HI7131
- Direct LED Display Drive - HI7133
- Low Noise, 15μVp-p Without Hysteresis or Overrange Hangover
- Low Power Dissipation, Guaranteed Less Than 1mW, Results 8000 Hours Typical 9V Battery Life
- No Additional Active Components Required

Applications

- Handheld Instruments
- Basic Measurements: Voltage, Current, Resistance Pressure, Temperature, Fluid Flow and Level, pH, Weight, Light Intensity
- DMM's and DPM's

Description

The Harris HI7131 and HI7133 are $3^1/_2$ digit A/D converters that have been optimized for superior DC Common Mode Rejection (CMRR) when used with a split ±5V supply or a single 9V battery. The HI7131 contains all the necessary active components on a single IC to directly interface an LCD (Liquid Crystal Display). The supply current is under 100μA and is ideally suited for battery operation. The HI7133 contains all the necessary active components on a single IC to directly interface an LED (Light Emitting Diode).

The HI7131 and HI7133 feature high accuracy performance like, 120dB of CMRR, auto-zero to less than 10μV of offset, fast recovery from over load, zero drift of less than 1μV/°C, input bias current of 10pA maximum, and rollover error of less than one count. A true differential signal and reference inputs are useful features in all systems, but gives the designer an advantage when measuring load cells, strain gauges and other bridge-type transducers.

The HI7131 and HI7133 are supplied in a 40 lead plastic DIP and a 44 lead metric plastic quad flatpack package.

Ordering Information

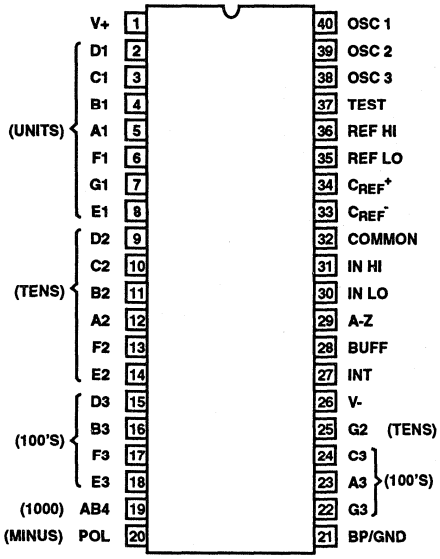
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI7131CPL	$0°C \le T_A \le +70°C$	40 Lead Plastic DIP
HI7131CM44	$0°C \le T_A \le +70°C$	44 Lead MQFP
HI7133CPL	$0°C \le T_A \le +70°C$	40 Lead Plastic DIP
HI7133CM44	$0°C \le T_A \le +70°C$	44 Lead MQFP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

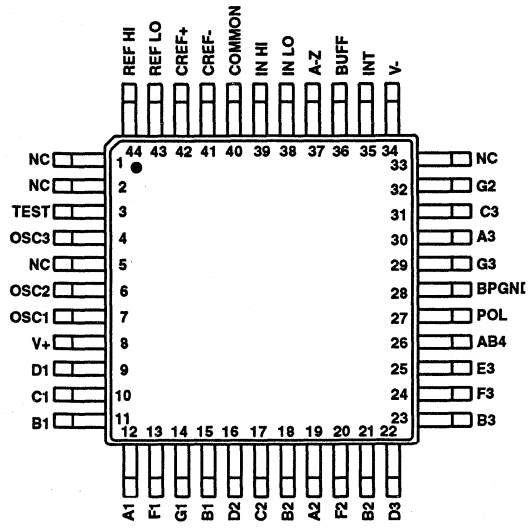
File Number **3373.1**

Pinouts

HI7131CPL, HI7133CPL
(PDIP)
TOP VIEW



HI7131CM44, HI7133CM44
(MQFP)
TOP VIEW



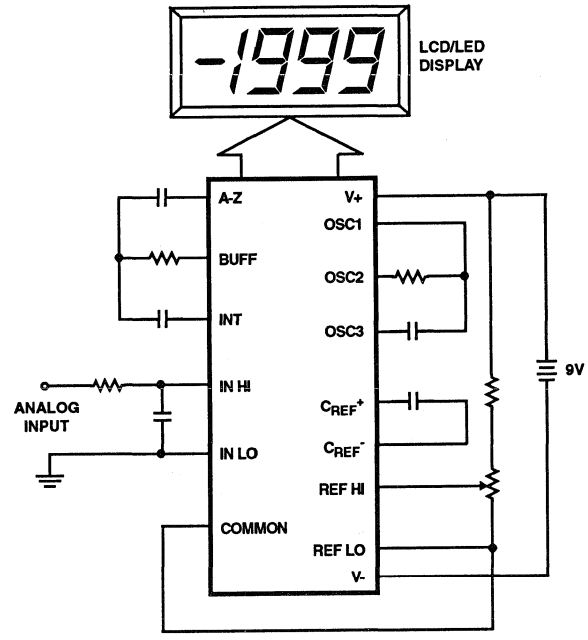
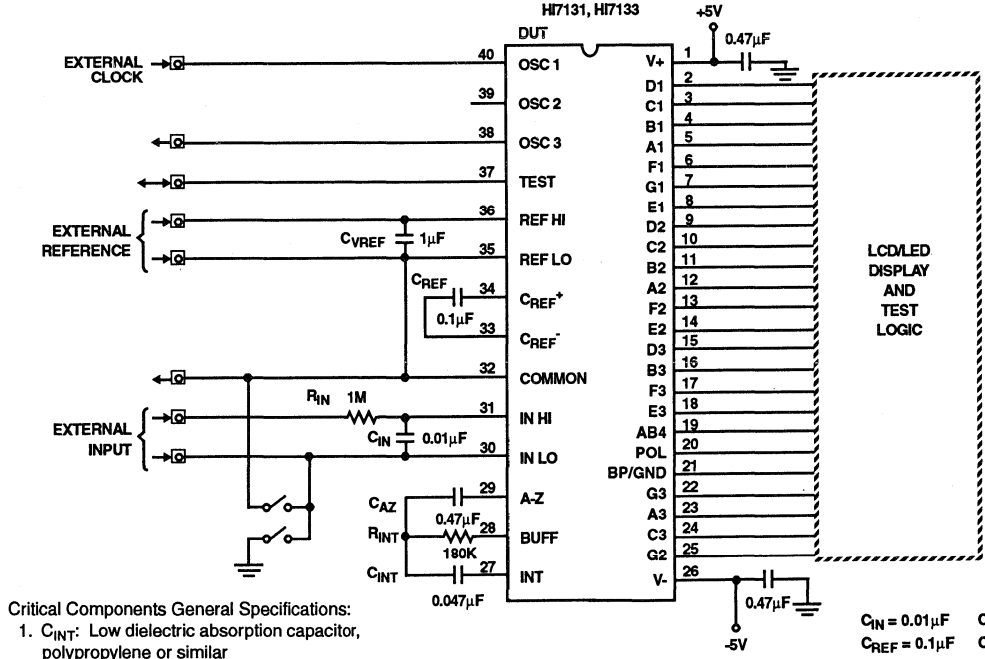


FIGURE 1. TYPICAL APPLICATION CIRCUIT



Critical Components General Specifications:

1. C_{INT}: Low dielectric absorption capacitor, polypropylene or similar
2. C_{AZ}, C_{REF}, C_{IN}: Low leakage capacitors

FIGURE 2. TEST CIRCUIT

Absolute Maximum Ratings

Supply Voltage, V+ to V- ..... +15V
Signal Inputs, pin# 30, 31 (Note 1) ..... V+ to V-
Reference Inputs, pin# 35, 36 ..... V+ to V-
Clock Input, OSC1, pin# 40 (Note 2) ..... TEST pin to V+
All Other Analog Leads, pin# 27-29, 32-34 ..... V+ to V-
All Other Digital Leads,
pin# 2-25, 38, 39 (Note 2) ..... TEST pin to V^+
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature PDIP (Soldering 10s) ..... +300 °C Max

Thermal Information

Thermal Resistance	θ_{JA}
HI7131 40 Lead Plastic DIP	50°C/W
HI7133 44 Lead Metric Quad Flatpack	80°C/W

Maximum Power Dissipation (Note 3)
HI7131 ..... 0.6W
HI7133 ..... 0.8W
Operating Temperature, T_A ..... 0°C to +70°C
Maximum Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

(Notes 4, 5, 6) T_A = 25°C. Device is Tested in the Circuit Shown in Figure 2. Full Scale Range (FSR) = 200.0mV, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Zero Input Reading	V_{IN} = 0V	-000	±000	+000	Reading
Ratiometric Reading	$V_{INHI} = V_{REFHI}$ $V_{INLO} = V_{REFLO} = V_{COMMON}$ $V_{REFHI} - V_{REFLO}$ = 100.0mV	999	999/ 1000	1001	Reading
Rollover Error	V_{IN} = ±199mV	-	±0.2	±1	Count
Linearity Error	FSR = 200mV or 2V (Note 4, 7)	-	±0.2	±1	Count
Zero Input Reading Drift	V_{IN} = 0V Over Full Temperature Range (Note 4, 7)	-	±0.2	±1 ±0.01	µV/°C Count/°C
Scale Factor Temperature Coefficient	V_{IN} = 199mV, Over Full Temperature Range, Reference Drift Not Included (Note 4, 7)	-	±1	±5 ±0.01	ppm/°C Count/°C
Equivalent Input Noise (PK-PK value not exceeded 95% of the times)	V_{IN} = 0V (Note 4, 7)	-	15 0.15	-	µV Count
INPUT					
Common Mode Voltage Sensitivity	V_{CM} = ±1V, V_{IN} = 0V (Note 4, 5, 7, 8)	-	-	1 0.01	µV/V Count/V
Input Leakage Current	V_{IN} = 0V (Note 4, 7)	-	1	10	pA
Overload Recovery Period	V_{IN} Changing from ±10V to 0V (Note 4, 7)	-	-	1	Conversion Cycle
COMMON PIN					
COMMON Pin Voltage (With respect to V+, i.e. V+ - V_{COMMON})	V+ to V- = 10V	2.4	2.8	3.2	V
COMMON Pin Voltage Temperature Coefficient	V+ to V- = 10V (Note 4, 7)	-	150	-	ppm/°C
COMMON Pin Sink Current	+0.1V Change on V_{COMMON} (Note 4)	-	3	-	mA
COMMON Pin Source Current	-0.1V Change on V_{COMMON} (Note 4)	-	1	-	µA

Electrical Specifications (Notes 4, 5, 6) T_A = 25°C. Device is Tested in the Circuit Shown in Figure 2. Full Scale Range (FSR) = 200.0mV, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DISPLAY DRIVER (HI7131)					
PK-PK Segment Drive Voltage	V+ to V- = 10V	4	5	6	V
PK-PK Backplane Drive Voltage		4	5	6	V
POWER SUPPLY (Nominal Supply Voltage; V+ to V- = 10V)					
Supply Current (Does not include COMMON pin current)	V_{IN} = 0V (Note 9) Oscillator Frequency = 16kHz	-	70	100	µA
Power Dissipation Capacitance	VS Clock Frequency (Note 4, 7)	-	40	-	pF
DISPLAY DRIVER (HI7133)					
Segment Sink Current (Except Pins 19 and 20)	V+ = +5.0V Driver Pin Voltage = 3.0V	5	8.5	-	mA
Pin 19 Sink Current		10	16	-	mA
Pin 20 Sink Current		4	7	-	mA
POWER SUPPLY (Nominal Supply Voltage; V+ = +5V, V- = -5V both respect to GND pin)					
V+ Supply Current (Note 9)	V_{IN} = 0V Oscillator Frequency = 16kHz Does not include COMMON pin and display current	-	70	100	µA
V- Supply Current (Note 4, 9)		-	40	-	µA
Power Dissipation Capacitance	Versus Clock Frequency (Note 4, 7)	-	40	-	pF

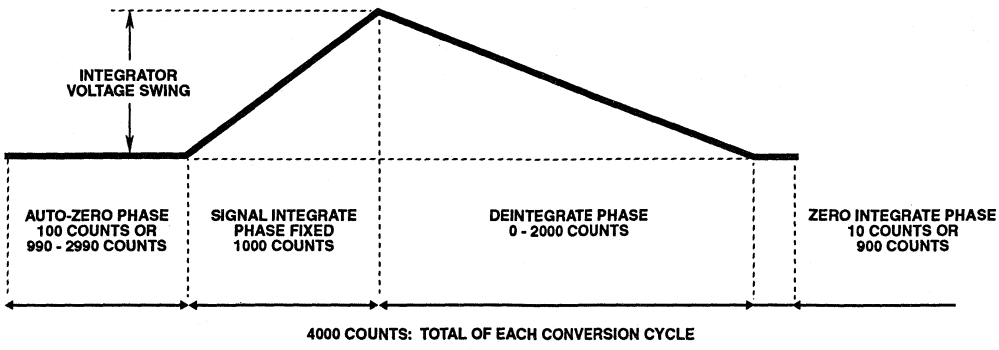
NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.
2. TEST pin is connected to internally generated digital ground through a 500Ω resistor (See text for TEST pin description).
3. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
4. All typical values have been characterized but not tested.
5. See "Parameters Definition" section.
6. Count is equal to one number change in the least significant digit of the display.
7. Parameter not tested on a production basis, guaranteed by design and/or characterization.
8. See "Differential Input" section.
9. 48kHz oscillator increases current by 20µA (typ).

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**
  $f_{OSC} \approx 0.45/RC_{(OSC)}$
  $C_{OSC} \geq 50pF$
  $R_{OSC} > 50k\Omega$
  $C_{OSC} = 50pF$, $R_{OSC} = 180k\Omega$; $f_{OSC\ Typ.} = 48kHz$
- **CLOCK FREQUENCY**
  $f_{CLOCK} = f_{OSC}/4$
- **CLOCK PERIOD**
  $t_{CLOCK} = 1/f_{CLOCK}$
- **CONVERSION CYCLE**
  $T_{CYC} = 4000 \times t_{CLOCK} = 16000 \times t_{OSC}$
  For $f_{OSC} = 40kHz$; $T_{CYC} = 400ms$
- **SIGNAL INTEGRATION PERIOD**
  $T_{INT} = 1000 \times t_{CLOCK}$
- **60/50Hz REJECTION CRITERIA**
  T_{INT} / t_{60Hz} or T_{INT} / t_{50Hz} = Integer
- **OPTIMUM FULL SCALE ANALOG INPUT RANGE**
  $V_{INFS} = 200mV$ to 2V
- **INPUTS VOLTAGE RANGE**
  $(V- + 1V) < V_{INLO}$ or $V_{INHI} < (V+ - 1V)$
- **MAXIMUM INTEGRATION CURRENT**
  $I_{INTmax} = V_{INFS} / R_{INT}$
  Maximum integration current should be the maximum buffer output current with no nonlinearity effect.
  Maximum Buffer Output Current = 1µA
- **INTEGRATOR MAXIMUM OUTPUT VOLTAGE SWING**
  $V_{INTmax} = (T_{INT})\ (I_{INTmax})/C_{INT}$
  $(V- + 0.5) < V_{INTmax} < (V+ - 0.5)$
  Typical $V_{INTmax} = 2V$
- **INTEGRATING RESISTOR**
  $R_{INT} = V_{INFS} / I_{INTmax}$
- **INTEGRATING CAPACITOR**
  $C_{INT} = (T_{INT})\ (I_{INTmax}) / V_{INTmax}$
- **AUTO-ZERO CAPACITOR VALUE**
  $0.01\mu F < C_{AZ} < 1.0\mu F$
- **REFERENCE CAPACITOR VALUE**
  $0.1\mu F < C_{REF} < 1.0\mu F$
- **REFERENCE INPUTS VOLTAGE RANGE**
  $V- < V_{REFLO}$ or $V_{REFHI} < V+$
- **REFERENCE VOLTAGE**
  $V_{REF} = V_{INFS} / 2$
- **COMMON PIN VOLTAGE**
  $V_{COMMON} = V+ - 2.8$, Typical, V_{COMMON} is regulated and can be used as a reference. It is biased between V+ and V- and regulation is lost at $(V+ - V-) < 6.8V$. V_{COMMON} pin does not have sink capability and can be externally pulled down to lower voltages.
- **DISPLAY TYPE**
  LCD, Non-Multiplexed
- **POWER SUPPLY, V+ TO V⁻**
  Single +9V or ±5V Nominal, +5V to +12V Functional
- **DISPLAY READING**
  Reading = $1000 \times (V_{IN} / V_{REF})$
  Maximum Reading = 1999, for $V_{IN} = 1.999 \times V_{REF}$

Typical Integrator Amplifier Output Waveform (INT Pin)



NOTE: 1 Count = 1 Clock Cycle = 4 Oscillator Cycle

Pin Description

PIN NUMBER		NAME	FUNCTION	DESCRIPTION
40 PIN DIP	44 PIN FLATPACK			
1	8	V+	SUPPLY	Power Supply
2	9	D1	OUTPUT	Driver Pin for Segment "D" of the display units digit
3	10	C1	OUTPUT	Driver Pin for Segment "C" of the display units digit
4	11	B1	OUTPUT	Driver Pin for Segment "B" of the display units digit
5	12	A1	OUTPUT	Driver Pin for Segment "A" of the display units digit
6	13	F1	OUTPUT	Driver Pin for Segment "F" of the display units digit
7	14	G1	OUTPUT	Driver Pin for Segment "G" of the display units digit
8	15	E1	OUTPUT	Driver Pin for Segment "E" of the display units digit
9	16	D2	OUTPUT	Driver Pin for Segment "D" of the display tens digit
10	17	C2	OUTPUT	Driver Pin for Segment "C" of the display tens digit
11	18	B2	OUTPUT	Driver Pin for Segment "B" of the display tens digit
12	19	A2	OUTPUT	Driver Pin for Segment "A" of the display tens digit
13	20	F2	OUTPUT	Driver Pin for Segment "F" of the display tens digit
14	21	E2	OUTPUT	Driver Pin for Segment "E" of the display tens digit
15	22	D3	OUTPUT	Driver pin for segment "D" of the display hundreds digit
16	23	B3	OUTPUT	Driver pin for segment "B" of the display hundreds digit
17	24	F3	OUTPUT	Driver pin for segment "F" of the display hundreds digit
18	25	E3	OUTPUT	Driver pin for segment "E" of the display hundreds digit
19	26	AB4	OUTPUT	Driver pin for both "A" and "B" segments of the display thousands digit
20	27	POL	OUTPUT	Driver pin for the negative sign of the display
21	28	BP/GND	OUTPUT	Driver pin for the LCD backplane/Power Supply Ground
22	29	G3	OUTPUT	Driver pin for segment "G" of the display hundreds digit
23	30	A3	OUTPUT	Driver pin for segment "A" of the display hundreds digit
24	31	C3	OUTPUT	Driver pin for segment "C" of the display hundreds digit
25	32	G2	OUTPUT	Driver pin for segment "G" of the display tens digit
26	34	V-	SUPPLY	Negative power supply
27	35	INT	OUTPUT	Integrator amplifier output. To be connected to integrating capacitor
28	36	BUFF	OUTPUT	Input buffer amplifier output. To be connected to integrating resistor
29	37	A-Z	INPUT	Integrator amplifier input.To be connected to auto-zero capacitor
30 31	38 39	IN LO IN HI	INPUT	Differential inputs. To be connected to input voltage to be measured. LO & HI designators are for reference and do not imply that LO should be connected to lower potential, e.g. for negative inputs IN LO has a higher potential than IN HI.
32	40	COMMON	SUPPLY/ OUTPUT	Internal voltage reference output
33 34	41 42	C_{REF-} C_{REF+}		Connection pins for reference capacitor
35 36	43 44	REF LO REF HI	INPUT	Input pins for reference voltage to the device. REF HI should be positive reference to REF LO.
37	3	TEST	INPUT	Display test. Turns on all segments when tied to V+.
38 39 40	4 6 7	OSC3 OSC2 OSC1	OUTPUT OUTPUT INPUT	Device clock generator circuit connection pins

Definition of Specifications

Count

A Count is equal to one number change in the least significant digit of the display. The analog size of a count referred to ADC input is:

$$\text{Analog Count Size} = \frac{\text{Full Scale Range}}{\text{Max Reading} + 1}$$

Max reading +1 for a $3^1/_2$ digit display is 2000 (1999+1).

Zero Input Reading

The reading of the ADC display when input voltage is zero and there is no common mode voltage, i.e. the inputs are shorted to COMMON pin.

Ratiometric Reading

The reading of the ADC display when input voltage is equal to reference voltage, i.e. IN HI tied to REF HI and IN LO tied to REF LO and COMMON pins. The accuracy of reference voltage is not important for this test.

Rollover Error

Difference in the absolute value reading of ADC display for equal magnitude but opposite polarity inputs. The input voltage should be close to full scale, which is the worst case condition.

Linearity

Deviation of the ADC transfer function (output reading versus input voltage transfer plot) from the best straight line fitted to ADC transfer plot.

Scale Factor Temperature Coefficient

The rate of change of the slope of ADC transfer function due to the change of temperature.

Equivalent Input Noise

The total random uncertainty of the ADC for converting a fixed input value to an output reading. This uncertainty is referred to input as a noise source which produces the equivalent effect. It is given for zero input and is expressed as p-p noise value and submultiples of Counts.

Overload Recovery Period

A measure of how fast the ADC will display an accurate reading when input changes from an overload condition to a value within the range. This is given as the number of conversion cycles required after the input goes within the range.

Theory of Operation

The HI7131 and HI7133 are dual-slope integrating type A/D converters. As the name implies, its output represents the integral or average of the input signal. A basic block diagram of a dual-slope integrating converter is shown in Figure 3. A conventional conversion cycle has two distinct phases:

First, the input signal is integrated for a fixed interval of time. This is called the signal integration phase. In this phase the input of the integrator is connected to the input signal through the switch. During this time, charge builds up on C_{INT} which is proportional to the input voltage.

The next phase is to discharge C_{INT}. This is called reference integration or deintegration phase, with the use of a fixed reference voltage. The time it takes to discharge the C_{INT} is directly proportional to the input signal. This time is converted to a digital readout by means of a BCD counter, driven by a clock oscillator. During this phase, the integrator input is connected to an opposite polarity reference voltage through the switch to discharge C_{INT}.

Notice that during the integration phase, the rate of charge built up on the capacitor is proportional to the level of the input signal, and there is a fixed period of time to integrate the input. However, during the discharge cycle the rate of discharge is fixed and there is a variable time period for complete discharge

A $3^1/_2$ digit BCD counter is shown in the block diagram, the period of integration is determined by 1000 counts of this counter. Just prior to a measurement, the counter is reset to zero and C_{INT} has no charge. At the beginning of the measurement, the control logic enables the counter and the integrator input is connected to the input node. Charge begins accumulating on C_{INT} and the output of the integrator moves down or up respectively for positive or negative inputs. This process continues until the counter reaches 1000 counts. This will signal the control logic for the start of the deintegrating cycle. The control logic resets the counter and connects the integrator input to a reference voltage opposite to that of the input signal. The charge accumulated on C_{INT} is now starting to be removed and the counter starts to count up again. As soon as all the charge is removed, the output of the integrator reaches 0 volts. This is detected by the comparator and the control logic is signaled for the end of a measurement cycle. At this time the number accumulated in the counter is the representation of the input signal. This number will be stored on the latches and displayed until the end of the next measurement cycle.

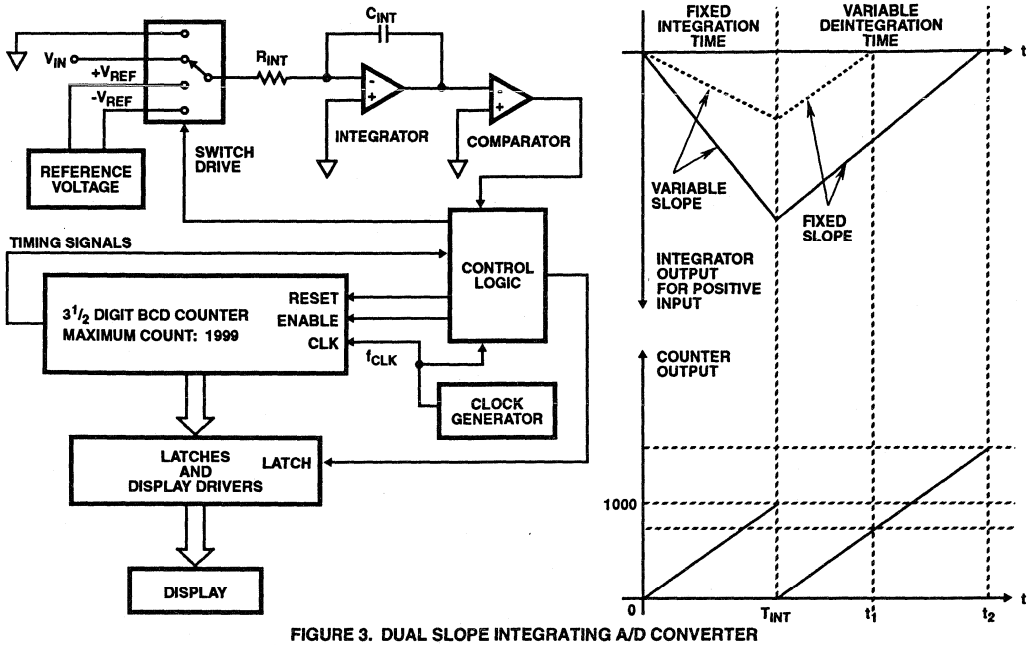


FIGURE 3. DUAL SLOPE INTEGRATING A/D CONVERTER

Figure 3 shows a typical waveform of the integrator output for 2 different positive input values and the associated representation of the counter output for those inputs. T_{INT} is the time period of integrating phase. t_1 and t_2 are the end of measurement for 2 different inputs.

The dual slope integrating technique puts the primary responsibility for accuracy on the reference voltage. The values of R_{INT} and C_{INT} and the clock frequency (f_{CLK}) are not important, provided they are stable during each conversion cycle. This can be expressed mathematically as follows:

$$\Delta V_{INT} = \frac{1}{R_{INT}C_{INT}} \int_0^{T_{INT}} V_{IN}dt = \frac{1}{R_{INT}C_{INT}} \int_0^{T_{DEINT}} V_{REF}dt$$

$$\Delta V_{INT} = \frac{\overline{V_{IN}}T_{INT}}{R_{INT}C_{INT}} = \frac{V_{REF}t_{DEINT}}{R_{INT}C_{INT}}$$

$\overline{V_{IN}}$: Input Average Value During Integration Time

$$T_{INT} = 1000\left(\frac{1}{f_{CLK}}\right)$$

$$t_{DEINT} = \text{Accumulated Counts}\left(\frac{1}{f_{CLK}}\right)$$

$$\text{Accumulated Counts} = 1000\frac{\overline{V_{IN}}}{V_{REF}} = \text{Display Reading}$$

It can be seen that the output reading of the ADC is only proportional to the ratio of V_{IN} over V_{REF}. The last equation also demonstrates that for the maximum display reading (i.e. 1999) we will have $V_{IN} = 1.999\ V_{REF}$. This implies that in this configuration the full scale range of the converter is twice its reference voltage.

The inherent advantages of integrating A/D converters are; very small nonlinearity error, no possibility of missing codes and good high frequency noise rejection.

Furthermore, the integrating converter has extremely high normal mode rejection of frequencies whose periods are an integral multiple of the integrating period (T_{INT}). This feature can be used to reject the line frequency related noises which are riding on input voltage by appropriate selection of clock frequency. This is shown in Figure 4.

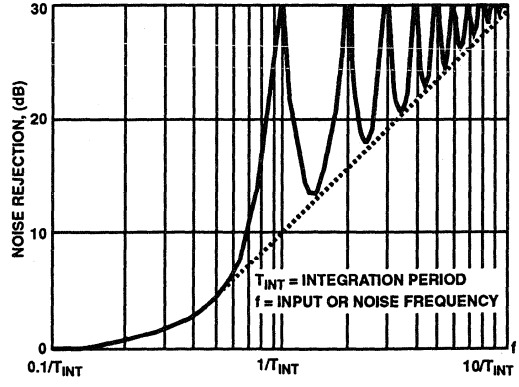


FIGURE 4. NOISE REJECTION FOR INTEGRATING TYPE A/D CONVERTER

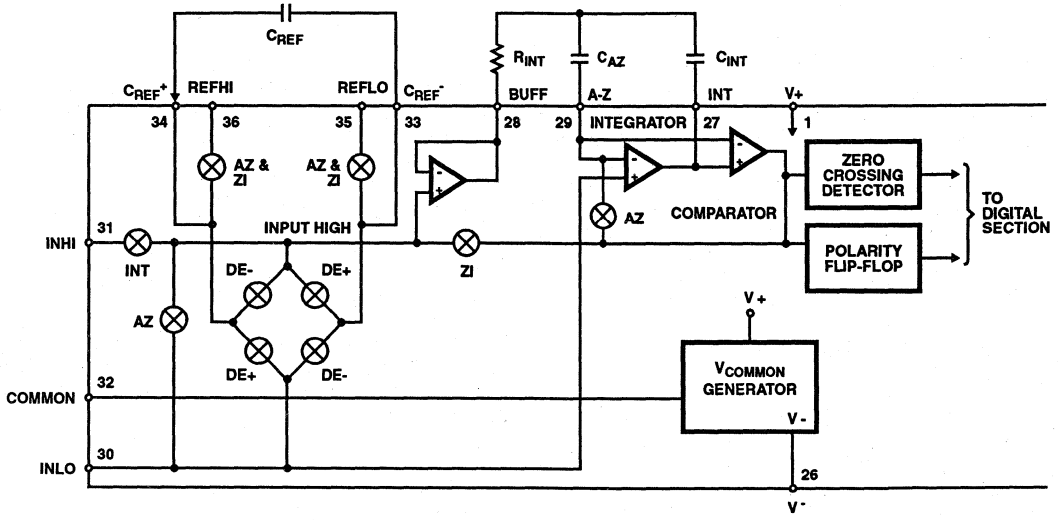


FIGURE 5A. HI7131 AND HI7133 ANALOG SECTION FUNCTIONAL DIAGRAM

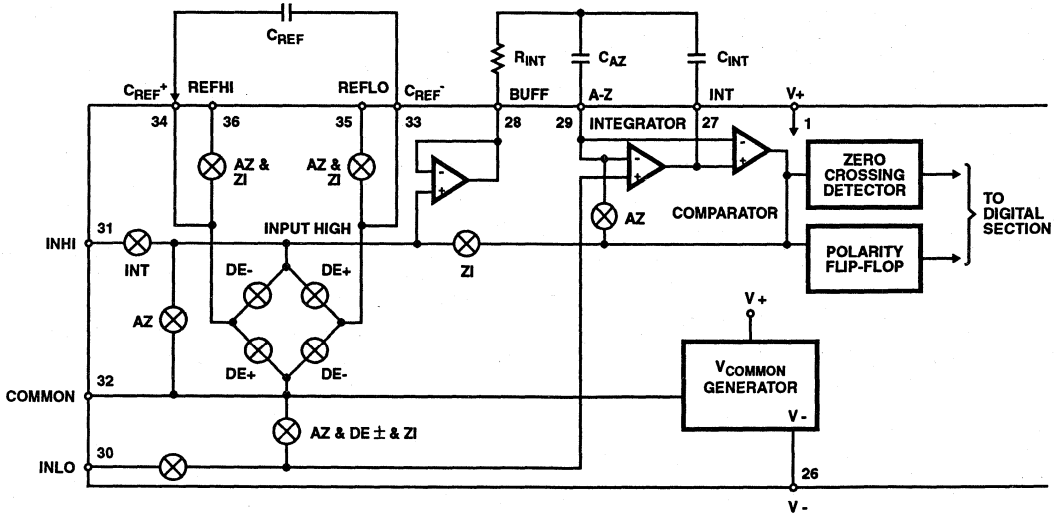


FIGURE 5B. ICL7136 AND ICL7137 ANALOG SECTION FUNCTIONAL DIAGRAM

FIGURE 5. HI7131, HI7133 vs ICL7136, ICL7137 ANALOG SECTIONS

HI7131/33 vs ICL7136/37

Figure 5 shows the analog front end block diagram of both HI7131/33 and ICL7136/37. The difference is the common reference voltage generator connection and 2 extra analog switches in the ICL7136. The HI7131 architecture uses the INLO as the reference point of the integrator (non-inverting input of the integrator amplifier) in all the phases of the conversion cycle. The ICL7136 uses INLO as a reference point only during integration cycle and COMMON pin is used as the integrator reference point during auto-zero, deintegrate, and zero integrate phases.

The circuit configuration of the HI7131 results in a superior 120dB rejection of DC common mode on the inputs. However, the HI7131 has reduced AC common mode noise rejection, since the noise on the INLO input can cause errors during the deintegration phase.

The circuit configuration of the ICL7136 is unaffected by the AC noise riding on the inputs, but the DC common mode rejection on the input is only 86dB.

Analog Section Description

Figure 5-A shows a simplified diagram of the analog section of the HI7131 and HI7133. The circuit performs basic phases of dual slope integration. Furthermore, the device incorporates 2 additional phases called "Auto-Zero" and "Zero Integrate". The device accepts differential input signals and reference voltages. Also, there is a reference voltage generator which sets the COMMON pin 2.8 volts below the V+ supply. A complete conversion cycle is divided into the following four phases:

1. Auto-Zero (A/Z)
2. Signal Integrate (INT)
3. Deintegrate or Reference Integrate (DE±)
4. Zero Integrate (ZI)

Digitally controlled analog switches direct the appropriate signals for each phase of the conversion.

Auto-Zero Phase

During auto-zero three things occur. First, IN HI is disconnected from the device internal circuitry and internally shorted to IN LO. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} and integrating capacitor C_{INT} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A/Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

Signal Integrate Phase

During signal integrate the auto-zero loop is opened and the internal INPUT HIGH is connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide input common mode range: up to one volt from either supply. At the end of this phase, the polarity of the integrated signal is determined.

Deintegrate Phase

During this phase the IN LO and the internal INPUT HIGH are connected across the previously charged reference capacitor. The bridge type circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. As specified before, the digital reading displayed is:

$$\text{DIGITAL READING} = 1000\left(\frac{V_{INHI} - V_{INLO}}{V_{REFHI} - V_{REFLO}}\right)$$

Zero Integrate Phase

This phase is provided to eliminate overrange hangover and causes fast recovery from heavy overrange. During this phase a feedback loop is closed around the system by connecting comparator output to internal INPUT HIGH. This will discharge the integrator capacitor (C_{INT}), causing the integrator output return to zero. During this phase the reference capacitor is also connected to reference input, charging to the reference voltage.

A typical integrator output voltage during different phases is shown on the "Design Information Summary Sheet". This integrator output is for negative inputs and is referred to INLO. For positive inputs the integrator output will go negative.

Digital Section Description

Figure 6 shows the block diagram of the digital section of the HI7131. The diagram shows the clock generator, control logic, counters, latches and display decoder drivers. An internal digital ground is generated from a 6V Zener diode and a large P channel source follower. This supply is capable of absorbing the relatively large capacitive currents when the LCD backplane (BP) and segment drivers are switched.

Display Drivers

A typical segment output driver consists of P and N channel MOSFETs.

An LCD consists of a backplane (BP) and segments. BP covers the whole area under the segments. Because of the nature of the LCD's, they should be driven by square-waves. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square-wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments. The polarity indication is "ON" for negative analog inputs. If INLO and INHI are reversed, this indication can be reversed also, if desired.

The HI7131 is a direct display drive (versus multiplexed) and each segment in each digit has its own segment driver. The display font and the segment assignment on the display are also shown in Figure 6.

Figure 6 shows the block diagram of the digital section of the HI7133. The diagram shows the clock generator, control logic, counters, latches and display decoder drivers. The supply rails of the digital circuitry are V+ and GND.

Display Drivers

A typical segment output consists of a P and an N channel MOSFET. This configuration is designed to drive common anode LED displays. The nominal sink current for each segment is 8mA, a typical value for instrument size common anode LED displays. The driver for the thousand digit is twice as big as other segments and can sink 16mA since it is actually driving 2 segments. The sink current for the polarity driver is 7mA. The polarity driver is on for negative inputs. The HI7133 is a direct display drive (versus multiplexed) and each segment in each digit has its own segment driver. The display font and the segment assignment on the display are also shown in Figure 7.

Clock Generator

The clock generator circuit basically includes 2 CMOS inverters and a divide by 4 counter. It is designed to be used in 2 different basic configurations.

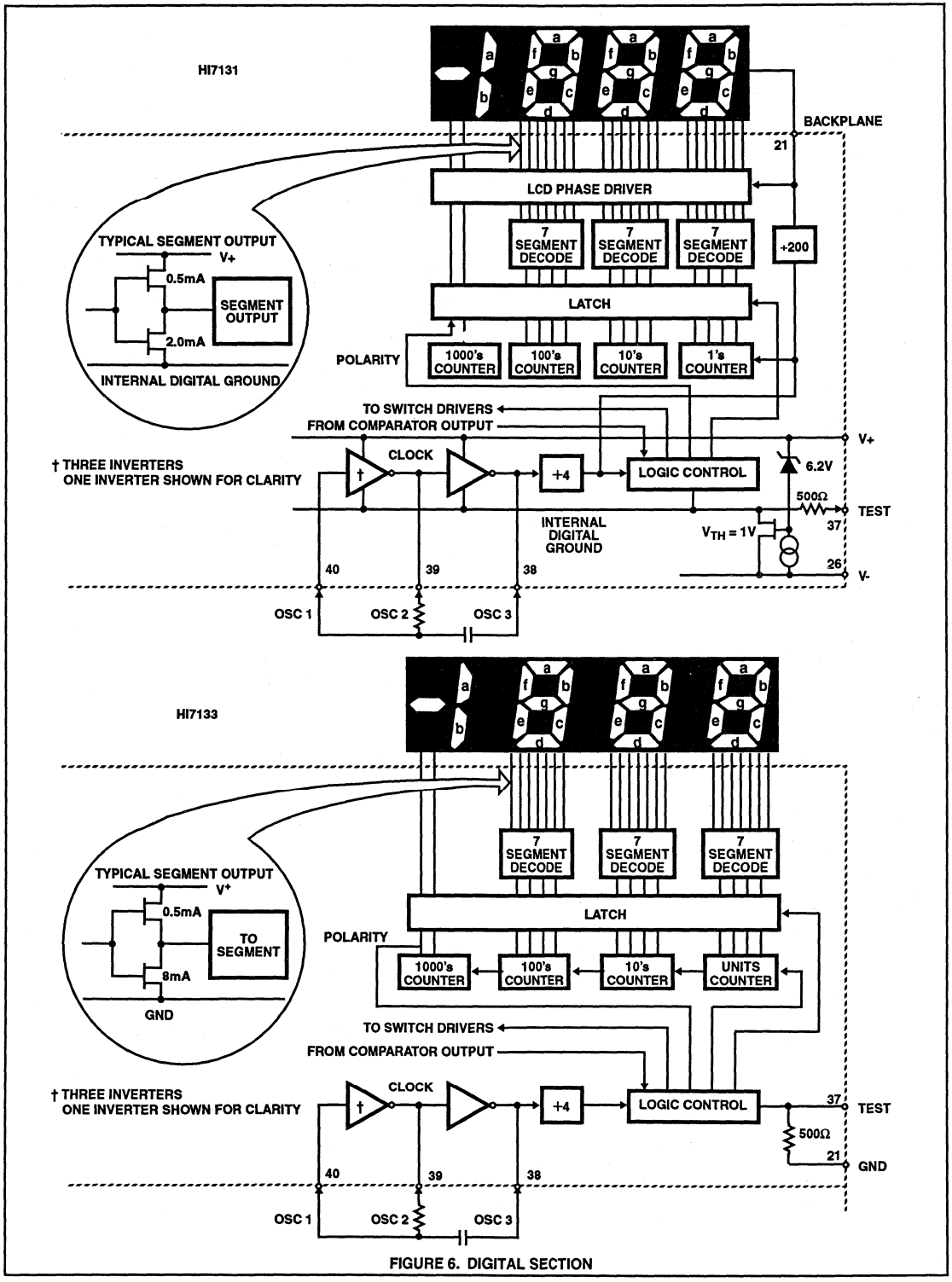


FIGURE 6. DIGITAL SECTION

1. An External Oscillator Driving OSC 1.
2. An RC Oscillator Using All 3 Oscillator Circuit Pins.

These are shown in Figure 7.

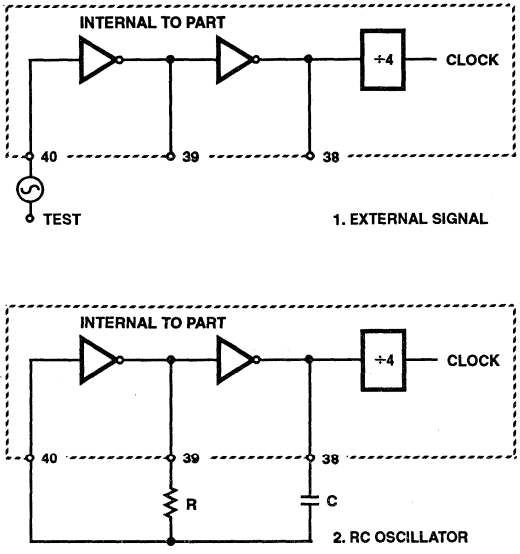


FIGURE 7. CLOCK CIRCUITS

The oscillator output frequency is divided by 4 before it clocks the rest of the digital section. Notice that there are 2 separate frequencies which are referred to as; oscillator frequency (f_{OSC}) and clock frequency (f_{CLK}) with the relation of:

$$f_{CLK} = \frac{f_{OSC}}{4}$$

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. For 60Hz rejection oscillator frequencies of, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of, 100kHz, 66 2/3kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

For the RC oscillator configuration the relationship between oscillator frequency, R and C values are:

$$f_{OSC} \approx \frac{0.45}{R_{OSC}C_{OSC}}$$

(R in Ohms and C in Farads)

System Timing

As it has been mentioned, the oscillator output is divided by 4 prior to clocking the digital section and specifically, the internal decade counters. The control logic looks at the counter outputs and comparator output (see analog section) to form the appropriate timing for 4 phases of conversion cycle.

The total length of a conversion cycle is equal to 4000 counts and is independent of the input signal magnitude or full scale range. Each phase of the conversion cycle has the following length:

Auto-Zero Phase

100 counts in case an overrange is detected. 990 to 2990 counts for normal conversion. For those inputs which are less than full scale, the deintegrate length is less than 2000 counts. Those extra counts on deintegrate phase are assigned to auto-zero phase to keep the conversion cycle constant.

Signal Integrate Phase

1000 counts, a fixed period of time. The time of integration can be calculated as:

$$T_{INT} = 1000\left(\frac{1}{f_{CLK}}\right) = 4000\left(\frac{1}{f_{OSC}}\right)$$

Deintegrate Phase

0 to 2000 counts, variable length phase depending on the input voltage.

Zero Integrate Phase

10 counts in case of normal conversion. 900 counts in case an overrange is detected.

Functional Considerations of Device Pins

COMMON Pin

The COMMON pin is the device internal reference generator output.

The COMMON pin sets a voltage that is about 2.8V less than the V+ supply rail. This voltage (V+ - V_{COMMON}) is the on-chip reference which can be used for setting converter reference voltage.

Within the IC, the COMMON pin is tied to an N-channel transistor capable of sinking up to 3mA of current and still keeping COMMON voltage within the range. However, there is only 1µA of source current capability. The COMMON pin can be used as a virtual ground in single supply applications when the external analog signals need a reference point in between the supply rails. If higher sink and source current capability is needed for virtual ground a unity gain op-amp can be used as a buffer.

Differential Inputs (IN LO, IN HI)

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 1.0 volts below the positive supply to 1.0 volt above the negative supply. In this range, the system has a CMRR of 120dB (typical). However, care must be exercised to assure the integrator output does not saturate. This is illustrated in Figure 8, which shows how common mode voltage affects maximum swing on the integrator output. Figure 8 shows the circuit configuration during conversion. In this figure, common mode voltage is considered as a voltage on the IN LO pin referenced to (V+ - V-) / 2, which is usually the GND in a dual supply system.

A worst case condition would be a large positive common-mode voltage with a near full scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing to within 0.3 volts of either supply without loss of linearity.

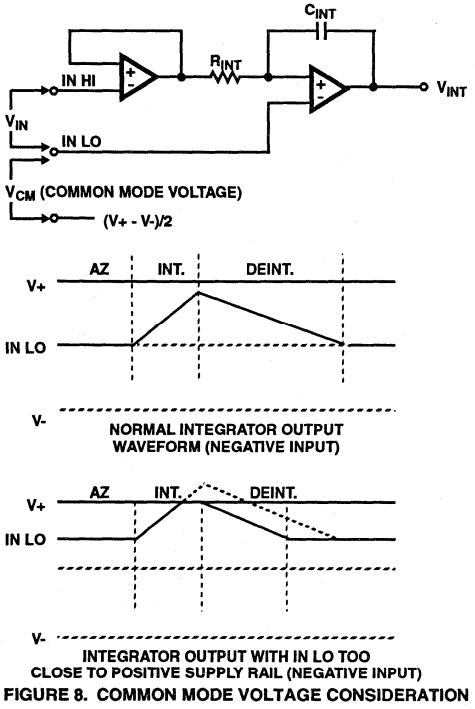


FIGURE 8. COMMON MODE VOLTAGE CONSIDERATION

Differential Reference (REF HI, REF LO) and Reference Capacitor Pins (C_{REF}^+, C_{REF}^-).

As was discussed in the analog section (Figure 5), the differential reference pins are connected across the reference capacitor (connected to pins C_{REF}^+ and C_{REF}^-) to charge it during the zero integrate and the auto-zero phase. Then the reference capacitor is used as either a positive or negative reference during the deintegrate phase. The reference capacitor acts as a flying capacitor between the reference voltage and integrator inputs in the deintegrate phase.

The common mode voltage range for the reference inputs is V+ to V-. The reference voltage can be generated anywhere within the power supply range of the converter. The main source of rollover error is reference common mode voltage caused by the reference capacitor losing or gaining charge to or from stray capacitance on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called upon to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This change in reference for positive or negative input voltage will give a rollover error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitances, this error can be held to less than 0.5 counts worst case. See the "Component Value Selection" section for auto-zero capacitor value.

TEST Pin

The TEST pin serves two functions. It is coupled to the internally generated digital ground through an effective 500Ω resistor. Thus, it can be used as the digital ground for external digital circuits such as segment drivers for decimal points or any other annunciator the user may want to include on the LCD display. For these applications the external digital circuit should be supplied between V+ and TEST pin. Figures 9 and 10 show such an application. In Figure 9 a MOSFET transistor is used to invert the BP signal to drive the decimal point. The MOSFET can be any general purpose type with a threshold voltage less than 3.5V and ON resistance less than 500Ω. Figure 10 uses an CMOS IC XOR gate to generate controllable decimal point drives. No more than a 1mA load should be applied to TEST pin by any external digital circuitry.

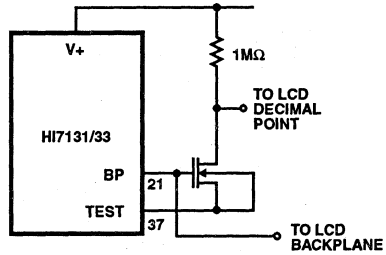


FIGURE 9. SIMPLE INVERTER FOR FIXED DECIMAL POINT DRIVE

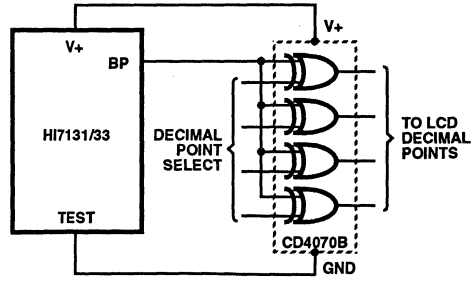


FIGURE 10. EXCLUSIVE "OR" GATE FOR DECIMAL POINTS AND ANNUNCIATORS DRIVE

The second function of the TEST pin is the "lamp test". When the TEST pin is pulled high (to V+) all segments will be turned on and the display should read -1888. The test pin will sink about 10mA under these conditions.

CAUTION: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

Component Selection

Integrating resistors and capacitors (R_{INT}, C_{INT}): A guideline to achieving the best performance from an integrating A/D converter is to try to reduce the value of R_{INT}, increase the value of C_{INT}, while having the highest possible voltage swing at the output of the integrator. This will reduce the sensitivity of the circuit to noise and leakage currents. In addition to these guidelines the circuit limitations should also be considered.

To determine R_{INT}, the imposed circuit limitation is the maximum output drive current of the buffer amplifier (see Figure 5) while maintaining its linearity. This current for the buffer amplifier is about 1µA. The R_{INT} resistor can be calculated from the expression:

$$R_{INT} = \frac{V_{IN}\,(\text{Full Scale})}{1\mu A}$$

The standard optimum values for R_{INT} are 180kΩ for 200mV full scale and 1.8MΩ for 2V full scale. Type of resistor and its absolute value is not critical to the accuracy of conversion, as was discussed previously.

The integrating capacitor should be selected to yield the maximum allowable voltage range to the integrator output (INT pin). The maximum allowable range does not saturate the integrator output. The integrator output can swing up or down to 0.3V from either supply rail and still maintain its linearity.

A nominal ±2V maximum range is optimum. The maximum range values are selected in order to leave enough room for all the component and circuit tolerances and for a reasonable common mode voltage range. The C_{INT} value can now be calculated as:

$$C_{INT} = \frac{T_{INT} I_{INT}}{V_{INTMAX}}$$

Where T_{INT} depends on clock frequency and was discussed before and I_{INT} is expressed as:

$$I_{INT} = \frac{V_{IN}\,(\text{Full Scale})}{R_{INT}}$$

For 48kHz nominal oscillator frequency (12kHz clock internal frequency), R_{INT} equals 180kΩ for 1.8MΩ for the above mentioned swing, the optimum value for C_{INT} is 0.047µF.

An additional requirement of the integrating capacitor is to choose low dielectric absorption. This will minimize the converter's rollover, linearity and gain error. Furthermore, the integrating capacitor should also have low leakage current. Different types of capacitors are adequate for this application; polypropylene capacitors provide undetectable errors at reasonable cost and size. The absolute value of C_{INT} does not have any effect on accuracy.

Auto-Zero Capacitor (C_{AZ})

The value of the auto-zero capacitor has some influence on the noise of the converter. A larger value C_{AZ} has less sensitivity to noise. For 200mV full scale (resolution of 100µV), where noise is important, a 0.47µF or greater is recommended. On the 2V full scale, (resolution of 1mV), a 0.047µF capacitor is adequate for low noise.

The auto-zero capacitor should be a low leakage type to hold the voltage during conversion cycle. A mylar or polypropylene capacitor is recommended for C_{AZ}.

Reference Capacitor (C_{REF})

As discussed earlier, the input to the integrator during the deintegrate phase is the voltage at the reference capacitor. The sources of error related to the reference capacitor are stray capacitances at the C_{REF} terminals, and the leakage currents. Where a large common mode voltage exists for V_{REF}, the stray capacitances increase the rollover error by absorbing or pumping charge onto C_{REF} when positive or negative inputs are measured. Leakage of the capacitor itself or leakages through circuit boards will drop the voltage across C_{REF} and cause gain and rollover errors. The circuit boards should be designed to minimize stray capacitances and should be well cleaned to reduce leakage currents.

A 0.1µF capacitor for C_{REF} should work properly for most applications. When common mode voltage exists or at higher temperatures (where device leakage currents increase) a 1.0µF reference capacitor is recommended to reduce errors. The C_{REF} capacitor can be any low leakage type, a mylar capacitor is adequate.

Those applications which have variable reference voltage should also use a low dielectric absorption capacitor such as polypropylene, for example, a ratiometric measurement of resistance.

Oscillator Components

When an RC type of oscillator is desired, the oscillator frequency is approximately expressed by:

$$OSC = \frac{0.45}{RC}$$

(R in Ohms and C in Farads), where R > 50kΩ and C > 50pF. For 40kHz frequency which gives 2.5 readings per second, use 100k and 100pF or use 180kΩ and 50pF for lower power loss.

There is a typical variation of about 5% between oscillator frequencies of different parts. The oscillator frequency will decrease 1% for each +25°C rise. For those applications in which normal mode rejection of 60Hz or 50Hz line frequency is critical, a crystal or a precision external oscillator should be used.

Reference Voltage Selection

For a full scale reading the input signal is required to be twice the reference voltage. To be more precise, the full scale reading (±1999) takes place when the input is 1.999 times the V_{REF}. V_{REF} is the potential difference between REF HI and REF LO inputs. Thus, for the nominal 200mV and 2V ranges, V_{REF} should be 100mV and 1V respectively.

In many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0mV, the designer should use the input voltage directly and adjust the V_{REF} for 0.341V. Suitable values for integrating resistor and capacitor would be 620kΩ and 0.047μF. This makes the system slightly quieter and also avoids a divider network on the input.

The on-chip voltage reference (V+ - V_{COMMON}) is normally used to provide the converter reference voltage. However, some applications may desire to use an external reference generator. Various possible schemes exist for reference voltage settings. Figure 11 shows the normal way of using on-chip reference and also a way of using external reference. The value of resistors on both circuit depends on the converter input voltage range. Refer to "Typical Applications" section for various schemes.

Typical Applications

The HI7131 and HI7133 A/D Converters may be used in a wide variety of configurations. The following application circuits show some of the possibilities, and serves to illustrate the exceptional versatility of these devices.

The following application notes contain very useful information on understanding and applying these parts and are available from Harris Semiconductor.

A016
Selecting A/D Converters

A017
The Integrating A/D Converter

A018
Do's and Don'ts of Applying A/D Converters

A032
Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family

A052
Tips for Using Single-Chip $3^1/_2$ Digit A/D Converters

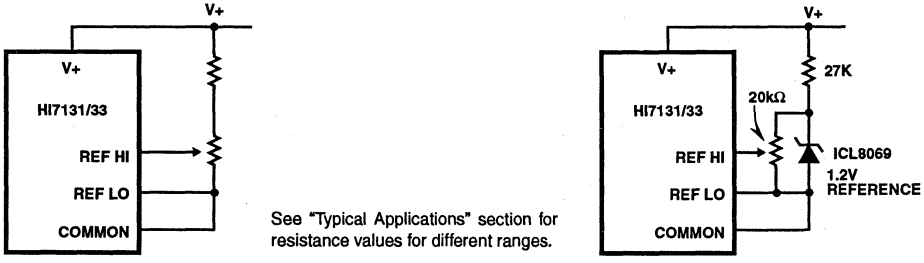
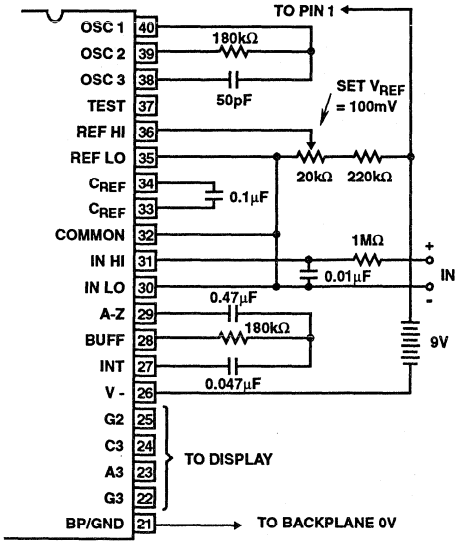


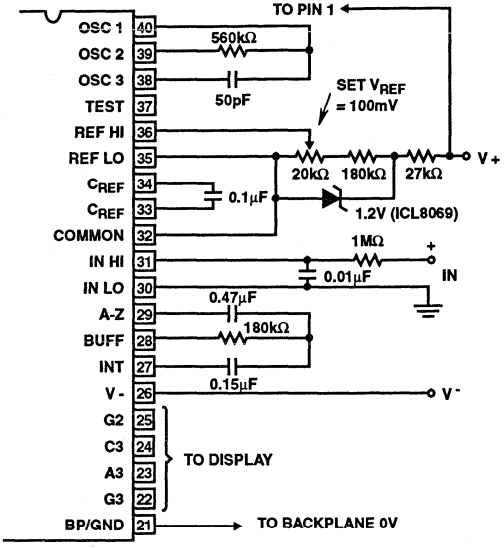
FIGURE 11. HI7131 TYPICAL REFERENCE CIRCUITS

Typical Applications



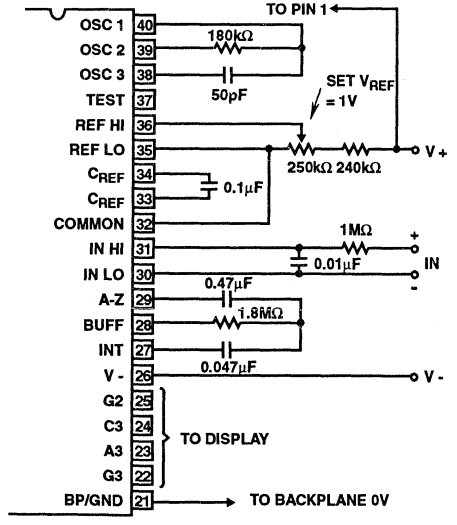
Values shown are for 200mV full-scale, 3 readings/sec., floating supply voltage (9V battery).

FIGURE 12. HI7131 AND HI7133 USING THE INTERNAL REFERENCE



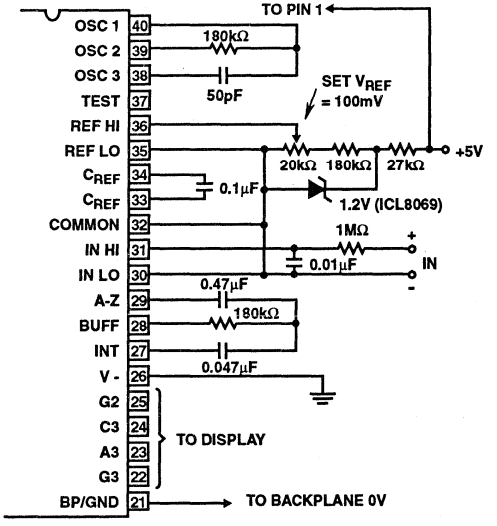
IN LO is tied to supply GND establishing the correct common-mode voltage. COMMON acts as a pre-regulator for the reference. Values shown are for 1 reading/sec.

FIGURE 13. HI7131 AND HI7133 WITH AN EXTERNAL BAND-GAP REFERENCE (1.2V TYPE)



For 1 reading/sec., change C_{INT}, R_{OSC} to values of Figure 12.

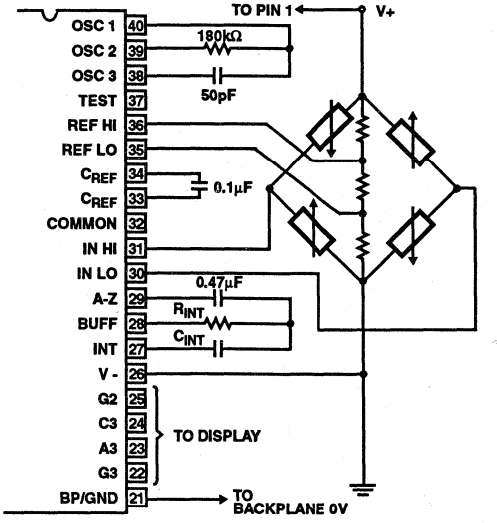
FIGURE 14. RECOMMENDED COMPONENT VALUES FOR 2.000V FULL-SCALE, 3 READINGS PER SEC



An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference. COMMON holds the IN LO almost at the middle of the supply, ≈ 2.7V.

FIGURE 15. HI7131 AND HI7133 OPERATED FROM SINGLE +5V SUPPLY

Typical Applications (Continued)



The resistor values within the bridge are determined by the desired sensitivity.

FIGURE 16A. HI7131 AND HI7133 MEASURING RATIOMETRIC VALUES OF QUAD LOAD CELL

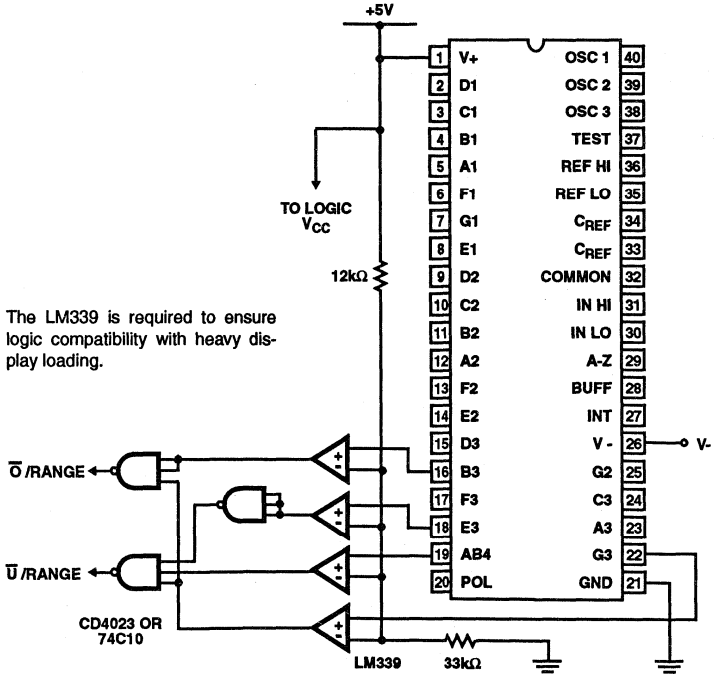
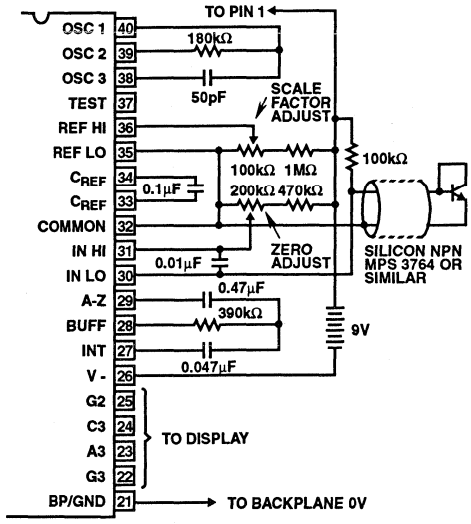


FIGURE 16B. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM HI7133 OUTPUTS

Typical Applications (Continued)



A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading. See AD590 data sheets for alternative circuits.

FIGURE 17A. HI7131 AND HI7133 USED AS A DIGITAL CENTIGRADE THERMOMETER

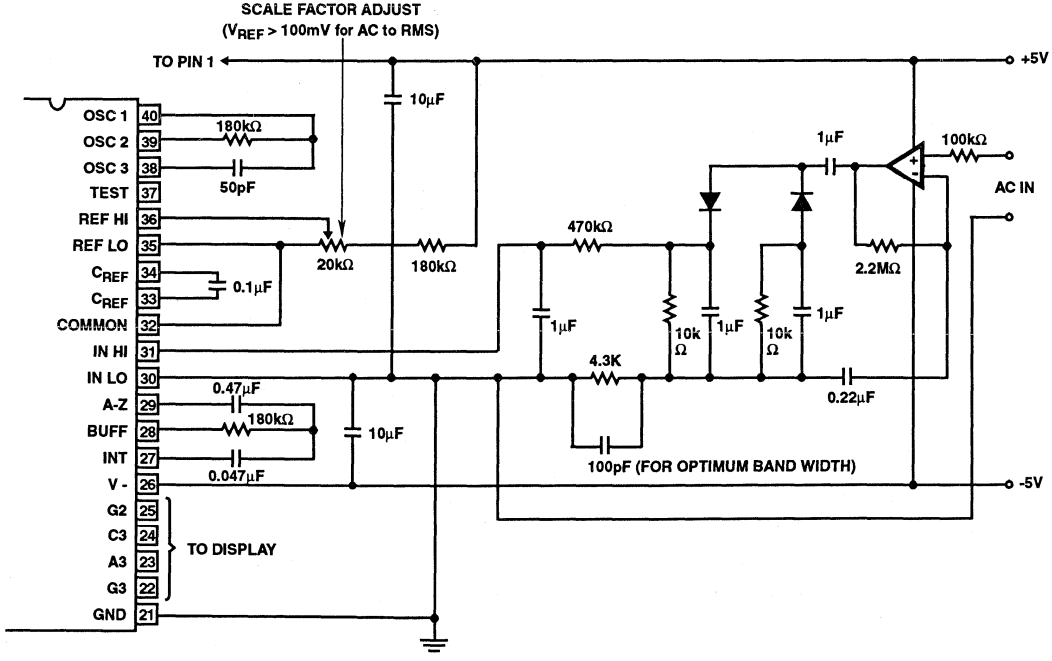
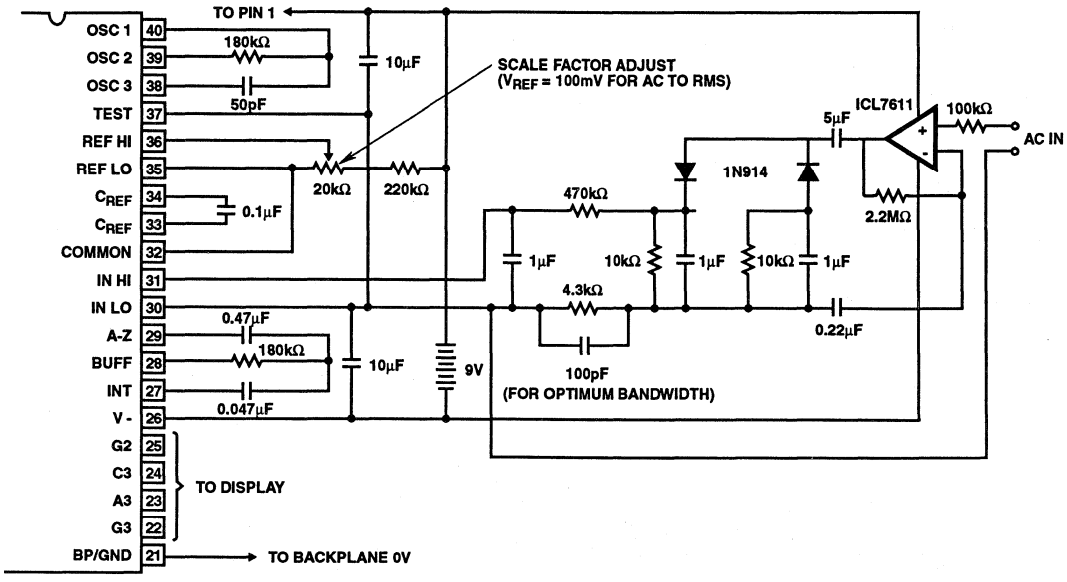


FIGURE 17B. AC TO DC CONVERTER AND HI7133 FOR RMS DISPLAY

FIGURE 17.

Typical Applications (Continued)



Test is used as a common-mode reference level to ensure compatibility with most op amps.

FIGURE 18. AC TO DC CONVERTER WITH HI7131 AND HI7133

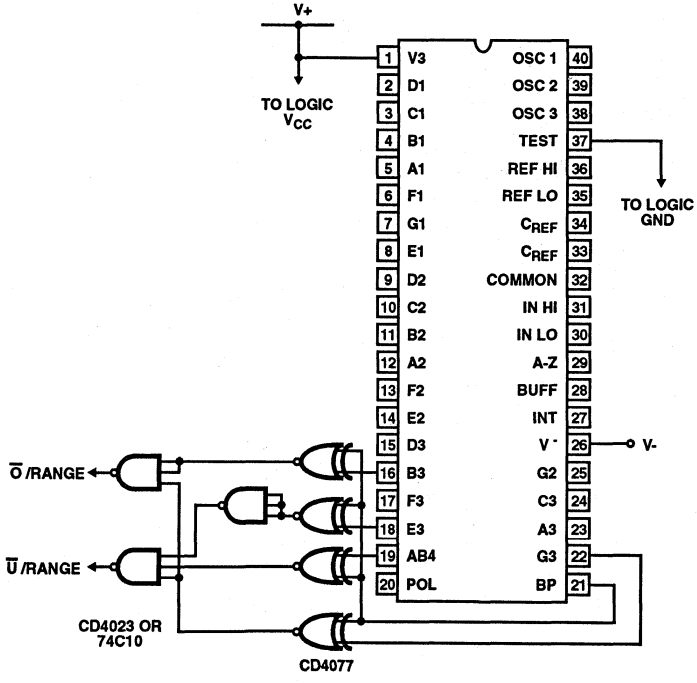


FIGURE 19. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM HI7131 OUTPUTS

Die Characteristics

DIE DIMENSIONS:
127 x 149 Mils

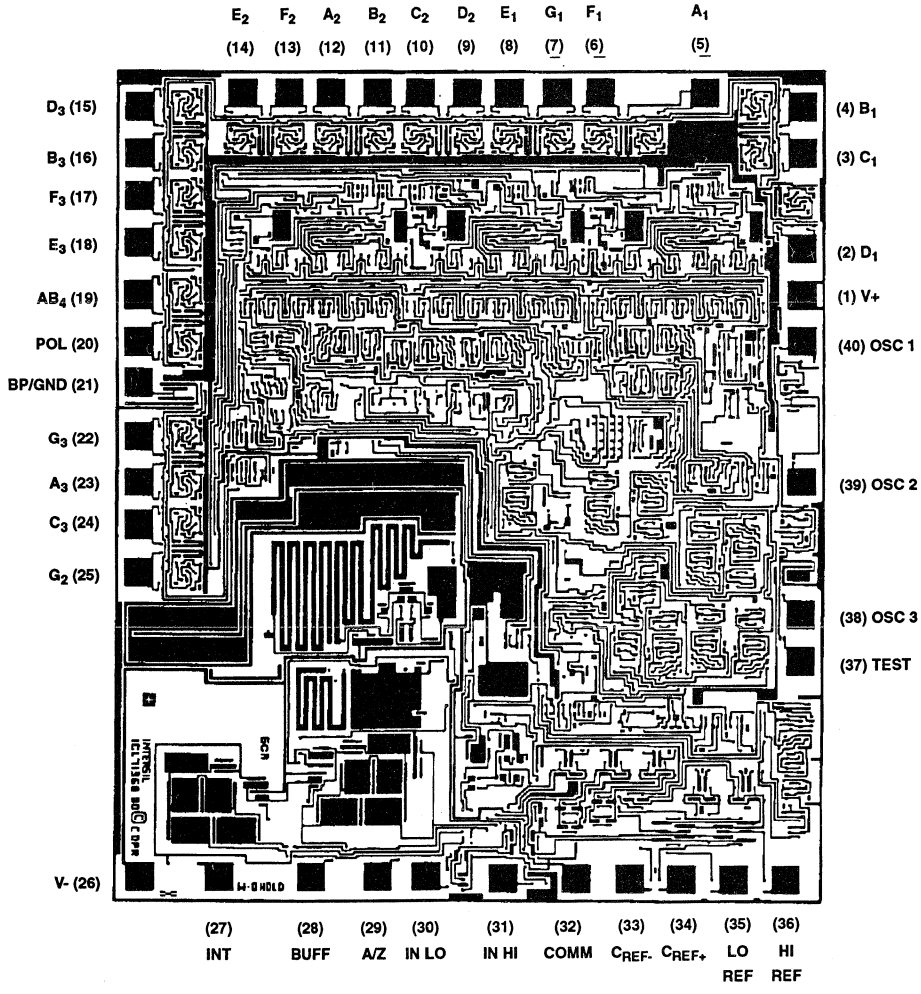
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG Nitride
Thickness: 15kÅ ± 3kÅ

WORST CASE CURRENT DENSITY:
9.1 x 10^4A/cm^2

Metallization Mask Layout

HI7131, HI7133



HARRIS SEMICONDUCTOR

ICL7106, ICL7107

$3^1/_2$ Digit LCD/LED Display A/D Converter

December 1993

Features

- Guaranteed Zero Reading for 0V Input on All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference, Direct Display Drive
  - LCD ICL7106
  - LED ICL7107
- Low Noise - Less Than 15μVp-p
- On Chip Clock and Reference
- Low Power Dissipation - Typically Less Than 10mW
- No Additional Active Circuits Required
- New Small Outline Surface Mount Package Available

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7106CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7106RCPL	0°C to +70°C	40 Lead Plastic DIP (Note 1)
ICL7106CM44	0°C to +70°C	44 Lead Metric Plastic Quad Flatpack
ICL7107CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7107RCPL	0°C to +70°C	40 Lead Plastic DIP (Note 1)
ICL7107CM44	0°C to +70°C	44 Lead Metric Plastic Quad Flatpack

NOTE: 1. "R" indicates device with reversed leads.

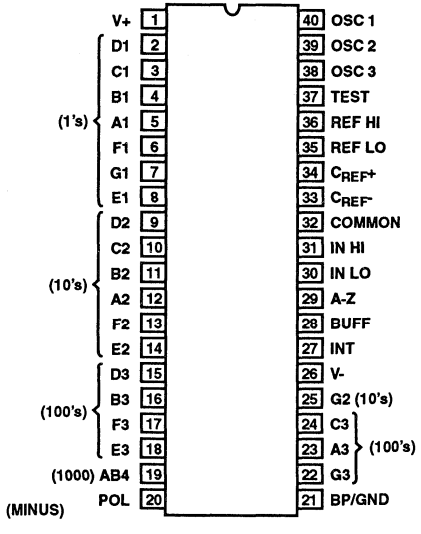
Description

The Harris ICL7106 and ICL7107 are high performance, low power $3^1/_2$ digit A/D converters. Included are seven segment decoders, display drivers, a reference, and a clock. The ICL7106 is designed to interface with a liquid crystal display (LCD) and includes a multiplexed backplane drive; the ICL7107 will directly drive an instrument size light emitting diode (LED) display.

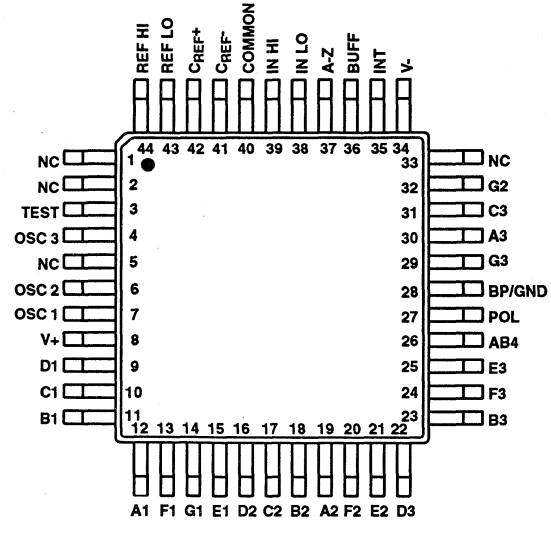
The ICL7106 and ICL7107 bring together a combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge type transducers. Finally, the true economy of single power supply operation (ICL7106), enables a high performance panel meter to be built with the addition of only 10 passive components and a display.

Pinouts

ICL7106, ICL7107
(PDIP)
TOP VIEW



ICL7106, ICL7107
(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3082**

Absolute Maximum Ratings

Supply Voltage
- ICL7106, V+ to V- 15V
- ICL7107, V+ to GND 6V
- ICL7107, V- to GND ..... -9V

Analog Input Voltage (Either Input) (Note 1) ..... V+ to V-
Reference Input Voltage (Either Input) ..... V+ to V-
Clock Input
- ICL7106 ..... TEST to V+
- ICL7107 ..... GND to V+

Thermal Information

Thermal Resistance (MAX, See Note 1) θ_{JA}
- 40 Pin Plastic Package ..... 50°C/W
- 44 Pin MQFP Package ..... 80°C/W

Maximum Power Dissipation
- ICL7106 ..... 1.0W
- ICL7107 ..... 1.2W

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s Max) ..... +265°C
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications (Note 3)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Zero Input Reading	V_{IN} = 0.0V, Full-Scale = 200mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/ 1000	1000	Digital Reading
Rollover Error	$-V_{IN} = +V_{IN} \equiv$ 200mV Difference in Reading for Equal Positive and Negative Inputs Near Full-Scale	-	±0.2	±1	Counts
Linearity	Full-Scale = 200mV or Full-Scale = 2V Maximum Deviation from Best Straight Line Fit (Note 5)	-	±0.2	±1	Counts
Common Mode Rejection Ratio	V_{CM} = 1V, V_{IN} = 0V, Full-Scale = 200mV (Note 5)	-	50	-	µV/V
Noise	V_{IN} = 0V, Full-Scale = 200mV (Pk-Pk Value Not Exceeded 95% of Time)	-	15	-	µV
Leakage Current Input	V_{IN} = 0 (Note 5)	-	1	10	pA
Zero Reading Drift	V_{IN} = 0, 0° < T_A < +70°C (Note 5)	-	0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199mV, 0° < T_A < +70°C, (Ext. Ref. 0ppm/°C) (Note 5)	-	1	5	ppm/°C
End Power Supply Character V+ Supply Current	V_{IN} = 0 (Does Not Include LED Current for ICL7107)	-	0.8	1.8	mA
End Power Supply Character V- Supply Current	ICL7107 Only	-	0.6	1.8	mA
COMMON Pin Analog Common Voltage	25kΩ Between Common and Positive Supply (With Respect to + Supply)	2.4	2.8	3.2	V
Temperature Coefficient of Analog Common	25kΩ Between Common and Positive Supply (With Respect to + Supply)	-	80	-	ppm/°C
DISPLAY DRIVER ICL7106 ONLY					
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V+= to V- = 9V, (Note 4)	4	5	6	V

Electrical Specifications (Note 3) (Continued)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ICL7107 ONLY					
Segment Sinking Current	V+ = 5V, Segment Voltage = 3V				
(Except Pin 19 and 20)		5	8	-	mA
Pin 19 Only		10	16	-	mA
Pin 20 Only		4	7	-	mA

NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless otherwise noted, specifications apply to both the ICL7106 and ICL7107 at T_A = +25°C, f_{CLOCK} = 48kHz. ICL7106 is tested in the circuit of Figure 1. ICL7107 is tested in the circuit of Figure 2.
4. Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
5. Not tested, guaranteed by design.

Typical Applications and Test Circuits

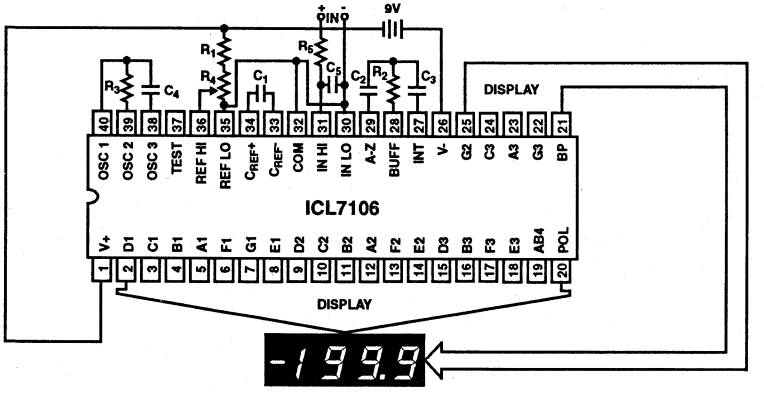


FIGURE 1. ICL7106 TEST CIRCUIT AND TYPICAL APPLICATION WITH LCD DISPLAY COMPONENTS SELECTED FOR 200mV FULL-SCALE

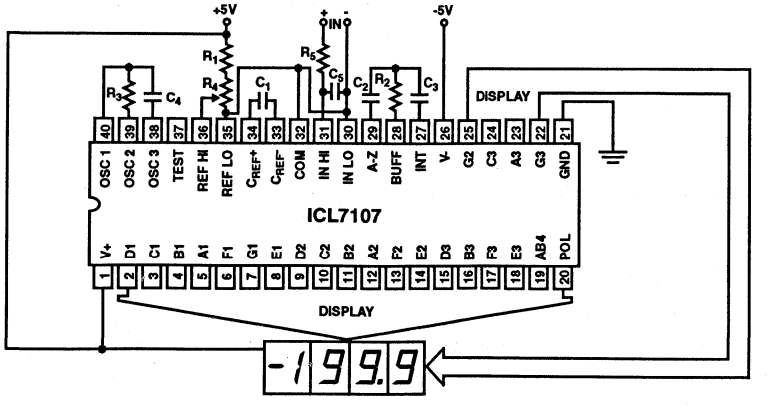
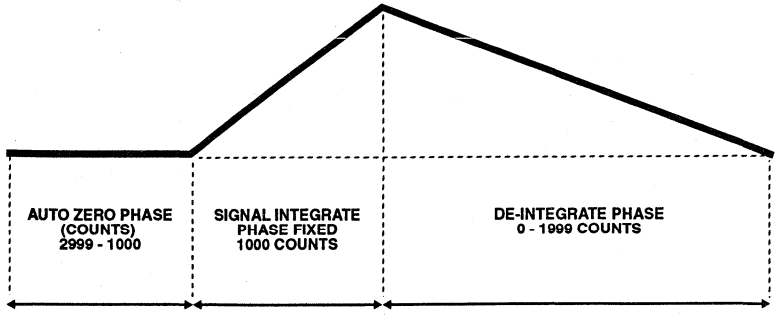


FIGURE 2. ICL7107 TEST CIRCUIT AND TYPICAL APPLICATION WITH LED DISPLAY COMPONENTS SELECTED FOR 200mV FULL-SCALE

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**
  $f_{OSC} = 0.45/RC$
  $C_{OSC} > 50pF$; $R_{OSC} > 50K\Omega$
  f_{OSC} Typ. = 48KHz
- **OSCILLATOR PERIOD**
  $t_{OSC} = RC/0.45$
- **INTEGRATION CLOCK FREQUENCY**
  $f_{CLOCK} = f_{OSC}/4$
- **INTEGRATION PERIOD**
  $t_{INT} = 1000 \times (4/f_{OSC})$
- **60/50Hz REJECTION CRITERION**
  t_{INT}/t_{60Hz} or t_{INT}/t_{60Hz} = Integer
- **OPTIMUM INTEGRATION CURRENT**
  $I_{INT} = 4.0\mu A$
- **FULL-SCALE ANALOG INPUT VOLTAGE**
  V_{INFS} Typically = 200mV or 2.0V
- **INTEGRATE RESISTOR**
  $$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$
- **INTEGRATE CAPACITOR**
  $$C_{INT} = \frac{(t_{INT})\,(I_{INT})}{V_{INT}}$$
- **INTEGRATOR OUTPUT VOLTAGE SWING**
  $$V_{INT} = \frac{(t_{INT})\,(I_{INT})}{C_{INT}}$$
- **V_{INT} MAXIMUM SWING:**
  $(V- + 0.5V) < V_{INT} < (V+ - 0.5V)$, V_{INT} typically = 2.0V
- **DISPLAY COUNT**
  $$COUNT = 1000 \times \frac{V_{IN}}{V_{REF}}$$
- **CONVERSION CYCLE**
  $t_{CYC} = t_{CLOCK} \times 4000$
  $t_{CYC} = t_{OSC} \times 16{,}000$
  when $f_{OSC} = 48KHz$; $t_{CYC} = 333ms$
- **COMMON MODE INPUT VOLTAGE**
  $(V- + 1.0V) < V_{IN} < (V+ - 0.5V)$
- **AUTO-ZERO CAPACITOR**
  $0.01\mu F < C_{AZ} < 1.0\mu F$
- **REFERENCE CAPACITOR**
  $0.1\mu F < C_{REF} < 1.0\mu F$
- **V_{COM}**
  Biased between Vi and V-.
- **$V_{COM} \cong V+ - 2.8V$**
  Regulation lost when V+ to V- < ≅6.8V.
  If V_{COM} is externally pulled down to (V + to V -)/2, the V_{COM} circuit will turn off.
- **ICL7106 POWER SUPPLY: SINGLE 9V**
  V+ - V- = 9V
  Digital supply is generated internally
  $V_{GND} \cong V+ - 4.5V$
- **ICL7106 DISPLAY: LCD**
  Type: Direct drive with digital logic supply amplitude.
- **ICL7107 POWER SUPPLY: DUAL ±5.0V**
  V+ = +5.0V to GND
  V- = -5.0V to GND
  Digital Logic and LED driver supply V+ to GND
- **ICL7107 DISPLAY: LED**
  Type: Non-Multiplexed Common Anode

Typical Integrator Amplifier Output Waveform (INT Pin)



TOTAL CONVERSION TIME = 4000 x t_{CLOCK} = 16,000 x t_{OSC}

Detailed Description

Analog Section

Figure 3 shows the Analog Section for the ICL7106 and ICL7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to 1V from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is:

$$\text{DISPLAY COUNT} = 1000\left(\frac{V_{IN}}{V_{REF}}\right).$$

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

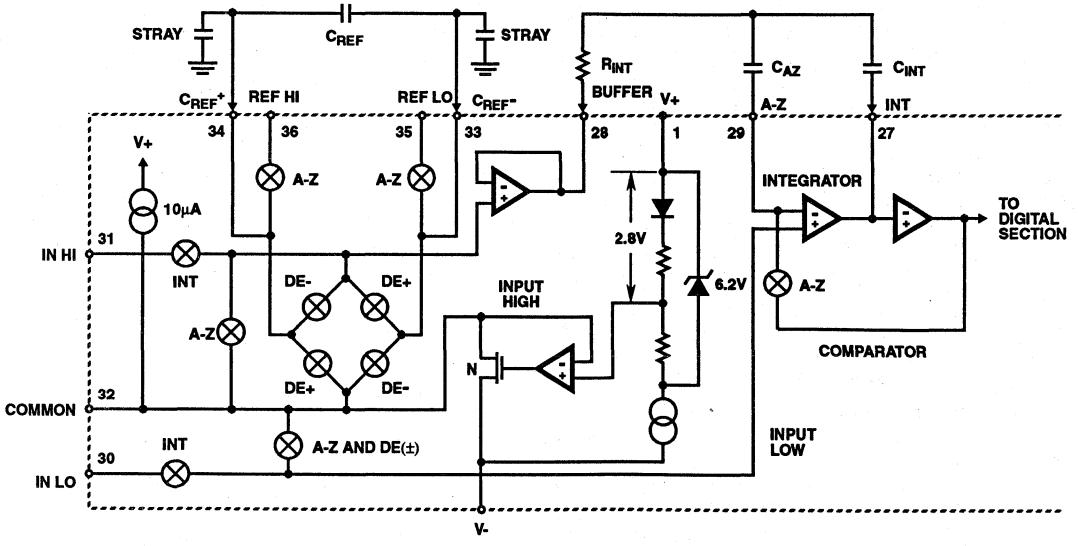


FIGURE 3. ANALOG SECTION OF ICL7106 AND ICL7107

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (ICL7106) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/V), low output impedance (≅15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on chip reference should also be recognized, however. With the ICL7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full-scale from 25μV to 80μVp-p. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111(8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an over-range condition. This is because over-range is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between over-range and a non-over-range count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The ICL7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink approximately 30mA of current to hold the voltage 2.8V below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus overriding the internal reference.

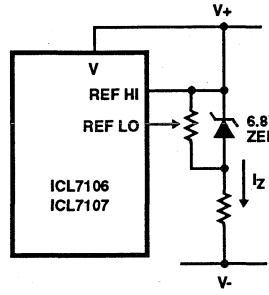


FIGURE 4A.

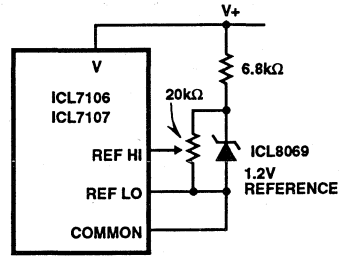


FIGURE 4B.

FIGURE 4. USING AN EXTERNAL REFERENCE

TEST

The TEST pin serves two functions. On the ICL7106 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

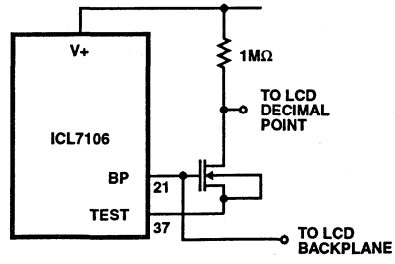


FIGURE 5. SIMPLE INVERTER FOR FIXED DECIMAL POINT

The second function is a "lamp test". When TEST is pulled high (to V+) all segments will be turned on and the display should read "1888". The TEST pin will sink about 15mA under these conditions.

CAUTION: In the lamp test mode, the segments have a constant DC voltage (no square-wave). This may burn the LCD display if maintained for extended periods.

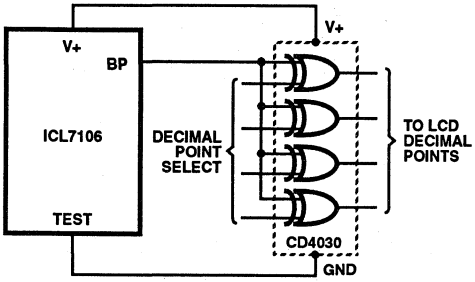


FIGURE 6. EXCLUSIVE 'OR' GATE FOR DECIMAL POINT DRIVE

Digital Section

Figures 7 and 8 show the digital section for the ICL7106 and ICL7107, respectively. In the ICL7106, an internal digital ground is generated from a 6V Zener diode and a large P-channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 8 is the Digital Section of the ICL7107. It is identical to the ICL7106 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2mA to 8mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is "on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

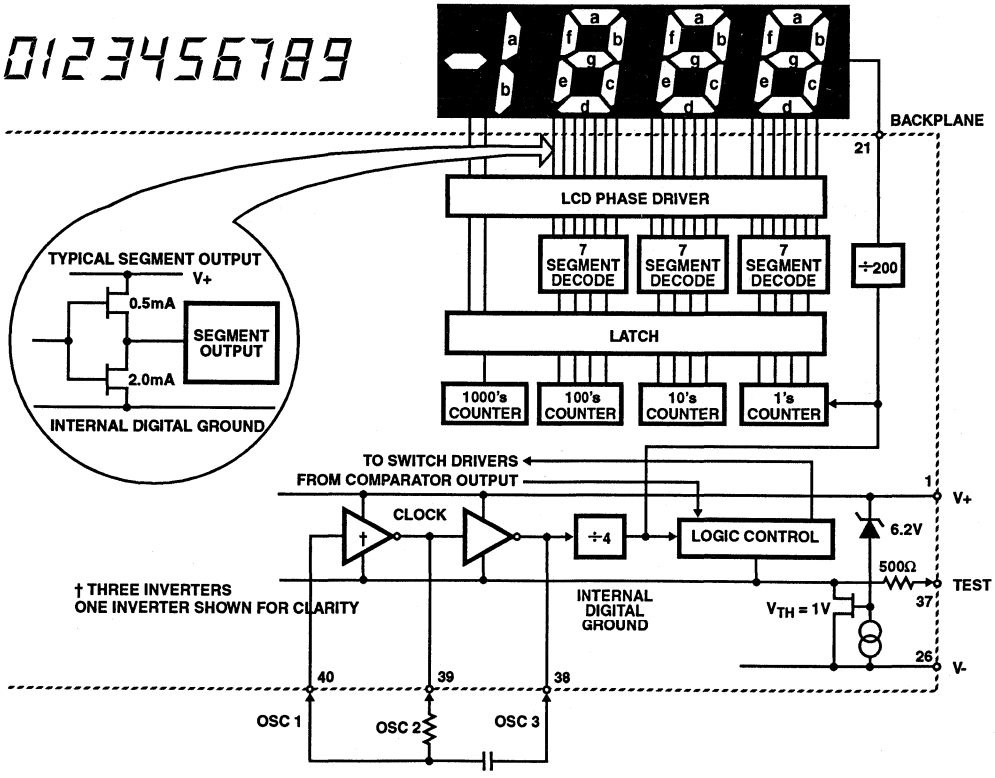


FIGURE 7. ICL7106 DIGITAL SECTION

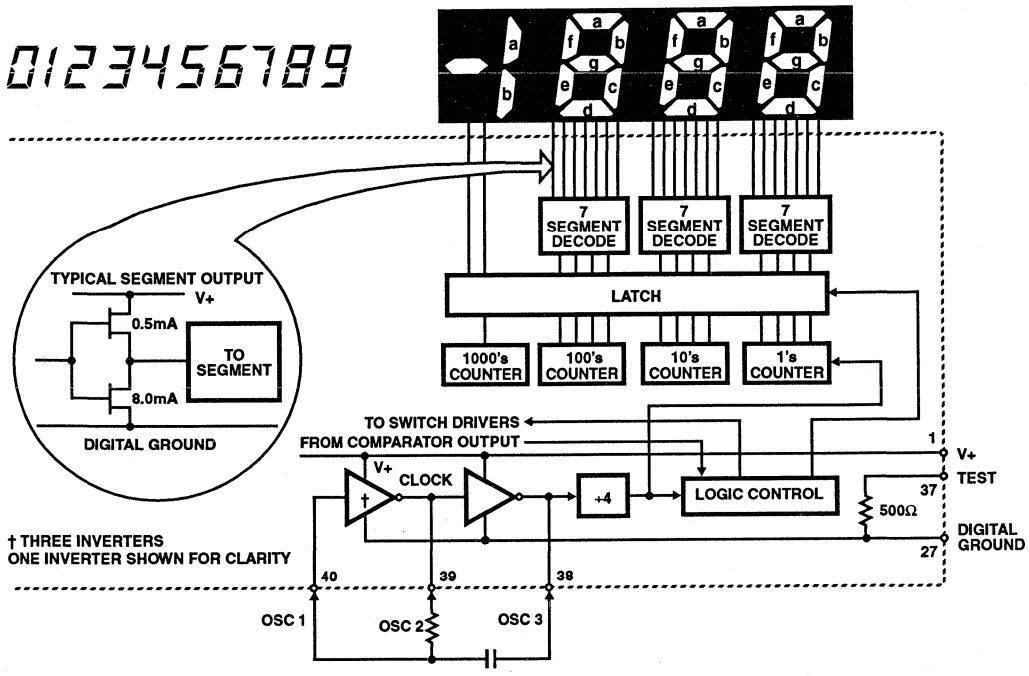


FIGURE 8. ICL7107 DIGITAL SECTION

System Timing

Figure 9 shows the clocking arrangement used in the ICL7106 and ICL7107. Two basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, $33^1/_3$kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, $66^2/_3$kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz).

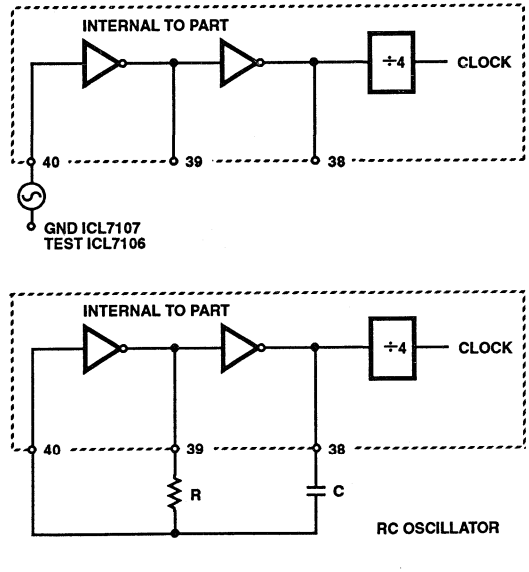


FIGURE 9. CLOCK CIRCUITS

Component Value Selection

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 4μA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 470kΩ is near optimum and similarly a 47kΩ for a 200mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance buildup will not saturate the integrator swing (approximately. 0.3V from either supply). In the ICL7106 or the ICL7107, when the analog COMMON is used as a reference, a nominal +2V full-scale integrator swing is fine. For the ICL7107 with +5V supplies and analog COMMON tied to supply ground, a ±3.5V to +4V swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22μF and 0.10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47μF capacitor is recommended. On the 2V scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation

$f = \frac{0.45}{RC}$ For 48kHz Clock (3 Readings/second),

C = 100pF

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200mV and 2V scale, V_{REF} should equal 100mV and 1V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.662V. Instead of dividing the input down to 200mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. Suitable values for integrating resistor and capacitor would be 1 20kΩ and 0.22μF. This makes the system slightly quieter and also avoids a divider network on the input. The ICL7107 with ±5V supplies can accept input signals up to ±4V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable fare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

ICL7107 Power Supplies

The ICL7107 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application. See ICL7660 data sheet for an alternative.

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5V.
3. An external reference is used.

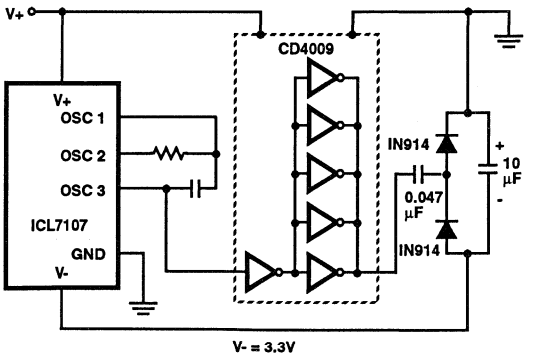


FIGURE 10. GENERATING NEGATIVE SUPPLY FROM +5V

Typical Applications

The ICL7106 and ICL7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

The following application notes contain very useful information on understanding and applying this part and are available from Harris semiconductor.

Application Notes

A016 "Selecting A/D Converters"

A017 "The Integrating A/D Converter"

A018 "Do's and Don'ts of Applying A/D Converters"

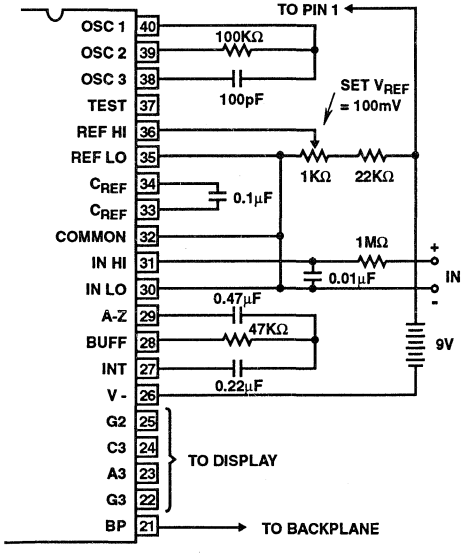
A023 "Low Cost Digital Panel Meter Designs"

A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family"

A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7106"

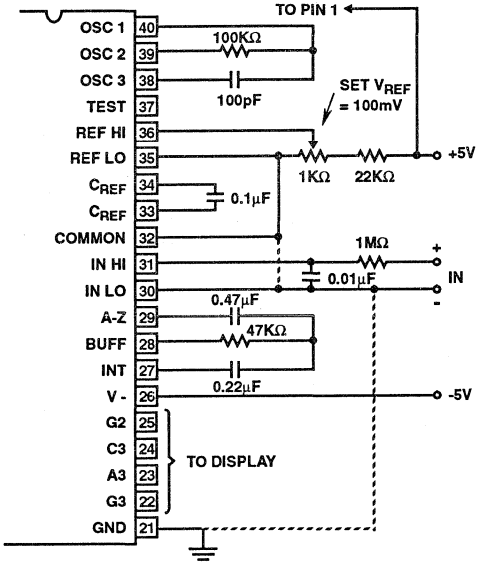
A052 "Tips for Using Single Chip $3^1/_2$ Digit A/D Converters"

Typical Applications



Values shown are for 200mV full-scale, 3 readings/sec., floating supply voltage (9V battery).

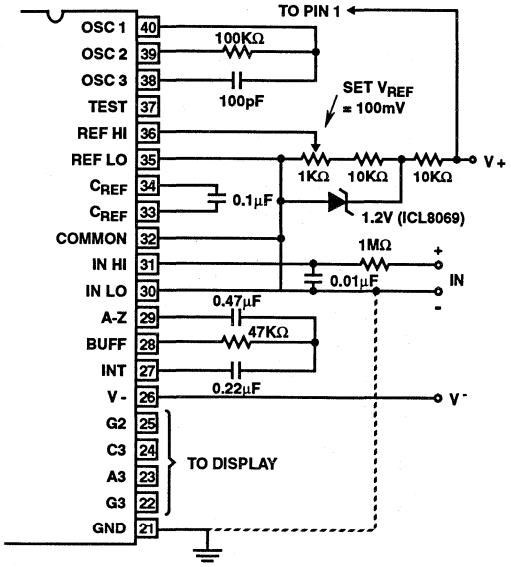
FIGURE 11. ICL7106 USING THE INTERNAL REFERENCE



Values shown are for 200mV full-scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

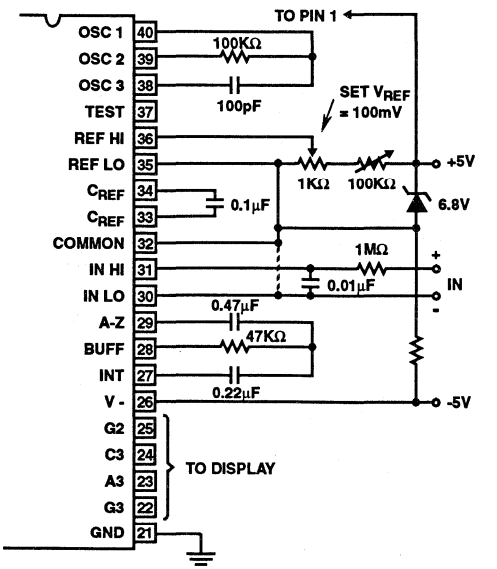
FIGURE 12. ICL7107 USING THE INTERNAL REFERENCE

Typical Applications (Continued)



IN LO is tied to supply COMMON establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply GND) and the pre-regulator is overridden.

FIGURE 13. ICL7107 WITH AN EXTERNAL BAND-GAP REFERENCE (1.2V TYPE)



Since low TC zeners have breakdown voltages ~ 6.8V, diode must be plasced across the total supply (10V). As in the case of Figure 14, IN LO may be tied to either COMMON or GND

FIGURE 14. ICL7107 WITH ZENER DIODE REFERENCE

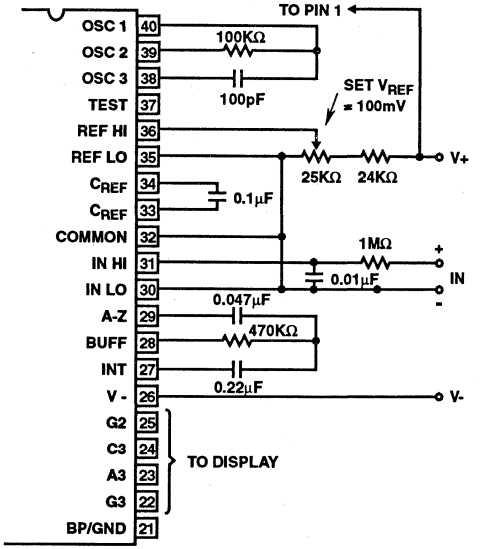
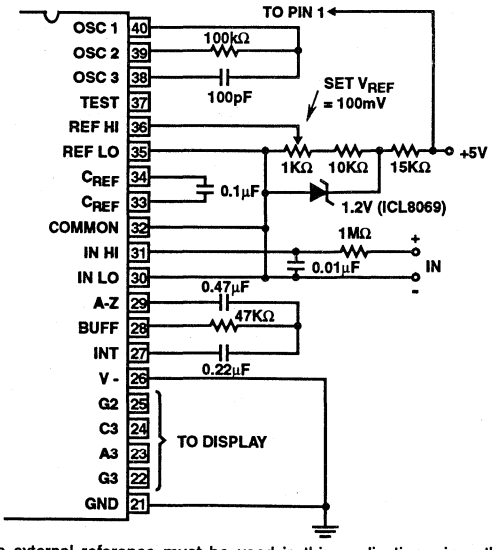


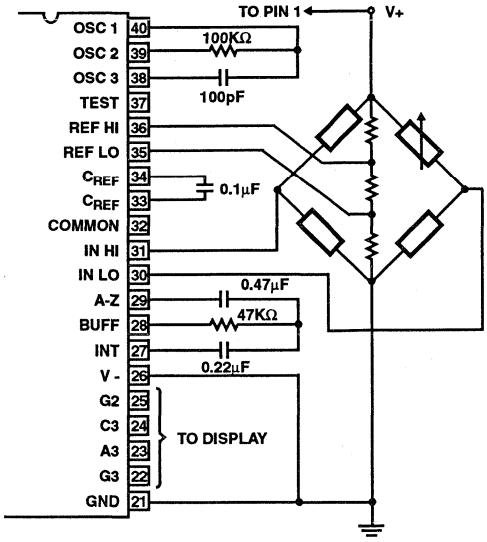
FIGURE 15. ICL7106 AND ICL7107: RECOMMENDED COMPONENT VALUES FOR 2.0V FULL-SCALE



An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.

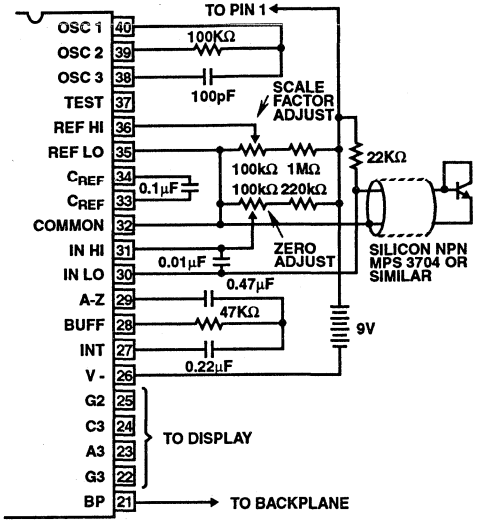
FIGURE 16. ICL7107 OPERATED FROM SINGLE +5V

Typical Applications (Continued)



The resistor values within the bridge are determined by the desired sensitivity.

FIGURE 17. ICL7107 MEASUREING RATIOMETRIC VALUES OF QUAD LOAD CELL



A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

FIGURE 18. ICL7106 USED AS A DIGITAL CENTIGRADE THERMOMETER

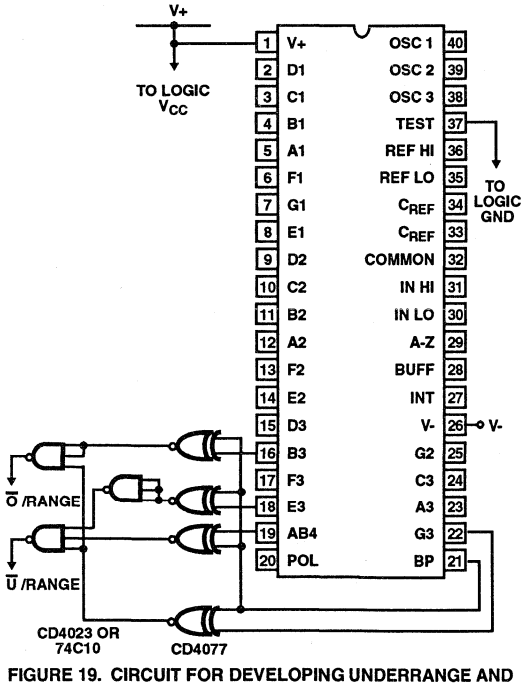


FIGURE 19. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNAL FROM ICL7106 OUTPUTS

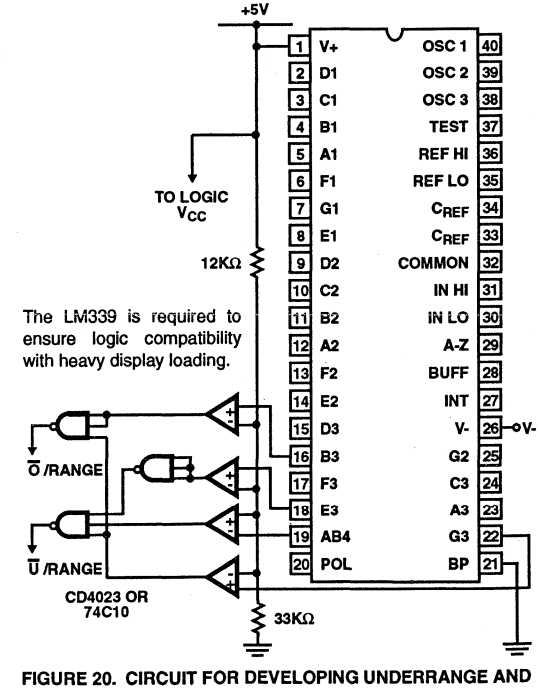
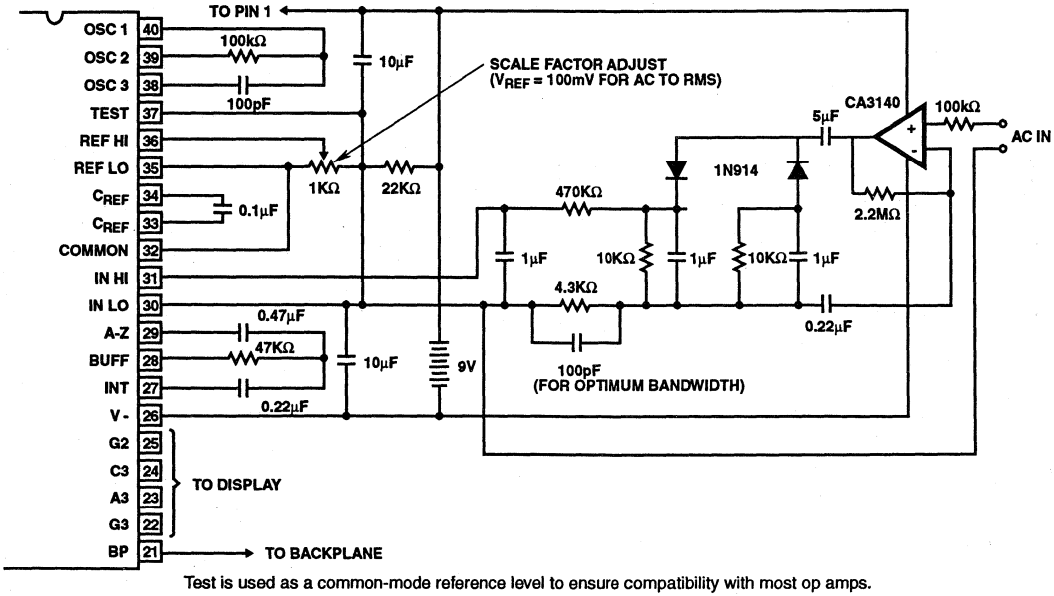


FIGURE 20. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM ICL7107 OUTPUT

Typical Applications (Continued)



Test is used as a common-mode reference level to ensure compatibility with most op amps.

FIGURE 21. AC TO DC CONVERTER WITH ICL7106

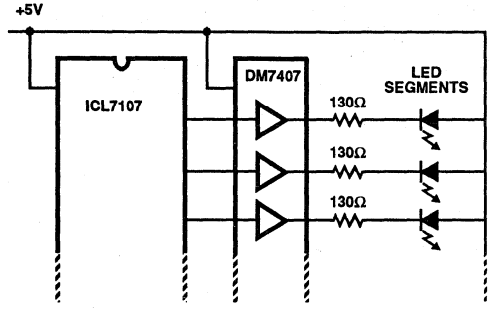


FIGURE 22. DISPLAY BUFFERING FOR INCREASED DRIVE CURRENT

HARRIS SEMICONDUCTOR

ICL7116, ICL7117

$3^1/_2$ Digit LCD/LED Display A/D Converter with Display Hold

December 1993

Features

- HOLD Reading Input Allows Indefinite Display Hold
- Guaranteed Zero Reading for 0V Input
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- Direct Display Drive
  - LCD ICL7116
  - LED ICL7117
- Low Noise - Less Than 15μVp-p (Typ)
- On Chip Clock and Reference
- Low Power Dissipation - Typically Less Than 10mW
- No Additional Active Circuits Required
- Small Outline Surface Mount Package Available

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7116CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7116CM44	0°C to +70°C	44 Lead Metric Plastic Quad Flatpack
ICL7117CPL	0°C to +70°C	40 Lead Plastic DIP

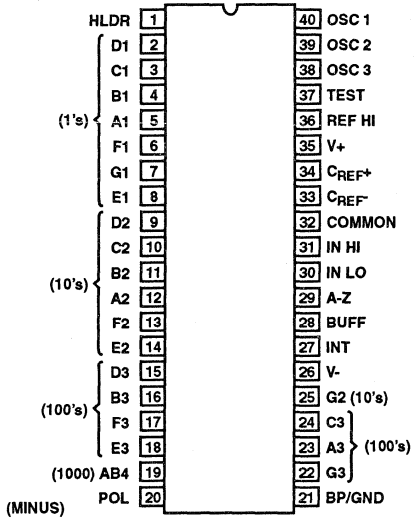
Description

The Harris ICL7116 and ICL7117 are high performance, low power $3^1/_2$ digit A/D converters. Included are seven segment decoders, display drivers, a reference, and a clock. The ICL7116 is designed to interface with a liquid crystal display (LCD) and includes a multiplexed backplane drive. The ICL7117 will directly drive an instrument size, light emitting diode (LED) display.

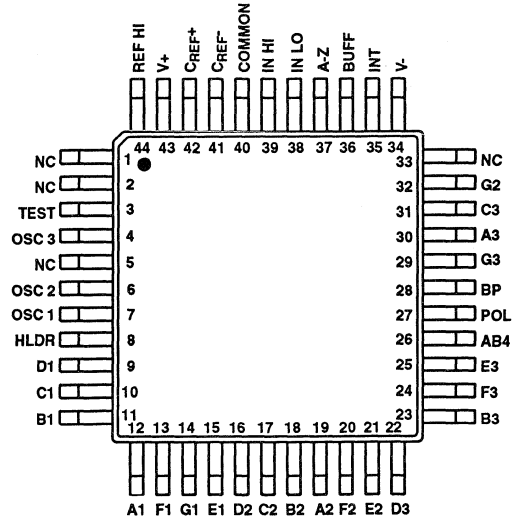
The ICL7116 and ICL7117 have all of the features of the ICL7106 and ICL7107 with the addition of a HOLD Reading input. With this input, it is possible to make a measurement and retain the value on the display indefinitely. To make room for this feature the reference low input has been connected to Common internally rather than being fully differential. These circuits retain the accuracy, versatility, and true economy of the ICL7106 and ICL7107. They feature auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally, the true economy of single power supply operation (ICL7116) enables a high performance panel meter to be built with the addition of only eleven passive components and a display.

Pinouts

ICL7116, ICL7117
(PDIP)
TOP VIEW



ICL7116
(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3083**

Absolute Maximum Ratings

Supply Voltage
- ICL7116, V+ to V- 15V
- ICL7117, V+ to GND 6V
- ICL7117, V- to GND ..... -9V

Analog Input Voltage (Either Input) (Note 1) ..... V+ to V-
Reference Input Voltage (Either Input) ..... V+ to V-
Clock Input
- ICL7116 ..... TEST to V+
- ICL7117 ..... GND to V+

Thermal Information

Thermal Resistance (MAX, See Note 1)	θ_{JA}
40 Lead Plastic Package	50°C/W
44 Lead MQFP Package	80°C/W

Maximum Power Dissipation (Note 1)
- ICL7116 ..... 1.0W
- ICL7117 ..... 1.2W

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s Max) ..... +300°C
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications (Notes 2, 3) T_A = +25°C, f_{CLOCK} = 48kHz, V_{REF} = 100mV

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Zero Input Reading	V_{IN} = 0.0V, Full-Scale = 200mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error	$-V_{IN} = +V_{IN} \cong$ 195mV Difference in Reading for Equal Positive and Negative Inputs Near Full-Scale	-	±0.2	±1	Counts
Linearity	Full-Scale = 200mV or Full-Scale = 2V Maximum Deviation from Best Straight Line Fit (Note 5)	-	±0.2	±1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V, Full-Scale = 200mV (Note 5)	-	50	-	µV/V
Noise	V_{IN} = 0V, Full-Scale = 200mV (Pk-Pk Value Not Exceeded 95% of Time) (Note 5)	-	15	-	µV
Leakage Current Input	V_{IN} = 0 (Note 5)	-	1	10	pA
Zero Reading Drift	V_{IN} = 0, 0° < T_A < +70°C (Note 5)	-	0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199mV, 0° < T_A < +70°C, (Note 5)	-	1	5	ppm/°C
V+ Supply Current	V_{IN} = 0 (Does Not Include LED Current for ICL7117)	-	0.8	1.8	mA
V- Supply Current	ICL7117 Only	-	0.6	1.8	mA
COMMON Pin Analog Common Voltage	25kΩ Between Common and Positive Supply (With Respect to + Supply)	2.4	2.8	3.2	V
Temperature Coefficient of Analog Common	25kΩ Between Common and Positive Supply (With Respect to + Supply) (Note 5)	-	80	-	ppm/°C
DISPLAY DRIVER ICL7116 ONLY					
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V+ = to V- = 9V, (Note 4)	4	5	6	V
ICL7117 ONLY					
Segment Sinking Current	V+ = 5V, Segment Voltage = 3V				
(Except Pin 19 and 20)		5	8	-	mA
Pin 19 Only		10	16	-	mA
Pin 20 Only		4	7	-	mA

NOTES:
1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.
3. Unless otherwise noted, specifications apply to both the ICL7116 and ICL7117. ICL7116 is tested in the circuit of Figure 1. ICL7117 is tested in the circuit of Figure 2.
4. Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
5. Not tested, guaranteed by design.

Typical Applications and Test Circuits

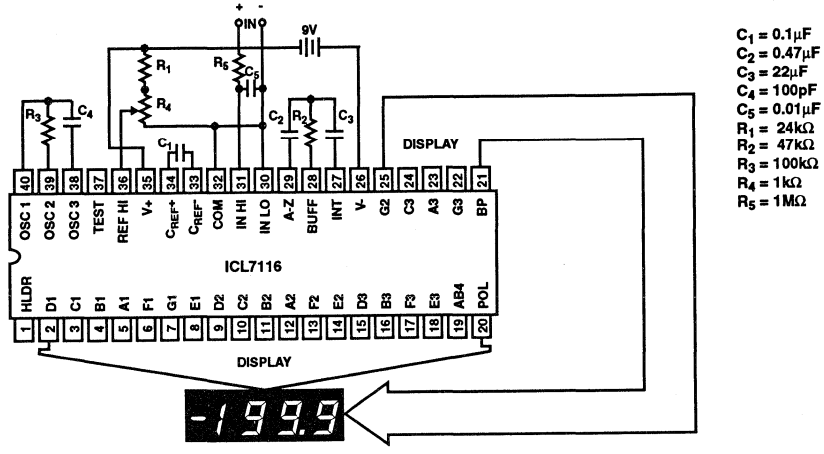


FIGURE 1. ICL7116 TEST CIRCUIT AND TYPICAL APPLICATION WITH LCD DISPLAY COMPONENTS SELECTED FOR 200mV FULL-SCALE

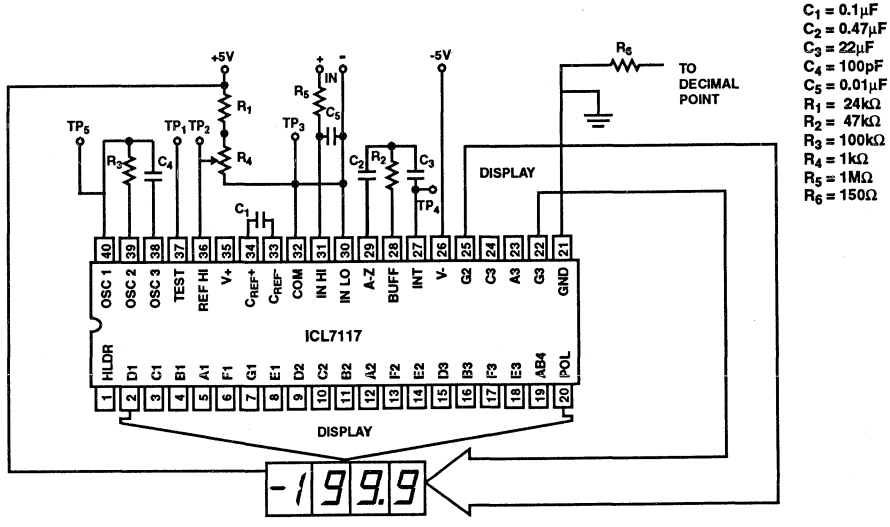
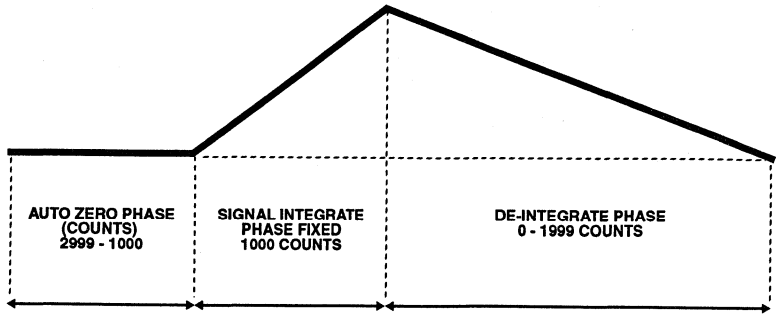


FIGURE 2. ICL7117 TEST CIRCUIT AND TYPICAL APPLICATION WITH LED DISPLAY COMPONENTS SELECTED FOR 200mV FULL-SCALE

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**
  $f_{OSC} = 0.45/RC$
  $C_{OSC} > 50pF$; $R_{OSC} > 50K\Omega$
  f_{OSC} Typ. = 48KHz
- **OSCILLATOR PERIOD**
  $t_{OSC} = RC/0.45$
- **INTEGRATION CLOCK FREQUENCY**
  $f_{CLOCK} = f_{OSC}/4$
- **INTEGRATION PERIOD**
  $t_{INT} = 1000 \times (4/f_{OSC})$
- **60/50Hz REJECTION CRITERION**
  t_{INT}/t_{60Hz} or t_{INT}/t_{50Hz} = Integer
- **OPTIMUM INTEGRATION CURRENT**
  $I_{INT} = 4.0\mu A$
- **FULL-SCALE ANALOG INPUT VOLTAGE**
  V_{INFS} Typically = 200mV or 2.0V
- **INTEGRATE RESISTOR**
  $$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$
- **INTEGRATE CAPACITOR**
  $$C_{INT} = \frac{(t_{INT})\ (I_{INT})}{V_{INT}}$$
- **INTEGRATOR OUTPUT VOLTAGE SWING**
  $$V_{INT} = \frac{(t_{INT})\ (I_{INT})}{C_{INT}}$$
- **V_{INT} MAXIMUM SWING:**
  $(V- + 1.0V) < V_{INT} < (V+ - 0.5V)$, V_{INT} typically = 2.0V
- **DISPLAY COUNT**
  $$COUNT = 1000 \times \frac{V_{IN}}{V_{REF}}$$
- **CONVERSION CYCLE**
  $t_{CYC} = t_{CLOCK} \times 4000$
  $t_{CYC} = t_{OSC} \times 16{,}000$
  when f_{OSC} = 48KHz; t_{CYC} = 333ms
- **COMMON MODE INPUT VOLTAGE**
  $(V- + 1.0V) < V_{IN} < (V+ - 0.5V)$
- **AUTO-ZERO CAPACITOR**
  $0.01\mu F < C_{AZ} < 1.0\mu F$
- **REFERENCE CAPACITOR**
  $0.1\mu F < C_{REF} < 1.0\mu F$
- **V_{COM}**
  Biased between V+ and V-.
- **$V_{COM} \cong$ V+ - 2.8V**
  Regulation lost when V+ to V- < ≅6.8V.
  If V_{COM} is externally pulled down to (V + to V -)/2, the V_{COM} circuit will turn off.
- **ICL7116 POWER SUPPLY: SINGLE 9V**
  V+ - V- = 9V
  Digital supply is generated internally
  $V_{TEST} \cong$ V+ - 4.5V
- **ICL7116 DISPLAY: LCD**
  Type: Direct drive with digital logic supply amplitude.
- **ICL7117 POWER SUPPLY: DUAL ±5.0V**
  V+ = +5.0V to GND
  V- = -5.0V to GND
  Digital Logic and LED driver supply V+ to GND
- **ICL7117 DISPLAY: LED**
  Type: Non-Multiplexed Common Anode

Typical Integrator Amplifier Output Waveform (INT Pin)



TOTAL CONVERSION TIME = 4000 x t_{CLOCK} = 16,000 x t_{OSC}

Pin Description

PIN NUMBER				
40 PIN DIP	44 PIN FLATPACK	NAME	FUNCTION	DESCRIPTION
1	8	HLDR	INPUT	Display Hold Control
2	9	D1	OUTPUT	Driver Pin for Segment "D" of the display units digit
3	10	C1	OUTPUT	Driver Pin for Segment "C" of the display units digit
4	11	B1	OUTPUT	Driver Pin for Segment "B" of the display units digit
5	12	A1	OUTPUT	Driver Pin for Segment "A" of the display units digit
6	13	F1	OUTPUT	Driver Pin for Segment "F" of the display units digit
7	14	G1	OUTPUT	Driver Pin for Segment "G" of the display units digit
8	15	E1	OUTPUT	Driver Pin for Segment "E" of the display units digit
9	16	D2	OUTPUT	Driver Pin for Segment "D" of the display tens digit
10	17	C2	OUTPUT	Driver Pin for Segment "C" of the display tens digit
11	18	B2	OUTPUT	Driver Pin for Segment "B" of the display tens digit
12	19	A2	OUTPUT	Driver Pin for Segment "A" of the display tens digit
13	20	F2	OUTPUT	Driver Pin for Segment "F" of the display tens digit
14	21	E2	OUTPUT	Driver Pin for Segment "E" of the display tens digit
15	22	D3	OUTPUT	Driver pin for segment "D" of the display hundreds digit
16	23	B3	OUTPUT	Driver pin for segment "B" of the display hundreds digit
17	24	F3	OUTPUT	Driver pin for segment "F" of the display hundreds digit
18	25	E3	OUTPUT	Driver pin for segment "E" of the display hundreds digit
19	26	AB4	OUTPUT	Driver pin for both "A" and "B" segments of the display thousands digit
20	27	POL	OUTPUT	Driver pin for the negative sign of the display
21	28	BP/GND	OUTPUT	Driver pin for the LCD backplane/Power Supply Ground
22	29	G3	OUTPUT	Driver pin for segment "G" of the display hundreds digit
23	30	A3	OUTPUT	Driver pin for segment "A" of the display hundreds digit
24	31	C3	OUTPUT	Driver pin for segment "C" of the display hundreds digit
25	32	G2	OUTPUT	Driver pin for segment "G" of the display tens digit
26	34	V-	SUPPLY	Negative power supply
27	35	INT	OUTPUT	Integrator amplifier output. To be connected to integrating capacitor
28	36	BUFF	OUTPUT	Input buffer amplifier output. To be connected to integrating resistor
29	37	A-Z	INPUT	Integrator amplifier input.To be connected to auto-zero capacitor
30 31	38 39	IN LO IN HI	INPUT	Differential inputs. To be connected to input voltage to be measured. LO & HI designators are for reference and do not imply that LO should be connected to lower potential, e.g. for negative inputs IN LO has a higher potential than IN HI.
32	40	COMMON	SUPPLY/ OUTPUT	Internal voltage reference output.
33 34	41 42	C_{REF}- C_{REF}+		Connection pins for reference capacitor.
35 36	43 44	V+ REF HI	SUPPLY	Power Supply
37	3	TEST	INPUT	Display test. Turns on all segments when tied to V+.
38 39 40	4 6 7	OSC3 OSC2 OSC1	OUTPUT OUTPUT INPUT	Device clock generator circuit connection pins

Detailed Description

Analog Section

Figure 3 shows the Analog Section for the ICL7116 and ICL7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to 1V from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is

$$\text{DISPLAY COUNT} = 1000\left(\frac{V_{IN}}{V_{REF}}\right).$$

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing to within 0.5V of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by

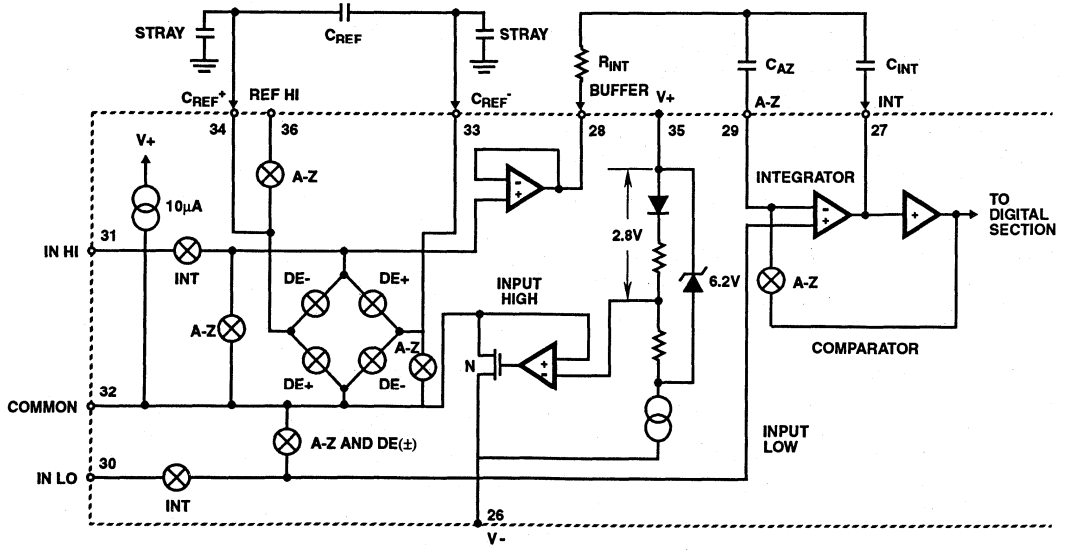


FIGURE 3. ANALOG SECTION OF ICL7116 AND ICL7117

selecting the reference capacitor such that it is large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (ICL7116) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8V less than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6.8V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>6.8V), the COMMON voltage will have a low voltage coefficient (0.001%/V), low output impedance (≅15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on chip reference should also be recognized, however. With the ICL7117, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full-scale from 25μV to 80μVp-p. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111(8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an over-range condition. This is because over-range is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between over range and a non-over range count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The ICL7116, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink approximately 30mA of current to hold the voltage 2.8V below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus overriding the internal reference.

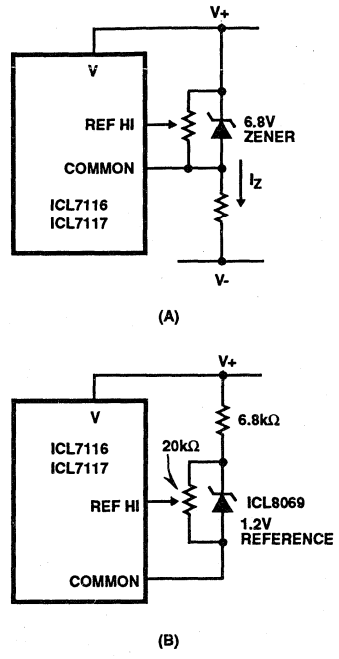


FIGURE 4. USING AN EXTERNAL REFERENCE

TEST

The TEST pin serves two functions. On the ICL7116 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other annunciator the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

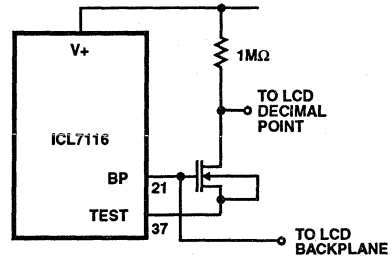


FIGURE 5. SIMPLE INVERTER FOR FIXED DECIMAL POINT

The second function is a "lamp test". When TEST is pulled high (to V+) all segments will be turned on and the display should read "-1888". The TEST pin will sink about 5mA under these conditions.

CAUTION: On the ICL7116, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

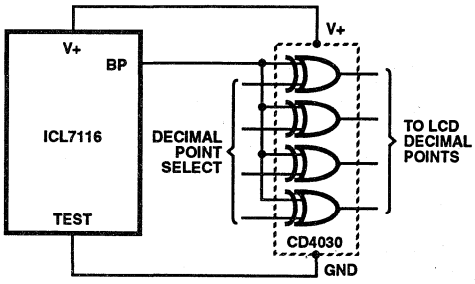


FIGURE 6. EXCLUSIVE 'OR' GATE FOR DECIMAL POINT DRIVE

HOLD Reading Input

The HLDR input will prevent the latch from being updated when this input is at logic "1". The chip will continue to make A/D conversions, however, the results will not be updated to the internal latches until this input goes low. This input can be left open or connected to TEST (ICL7116) or GROUND (ICL7117) to continuously update the display. This input is CMOS compatible, and has a 70kΩ (See Figure 7) typical resistance to either TEST (ICL7116) or GROUND (ICL7117).

Digital Section

Figures 7 and 8 show the digital section for the ICL7116 and ICL7117, respectively. In the ICL7116, an internal digital ground is generated from a 6V Zener diode and a large P-channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 8 is the Digital Section of the ICL7117. It is identical to the ICL7116 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2mA to 8mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is "on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

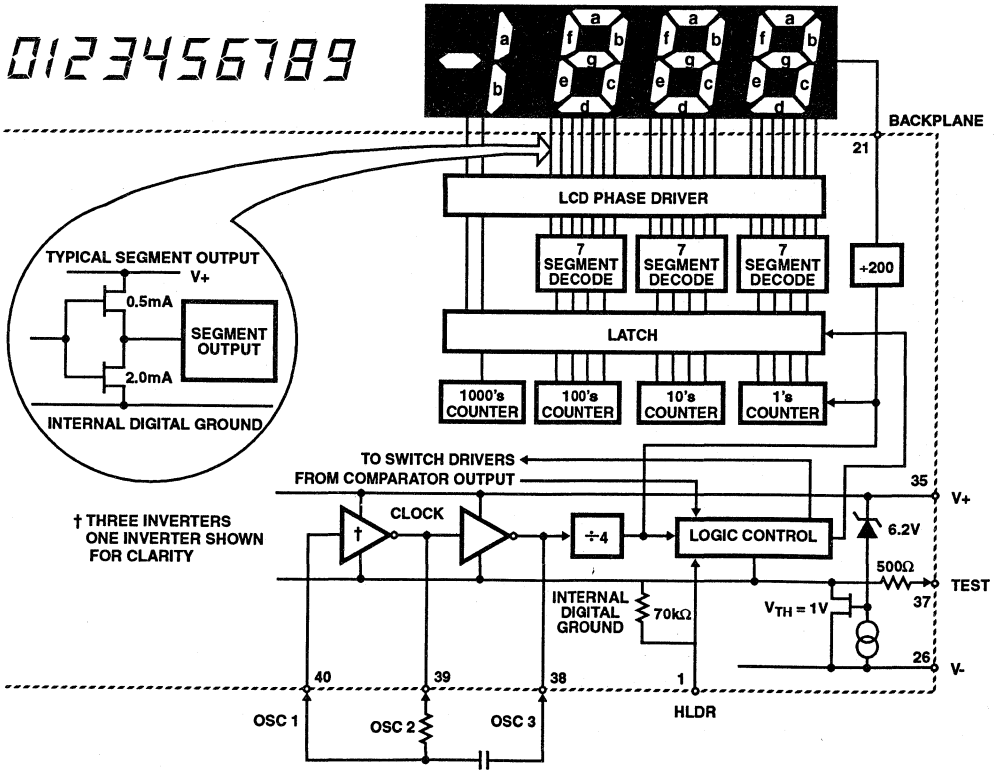


FIGURE 7. ICL7116 DIGITAL SECTION

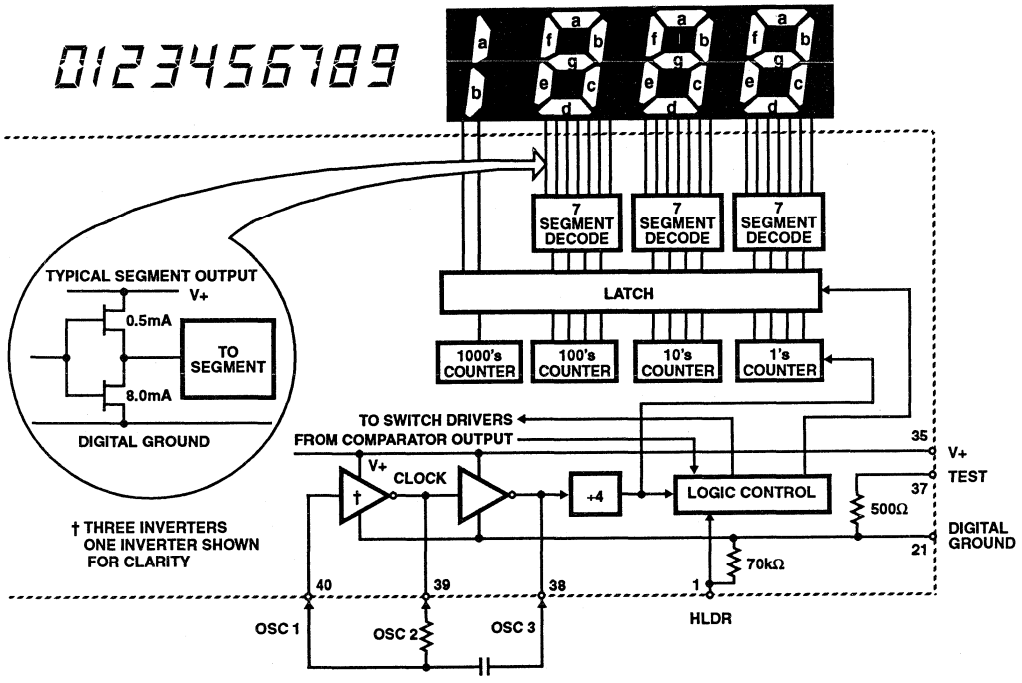


FIGURE 8. ICL7117 DIGITAL SECTION

System Timing

Figure 9 shows the clocking arrangement used in the ICL7116 and ICL7117. Two basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 counts to 3000 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, $33^1/_3$kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, $66^2/_3$kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz).

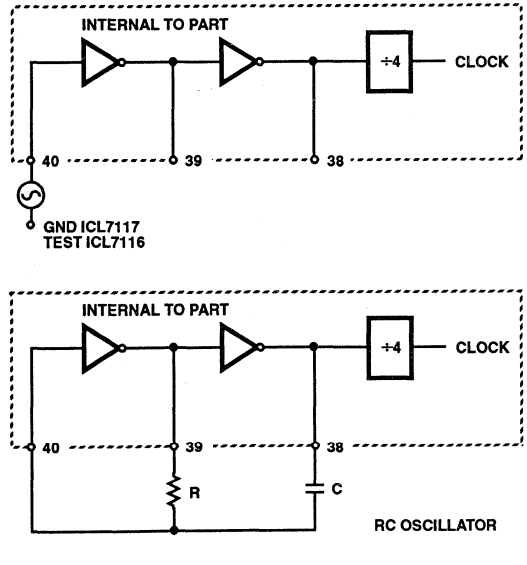


FIGURE 9. CLOCK CIRCUITS

Component Value Selection

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100µA of quiescent current. They can supply 4µA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 470kΩ is near optimum and similarly a 47kΩ for a 200mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance buildup will not saturate the integrator swing (approximately. 0.5V from either supply). In the ICL7116 or the ICL7117, when the analog COMMON is used as a reference, a nominal +2V full-scale integrator swing is fine. For the ICL7117 with +5V supplies and analog COMMON tied to supply ground, a ±3.5V to +4V swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.22µF and 0.10µF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47µF capacitor is recommended. On the 2V scale, a 0.047µF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1µF capacitor gives good results in most applications. Generally 1.0µF will hold the roll-over error to 0.5 counts in this instance.

Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation

$$f = \frac{0.45}{RC}$$ For 48kHz Clock (3 Readings/second), C = 100pF

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200mV and 2V scale, V_{REF} should equal 100mV and 1V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200mV, the designer should use the input voltage directly and select V_{REF} = 0.341V. Suitable values for integrating resistor and capacitor would be 120kΩ and 0.22µF. This makes the system slightly quieter and also avoids a divider network on the input. The ICL7117 with ±5V supplies can accept input signals up to ±4V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable fare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

ICL7117 Power Supplies

3. The ICL7117 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application. See ICL7660 data sheet for an alternative.

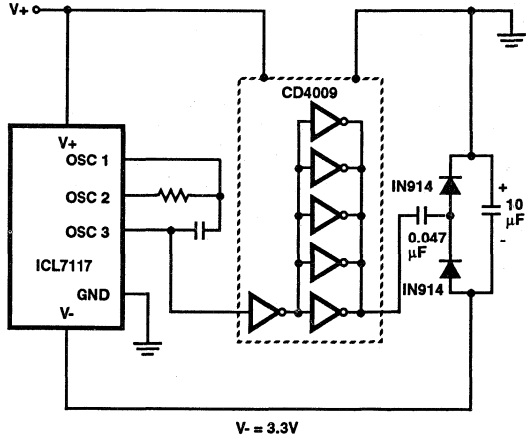


FIGURE 10. GENERATING NEGATIVE SUPPLY FROM +5V

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5V.
3. An external reference is used.

Typical Applications

The ICL7116 and ICL7117 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

The following application notes contain very useful information on understanding and applying this part and are available from Harris semiconductor.

Application Notes

A016 "Selecting A/D Converters"

A017 "The Integrating A/D Converter"

A018 "Do's and Don'ts of Applying A/D Converters"

A023 "Low Cost Digital Panel Meter Designs"

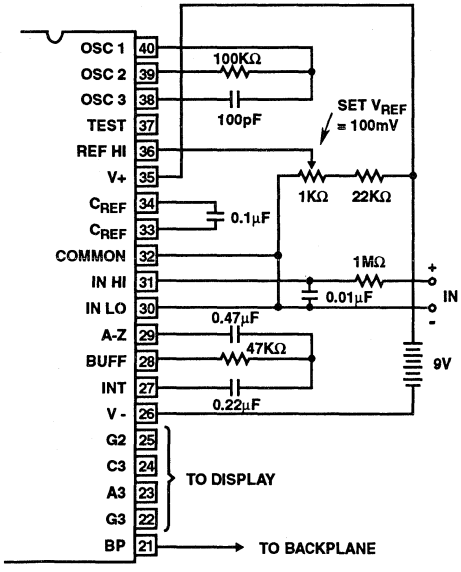
A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7116/7/9 Family"

A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7116"

A047 "Games People Play with Harris' A/D Converters," edited by Peter Bradshaw

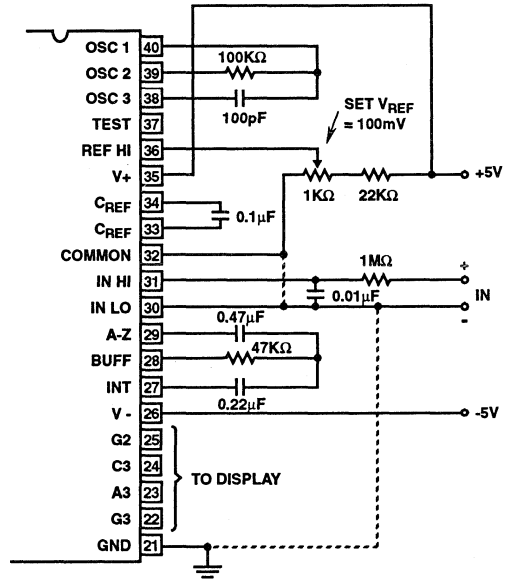
A052 "Tips for Using Single Chip $3^1/_2$ Digit A/D Converters"

Typical Applications



Values shown are for 200mV full-scale, 3 readings/sec., floating supply voltage (9V battery).

FIGURE 11. ICL7116 USING THE INTERNAL REFERENCE



Values shown are for 200mV full-scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

FIGURE 12. ICL7117 USING THE INTERNAL REFERENCE

Typical Applications (Continued)

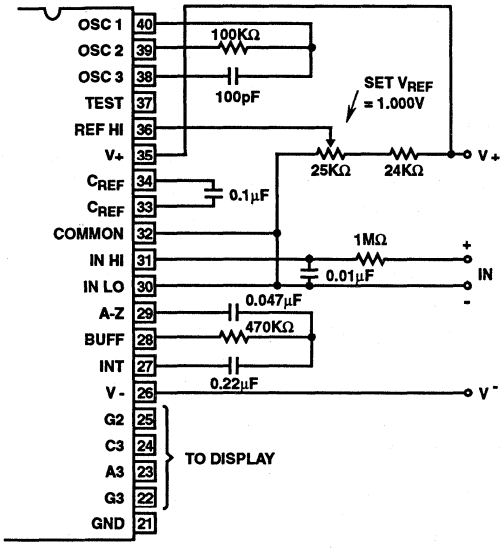
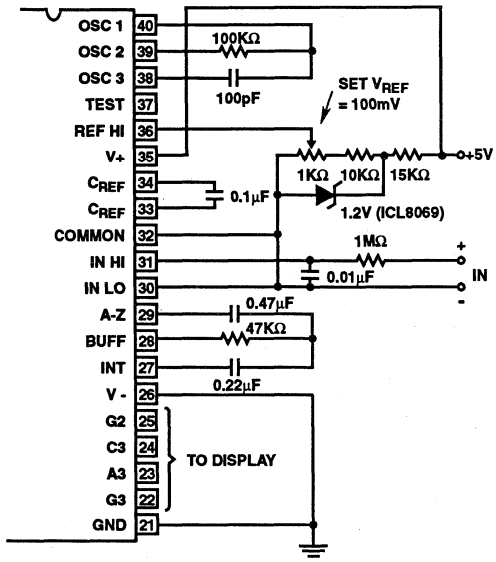
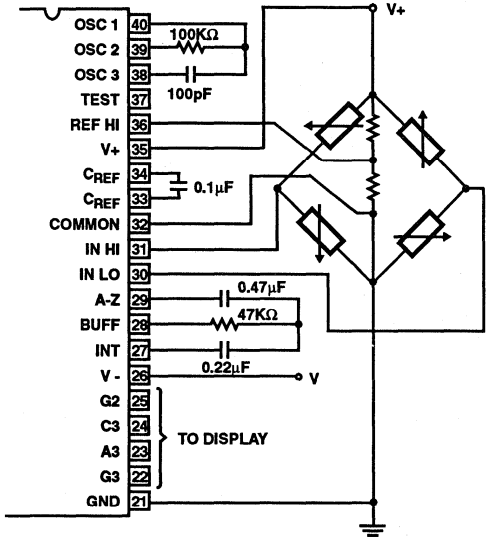


FIGURE 13. ICL7116 AND ICL7117: RECOMMENDED COMPONENT VALUES FOR 2.0V FULL-SCALE



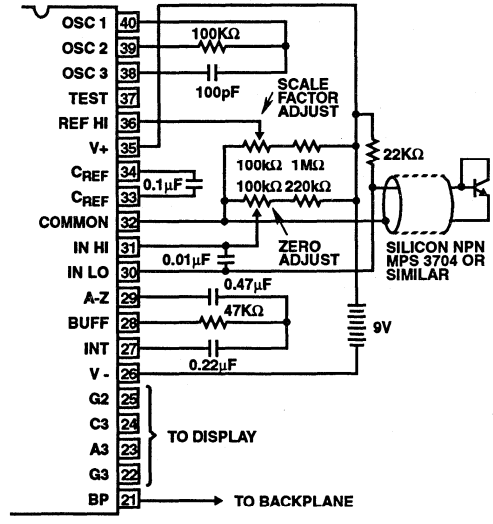
An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.

FIGURE 14. ICL7117 OPERATED FROM SINGLE +5V SUPPLY



The resistor values within the bridge are determined by the desired sensitivity.

FIGURE 15. ICL7117 MEASUREING RATIOMETRIC VALUES OF QUAD LOAD CELL



A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

FIGURE 16. ICL7116 USED AS A DIGITAL CENTIGRADE THERMOMETER

HARRIS SEMICONDUCTOR

ICL7129

$4^1/_2$ Digit LCD Single-Chip A/D Converter

December 1993

Features

- ±19,999 Count A/D Converter Accurate to ±4 Count
- 10µV Resolution on 200mV Scale
- 110dB CMRR
- Direct LCD Display Drive
- True Differential Input and Reference
- Low Power Consumption
- Decimal Point Drive Outputs
- Overrange and Underrange Outputs
- Low Battery Detection and Indication
- 10:1 Range Change Input

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7129CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7129RCPL	0°C to +70°C	40 Lead Plastic DIP (Note 1)
ICL7129CM44	0°C to +70°C	44 Lead Metric Plastic Quad Flatpack

NOTE:

1. "R" indicates device with reversed leads.

Description

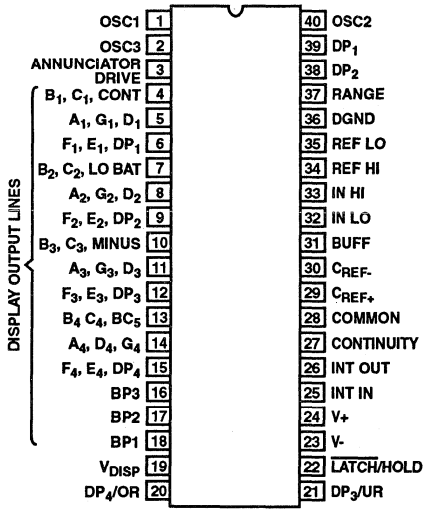
The Harris ICL7129 is a very high performance $4^1/_2$-digit analog-to-digital converter that directly drives a multiplexed liquid crystal display. This single chip CMOS integrated circuit requires only a few passive components and a reference to operate. It is ideal for high resolution hand-held digital multimeter applications.

The performance of the ICL7129 has not been equaled before in a single chip A/D converter. The successive integration technique used in the ICL7129 results in accuracy better than 0.005% of full-scale and resolution down to 10µV/count.

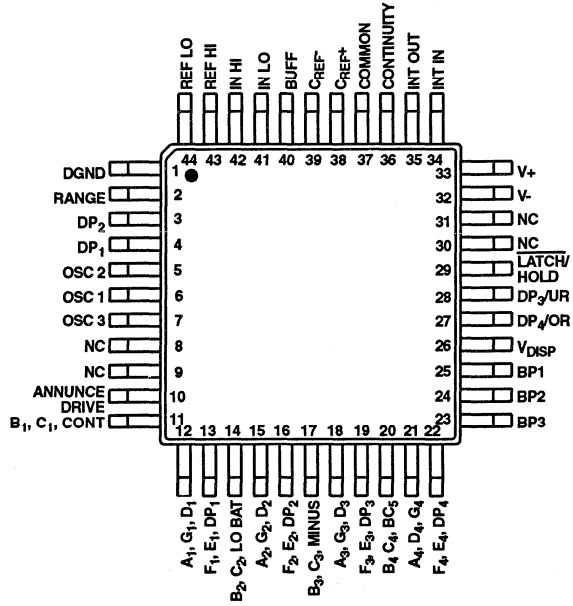
The ICL7129, drawing only 1mA from a 9V battery, is well suited for battery powered instruments. Provision has been made for the detection and indication of a "LOW/BATTERY" condition. Autoranging instruments can be made with the ICL7129 which provides overrange and underrange outputs and 10:1 range changing input. The ICL7129 instantly checks for continuity, giving both a visual indication and a logic level output which can enable an external audible transducer. These features and the high performance of the ICL7129 make it an extremely versatile and accurate instrument-on-a-chip.

Pinouts

ICL7129
(PDIP)
TOP VIEW



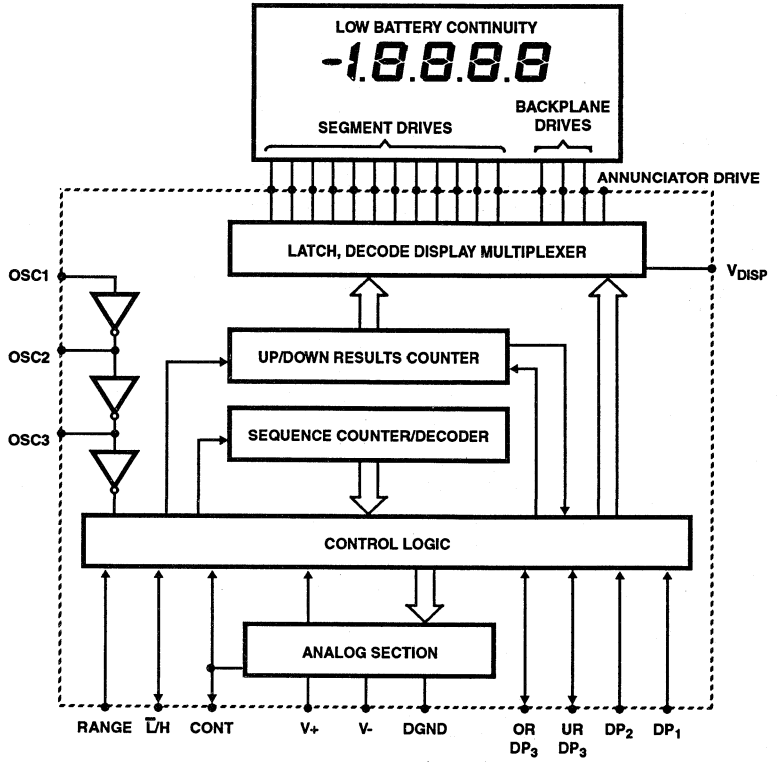
ICL7129
(MQFP)
TOP VIEW



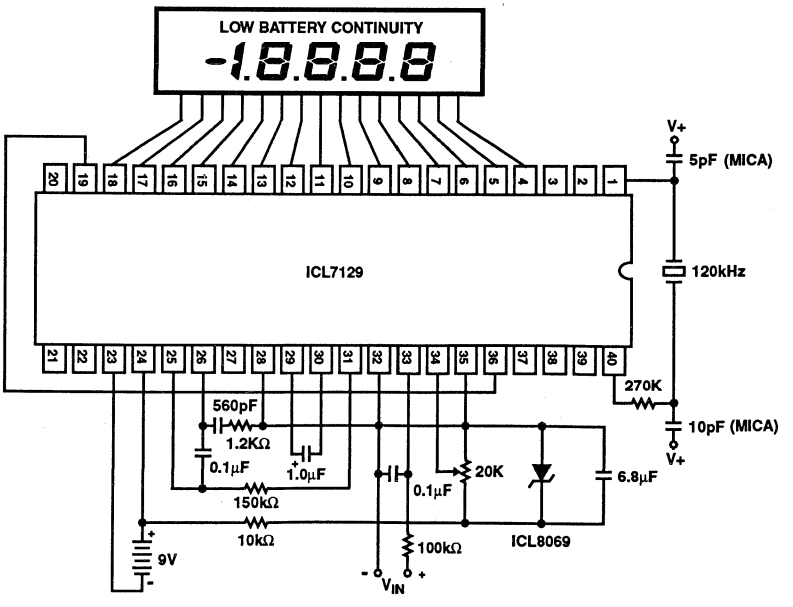
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3085**

Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage 15V
Reference Voltage (REF HI or REF LO) ..... V+ to V-
Input Voltage (Note 1), IN HI or IN LO ..... V+ to V-
V_{DISP} ..... DGND -0.3V to V+
Digital Input Pins
1, 2, 19, 20, 21, 22, 27, 37, 38, 39, 40 ..... DGND to V+
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}
PDIP	50°C/W
MQFP	80°C/W
Maximum Power Dissipation (Note 2)	
Plastic Package	800mW
Junction Temperature	+150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V- to V+ = 9V, V_{REF} = 1.00V. T_A = +25°C, f_{CLK} = 120kHz, Unless Otherwise Specified.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0V, 200mV Scale	-0000	0000	+0000	Counts
Zero Reading Drift	V_{IN} = 0V, 0°C < T_A < +70°C	-	±0.5	-	µV/°C
Ratiometric Reading	V_{IN} = V_{REF} = 1000mV, RANGE = 2V	9996	9999	10000	Counts
Range Change Accuracy	V_{IN} = 0.10000V on Low, Range ≈ V_{IN} = 1.0000V on High Range	0.9999	1.0000	1.0001	Ratio
Rollover Error	-V_{IN} = +V_{IN} = 199mV	-	1.5	3.0	Counts
Linearity Error	200mV Scale	-	1.0	-	Counts
Input Common-Mode Rejection Ratio	V_{CM} =1.0V,V_{IN} = 0V, 200mV Scale	-	110	-	dB
Input Common-Mode Voltage Range	V_{IN} = 0V, 200mV Scale	-	(V-) +1.5 (V+) -1.0	-	V
Noise (p-p Value not Exceeding 95% of Time)	V_{IN} = 0V 200mV Scale	-	14	-	µV
Input Leakage Current	V_{IN} = 0V, Pin 32, 33	-	1	10	pA
Scale Factor Tempco	V_{IN} = 199mV 0°C < T_A < +70°C External V_{REF} = 0ppm/°C	-	2	7	ppm/°C
COMMON Voltage	V+ to Pin 28	2.8	3.2	3.5	V
COMMON Sink Current	ΔCommon = + 0.1V	-	0.6	-	mA
COMMON Source Current	ΔCommon = -0.1V	-	10	-	µA
DGND Voltage	V+ to Pin 36, V+ to V- = 9V	4.5	5.3	5.8	V
DGND Sink Current	ΔDGND = +0.5V	-	1.2	-	mA
Supply Voltage Range	V+ to V- (Note 3)	6	9	12	V
Supply Current Excluding COMMON Current	V+ to V- = 9V	-	1.0	1.5	mA
Clock Frequency	(Note 3)	-	120	360	kHz
V_{DISP} Resistance	V_{DISP} to V+	-	50	-	kΩ
Low Battery Flag Activation Voltage	V+ to V-	6.3	7.2	7.7	V
CONTINUITY Comparator Threshold Voltages	V_{OUT} Pin 27 = HI	100	200	-	mV
	V_{OUT} Pin 27 = LO	-	200	400	mV
Pull-Down Current	Pins 37, 38, 39	-	2	10	µA
"Weak Output" Current Sink/Source	Pin 20, 21 Sink/Source	-	3/3	-	µA
	Pin 27 Sink/Source	-	3/9	-	µA
Pin 22 Source Current		-	40	-	µA
Pin 22 Sink Current		-	3	-	µA

NOTE:

1. Input voltages may exceed the supply voltages provided that input current is limited to 1400mA. Currents above this value may result in valid display readings but will not destroy the device if limited to ±1mA.
2. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.
3. Device functionality is guaranteed at the stated Min/Max limits. However, accuracy can degrade under these conditions.

Pin Descriptions

PIN	SYMBOL	DESCRIPTION
1	OSC_1	Input to first clock inverter.
2	OSC_3	Output of second clock inverter.
3	ANNUNCIATOR DRIVE	Backplane squarewave output for driving annunciators.
4	B_1,C_1, CONT	Output to display segments.
5	A_1, G_1, D_1	Output to display segments.
6	F_1, E_1, DP_1	Output to display segments.
7	B_2, C_2, LO BATT	Output to display segments.
8	A_2, G_2, D_2	Output to display segments.
9	F_2, E_2, DP_2	Output to display segments.
10	B_3, C_3, MINUS	Output to display segments.
11	A_3, G_3, D_3	Output to display segments.
12	F_3, E_3, DP_3	Output to display segments.
13	B_4, C_4, BC_5	Output to display segments.
14	A_4, D_4, G_4	Output to display segments.
15	F_4, E_4, DP_4	Output to display segments.
16	BP_3	Backplane #3 output to display.
17	BP_2	Backplane #2 output to display.
18	BP_1	Backplane #1 output to display.
19	V_{DISP}	Negative rail for display drivers.
20	DP_4/OR	INPUT: When HI, turns on most significant decimal point. OUTPUT: Pulled HI when result count exceeds ±19,999.
21	DP_3/UR	INPUT: Second most significant decimal point on when HI. OUTPUT: Pulled HI when result count is less than ±1,000.
22	$\overline{\text{LATCH}}$/HOLD	INPUT: When floating, A/D converter operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle. OUTPUT: Negative going edge occurs when the data latches are updated. Can be used for converter status signal.

PIN	SYMBOL	DESCRIPTION
23	V-	Negative power supply terminal.
24	V+	Positive power supply terminal, and positive rail for display drivers.
25	INT IN	Input to integrator amplifier.
26	INT OUT	Output of integrator amplifier.
27	CONTINUITY	INPUT: When LO, continuity flag on the display is off. When HI, continuity flag is on. OUTPUT: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV.
28	COMMON	Sets common-mode voltage of 3.2V below V+ for DE, 10X, etc. Can be used as pre-regulator for external reference.
29	C_{REF+}	Positive side of external reference capacitor.
30	C_{REF-}	Negative side of external reference capacitor.
31	BUFFER	Output of buffer amplifier.
32	IN LO	Negative input voltage terminal.
33	IN HI	Positive input voltage terminal.
34	REF HI	Positive reference voltage input terminal.
35	REF LO	Negative reference voltage input terminal.
36	DGND	Ground reference for digital section.
37	RANGE	3µA pull-down for 200mV scale. Pulled HIGH externally for 2V scale.
38	DP_2	Internal 3µA pull-down. When HI, decimal point 2 will be on.
39	DP_1	Internal 3µA pull-down. When HI, decimal point 1 will be on.
40	OSC2	Output of first clock inverter. Input of second clock inverter.

Detailed Description

The ICL7129 is a uniquely designed single chip A/D converter. It features a new "successive integration" technique to achieve 10μV resolution on a 200mV full-scale range. To achieve this resolution a 10:1 improvement in noise performance over previous monolithic CMOS A/D converters was accomplished. Previous integrating converters used an external capacitor to store an offset correction voltage. This technique worked well but greatly increased the equivalent noise bandwidth of the converter. The ICL7129 removes this source of error (noise) by not using an auto-zero capacitor. Offsets are cancelled using digital techniques instead. Savings in external parts cost are realized as well as improved noise performance and elimination of a source of electromagnetic and electrostatic pick-up.

In the overall Functional Block Diagram of the ICL7129 the heart of this A/D converter is the sequence counter/decoder which drives the control logic and keeps track of the many separate phases required for each conversion cycle. The sequence counter is constantly running and is a separate counter from the up/down results counter which is activated only when the integrator is de-integrating. At the end of a conversion the data remaining in the results counter is latched, decoded and multiplexed to the liquid crystal display.

The analog section block diagram shown in Figure 1 includes all of the analog switches used to configure the voltage sources and amplifiers in the different phases of the cycle. The input and reference switching schemes are very similar to those in other less accurate integrating A/D converters. There are 5 basic configurations used in the full conversion cycle. Figure 2 illustrates a typical waveform on the integrator output. INT, INT_1, and INT_2 all refer to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage.

DE_1, DE_2, and DE_3 are the de-integrate phases where the reference capacitor is switched in series with the buffer amplifier and the integrator ramps back down to the level it started from before integrating. However, since the de-integrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The ICL7129 amplifies this overshoot by 10 and DE_2 begins. Similarly DE_2's overshoot is amplified by 10 and DE_3 begins. At the end of DE_3 the results counter holds a number with 5 1/2 digits of resolution. This was obtained by feeding counts into the results counter at the 3 1/2 digit level during DE_1, into the 4 1/2 digit level during DE_2 and the 5 1/2 digit level for DE_3. The effects of offset in the buffer,

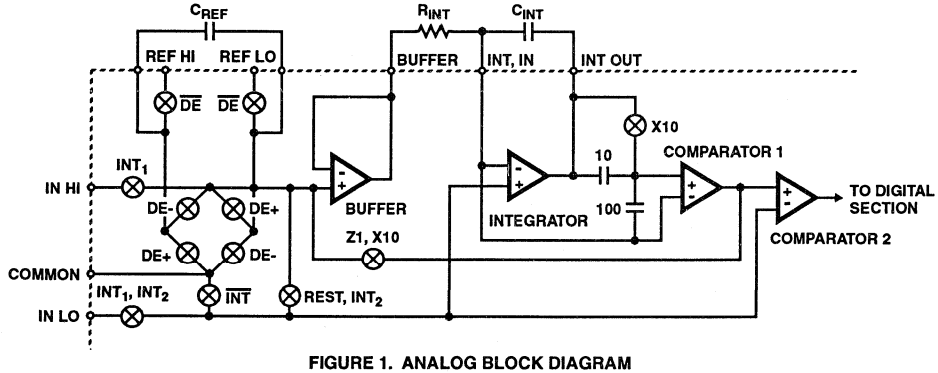


FIGURE 1. ANALOG BLOCK DIAGRAM

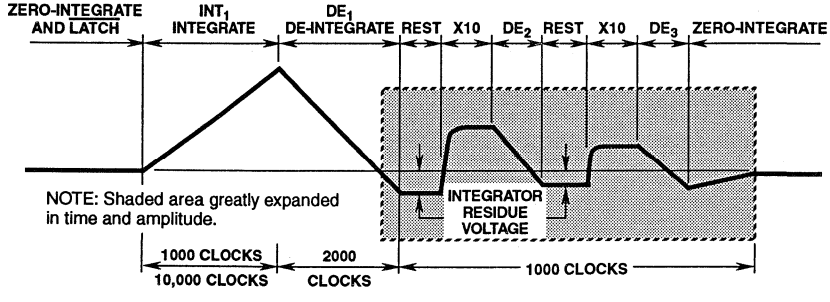


FIGURE 2. INTEGRATOR WAVEFORM FOR NEGATIVE INPUT VOLTAGE SHOWING SUCCESSIVE INTEGRATION PHASES AND RESIDUE VOLTAGE

integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted and subtracting the results from the original reading. For this phase INT_2 switch is closed to give the same common-mode voltage as the measurement cycle. This assures excellent CMRR. At the end of the cycle the data in the up/down results counter is accurate to 0.02% of full-scale and is sent to the display driver for decoding and multiplexing.

COMMON, DGND, and "Low Battery"

The COMMON and DGND (Digital GrouND) outputs of the ICL7129 are generated from internal zener diodes (Figure 3). COMMON is included primarily to set the common-mode voltage for battery operation or for any system where the input signals float with respect to the power supplies. It also functions as a pre-regulator for an external precision reference voltage source. The voltage between DGND and V+ is the supply voltage for the logic section of the ICL7129 including the display multiplexer and drivers. Both COMMON and DGND are capable of sinking current from external loads, but caution should be taken to ensure that these outputs are not overloaded. Figure 4 shows the connection of external logic circuitry to the ICL7129. This connection will work providing that the supply current requirements of the logic do not exceed the current sink capability of the DGND pin. If more supply current is required, the buffer in Figure 5 can be used to keep the loading on DGND to a minimum. COMMON can source approximately 12µA while DGND has no source capability.

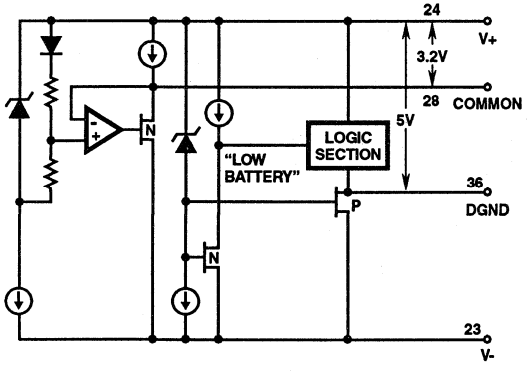


FIGURE 3. BIASING STRUCTURE FOR COMMON AND DGND

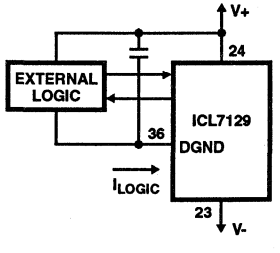


FIGURE 4. DGND SINK CURRENT

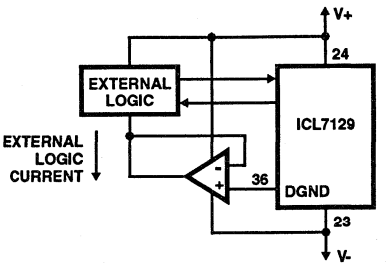


FIGURE 5. BUFFERED DGND

The "LOW BATTERY" annunciator of the display is turned on when the voltage between V+ and V- drops below 7.2V typically. The exact point at which this occurs is determined by the 6.3V zener diode and the threshold voltage of the n-channel transistor connected to the V- rail in Figure 3. As the supply voltage decreases, the n-channel transistor connected to the V-rail eventually turns off and the "LOW BATTERY" input to the logic section is pulled HIGH, turning on the "LOW BATTERY" annunciator.

I/O Ports

Four pins of the ICL7129 can be used as either inputs or outputs. The specific pin numbers and functions are described in the Pin Description table. If the output function of the pin is not desired in an application it can easily be overridden by connecting the pin to V+ (HI) or DGND (LO). This connection will not damage the device because the output impedance of these pins is quite high. A simplified schematic of these input/output pins is shown in Figure 6. Since there is approximately 500kΩ in series with the output driver, the pin (when used as an output) can only drive very light loads such as 4000 series, 74CXX type CMOS logic, or other high input impedance devices. The output drive capability of these four pins is limited to 3µA, nominally, and the input switching threshold is typically DGND + 2V.

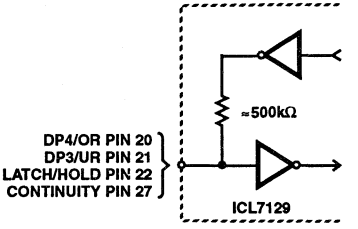


FIGURE 6. "WEAK OUTPUT"

$\overline{\text{LATCH}}$/HOLD, Overrange, and Underrange Timing

The $\overline{\text{LATCH}}$/HOLD output (pin 22) will be pulled low during the last 100 clock cycles of each full conversion cycle. During this time the final data from the ICL7129 counter is latched and transferred to the display decoder and multiplexer. The conversion cycle and $\overline{\text{LATCH}}$/HOLD timing are directly related to the clock frequency. A full conversion cycle takes 30,000 clock cycles which is equivalent to 60,000 oscillator cycles. OverRange (OR pin 20) and UnderRange

(UR pin 21) outputs are latched on the falling edge of LATCH/HOLD and remain in that state until the end of the next conversion cycle. In addition, digits 1 through 4 are blanked during overrange. All three of these pins are "weak outputs" and can be overridden with external drivers or pull-up resistors to enable their input functions as described in the Pin Description table.

Instant Continuity

A comparator with a built-in 200mV offset is connected directly between INPUT HI and INPUT LO of the ICL7129 (Figure 7). The CONTINUITY output (pin 27) will be pulled high whenever the voltage between the analog inputs is less than 200mV. This will also turn on the "CONTINUITY" annunciator on the display. The CONTINUITY output may be used to enable an external alarm or buzzer, thereby giving the ICL7129 an audible continuity checking capability.

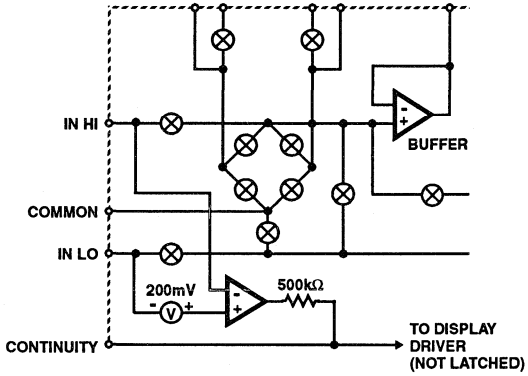


FIGURE 7. "INSTANT CONTINUITY" COMPARATOR AND OUTPUT STRUCTURE

Since the CONTINUITY output is one of the four "weak outputs" of the ICL7129, the "continuity" annunciator on the display can be driven by an external source if desired. The continuity function can be overridden with a pull-down resistor connected between CONTINUITY pin and DGND (pin 36).

Display Configuration

The ICL7129 is designed to drive a triplexed liquid crystal display. This type of display has three backplanes and is driven in a multiplexed format similar to the ICM7231 display driver family. The specific display format is shown in Figure 8. Notice that the polarity sign, decimal points, "LOW BATTERY", and "CONTINUITY" annunciators are directly driven by the ICL7129. The individual segments and annunciators are addressed in a manner similar to row-column addressing. Each backplane (row) is connected to one-third of the total number of segments. BP1 has all F, A, and B segments of the four least significant digits. BP2 has all of the C, E, and G segments. BP3 has all D segments, decimal points, and annunciators. The segment lines (columns) are connected in groups of three bringing all segments of the display out on just 12 lines.

Annunciator Drive

A special display driver output is provided on the ICL7129 which is intended to drive various kinds of annunciators on custom multiplexed liquid crystal displays. The ANNUNCIATOR DRIVE output (pin 3) is a squarewave signal running at the backplane frequency, approximately 100Hz. This signal swings from V_{DISP} to V+ and is in sync with the three backplane outputs BP1, BP2, and BP3. Figure 9 shows these four outputs on the same time and voltage scales.

Any annunciator associated with any of the three backplanes can be turned on simply by connecting it to the ANUNCIATOR DRIVE pin. To turn an annunciator off connect if to its backplane. An example of a display and annunciator drive scheme is shown in Figure 10.

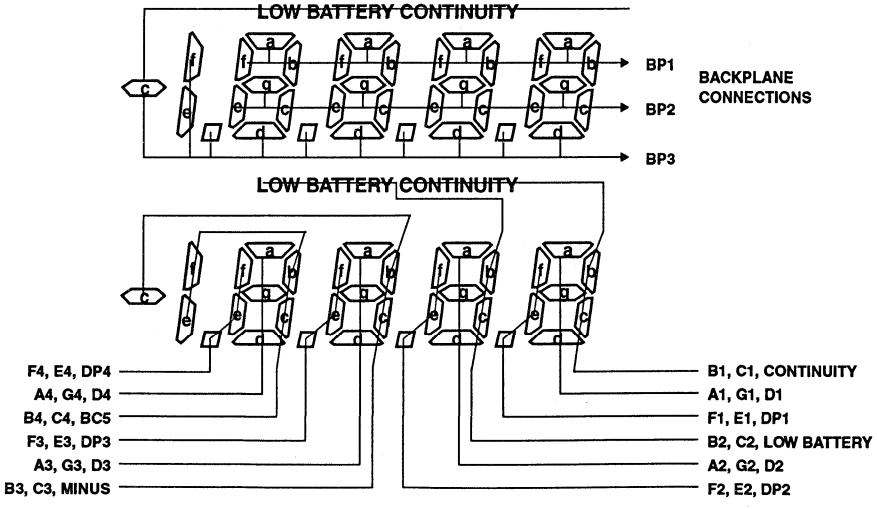


FIGURE 8. TRIPLEXED LIQUID CRYSTAL DISPLAY LAYOUT FOR ICL7129

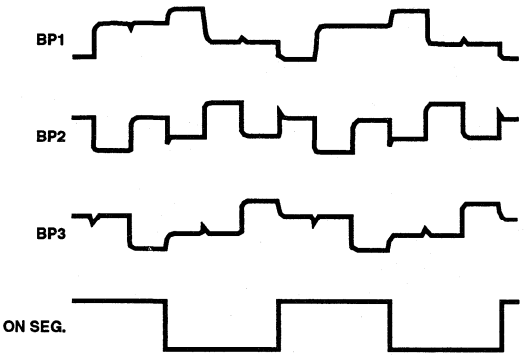


FIGURE 9. TYPICAL BACKPLANE AND ANNUNCIATOR DRIVE WAVEFORMS

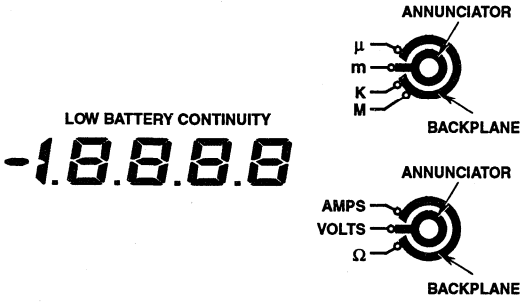


FIGURE 10. MULTIMETER EXAMPLE SHOWING USE OF ANNUNCIATOR DRIVE OUTPUT

Display Temperature Compensation

For most applications an adequate display can be obtained by connecting V_{DISP} (pin 19) to DGND (pin 36). In applications where a wide temperature range is encountered, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Display manufacturers can supply the temperature compensation requirements for their displays. Figure 11 shows two circuits that can be adjusted to give a temperature compensation of ≈ + 10mV/°C between V+ and V_{DISP} The diode between DGND and V_{DISP} should have a low turn-on voltage to assure that no forward current is injected into the chip if V_{DISP} is more negative than DGND.

Component Selection

There are only three passive components around the ICL7129 that need special consideration in selection. They are the reference capacitor, integrator resistor, and integrator capacitor. There is no auto-zero capacitor like that found in earlier integrating A/D converter designs.

The integrating resistor is selected to be high enough to assure good current linearity from the buffer amplifier and integrator and low enough that PC board leakage is not a problem. A value of 150kΩ should be optimum for most applications. The integrator capacitor is selected to give an optimum integrator swing at full-scale. A large integrator swing will reduce the effect of noise sources in the comparator but will affect rollover error if the swing gets too close to the positive rail (≈0.7V). This gives an optimum swing of ≈2.5V at full-scale. For a 150kΩ integrating resistor and 2 conversions per second the value is 0.10μF. For different conversion rates, the value will change in inverse proportion. A second requirement for good linearity is that the capacitor have low dielectric absorption. Polypropylene caps give good performance at a reasonable price. Finally the foil side of the cap should be connected to the integrator output to shield against pickup.

The only requirement for the reference cap is that it be low leakage. In order to reduce the effects of stray capacitance, a 1.0μF value is recommended.

Clock Oscillator

The ICL7129 achieves its digital range changing by integrating the input signal for 1000 clock pulses (2,000 oscillator cycles) on the 2V scale and 10,000 clock pulses on the 200mV scale. To achieve complete rejection of 60Hz on both scales, an oscillator frequency of 120kHz is required, giving two conversions per second.

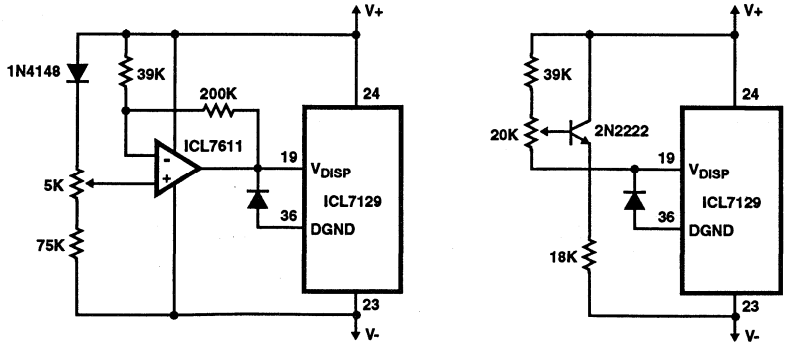


FIGURE 11. TWO METHODS FOR TEMPERATURE COMPENSATING THE LIQUID CRYSTAL DISPLAY

In low resolution applications, where the converter uses only 3 1/2 digits and 100μV resolution, an R-C type oscillator is adequate. In this application a C of 51pF is recommended and the resistor value selected from f_{OSC} = 0.45/RC. However, when the converter is used to its full potential (4 1/2 digits and 10μV resolution) a crystal oscillator is recommended to prevent the noise from increasing as the input signal is increased due to frequency jitter of the R-C oscillator. Both R-C and crystal oscillator circuits are shown in Figure 12.

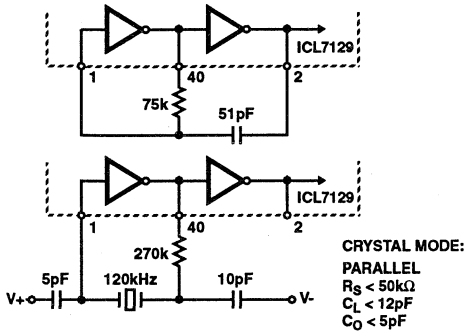


FIGURE 12. RC AND CRYSTAL OSCILLATOR CIRCUITS

Powering the ICL7129

The ICL7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies. Figures 13, 14, and 15 show various powering modes that may be used with the ICL7129.

The standard supply connection using a 9V battery is shown in the Typical Application Schematic.

The power connection for systems with +5V and -5V supplies available is shown in Figure 13. Notice that measurements are with respect to ground. COMMON is also tied to INLO to remove any common-mode voltage swing on the integrator amplifier inputs.

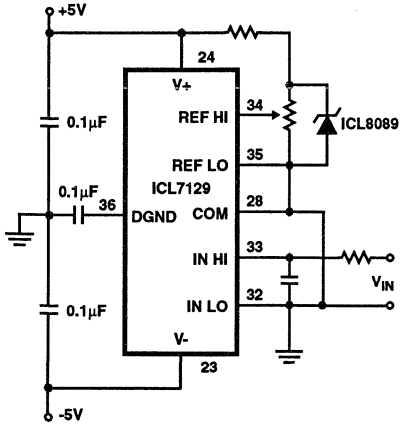


FIGURE 13. POWERING THE ICL7129 FROM +5V AND -5V

It is important to notice that in Figure 13, digital ground of the ICL7129 (DGND pin 36) is not directly connected to power supply ground. DGND is set internally to approximately 5V less than the V+ terminal and is not intended to be used as a power input pin. It may be used as the ground reference for external logic, as shown in Figure 4 and 5. In Figure 4, DGND is used as the negative supply rail for external logic provided that the supply current for the external logic does not cause excessive loading on DGND. The DGND output can be buffered as shown in Figure 5. Here, the logic supply current is shunted away from the ICL7129 keeping the load on DGND low. This treatment of the DGND output is necessary to insure compatibility when the external logic is used to intertace directly with the logic inputs and outputs of the ICL7129.

When a battery voltage between 3.8V and 6V is desired for operation, a voltage doubling circuit should be used to bring the voltage on the ICL7129 up to a level within the power supply voltage range. This operating mode is shown in Figure 14.

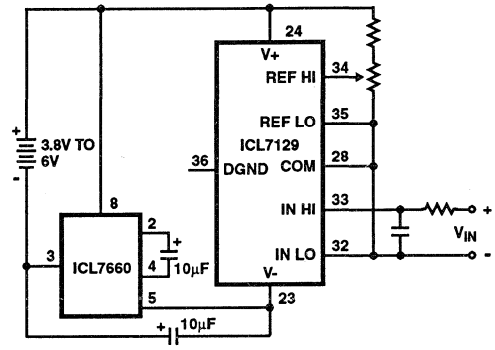


FIGURE 14. POWERING THE ICL7129 FROM A 3.8V TO 6V BATTERY

Again measurements are made with respect to COMMON since the entire system is floating. Voltage doubling is accomplished by using an ICL7660 CMOS voltage converter and two inexpensive electrolytic capacitors. The same principle applies in Figure 15 where the ICL7129 is being used in a system with only a single +5V power supply. Here measurements are made with respect to power supply ground.

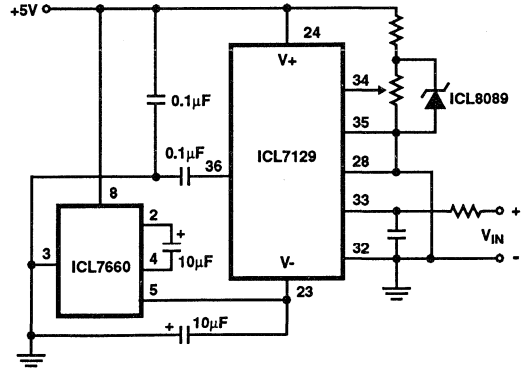


FIGURE 15. POWERING THE ICL7129 FROM A SINGLE POLARITY POWER SUPPLY

A single polarity power supply can be used to power the ICL7129 in applications where battery operation is not appropriate or convenient only if the power supply is isolated from system ground. Measurements must be made with respect to COMMON or some other voltage within its input common-mode range

Voltage References

The COMMON output of the ICL7129 has a temperature coefficient of ±80ppm/°C typically. This voltage is only suitable as a reference voltage for applications where ambient temperature variations are expected to be minimal. When the ICL7129 is used in most environments, other voltage references should be considered. The diagram in the Typical Application Schematic and Figure 15 show the ICL8069 1.2V band-gap voltage source used as the reference for the ICL7129, and the COMMON output as its pre-regulator. The reference voltage for the ICL7129 is set to 1.000V for both 2V and 200mV full-scale operation

Multiple Integration A/D Converter Equations

Oscillator Frequency

$f_{OSC} = 0.45/RC$

$C_{OSC} > 50pF$; $R_{OSC} > 50k\Omega$

f_{OSC} typ. = 120kHz

or

f_{OSC} = 120kHz Crystal (Recommended)

Oscillator Period

$t_{OSC} = 1/f_{OSC}$

Integration Clock Period

$t_{CLOCK} = 2*t_{OSC}$

Integration Period

$t_{INT(2V)} = 1000*t_{CLOCK}$ (Range = 1)

$t_{INT(200mV)} = 10{,}000*t_{CLOCK}$ (Range = 0)

60/50Hz Rejection Criterion

t_{INT}/t_{60Hz} or t_{INT}/t_{50Hz} = Integer

Optimum Integration Current

$I_{INT} = 13\mu A$

Full Scale Analog Input Voltage

V_{INFS} Typically = 200mV or 2.0V

Integrate Resistor

$R_{INT} = V_{INFS}/I_{INT}$

R_{INT} Typ. = 150kΩ

Integrate Capacitor

$$C_{INT} = \frac{(t_{INT})\ (I_{INT})}{V_{INT}}$$

Integrator Output Voltage Swing

$$V_{INT} = \frac{(t_{INT})\ (I_{INT})}{C_{INT}}$$

V_{INT} Maximum Swing: $(V- + 0.5V) < V_{INT} < (V+ - 0.7V)$

Display Count

$$\text{COUNT} = 10{,}000 \times \frac{V_{IN}}{V_{REF}} \quad \text{(Range = 1)}$$

(2.0V Range)

$$\text{COUNT} = 10{,}000 \times \frac{V_{IN} \times 10}{V_{REF}} \quad \text{(Range = 0)}$$

(200mV Range)

Minimum V_{REF}: 500mV

Common Mode Input Voltage

$(V- + 1.0V) < V_{IN} < (V+ - 0.5V)$

Auto Zero Capacitor: C_{AZ} not used

Reference Capacitor: $0.1\mu F < C_{REF} < 1.0\mu F$

V_{COM}

Biased Between V+ and V-.

$V_{COM} \cong V+ -2.9V$

Regulation lost when V+ to V- < ≅6.4V.

If V_{COM} is externally pulled down to (V+ to V-)/2, the V_{COM} circuit will turn off.

Power Supply: Single 9V

V+ - V- = 9V

Digital supply is generated internally

$V_{GND} \cong V+ - 4.5V$

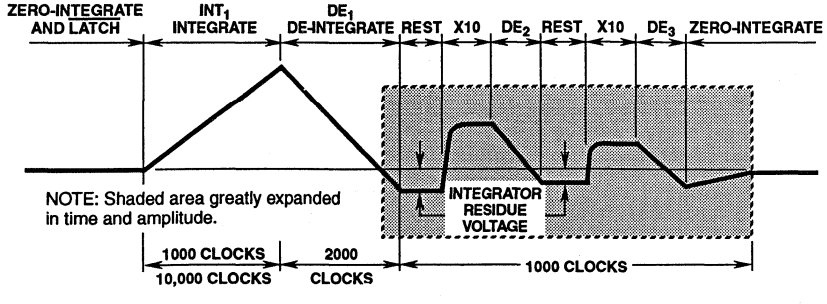
Display: Triplexed LCD

Continuity Output On if

V_{INHI} to V_{INLO} < 200mV

Conversion Cycle (In Both Ranges)

$t_{CYC} = t_{CLOCK}$ x 30,000



HARRIS SEMICONDUCTOR

ICL7136, ICL7137

$3^1/_2$ Digit LCD/LED Low Power Display A/D Converter with Overrange Recovery

December 1993

Features

- First Reading Overrange Recovery in One Conversion Period
- Guaranteed Zero Reading for 0V Input on All Scales
- True Polarity at Zero for Precise Null Detection
- 1pA Typical Input Current
- True Differential Input and Reference, Direct Display Drive
  - LCD ICL7136
  - LED ICL7137
- Low Noise - Less Than 15μVp-p
- On Chip Clock and Reference
- No Additional Active Circuits Required
- Low Power - Less Than 1mW
- Small Outline Surface Mount Package Available
- Drop-In Replacement for ICL7126, No Changes Needed

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7136CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7136RCPL	0°C to +70°C	40 Lead Plastic DIP (Note 1)
ICL7136CM44	0°C to +70°C	44 Lead Metric Plastic Quad Flatpack
ICL7137CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7137RCPL	0°C to +70°C	40 Lead Plastic DIP (Note 1)
ICL7137CM44	0°C to +70°C	44 Lead Metric Plastic Quad Flatpack

NOTE: 1. "R" indicates device with reversed leads.

Description

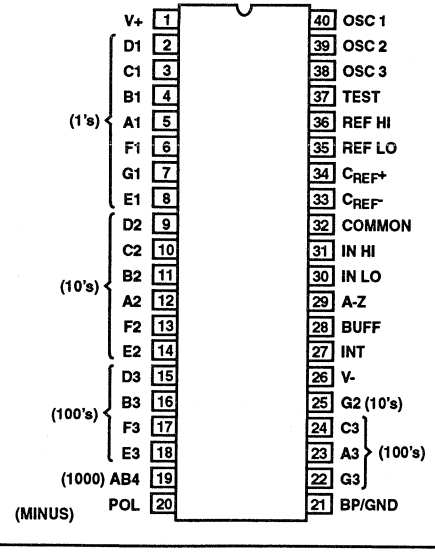
The Harris ICL7136 and ICL7137 are high performance, low power $3^1/_2$ digit A/D converters. Included are seven segment decoders, display drivers, a reference, and a clock. The ICL7136 is designed to interface with a liquid crystal display (LCD) and includes a multiplexed backplane drive; the ICL7137 will directly drive an instrument size, light emitting diode (LED) display.

The ICL7136 and ICL7137 bring together a combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. True differential inputs and reference are useful in all systems, but give the designer an uncommon advantage when measuring load cells, strain gauges and other bridge type transducers. Finally, the true economy of single power supply operation (ICL7136), enables a high performance panel meter to be built with the addition of only 10 passive components and a display.

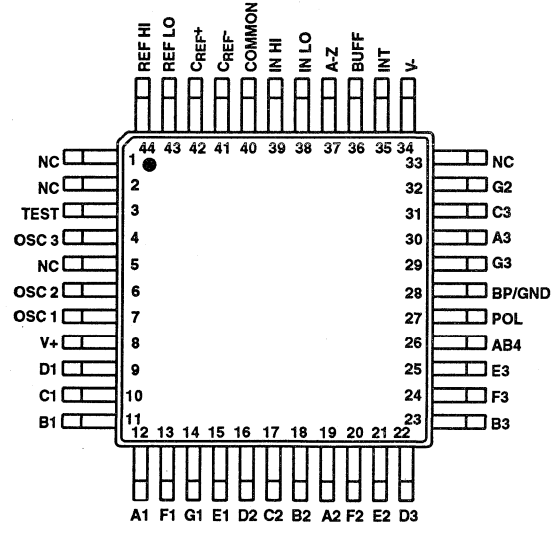
The ICL7136 and ICL7137 are improved versions of the ICL7126, eliminating the overrange hangover and hysteresis effects, and should be used in its place in all applications. It can also be used as a plug-in replacement for the ICL7106 in a wide variety of applications, changing only the passive components.

Pinouts

(PDIP)
TOP VIEW



(MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3086

Absolute Maximum Ratings

Supply Voltage
- ICL7136, V+ to V- 15V
- ICL7137, V+ to GND 6V
- ICL7137, V- to GND ..... -9V

Analog Input Voltage (Either Input) (Note 1) ..... V+ to V-
Reference Input Voltage (Either Input) ..... V+ to V-
Clock Input
- ICL7136 ..... TEST to V+
- ICL7137 ..... GND to V+

Thermal Information

Thermal Resistance θ_{JA}
- 40 Lead PDIP ..... 50°C/W
- 44 Lead MQFP Package ..... 80°C/W

Maximum Power Dissipation (Note 2)
- ICL7136 ..... 0.6W
- ICL7137 ..... 0.8W

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s Max) ..... +300°C
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications (Note 3)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Zero Input Reading	V_{IN} = 0.0V, Full-Scale = 200mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, V_{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error	$-V_{IN} = +V_{IN} \cong$ 200mV Difference in Reading for Equal Positive and Negative Inputs Near Full-Scale	-	±0.2	±1	Counts
Linearity	Full-Scale = 200mV or Full-Scale = 2V Maximum Deviation from Best Straight Line Fit (Note 5)	-	±0.2	±1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V, Full-Scale = 200mV (Note 5)	-	50	-	µV/V
Noise	V_{IN} = 0V, Full-Scale = 200mV (Pk-Pk Value Not Exceeded 95% of Time) (Note 5)	-	15	-	µV
Leakage Current Input	V_{IN} = 0 (Note 5)	-	1	10	pA
Zero Reading Drift	V_{IN} = 0, 0° < T_A < +70°C (Note 5)	-	0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199mV, 0° < T_A < +70°C, (Ext. Ref. 0ppm/°C) (Note 5)	-	1	5	ppm/°C
COMMON Pin Analog Common Voltage	25kΩ Between Common and Positive Supply (With Respect to + Supply)	2.4	2.8	3.2	V
Temperature Coefficient of Analog Common	25kΩ Between Common and Positive Supply (With Respect to + Supply) (Note 5)	-	150	-	ppm/°C
ICL7136					
V+ Supply Current	V_{IN} = 0 (Does Not Include Common Current) 16kHz Oscillator (Note 6)	-	70	100	µA
ICL7137					
V+ Supply Current	V_{IN} = 0 (Does Not Include Common Current) 16kHz Oscillator (Note 6)	-	70	200	µA
V- Supply Current		-	40	-	µA
DISPLAY DRIVER ICL7136 ONLY					
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V+ = to V- = 9V, (Note 4)	4	5	6	V
ICL7137 ONLY					
Segment Sinking Current	V+ = 5V, Segment Voltage = 3V				
(Except Pin 19 and 20)		5	8	-	mA
Pin 19 Only		10	16	-	mA
Pin 20 Only		4	7	-	mA

NOTES:
1. Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Unless otherwise noted, specifications apply to both the ICL7136 and ICL7137 at T_A = +25°C, f_{CLOCK} = 48kHz. ICL7136 is tested in the circuit of Figure 1. ICL7137 is tested in the circuit of Figure 2.
4. Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
5. Not tested, guaranteed by design.
6. 48kHz oscillator increases current by 20µA (TYP).

Typical Applications and Test Circuits

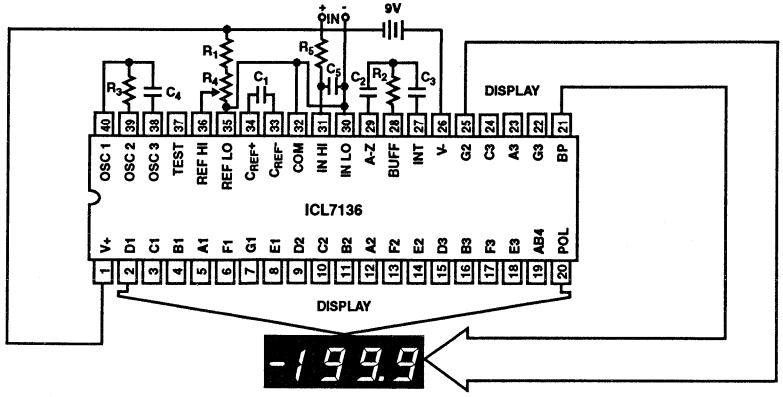


FIGURE 1. ICL7136 TEST CIRCUIT & TYPICAL APPLICATION WITH LCD DISPLAY COMPONENTS SELECTED FOR 200mV FULL-SCALE

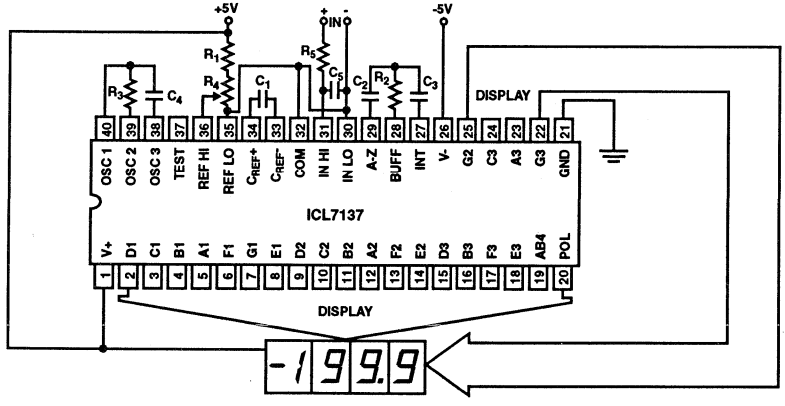
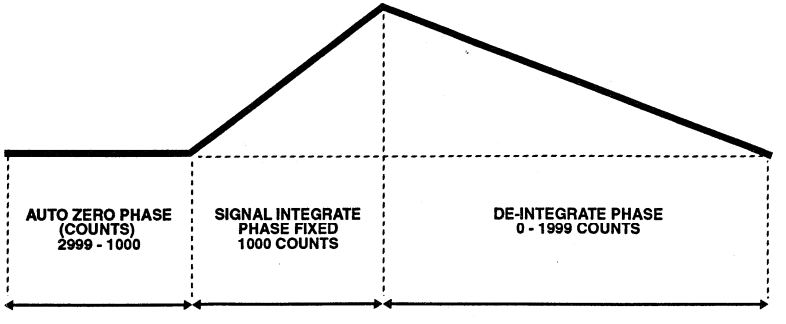


FIGURE 2. ICL7137 TEST CIRCUIT & TYPICAL APPLICATION WITH LED DISPLAY COMPONENTS SELECTED FOR 200mV FULL-SCALE

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**
  $f_{OSC} = 0.45/RC$
  $C_{OSC} > 50pF$; $R_{OSC} > 50K\Omega$
  f_{OSC} Typ. = 48KHz
- **OSCILLATOR PERIOD**
  $t_{OSC} = RC/0.45$
- **INTEGRATION CLOCK FREQUENCY**
  $f_{CLOCK} = f_{OSC}/4$
- **INTEGRATION PERIOD**
  $t_{INT} = 1000 \times (4/f_{OSC})$
- **60/50Hz REJECTION CRITERION**
  t_{INT}/t_{60Hz} or t_{INT}/t_{50Hz} = Integer
- **OPTIMUM INTEGRATION CURRENT**
  $I_{INT} = 1.0\mu A$
- **FULL-SCALE ANALOG INPUT VOLTAGE**
  V_{INFS} Typically = 200mV or 2.0V
- **INTEGRATE RESISTOR**
  $$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$
- **INTEGRATE CAPACITOR**
  $$C_{INT} = \frac{(t_{INT})\,(I_{INT})}{V_{INT}}$$
- **INTEGRATOR OUTPUT VOLTAGE SWING**
  $$V_{INT} = \frac{(t_{INT})\,(I_{INT})}{C_{INT}}$$
- **V_{INT} MAXIMUM SWING:**
  $(V- + 0.5V) < V_{INT} < (V+ - 0.5V)$, V_{INT} typically = 2.0V
- **DISPLAY COUNT**
  $$COUNT = 1000 \times \frac{V_{IN}}{V_{REF}}$$
- **CONVERSION CYCLE**
  $t_{CYC} = t_{CLOCK} \times 4000$
  $t_{CYC} = t_{OSC} \times 16{,}000$
  when f_{OSC} = 48KHz; t_{CYC} = 333ms
- **COMMON MODE INPUT VOLTAGE**
  $(V- + 1.0V) < V_{IN} < (V+ - 0.5V)$
- **AUTO-ZERO CAPACITOR**
  $0.01\mu F < C_{AZ} < 1.0\mu F$
- **REFERENCE CAPACITOR**
  $0.1\mu F < C_{REF} < 1.0\mu F$
- **V_{COM}**
  Biased between V+ and V-.
- **$V_{COM} \cong V+ - 2.8V$**
  Regulation lost when V+ to V- < ≅6.8V.
  If V_{COM} is externally pulled down to (V + to V -)/2, the V_{COM} circuit will turn off.
- **ICL7136 POWER SUPPLY: SINGLE 9V**
  V+ - V- = 9V
  Digital supply is generated internally
  $V_{TEST} \cong V+ - 4.5V$
- **ICL7136 DISPLAY: LCD**
  Type: Direct drive with digital logic supply amplitude.
- **ICL7137 POWER SUPPLY: DUAL ±5.0V**
  V+ = +5.0V to GND
  V- = -5.0V to GND
  Digital Logic and LED driver supply V+ to GND
- **ICL7137 DISPLAY: LED**
  Type: Non-Multiplexed Common Anode

Typical Integrator Amplifier Output Waveform (INT Pin)



TOTAL CONVERSION TIME = 4000 x t_{CLOCK} = 16,000 x t_{OSC}

Pin Description

PIN NUMBER		NAME	FUNCTION	DESCRIPTION
40 PIN DIP	44 PIN FLATPACK			
1	8	V+	SUPPLY	Power Supply
2	9	D1	OUTPUT	Driver Pin for Segment "D" of the display units digit
3	10	C1	OUTPUT	Driver Pin for Segment "C" of the display units digit
4	11	B1	OUTPUT	Driver Pin for Segment "B" of the display units digit
5	12	A1	OUTPUT	Driver Pin for Segment "A" of the display units digit
6	13	F1	OUTPUT	Driver Pin for Segment "F" of the display units digit
7	14	G1	OUTPUT	Driver Pin for Segment "G" of the display units digit
8	15	E1	OUTPUT	Driver Pin for Segment "E" of the display units digit
9	16	D2	OUTPUT	Driver Pin for Segment "D" of the display tens digit
10	17	C2	OUTPUT	Driver Pin for Segment "C" of the display tens digit
11	18	B2	OUTPUT	Driver Pin for Segment "B" of the display tens digit
12	19	A2	OUTPUT	Driver Pin for Segment "A" of the display tens digit
13	20	F2	OUTPUT	Driver Pin for Segment "F" of the display tens digit
14	21	E2	OUTPUT	Driver Pin for Segment "E" of the display tens digit
15	22	D3	OUTPUT	Driver pin for segment "D" of the display hundreds digit
16	23	B3	OUTPUT	Driver pin for segment "B" of the display hundreds digit
17	24	F3	OUTPUT	Driver pin for segment "F" of the display hundreds digit
18	25	E3	OUTPUT	Driver pin for segment "E" of the display hundreds digit
19	26	AB4	OUTPUT	Driver pin for both "A" and "B" segments of the display thousands digit
20	27	POL	OUTPUT	Driver pin for the negative sign of the display
21	28	BP/GND	OUTPUT	Driver pin for the LCD backplane/Power Supply Ground
22	29	G3	OUTPUT	Driver pin for segment "G" of the display hundreds digit
23	30	A3	OUTPUT	Driver pin for segment "A" of the display hundreds digit
24	31	C3	OUTPUT	Driver pin for segment "C" of the display hundreds digit
25	32	G2	OUTPUT	Driver pin for segment "G" of the display tens digit
26	34	V-	SUPPLY	Negative power supply
27	35	INT	OUTPUT	Integrator amplifier output. To be connected to integrating capacitor
28	36	BUFF	OUTPUT	Input buffer amplifier output. To be connected to integrating resistor
29	37	A-Z	INPUT	Integrator amplifier input.To be connected to auto-zero capacitor
30 31	38 39	IN LO IN HI	INPUT	Differential inputs. To be connected to input voltage to be measured. LO & HI designators are for reference and do not imply that LO should be connected to lower potential, e.g. for negative inputs IN LO has a higher potential than IN HI.
32	40	COMMON	SUPPLY/ OUTPUT	Internal voltage reference output.
33 34	41 42	C_{REF-} C_{REF+}		Connection pins for reference capacitor.
35 36	43 44	REF LO REF HI	INPUT	Input pins for reference voltage to the device. REF HI should be positive reference to REF LO.
37	3	TEST	INPUT	Display test. Turns on all segments when tied to V+.
38 39 40	4 6 7	OSC3 OSC2 OSC1	OUTPUT OUTPUT INPUT	Device clock generator circuit connection pins

Detailed Description

Analog Section

Figure 3 shows the Analog Section for the ICL7136 and ICL7137. Each measurement cycle is divided into four phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE), (4) zero integrate (ZI).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range: up to 1V from either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is

$$\text{DISPLAY READING} = 1000\left(\frac{V_{IN}}{V_{REF}}\right).$$

Zero Integrator Phase

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Finally, a feedback loop is closed around the system to IN HI to cause the integrator output to return to zero. Under normal conditions, this phase lasts for between 11 to 140 clock pulses, but after a "heavy" overrange conversion, it is extended to 740 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 0.5V below the positive supply to 1.0V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 2V full-scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

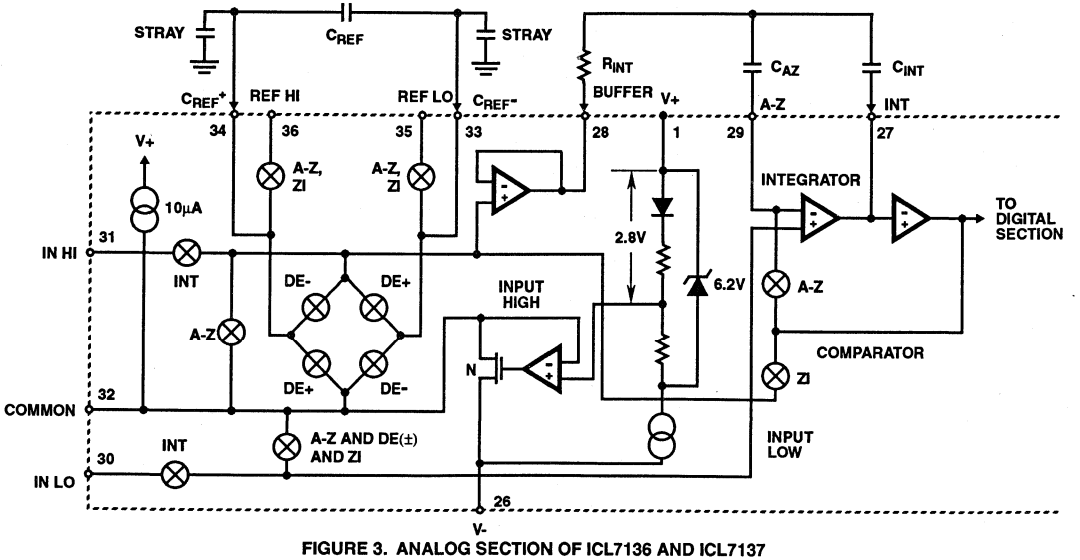


FIGURE 3. ANALOG SECTION OF ICL7136 AND ICL7137

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to de-integrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor such that it is large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection.)

Analog COMMON

This pin is included primarily to set the common mode voltage for battery operation (ICL7136) or for any system where the input signals are floating with respect to the power supply. The COMMON pin sets a voltage that is approximately 2.8V more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6.8V. However, analog COMMON has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the COMMON voltage will have a low voltage coefficient (0.001%/V), low output impedance (≅15Ω), and a temperature coefficient typically less than 150ppm/°C.

The limitations of the on chip reference should also be recognized, however. With the ICL7137, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full-scale from 25μV to 80μVp-p. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111(8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an over range condition. This is because over-range is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between over range and a non-over range count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The ICL7136, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Figure 4.

Analog COMMON is also used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently tied to analog COMMON, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog COMMON is tied to an N channel FET that can sink approximately 3mA of current to hold the voltage 2.8V below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so COMMON may easily be tied to a more negative voltage thus overriding the internal reference.

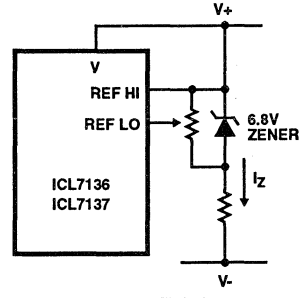


FIGURE 4A.

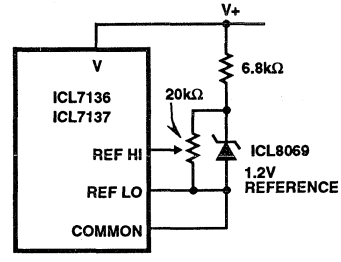


FIGURE 4B.

FIGURE 4. USING AN EXTERNAL REFERENCE

TEST

The TEST pin serves two functions. On the ICL7136 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application. No more than a 1mA load should be applied.

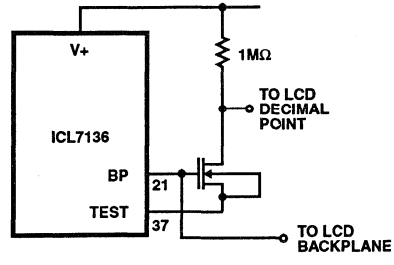


FIGURE 5. SIMPLE INVERTER FOR FIXED DECIMAL POINT

The second function is a "lamp test". When TEST is pulled high (to V+) all segments will be turned on and the display should read "-1888". The TEST pin will sink about 5mA under these conditions.

CAUTION: On the ICL7136, in the lamp test mode, the segments have a constant DC voltage (no square-wave) and may burn the LCD display if left in this mode for several minutes.

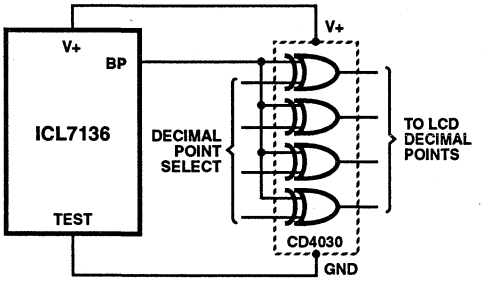


FIGURE 6. EXCLUSIVE 'OR' GATE FOR DECIMAL POINT DRIVE

Digital Section

Figures 7 and 8 show the digital section for the ICL7136 and ICL7137, respectively. In the ICL7136, an internal digital ground is generated from a 6V Zener diode and a large P-channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases negligible DC voltage exists across the segments.

Figure 8 is the Digital Section of the ICL7137. It is identical to the ICL7136 except that the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2mA to 8mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16mA.

In both devices, the polarity indication is "on" for negative analog inputs. If IN LO and IN HI are reversed, this indication can be reversed also, if desired.

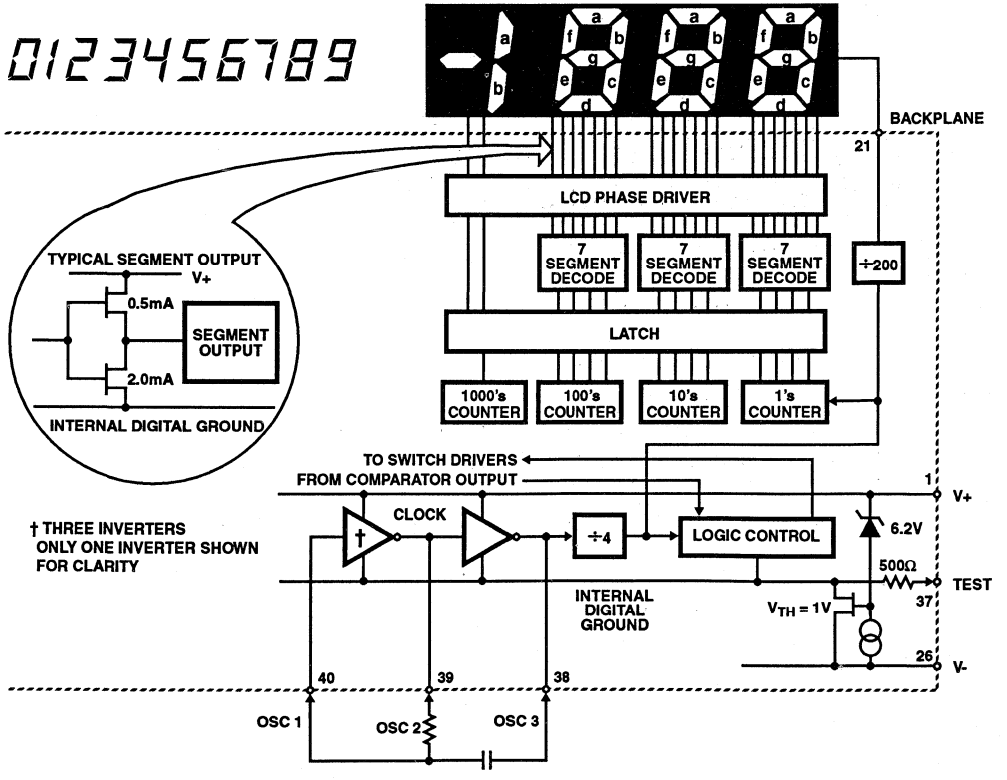


FIGURE 7. ICL7136 DIGITAL SECTION

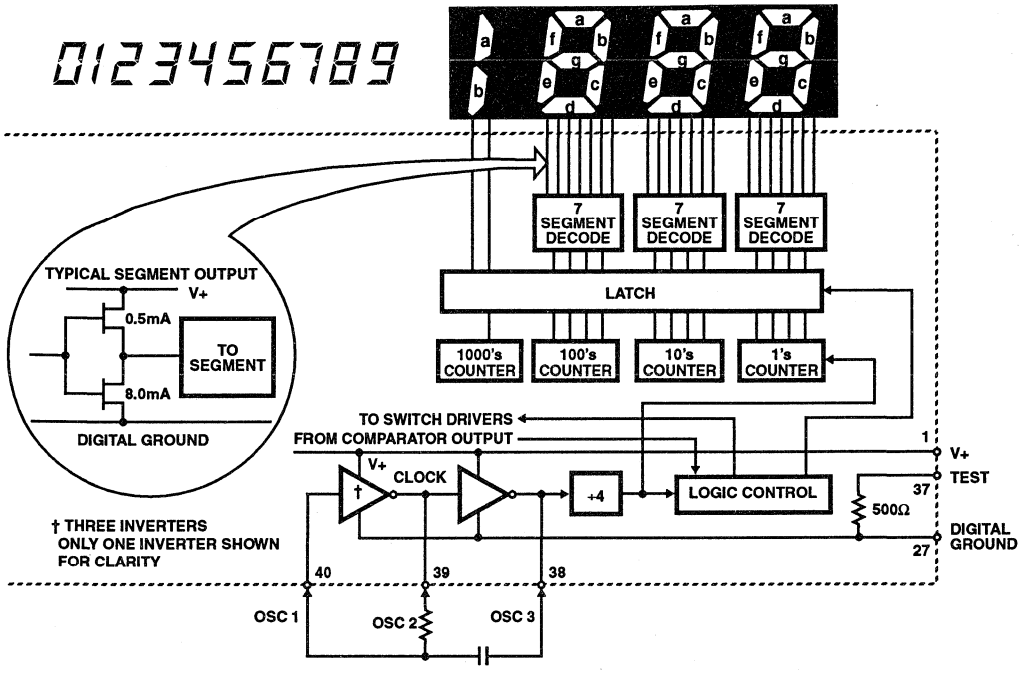


FIGURE 8. ICL7137 DIGITAL SECTION

System Timing

Figure 9 shows the clocking arrangement used in the ICL7136 and ICL7137. Two basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. An R-C oscillator using all three pins.

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full-scale, auto-zero gets the unused portion of reference de-integrate. This makes a complete measure cycle of 4,000 counts (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, $33^1/_3$kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, $66^2/_3$kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50Hz and 60Hz (also 400Hz and 440Hz).

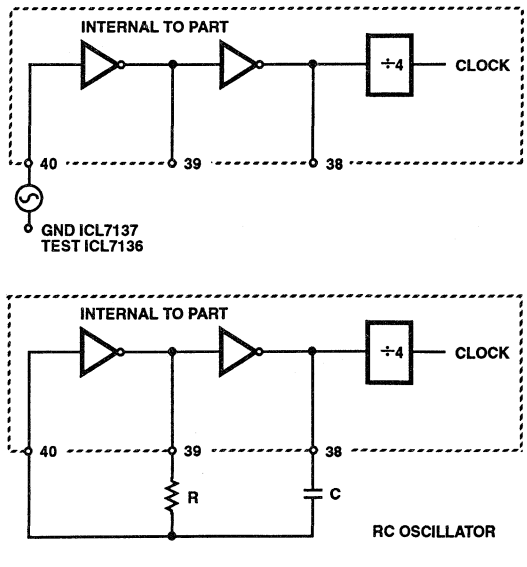


FIGURE 9. CLOCK CIRCUITS

Component Value Selection

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 1μA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2V full-scale, 1.8MΩ is near optimum and similarly a 180kΩ for a 200mV scale.

Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance buildup will not saturate the integrator swing (approximately. 0.3V from either supply). In the ICL7136 or the ICL7137, when the analog COMMON is used as a reference, a nominal +2V full-scale integrator swing is fine. For the ICL7137 with +5V supplies and analog COMMON tied to supply ground, a ±3.5V to +4V swing is nominal. For three readings/second (48kHz clock) nominal values for C_{INT} are 0.047μF and 0.5μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is that it must have a low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200mV full-scale where noise is very important, a 0.47μF capacitor is recommended. On the 2V scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the REF LO pin is not at analog COMMON) and a 200mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0μF will hold the roll-over error to 0.5 count in this instance.

Oscillator Components

For all ranges of frequency a 180kΩ resistor is recommended and the capacitor is selected from the equation

$$f = \frac{0.45}{RC}$$ For 48kHz Clock (3 Readings/second),

C = 50pF

Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: $V_{IN} = 2V_{REF}$. Thus, for the 200mV and 2V scale, V_{REF} should equal 100mV and 1V, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full-scale reading when the voltage from the transducer is 0.662V. Instead of dividing the input down to 200mV, the designer should use the input voltage directly and select V_{REF} = 0.341 V. Suitable values for integrating resistor and capacitor would be 330kΩ and 0.047μF. This makes the system slightly quieter and also avoids a divider network on the input. The ICL7137 with ±5V supplies can accept input signals up to ±4V. Another advantage of this system occurs when a digital reading of zero is desired for $V_{IN} \neq 0$. Temperature and weighing systems with a variable fare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between IN HI and COMMON and the variable (or fixed) offset voltage between COMMON and IN LO.

ICL7137 Power Supplies

The ICL7137 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application. See ICL7660 data sheet for an alternative.

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5V.
3. An external reference is used.

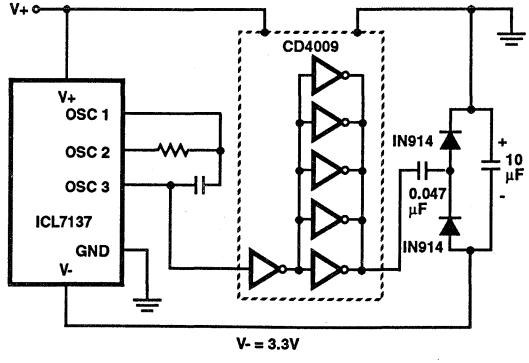


FIGURE 10. GENERATING NEGATIVE SUPPLY FROM +5V

Typical Applications

The ICL7136 and ICL7137 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

The following application notes contain very useful information on understanding and applying this part and are available from Harris semiconductor.

Application Notes

A016 "Selecting A/D Converters"

A017 "The Integrating A/D Converter"

A018 "Do's and Don'ts of Applying A/D Converters"

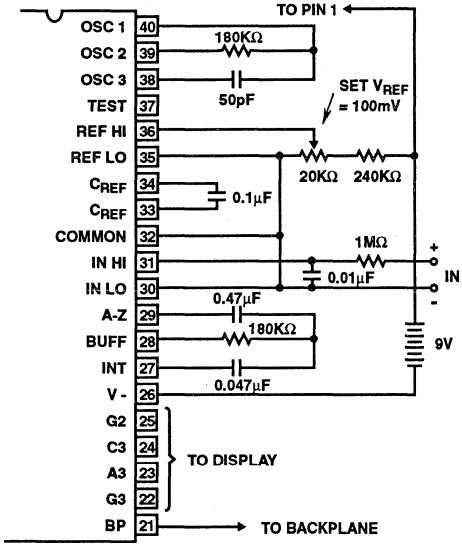
A023 "Low Cost Digital Panel Meter Designs"

A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7136/7/9 Family"

A046 "Building a Battery-Operated Auto Ranging DVM with the ICL7136"

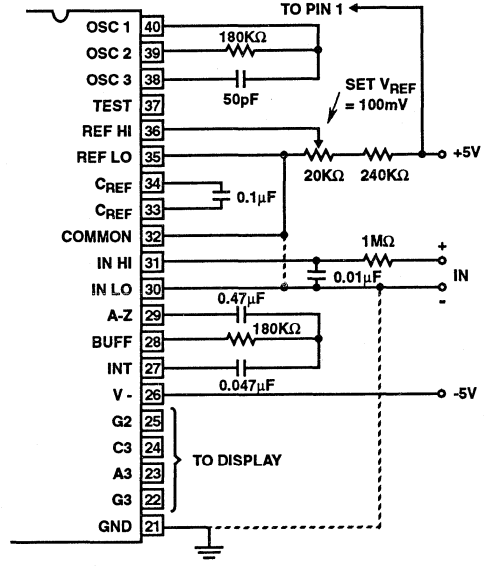
A052 "Tips for Using Single Chip $3^1/_2$ Digit A/D Converters"

Typical Applications



Values shown are for 200mV full-scale, 3 readings/sec., floating supply voltage (9V battery).

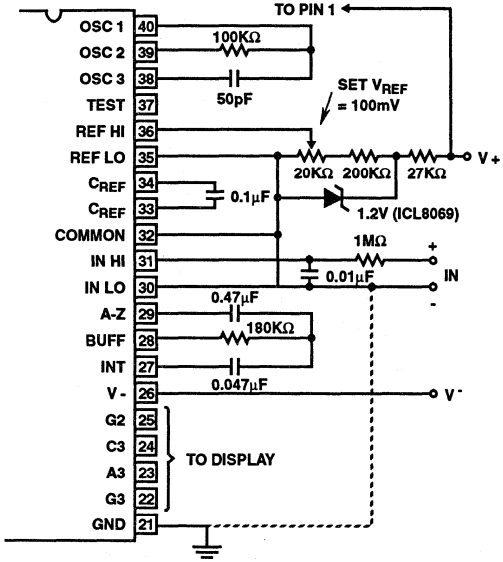
FIGURE 11. ICL7136 USING THE INTERNAL REFERENCE



Values shown are for 200mV full-scale, 3 readings/sec. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog COMMON.)

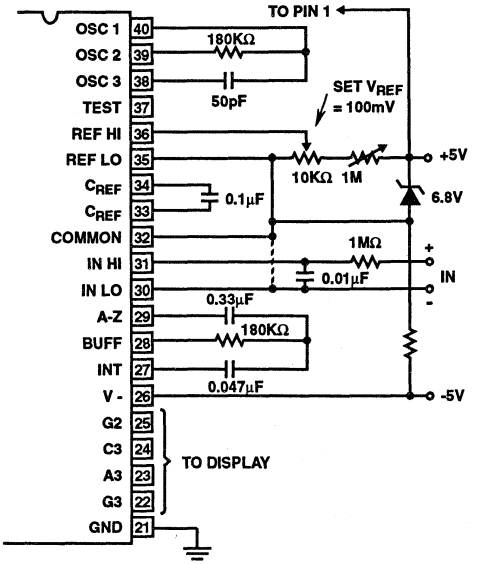
FIGURE 12. ICL7137 USING THE INTERNAL REFERENCE

Typical Applications (Continued)



IN LO is tied to supply COMMON establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply GND) and the pre-regulator is overridden.

FIGURE 13. ICL7137 WITH AN EXTERNAL BAND-GAP REFERENCE (1.2V TYPE)



Since low TC zeners have breakdown voltages ~ 6.8V, diode must be plasced across the total supply (10V). As in the case of Figure 14, IN LO may be tied to either COMMON or GND

FIGURE 14. ICL7137 WITH ZENER DIODE REFERENCE

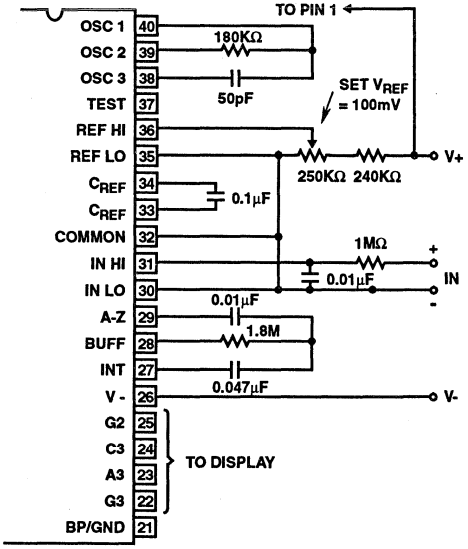
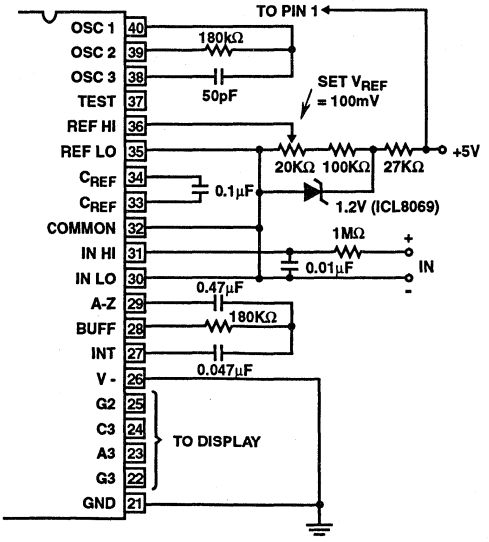


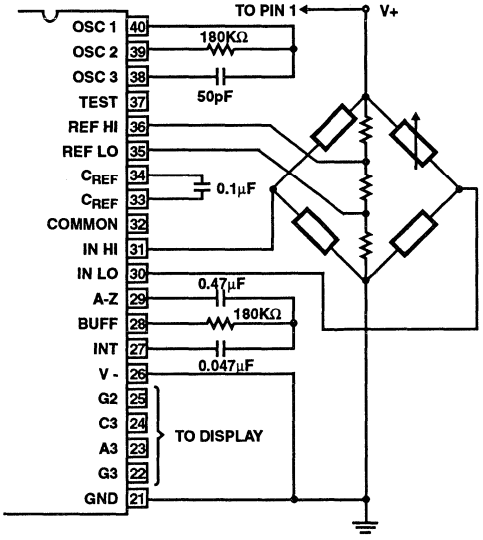
FIGURE 15. ICL7136 AND ICL7137: RECOMMENDED COMPONENT VALUES FOR 2.0V FULL-SCALE



An external reference must be used in this application, since the voltage between V+ and V- is insufficient for correct operation of the internal reference.

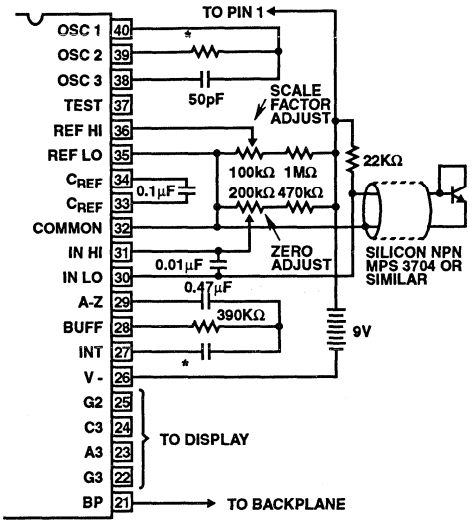
FIGURE 16. ICL7137 OPERATED FROM SINGLE +5V

Typical Applications (Continued)



The resistor values within the bridge are determined by the desired sensitivity.

FIGURE 17. ICL7137 MEASUREING RATIOMETRIC VALUES OF QUAD LOAD CELL



A silicon diode-connected transistor has a temperature coefficient of about -2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

* Value depends on clock frequency.

FIGURE 18. ICL7136 USED AS A DIGITAL CENTIGRADE THERMOMETER

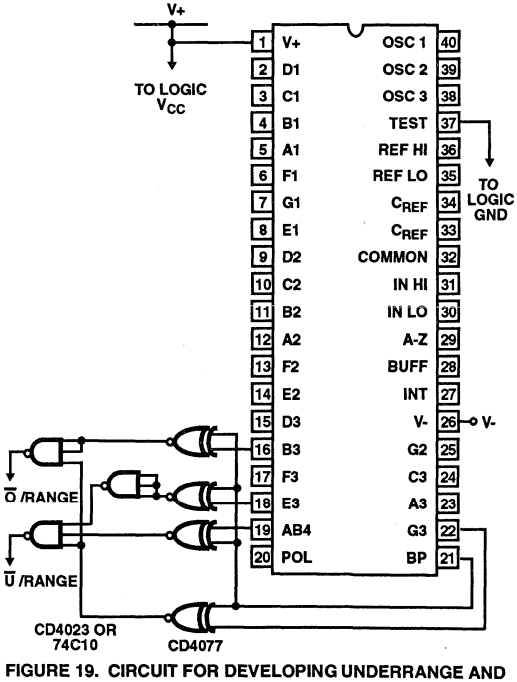


FIGURE 19. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNAL FROM ICL7136 OUTPUTS

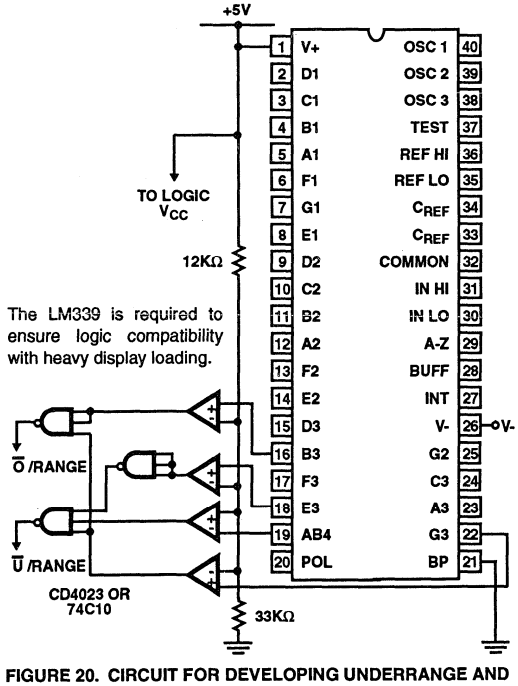
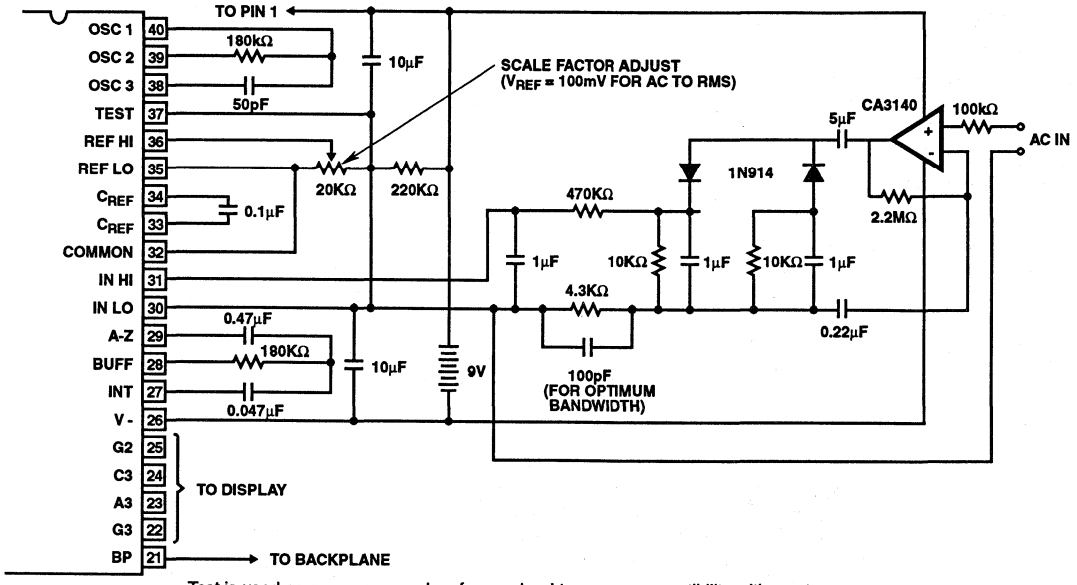


FIGURE 20. CIRCUIT FOR DEVELOPING UNDERRANGE AND OVERRANGE SIGNALS FROM ICL7137 OUTPUT

Typical Applications (Continued)



Test is used as a common-mode reference level to ensure compatibility with most op amps.

FIGURE 21. AC TO DC CONVERTER WITH ICL7136

Die Characteristics

DIE DIMENSIONS:
127 x 149 Mils

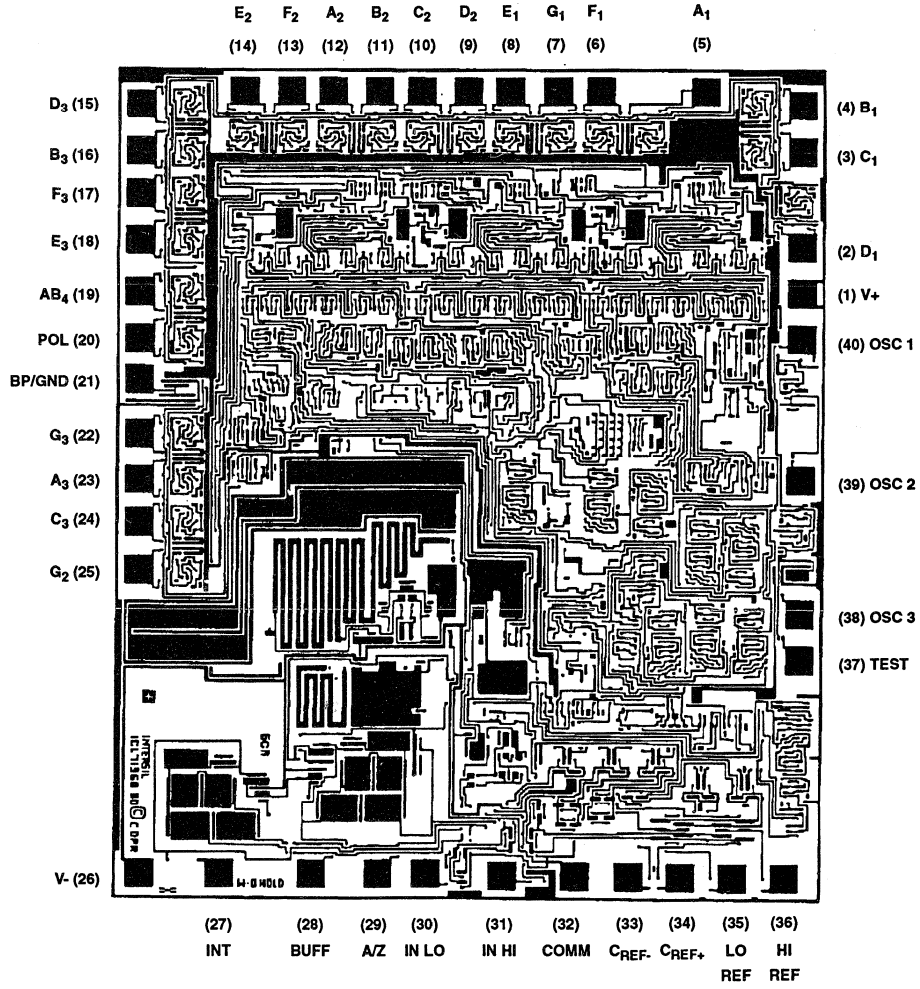
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG Nitride
Thickness: 15kÅ ± 3kÅ

WORST CASE CURRENT DENSITY:
$9.1 \times 10^4 A/cm^2$

Metallization Mask Layout

ICL7136, ICL7137



ICL7139, ICL7149

$3^3/_4$ Digit Autoranging Multimeter

December 1993

Features

- 13 Ranges - ICL7139
  - 4 DC Voltage 400mV, 4V, 40V, 400V
  - 1 AC Voltage 400V
  - 4 DC Current 4mA, 40mA, 400mA, 4A
  - 4 Resistance 4kΩ, 40kΩ, 400kΩ, 4MΩ
- 18 Ranges - ICL7149
  - 4 DC Voltage 400mV, 4V, 40V, 400V
  - 2 AC Voltage with Optional AC Circuit
  - 4 DC Current 4mA, 40mA, 400mA, 4A
  - 4 AC Current with Optional AC Circuit
  - 4 Resistance 4kΩ, 40kΩ, 400kΩ, 4MΩ
- Autoranging - First Reading is Always on Correct Range
- On-Chip Duplex LCD Display Drive Including Three Decimal Points and 11 Annunciators
- No Additional Active Components Required
- Low Power Dissipation - Less than 20mW - 1000 Hour Typical Battery Life
- Display Hold Input
- Continuity Output Drives Piezoelectric Beeper
- Low Battery Annunciator with On-Chip Detection
- Guaranteed Zero Reading for 0V Input on All Ranges

Description

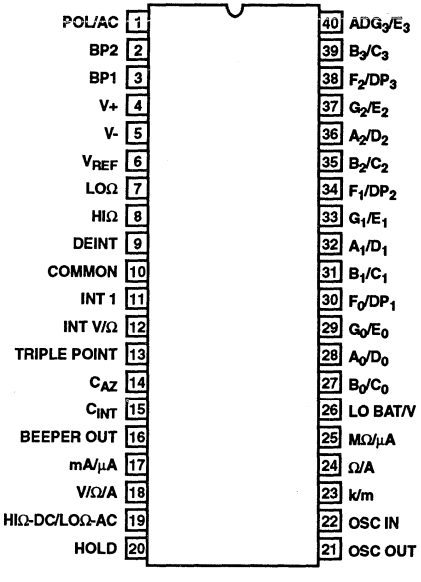
The Harris ICL7139 and ICL7149 are high performance, low power, auto-ranging digital multimeter ICs. Unlike other autoranging multimeter ICs, the ICL7139 and ICL7149 always display the result of a conversion on the correct range. There is no "range hunting" noticeable in the display. The unit will autorange between the four different ranges. A manual switch is used to select the 2 high group ranges. DC current ranges are 4mA and 40mA in the low current group, and 400mA and 4A in the high current group. Resistance measurements are made on 4 ranges, which are divided into two groups. The low resistance ranges are 4/40kΩ. The high resistance ranges are 0.4/4MΩ. Resolution on the lowest range is 1Ω.

Ordering Information

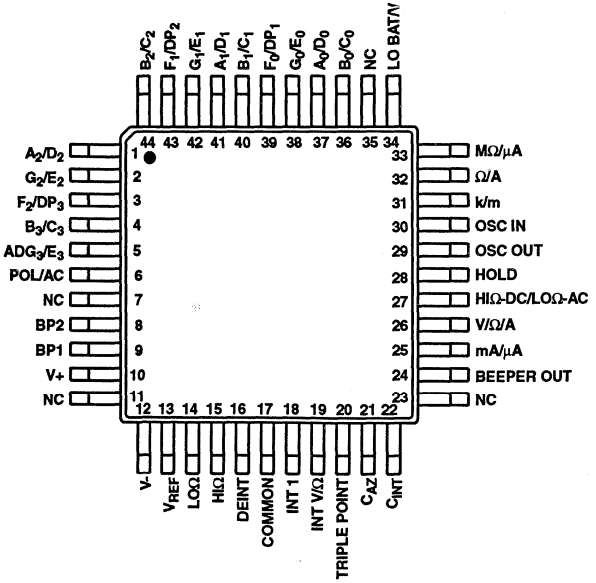
PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7139CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7149CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7149CM44	0°C to +70°C	44 Lead Surface Mount (MQFP)

Pinouts

ICL7139 AND ICL7149 (PDIP)
TOP VIEW



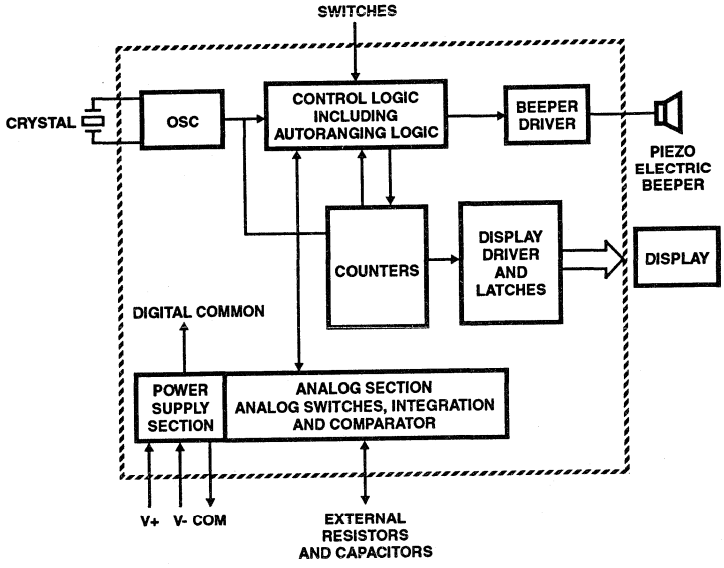
ICL7149 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3088

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (V+ to V-) 15V
Reference Input Voltage (V_{REF} to COM) 3V
Analog Input Current (IN + Current or IN + Voltage) 100µA
Clock Input Swing ..... V+ to V+ -3
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance θ_{JA}
PDIP ..... 50°C/W
MQFP ..... 80°C/W
Maximum Power Dissipation
Plastic Package 800mW
Operating Temperature Range ..... 0°C to +70°C
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = 9V, T_A = +25°C, V_{REF} adjusted for -3.700 reading on DC volts, test circuit as shown in Figure 3. Crystal = 120kHz. (See Figure 14)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} or I_{IN} or R_{IN} = 0.00	-00.0	-	+00.0	V, I, Ω
Linearity (Best Straight Line) (Note 6)	(Notes 1 and 8)	-1	-	+1	Counts
Accuracy DC V, 400V Range Only	(Notes 1 and 8)	-	-	±1	% of RDG ±1
Accuracy DC V, 400V Range Excluded	(Notes 1 and 8)	-	-	±0.30	% of RDG ±1
Accuracy Ω, 4K and 400K Range	(Notes 1 and 8)	-	-	±0.75	% of RDG ±8
Accuracy Ω, 4K and 4M Range	(Notes 1 and 8)	-	-	±1	% of RDG ±9
Accuracy DC I, Unadjusted for FS	(Notes 1 and 8)	-	-	±0.75	% of RDG ±1
Accuracy DC I, Adjusted for FS	(Notes 1 and 8)	-	±0.2	-	% of RDG ±1
Accuracy AC V	At 60Hz (Notes 5, 7, and 8)	-	±2	-	% of RDG
Open Circuit Voltage for Ω Measurements	$R_{UNKNOWN}$ = Infinity	-	V_{REF}	-	V
Noise	V_{IN} = 0, DC V (Note 2, 95% of Time)	-	0.1	-	LSB
Noise	V_{IN} = 0, AC V (Note 2, 95% of Time)	-	4	-	LSB
Supply Current	V_{IN} = 0, DC Voltage Range	-	1.5	2.4	mA
Analog Common (with Respect to V+)	I_{COMMON} < 10µA	2.7	2.9	3.1	V
Temperature Coefficient of Analog Common	I_{COMMON} < 10µA, Temp. = 0°C to +70°C	-	-100	-	ppm/°C
Output Impedance of Analog Common	I_{COMMON} < 10µA	-	1	10	Ω
Backplane/Segment Drive Voltage	Average DC < 50mV	2.8	3.0	3.2	V
Backplane/Segment Display Frequency		-	75	-	Hz
Switch Input Current	V_{IN} = V+ to V- (Note 3)	-50	-	+50	µA
Switch Input Levels (High Trip Point)		V+ - 0.5	-	V+	V
Switch Input Levels (Mid Trip Point)		V- + 3	-	V+ - 2.5	V
Switch Input Levels (Low Trip Point)		V-	-	V- + 0.5	V
Beeper Output Drive (Rise or Fall Time)	C_{LOAD} = 10nF	-	25	100	µs
Beeper Output Frequency		-	2	-	kHz
Continuity Detect	Range = Low Ω, V_{REF} = 1.00V	-	1.5	-	kΩ
Power Supply Functional Operation	V+ to V-	7	9	11	V
Low Battery Detect	V+ to V- (Note 4)	6.5	7	7.5	V

NOTE:
1. Accuracy is defined as the worst case deviation from ideal input value including: offset, linearity, and rollover error.
2. Noise is defined as the width of the uncertainty window (where the display will flicker) between two adjacent codes.
3. Applies to pins 17-20.
4. Analog Common falls out of regulation when the Low Battery Detect is asserted, however the ICL7139 and ICL7149 will continue to operate correctly with a supply voltage above 7V and below 11V.
5. For 50Hz use a 100kHz crystal.
6. Guaranteed by design, not tested.
7. ICL7139 only.
8. RDG = Reading

Timing Waveform

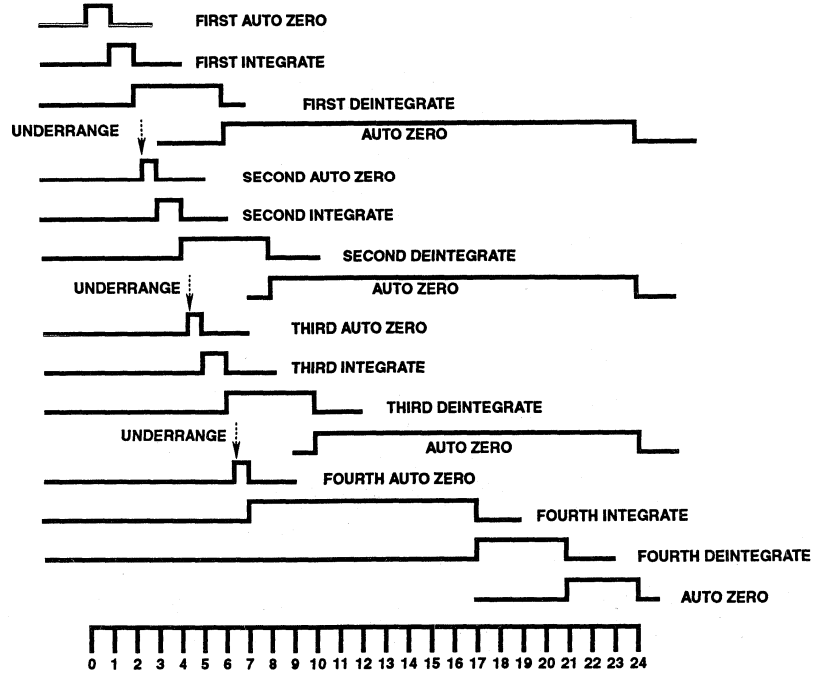


FIGURE 1. LINE FREQUENCY CYCLES (1 CYCLE = 1000 INTERNAL CLOCK PULSES = 2000 OSCILLATION CYCLES)

Pin Descriptions

I/O	PIN NUMBER	DESCRIPTION
O	1	Segment Driver POL/AC
O	2	Backplane 2
O	3	Backplane 1
I	4	V+
I	5	V-
I	6	Reference Input
O	7	Lo Ω
O	8	Hi Ω
I/O	9	Deintegrate
I/O	10	Analog Common
I	11	Int I
I	12	Int V/Ω
I	13	Triple Point
I	14	Auto Zero Capacitor (C_{AZ})
I	15	Integrate Capacitor (C_{INT})
O	16	Beeper Output
I	17	mA/μA
I	18	Ω/V/A
I	19	Hi Ω DC/Lo Ω AC

I/O	PIN NUMBER	DESCRIPTION
I	20	Hold
O	21	Oscillator Out
I	22	Oscillator In
O	23	Segment DRIVER k/m
O	24	Segment Driver Ω/A
O	25	Segment Driver M Ω/μA
O	26	Segment Driver Lo Bat/V
O	27	Segment Driver B_0/C_0
O	28	Segment Driver A_0/D_0
O	29	Segment Driver G_0/E_0
O	32	Segment Driver A_1/D_1
O	33	Segment Driver G_1/E_1
O	34	Segment Driver F_1/DP_1
O	35	Segment Driver B_2/C_1
O	39	Segment Driver B_3/C_3
O	40	Segment Driver ADG_3/E_3

NOTE: For segment drivers, segments are listed as (segment for backplane 1)/(segment for backplane 2). Example: pin 27; segment B_0 is on backplane 1, segment C_0 is on backplane 2.

Detailed Description

General

The Functional Block Diagram shows the digital section which includes all control logic, counters, and display drivers. The digital section is powered by V+ and Digital Common, which is about 3V below V+. The oscillator is also in the digital section. Normally 120kHz for rejection of 60Hz AC interference and 100kHz for rejection of 50Hz AC should be used. The oscillator output is divided by two to generate the internal master clock. The analog section contains the integrator, comparator, reference section, analog buffers, and several analog switches which are controlled by the digital logic. The analog section is powered from V+ and V-.

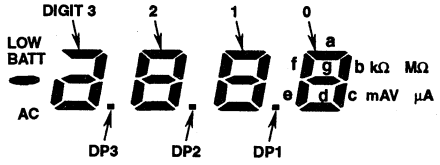


FIGURE 2. DISPLAY SEGMENT NOMENCLATURE

DC Voltage Measurement

Autozero

Only those portions of the analog section which are used during DC voltage measurements are shown in Figure 3. As shown in the timing diagram (Figure 1), each measurement starts with an autozero (AZ) phase. During this phase, the integrator and comparator are configured as unity gain buffers and their non-inverting inputs are connected to Common. The output of the integrator, which is equal to its offset, is stored on C_{AZ} - the autozero capacitor. Similarly, the offset of the comparator is stored in C_{INT}. The autozero cycle equals 1000 clock cycles which is one 60Hz line cycle with a 120kHz oscillator, or one 50Hz line cycle with a 100kHz oscillator.

Range 1 Integrate

The ICL7139 and ICL7149 perform a full autorange search for each reading, beginning with range 1. During the range 1 integrate period, internal switches connect the INT V/Ω terminal to the Triple Point (Pin 13). The input signal is integrated for 10 clock cycles, which are gated out over a period of 1000 clock cycles to ensure good normal mode rejection of AC line interference.

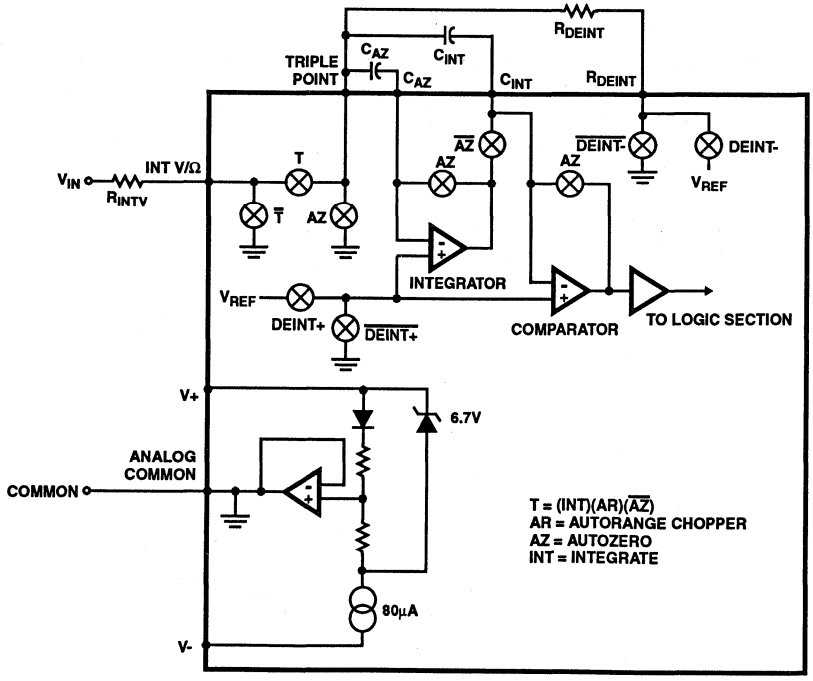


FIGURE 3. DETAILED CIRCUIT DIAGRAM FOR DC VOLTAGE MEASUREMENT

Range 1 Deintegrate

At the beginning of the deintegrate cycle, the polarity of the voltage on the integrator capacitor (C_{INT}) is checked, and either the DEINT+ or DEINT- is asserted. The integrator capacitor C_{INT} is then discharged with a current equal to V_{REF}/R_{DEINT}. The comparator monitors the voltage on C_{INT}. When the voltage on C_{INT} is reduced to zero (actually to the V_{OS} of the comparator), the comparator output switches, and the current count is latched. If the C_{INT} voltage zero-crossing does not occur before 4000 counts have elapsed, the overload flag is set. "OL" (overload) is then displayed on the LCD. If the latched result is between 360 and 3999, the count is transferred to the output latches and is displayed. When the count is less than 360, an underrange has occurred, and the ICL7139 and ICL7149 then switch to range 2 - the 40V scale.

Range 2

The range 2 measurement begins with an autozero cycle similar to the one that preceded range 1 integration. Range 2 cycle length however, is one AC line cycle, minus 360 clock cycles. When performing the range 2 cycle, the signal is integrated for 100 clock cycles, distributed throughout one line cycle. This is done to maintain good normal mode rejection. Range 2 sensitivity is ten times greater than range 1 (100 vs 10 clock cycle integration) and the full scale voltage of range 2 is 40V. The range 2 deintegrate cycle is identical to the range 1 deintegrate cycle, with the result being displayed only for readings greater than 360 counts. If the reading is below 360 counts, the ICL7139 and ICL7149 again asserts the internal underrange signal and proceeds to range 3.

Range 3

The range 3V or 4V full scale measurement is identical to the range 2 measurement, except that the input signal is integrated during the full 1000 clock cycles (one line frequency cycle). The result is displayed if the reading is greater than 360 counts. Underrange is asserted, and a range 4 measurement is performed if the result is below 360 counts.

Range 4

This measurement is similar to the range 1, 2 and 3 measurements, except that the integration period is 10,000 clock cycles (10 line cycles) long. The result of this measurement is transferred to the output latches and displayed even if the reading is less than 360.

Autozero

After finding the first range for which the reading is above 360 counts, the display is updated and an autozero cycle is entered. The length of the autozero cycle is variable which results in a fixed measurement period of 24,000 clock cycles (24 line cycles).

DC Current

Figure 4 shows a simplified block diagram of the analog section of the ICL7139 and ICL7149 during DC current measurement. The DC current measurements are very similar to DC voltage measurements except: 1) The input voltage is developed by passing the input current through a 0.1Ω (HI current ranges), or 9.9Ω (LOW current ranges)

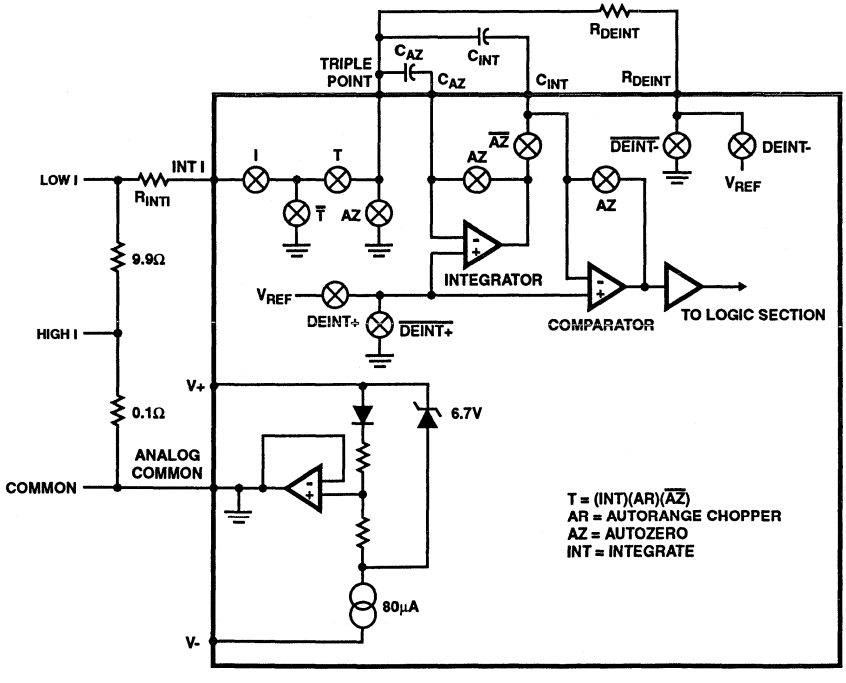


FIGURE 4. DETAILED CIRCUIT DIAGRAM FOR DC CURRENT MEASUREMENT

current sensing resistor; 2) Only those ranges with 1000 and 10,000 clock cycles of integration are used; 3) The $R_{INT\ I}$ resistor is 1MΩ, rather than the 10MΩ value used for the $R_{INT\ V}$ resistor.

By using the lower value integration resistor, and only the 2 most sensitive ranges, the voltage drop across the current sensing resistor is 40mV maximum on the 4mA and 400mA ranges; 400mV maximum on the 40mA and 4A scales. With some increase in noise, these "burden" voltages can be reduced by lowering the value of both the current sense resistors and the $R_{INT\ I}$ resistor proportionally. The DC current measurement timing diagram is similar to the DC voltage measurement timing diagram, except in the DC current timing diagram, the first and second integrate and deintegrate phases are skipped.

AC Voltage Measurement for ICL7139

As shown in Figure 5, the AC input voltage is applied directly to the ICL7139 input resistor. No separate AC to DC conversion circuitry is needed. The AC measurement cycle is begun by disconnecting the integrator capacitor and using the integrator as an autozeroed comparator to detect the positive-going zero crossing. Once synchronized to the AC input, the autozero loop is closed and a normal integrate/deintegrate cycle begins. The ICL7139 resynchronizes itself to the AC input prior to every reading. Because diode D4 is in series with the integrator capacitor, only positive current from the integrator flows into the integrator capacitor, C_{INT}. Since the voltage on C_{INT} is proportional to the half-wave rectified average AC input voltage, a conversion factor must be applied to convert the reading to RMS. This conversion factor is $\pi/2\sqrt{2}$ = 1.1107, and the system clock is manipulated to perform the RMS conversion. As a result the deintegrate and autozero cycle times are reduced by 10%.

AC Voltage Measurement for ICL7149

The ICL7149 is designed to be used with an optional AC to DC voltage converter circuit. It will autorange through two voltage ranges (400V and 40V), and the AC annunciator is enabled. A typical averaging AC to DC converter is shown in Figure 6, while an RMS to DC converter is shown in Figure 7. AC current can also be measured with some simple modifications to either of the two circuits in Figures 6 and 7.

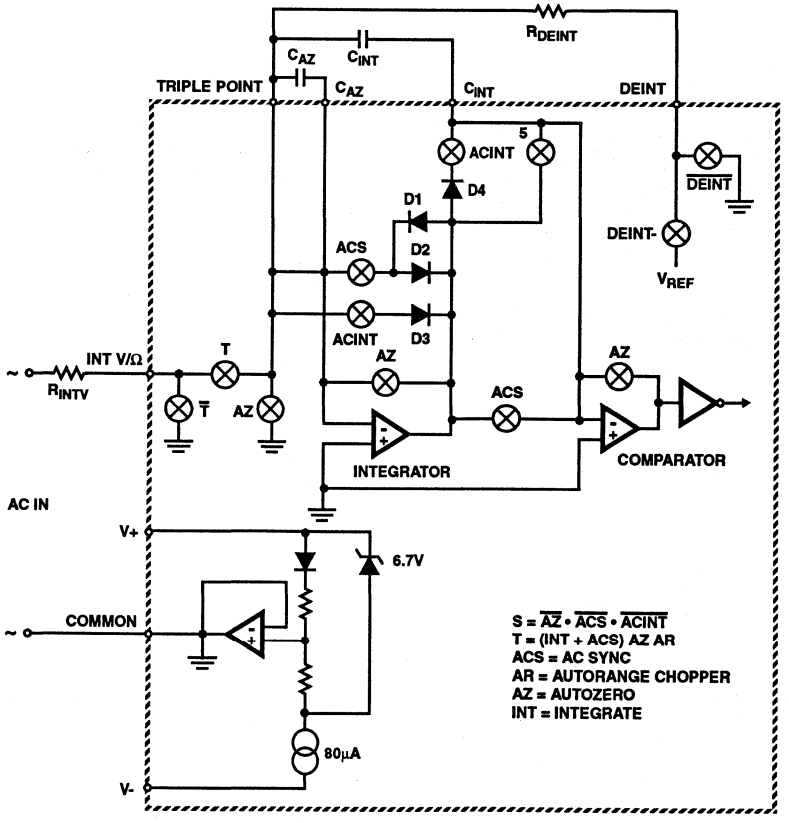


FIGURE 5. DETAILED CIRCUIT DIAGRAM FOR AC VOLTAGE MEASUREMENT FOR ICL7139 ONLY

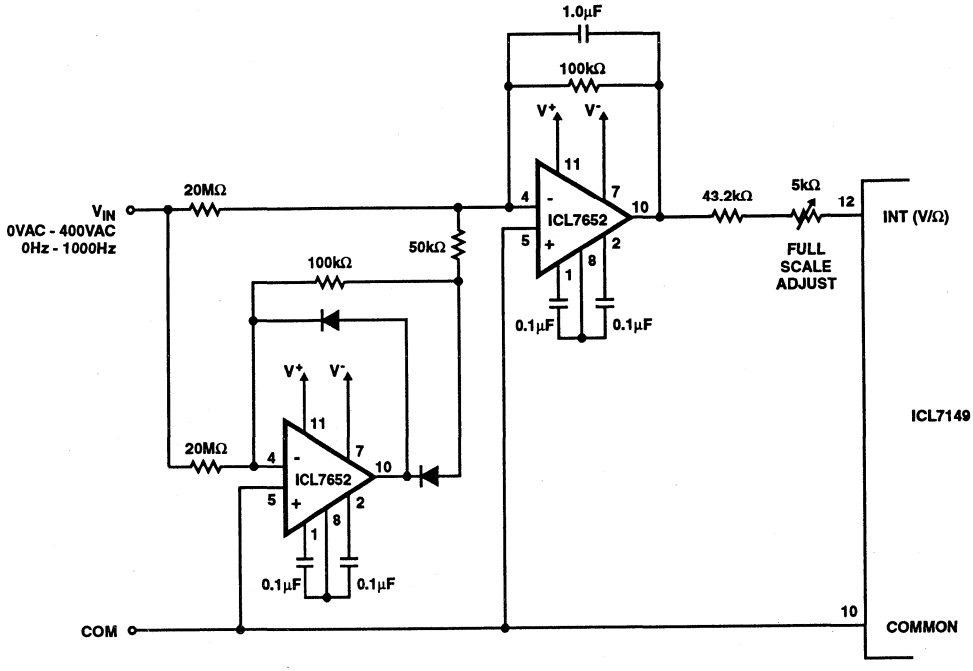


FIGURE 6. AC VOLTAGE MEASUREMENT USING OPTIONAL AVERAGING CIRCUIT

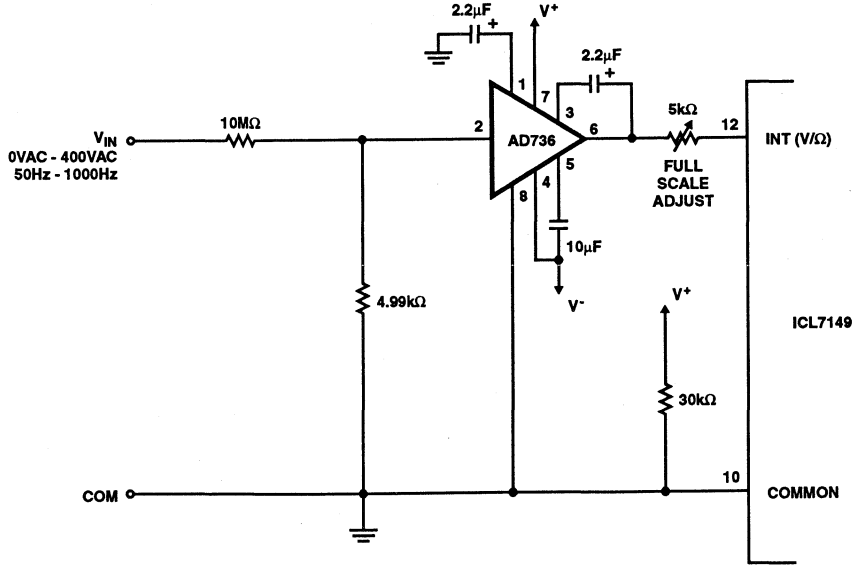


FIGURE 7. AC VOLTAGE MEASUREMENT USING OPTIONAL RMS CONVERTER CIRCUIT

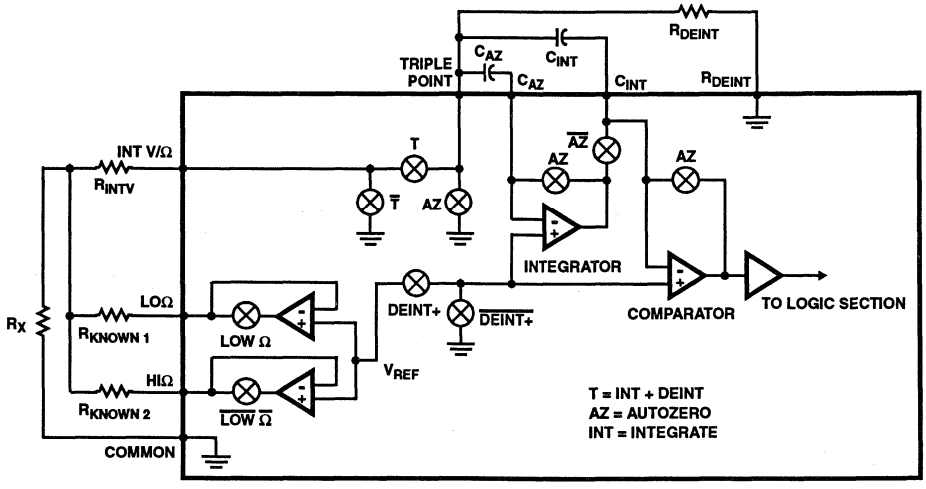


FIGURE 8. DETAILED CIRCUIT DIAGRAM FOR RATIOMETRIC Ω MEASUREMENT

Ratiometric Ω Measurement

The ratiometric Ω measurement is performed by first integrating the voltage across an unknown resistor, R_X, then effectively deintegrating the voltage across a known resistor (R_{KNOWN1} or R_{KNOWN2} of Figure 8). The shunting effect of R_{INTV} does not affect the reading because it cancels exactly between integration and deintegration. Like the current measurements, the Ω measurements are split into two sets of ranges. LO Ω measurements use a 10kΩ reference resistor, and the full scale ranges are 4kΩ and 40kΩ. HI Ω measurements use a 1MΩ reference resistor, and the full scale ranges are 0.4MΩ and 4MΩ. The measurement phases and timing are the same as the measurement phases and timing for DC current except: 1) During the integrate phases the input voltage is the voltage across the unknown resistor R_X, and; 2) During the deintegrate phases, the input voltage is the voltage across the reference resistor R_{KNOWN1} or R_{KNOWN2}.

Continuity Indication

When the ICL7139 and ICL7149 are in the LO Ω measurement mode, the continuity circuit of Figure 9 will be active. When the voltage across R_X is less than approximately 100mV, the beeper output will be on. When R_{KNOWN} is 10kΩ, the beeper output will be on when R_X is less than 1kΩ.

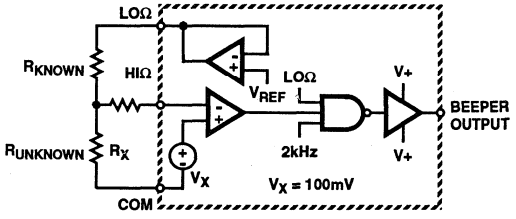


FIGURE 9. CONTINUITY BEEPER DRIVE CIRCUIT

Common Voltage

The analog and digital common voltages of the ICL7139 and ICL7149 are generated by an on-chip resistor/zener/diode combination, shown in Figure 10. The resistor values are chosen so the coefficient of the diode voltage cancels the positive temperature coefficient of the zener voltage. This voltage is then buffered to provide the analog common and the digital common voltages. The nominal voltage between V+ and analog common is 3V. The analog common buffer can sink about 20mA, or source 0.01mA, with an output impedance of 10Ω. A pullup resistor to V+ may be used if more sourcing capability is desired. Analog common may be used to generate the reference voltage, if desired.

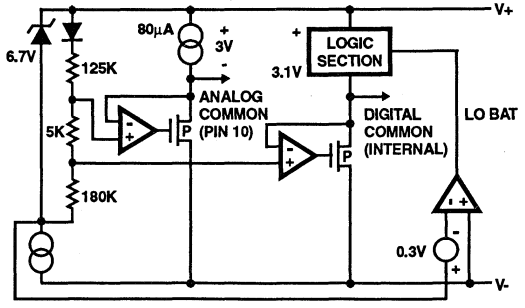


FIGURE 10. ANALOG AND DIGITAL COMMON VOLTAGE GENERATOR CIRCUIT

Oscillator

The ICL7139 and ICL7149 use a parallel resonant-type crystal in a Pierce oscillator configuration, as shown in Figure 11, and requires no other external components. The crystal eliminates the need to trim the oscillator frequency. An external signal may be capacitively coupled in OSC IN, with a signal level between 0.5V and 3V pk-pk. Because the OSC

OUT pin is not designed to drive large external loads, loading on this pin should not exceed a single CMOS input. The oscillator frequency is internally divided by two to generate the ICL7139 and ICL7149 clock. The frequency should be 120kHz to reject 60Hz AC signals, and 100kHz to reject 50Hz signals.

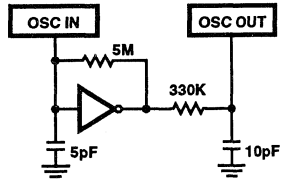


FIGURE 11. INTERNAL OSCILLATOR CIRCUIT DIAGRAM

Display Drivers

Figure 12 shows typical LCD Drive waveforms, RMS ON, and RMS OFF voltage calculations. Duplex multiplexing is used to minimize the number of connections between the ICL7139 and ICL7149 and the LCD. The LCD has two separate backplanes. Each drive line can drive two individual segments, one referenced to each backplane. The ICL7139 and ICL7149 drive $3^3/_4$ 7-segment digits, 3 decimal points, and 11 annunciators. Annunciators are used to indicate polarity, low battery condition, and the range in use. Peak drive voltage across the display is approximately 3V. An LCD with approximately 1.4V RMS threshold voltage should be used. The third voltage level needed for duplex drive waveforms is generated through an on-chip resistor string. The DC component of the drive waveforms is guaranteed to be less than 50mV.

Ternary Input

The Ω/Volts/Amps logic input is a ternary, or 3-level input. This input is internally tied to the common voltage through a high-value resistor, and will go to the middle, or "Volts" state, when not externally connected. When connected to V-, approximately 5µA of current flows out of the input. In this case, the logic level is the "Amps", or low state. When connected to V+, about 5µA of current flows into the input. Here, the logic level is the "Ω", or high state. For other pins, see Table 2.

TABLE 2. TERNARY INPUTS CONNECTIONS

PIN NUMBER	V+	OPEN OR COM	V-
17	mA	µA	Test
18	Ω	V	Amps
19	HiΩ/DC	LoΩ/AC	Test
20	Hold	Auto	Test

Component Selection

For optimum performance while maintaining the low-cost advantages of the ICL7139 and ICL7149, care must be taken when selecting external components. This section reviews specifications and performance effects of various external components.

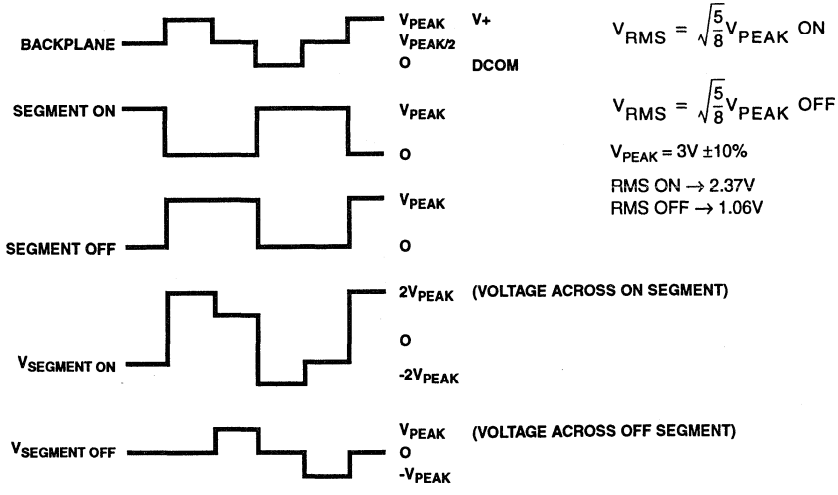


FIGURE 12. DUPLEXED LCD DRIVE WAVEFORMS

Integrator Capacitor, C_{INT}

As with all dual-slope integrating convertors, the integration capacitor must have low dielectric absorption to reduce linearity errors. Polypropylene capacitors add undetectable errors at a reasonable cost, while polystyrene and polycarbonate may be used in less critical applications. The ICL7139 and ICL7149 are designed to use a 3.3nF (0.0033µF) C_{INT} with an oscillator frequency of 120kHz and an R_{INTV} of 10MΩ. With a 100kHz oscillator frequency (for 50Hz line frequency rejection), C_{INT} and R_{INTV} affects the voltage swing of the integrator. Voltage swing should be as high as possible without saturating the integrator. Saturation occurs when the integrator output is within 1V of either V+ or V-. Integrator voltage swing should be about ±2V when using standard component values. For different R_{INTV} and oscillator frequencies the value of C_{INT} can be calculated from:

$$C_{INT} = \frac{(\text{Integrate Time}) \times (\text{Integrate Current})}{(\text{Desired Integrator Swing})}$$

$$= \frac{(10{,}000 \times 2 \times \text{Oscillator Period}) \times 0.4\text{V}/R_{INTV}}{(2\text{V})}$$

Integrator Resistors

The normal values of the $R_{INT\,V}$ and $R_{INT\,I}$ resistors are 10MΩ and 1MΩ respectively. Though their absolute values are not critical, unless the value of the current sensing resistors are trimmed, their ratio should be 10:1, within 0.05%. Some carbon composition resistors have a large voltage coefficient which will cause linearity errors on the 400V scale. Also, some carbon composition resistors are very noisy. The class "A" output of the integrator begins to have nonlinearities if required to sink more than 70µA (the sourcing limit is much higher). Because $R_{INT\,V}$ drives a virtual ground point, the input impedance of the meter is equal to $R_{INT\,V}$.

Deintegration Resistor, R_{DEINT}

Unlike most dual-slope A/D converters, the ICL7139 and ICL7149 use different resistors for integration and deintegration. R_{DEINT} should normally be the same value as $R_{INT\,V}$, and have the same temperature coefficient. Slight errors in matching may be corrected by trimming the reference voltage.

Autozero Capacitor, C_{AZ}

The C_{AZ} is charged to the integrator's offset voltage during the autozero phases, and subtracts that voltage from the input signal during the integrate phases. The integrator thus appears to have zero offset voltage. Minimum C_{AZ} value is determined by: 1) Circuit leakages; 2) C_{AZ} self-discharge; 3) Charge injection from the internal autozero switches. To avoid errors, the C_{AZ} voltage change should be less than 1/10 of a count during the 10,000 count clock cycle integration period for the 400mV range. These requirements set a lower limit of 0.047µF for C_{AZ} but 0.1µF is the preferred value. The upper limit on the value of C_{AZ} is set by the time constant of the autozero loop, and the 1 line cycle time period allotted to autozero. C_{AZ} may be several 10s of µF before approaching this limit.

The ideal C_{AZ} is a low leakage polypropylene or Teflon capacitor. Other film capacitors such as polyester, polystyrene, and polycarbonate introduce negligible errors. If a few seconds of settling time upon power-up is acceptable, the C_{AZ} may be a ceramic capacitor, provided it does not have excessive leakage.

Ω Measurement Resistors

Because the ICL7139 and ICL7149 use a ratiometric Ω measurement technique, the accuracy of Ω reading is primarily determined by the absolute accuracy of the R_{KNOWN1} and R_{KNOWN2}. These should normally be 10kΩ and 1MΩ, with an absolute accuracy of at least 0.5%.

Current Sensing Resistors

The 0.1Ω and 9.9Ω current sensing resistors convert the measured current to a voltage, which is then measured using $R_{INT\,I}$. The two resistors must be closely matched, and the ratio between $R_{INT\,I}$ and these two resistors must be accurate - normally 0.5%. The 0.1Ω resistor must be capable of handling the full scale current of 4 amps, which requires it to dissipate 1.6 watts.

Continuity Beeper

The Continuity Beeper output is designed to drive a piezoelectric transducer at 2kHz (using a 120kHz crystal), with a voltage output swing of V+ to V-. The beeper output off state is at the V+ rail. When crystals with different frequencies are used, the frequency needed to drive the transducer can be calculated by dividing the crystal frequency by 60.

Display

The ICL7139 and ICL7149 use a custom, duplexed drive display with range, polarity, and low battery annunciators. With a 3V peak display voltage, the RMS ON voltage will be 2.37V minimum; RMS OFF voltage will be 1.06V maximum. Because the display voltage is not adjustable, the display should have a 10% ON threshold of about 1.4V. Most display manufacturers supply a graph that shows contrast versus RMS drive voltage. This graph can be used to determine what the contrast ratio will be when driven by the ICL7139 and ICL7149. Most display thresholds decrease with increasing temperature. The threshold at the maximum operating temperature should be checked to ensure that the "off" segments will not be turned "on" at high temperatures.

Crystal

The ICL7139 and ICL7149 are designed to use a parallel resonant 120kHz or 100kHz crystal with no additional external components. The R_S parameter should be less than 25kΩ to ensure oscillation. Initial frequency tolerance of the crystal can be a relatively loose 0.05%.

Switches

Because the logic input draws only about 5µA, switches driving these inputs should be rated for low current, or "dry" operations. The switches on the external inputs must be able to reliably switch low currents, and be able to handle voltages in excess of 400V AC.

Reference Voltage Source

A voltage divider connected to V+ and Common is the simplest source of reference voltage. While minimizing external component count, this approach will provide the same voltage tempco as the ICL7139 and ICL7149 Common - about 100PPM/°C. To improve the tempco, an ICL8069 bandgap reference may be used (see Figure 13). The reference voltage source output impedance must be $\leq R_{DEINT}/4000$.

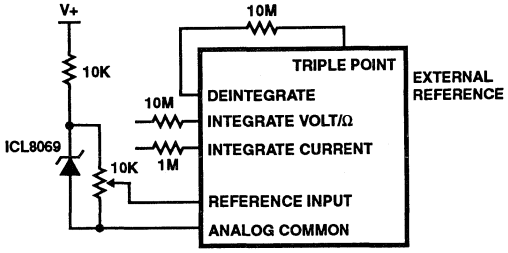


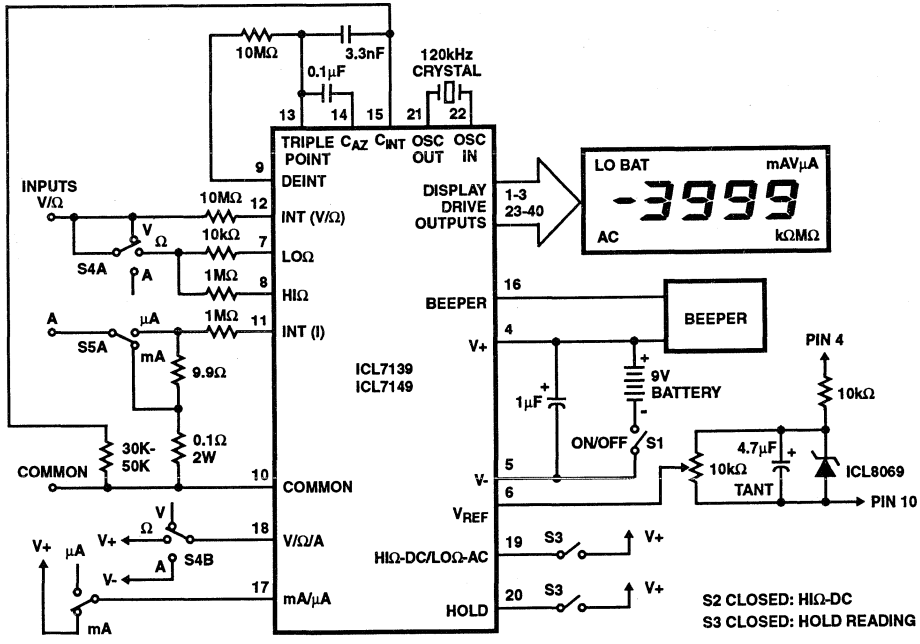
FIGURE 13. EXTERNAL VOLTAGE REFERENCE CONNECTION TO ICL7139 AND ICL7149

Applications, Examples, and Hints

A complete autoranging $3^3/_4$ digit multimeter is shown in Figure 14. The following sections discuss the functions of specific components and various options.

Meter Protection

The ICL7139 and ICL7149 and their external circuitry should be protected against accidental application of 110/220V AC line voltages on the Ω and current ranges. Without the necessary precautions, both the ICL7139 and ICL7149 and their external components could be damaged under such fault conditions. For the current ranges, fast-blow fuses should be used between S5A in Figure 14 and the 0.1Ω and 9.9Ω shunt resistors. For the Ω ranges, no additional protection circuitry is required. However, the 10kΩ resistor connected to pin 7 must be able to dissipate 1.2W or 4.8W for short periods of time during accidental application of 110V or 220V AC line voltages respectively.



NOTES:

1. Crystal is a Statek or SaRonix CX-IV type.
2. Multimeter protection components have not been shown.
3. Display is from LXD, part number 38D8R02H (or equivalent).
4. Beeper is from muRata, part number PKM24-4A0 (or equivalent).

FIGURE 14. BASIC MULTIMETER APPLICATION CIRCUIT FOR ICL7139 AND ICL7149

Printed Circuit Board Layout Considerations

Particular attention must be paid to rollover performance, leakages, and guarding when designing the PCB for a ICL7139 and ICL7149 based multimeter.

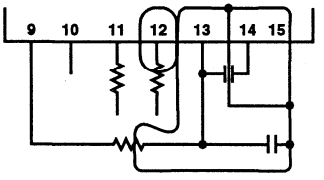


FIGURE 15. PC BOARD LAYOUT

Rollover Performance, Leakages, and Guarding

Because the ICL7139 and ICL7149 system measures very low currents, it is essential that the PCB have low leakage. Boards should be properly cleaned after soldering. Areas of particular importance are: 1) The INT V/Ω and INT I Pins; 2) The Triple Point; 3) The R_{DEINT} and the C_{AZ} pins.

The conversion scheme used by the ICL7139 and ICL7149 changes the common mode voltage on the integrator and the capacitors C_{AZ} and C_{INT} during a positive deintegrate cycle. Stray capacitance to ground is charged when this occurs, removing some of the charge on C_{INT} and causing rollover error. Rollover error increases about 1 count for each picofarad of capacitance between C_{AZ} or the Triple Point and ground, and is seen as a zero offset for positive voltages. Rollover error is not seen as gain error.

The rollover error causes the width of the +0 count to be larger than normal. The ICL7139 and ICL7149 will thus read zero until several hundred μV are applied in the positive direction. The ICL7139 and ICL7149 will read -1 when approximately -100μV is applied.

The rollover error can be minimized by guarding the Triple Point and C_{AZ} nodes with a trace connected to the C_{INT} pin, (see Figure 15) which is driven by the output of the integrator. Guarding these nodes with the output of the integrator reduces the stray capacitance to ground, which minimizes the charge error on C_{INT} and C_{AZ}. If possible, the guarding should be used on both sides of the PC board.

Stray Pickup

While the ICL7139 and ICL7149 have excellent rejection of line frequency noise and pickup in the DC ranges, any stray coupling will affect the AC reading. Generally, the analog circuitry should be as close as possible to the ICL7139 and ICL7149. The analog circuitry should be removed or shielded from any 120V AC power inputs, and any AC sources such as LCD drive waveforms. Keeping the analog circuit section close to the ICL7139 and ICL7149 will also help keep the area free of any loops, thus reducing magnetically coupled interference coming from power transformers, or other sources.

DATA ACQUISITION 3

A/D CONVERTERS - INTEGRATING

HARRIS SEMICONDUCTOR

HI-7159A

December 1993

NOT RECOMMENDED FOR NEW DESIGN

Microprocessor Compatible $5^1/_2$ Digit A/D Converter

Features

- ±200,000 Count A/D Converter
- 2V Full Scale Reading With 10µV Resolution
- 15 Conversions Per Second In $5^1/_2$ Digit Mode
- 60 Conversions Per Second In $4^1/_2$ Digit Mode
- Serial or Parallel Interface Modes
- Four Selectable Baud Rates
- Differential Analog Input
- Differential Reference Input
- Digital Autozero

Applications

- Weigh Scales
- Part Counting Scales
- Laboratory Instruments
- Process Control/Monitoring
- Energy Management
- Seismic Monitoring

Description

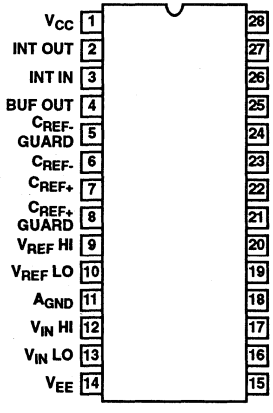
The Harris HI-7159A is a monolithic A/D converter that uses a unique dual slope technique which allows it to resolve input changes as small as 1 part in 200,000 (10µV) without the use of critical external components. Its digital autozeroing feature virtually eliminates zero drift over temperature. The device is fabricated in Harris' proprietary low noise BiMOS process, resulting in exceptional linearity and noise performance. The HI-7159A's resolution can be switched between a high resolution 200,000 count ($5^1/_2$ digit) mode, and a high speed 20,000 count ($4^1/_2$ digit) mode without any hardware modifications. In the $4^1/_2$ digit uncompensated mode, speeds of 60 conversions per second can be achieved. The HI-7159A is designed to be easily interfaced with most microprocessors through either of its three serial and one parallel interface modes. In the serial modes, any one of four common baud rates is available.

Ordering Information

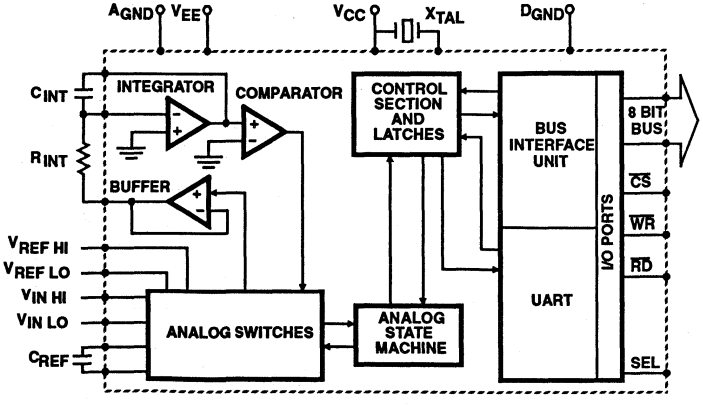
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-7159A-5	0°C to +75°C	28 Lead Plastic DIP

Pinout

HI-7159A
(PDIP)
TOP VIEW



Functional Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **2936.1**

Absolute Maximum Ratings

Supply Voltage
- V_{CC} to GND (A_{GND}/D_{GND}) . . . . . -0.3V < V_{CC} < +6V
- V_{EE} to GND (A_{GND}/D_{GND}) . . . . . +0.3V < V_{CC} < -6V

Digital Pins, (pins 15 - 28) . . . . . D_{GND} -0.3V < V_D < V_{CC} +0.3V
Analog Pins, (pins 2 - 13) . . . . . V_{EE} -0.3V < V_A < V_{CC} +0.3V
Storage Temperature, T_{STG} . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C

Thermal Information

Thermal Resistance θ_{JA}
- Plastic DIP Package . . . . . 55°C/W

Operating Temperature . . . . . 0°C to +70°C
Maximum Power Dissipation (+25°C) 300mW
- Derate Above +70°C by 10mW/°C

Junction Temperature . . . . . +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V_{CC} = +5V, V_{EE} = -5V, D_{GND} = 0V, A_{GND} = 0V, $V_{REF\ HI}$ = +1.00000V, $V_{REF\ LO}$ = AGND, f_{CLOCK} = 2.40MHz, R_{INT} = 400kΩ, C_{INT} = 0.01µF, T_A = +25°C, $V_{IN\ LO}$ = A_{GND}, C_{REF} = 1.0µF, $5^1/_2$ Digit Compensated Mode, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Integral Non-Linearity, INL	0.0V ≤ V_{IN} ≤ +2.0V (Notes 1, 2, 3, 4)	-	±0.0015	±0.0035	% FS
	-2.0V ≤ V_{IN} ≤ 0.0V (Notes 1, 2, 3, 4)	-	±0.0015	±0.0035	% FS
Ratiometric Reading	$V_{IN\ HI}$ = $V_{REF\ HI}$ = 1.00000V	99997	100000	100003	Counts
Zero Error, ZE	$V_{IN\ HI}$ = 0.00000V	-	0	±1	Counts
Voltage Range of $V_{IN\ LO}$ Input (pin 13), $V_{IN\ LO}$	-2V ≤ $V_{IN\ HI}$ - $V_{IN\ LO}$ ≤ 2V	-1	-	1	V
Voltage Range of $V_{IN\ HI}$ Input (pin 12), $V_{IN\ HI}$	-2V ≤ $V_{IN\ HI}$ - $V_{IN\ LO}$ ≤ 2V	$V_{IN\ LO}$-2V	-	$V_{IN\ LO}$ +2V	V
Common Mode Rejection, CMR	$V_{IN\ HI}$ = $V_{IN\ LO}$ = -3V to +3V	-	3	-	Counts
Input Leakage Current, I_{IN}	Pins 9, 10, 12, 13, V_{IN} = +3V, -3V	-	-	±1	nA
Input Capacitance, C_{IN}	Pins 9, 10, 12, 13	-	5	-	pF
Noise (Peak-to-Peak value, not exceeded 95% of time), e_N		-	±1	-	Counts
Zero Drift, $T_{C(ZE)}$	$V_{IN\ HI}$ = 0.00000V	-	0	-	Counts/°C
Full Scale Error Tempco, $T_{C(FSE)}$	$V_{IN\ HI}$ = ±2.00000V	-	±0.1	-	Counts/°C
Supply Range, V_{SUPPLY}					
V_{CC}		+4.75	+5.0	+5.5	V
V_{EE}		-4.75	-5.0	-5.5	V
V_{CC} Supply Current, I_{CC}		-	-	10	mA
V_{EE} Supply Current, I_{EE}		-	-	4.5	mA
Digital GND Current, I_{DGND}		-	-	5.5	mA
Analog GND Current, I_{AGND}		-	+3	-	µA
V_{CC}, V_{EE} Power Supply Rejection, PSR	$V_{IN\ HI}$ = $V_{REF\ HI}$ = 1.00000V V_{CC} = +4.75V, V_{EE} = -4.75V to V_{CC} = +5.50V, V_{EE} = -5.50V	-	3	-	Counts
Guard Driver Pins 5, 8 Output Current, I_{OGD}	V_{IN} (pins 9, 10) = +3V, -3V	±10	-	-	µA

NOTES:
1. All typical values have been characterized but are not production tested.
2. Not production tested, guaranteed by design and characterization.
3. Reference adjusted for correct full-scale reading.
4. V_{IN} = $V_{IN\ HI}$ - $V_{IN\ LO}$

Digital Performance, DC Characteristics

Test Conditions: V_{CC} = +5V, V_{EE} = -5V, D_{GND} = 0V, A_{GND} = 0V, $V_{REF\ HI}$ = +1.00000V, $V_{REF\ LO}$ = A_{GND}, f_{CLOCK} = 2.40MHz, R_{INT} = 400kΩ, C_{INT} = 0.01µF, T_A = +25°C, $V_{IN\ LO}$ = A_{GND}, C_{REF} = 1.0µF, $5^1/_2$ Digit Compensated Mode, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage, V_{IL}	Pins 15-25, 28	-	-	0.8	V
Input High Voltage, V_{IH}	Pins 15-25, 28	2.0	-	-	V
Output Low Voltage, V_{OL}	Pins 16, 18-25, I_{OL} = 1.6mA	-	-	0.4	V
Output High Voltage, V_{OH}	Pins 16, 18-25, I_{OH} = -400µA	2.4	-	-	V
Tri-State Leakage Current, Pins 18-25, I_{OL}	All Digital Drivers In High Impedance State, Parallel Mode. CS = V_{CC}, V_{IN} = 0V, V_{CC}	-	-	±10	µA
Leakage, Pins 15-17, 28, I_{IN}	V_{IN} = 0V, V_{CC}	-	-	±1	µA
Input Capacitance, C_{IN}	Pins 15, 17-25, 28	-	5	-	pF
	Pin 16	-	10	-	pF
Input Pullup Current (Pins 18-25), I_{PU}	Pins 18-25 at D_{GND} SEL = D_{GND} (Serial Modes)	-	-5	-	µA

AC Characteristics

(T_A = 0°C to +75°C) Test Conditions: V_{CC} = +4.75V, V_{EE} = -5.00V (Note 3), D_{GND} = 0V, A_{GND} = 0V, $V_{IN\ LO}$ = A_{GND}, $V_{REF\ HI}$ = +1.00000V, $V_{REF\ LO}$ = A_{GND}, f_{CLOCK} = 2.40MHz, R_{INT} = 400kΩ, C_{INT} = 0.01µF, V_{IL} = 0V, V_{IH} = 4V, V_{OL} = V_{OH} = 1.5V, t_R = t_F < 10ns, $5^1/_2$ Digit Compensated Mode, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Setup/Hold of $\overline{WR}$, T_1		0	-	-	ns
$\overline{WR}$ Setup of Data In, T_2		50	-	-	ns
$\overline{WR}$ Pulse Width, T_3		150	-	-	ns
Data Hold After $\overline{WR}$, T_4		20	-	-	ns
$\overline{CS}$ Setup/Hold of $\overline{RD}$, T_5	(Note 2)	25	-	-	ns
$\overline{RD}$ to Data Out, T_6	C_L = 50pF, V_O = 1.5V	-	-	100	ns
$\overline{RD}$ to High Z State, T_7		-	-	70	ns
$\overline{WR}$ to $\overline{RD}$, $\overline{WR}$ to $\overline{WR}$, T_A	(Note 2)	$5/f_{CLOCK}$	-	-	s
$\overline{RD}$ to $\overline{WR}$, T_B	(Note 2)	200	-	-	ns
RXD Setup of Data In, T_C	(Note 2)	60	-	-	ns
Data Hold After EXT CLK, T_D		40	-	-	ns
EXT CLK to data out, T_E		-	-	300	ns
$\overline{CS}$ Setup of TXD, T_F		100	-	-	ns

NOTES:

1. All typical values have been characterized but are not production tested.
2. Not production tested, guaranteed by design and characterization.
3. All AC characteristics are guaranteed for V_{CC} = +5V 15%, V_{EE} = -5V 15%, over T_A = 0°C to +75°C.

Timing Waveforms

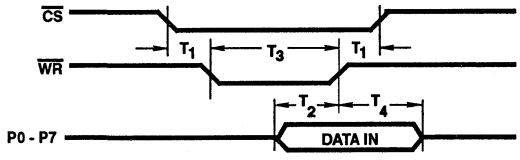


FIGURE 1A. WRITE

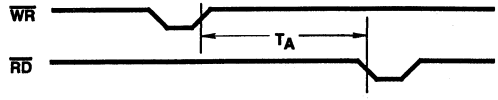


FIGURE 1B. WRITE TO READ CYCLE

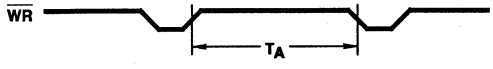


FIGURE 1C. WRITE TO WRITE CYCLE

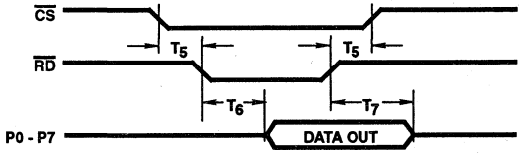


FIGURE 1D. READ

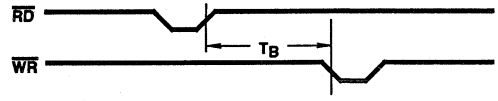


FIGURE 1E. READ TO WRITE CYCLE

FIGURE 1. PARALLEL MODE TIMING

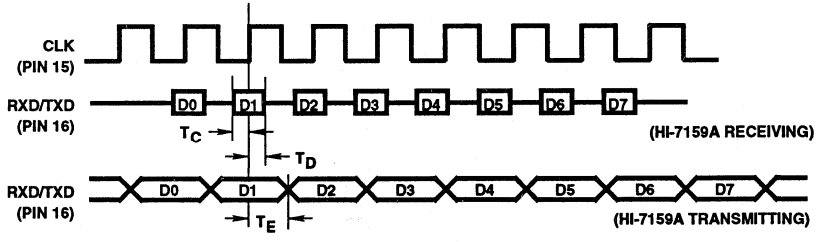


FIGURE 2A. SERIAL MODE 0 TIMING

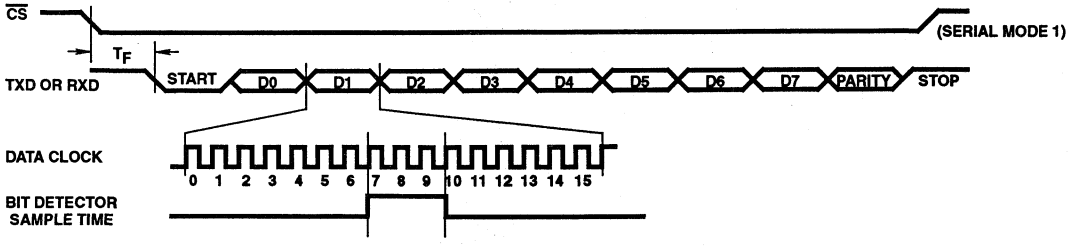


FIGURE 2B. SERIAL MODE TIMING

NOTE: All input timing shown is defined at 50% points.

Pin Description

PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Positive 5V power supply for analog and digital sections.
2	INT OUT	Integrator output; external component terminal.
3	INT IN	Integrator input; external component terminal.
4	BUF OUT	$V_{IN\ HI}$ voltage buffer output; external component terminal.
5	C_{REF}- Guard	Reference capacitor guard ring terminal (negative).
6	C_{REF}-	Reference capacitor negative terminal.
7	C_{REF}+	Reference capacitor positive terminal.
8	C_{REF}+ Guard	Reference capacitor guard ring terminal (positive).
9	$V_{REF\ HI}$	Positive reference input terminal.
10	$V_{REF\ LO}$	Negative reference input terminal.
11	A_{GND}	Analog Ground (0V).
12	$V_{IN\ HI}$	Positive analog input voltage terminal.
13	$V_{IN\ LO}$	Negative analog input voltage terminal.
14	V_{EE}	Negative 5V power supply for analog section.
15	$\overline{RD}$/RXD	Parallel read; serial receive (modes 1 and 2), serial clock (mode 0).
16	$\overline{WR}$/TXD	Parallel write; serial transmit (modes 1 and 2), serial receive/transmit (mode 0).
17	$\overline{CS}$/SAD4	Chip select (parallel and serial modes 0 and 1), serial address bit 4 (mode 2).
18	P0/SMS0	Parallel I/O port (P0); serial mode select pin.
19	P1/SMS1	Parallel I/O port (P1); serial mode select pin.
20	P2/SAD0	Parallel I/O port (P2); serial address bit 0.
21	P3/SAD1	Parallel I/O port (P3); serial address bit 1.
22	P4/SAD2	Parallel I/O port (P4); serial address bit 2.
23	P5/SAD3	Parallel I/O port (P5); serial address bit 3.
24	P6/BRS0	Parallel I/O port (P6); serial baud rate select.

MODE	SMS0	SMS1
Serial Mode 0	0	0
Serial Mode 1	0	1
Serial Mode 2	1	0
Reserved	1	1

Pin Description (Continued)

<table>
<tr><th>PIN</th><th>SYMBOL</th><th>DESCRIPTION</th></tr>
<tr><td>25</td><td>P7/BRS1</td><td>Parallel I/O port (P7); serial baud rate select.
<table>
<tr><th>BAUD RATE</th><th>BRS0</th><th>BRS1</th></tr>
<tr><td>300</td><td>0</td><td>0</td></tr>
<tr><td>1200</td><td>0</td><td>1</td></tr>
<tr><td>9600</td><td>1</td><td>0</td></tr>
<tr><td>19200</td><td>1</td><td>1</td></tr>
</table></td></tr>
<tr><td>26</td><td>D_{GND}</td><td>Digital Ground (0V).</td></tr>
<tr><td>27</td><td>X_{TAL}</td><td>Oscillator out; crystal connection pin (other crystal pin connected to V_{CC}).</td></tr>
<tr><td>28</td><td>SEL</td><td>Select pin for parallel or serial operation.
Parallel SEL = 1
Serial Modes SEL = 0</td></tr>
</table>

Theory of Operation

The HI-7159A attains its $5^1/_2$ digit resolution through the use of multiple integrations per conversion, creating an effective integrator swing greater than the supply rails, and a successive integration technique used to measure the residue on the integrator capacitor to $5^1/_2$ digit accuracy.

In the $5^1/_2$ digit mode, the input voltage is integrated and reference de-integrated four times. This results in a count with the same effective resolution as a single integration with four times the integrator swing amplitude. In this manner effective integrator swings of ±12V or greater can be achieved with ±5V supplies. The four integrations are spaced so that common-mode signals whose frequency is an integer multiple of $f_{CRYSTAL}/40{,}000$ are rejected. In the $4^1/_2$ digit mode, only one input integration is performed, thus the minimum frequency for common-mode rejection becomes $f_{CRYSTAL}/10{,}000$.

These first four integrations measure the input voltage to an resolution of $3^1/_2$ digits, or 1mV/count. To achieve $5^1/_2$ digit accuracy (10µV/count), the error voltage remaining on the integrator capacitor (representing the over-shoot of the integrator due to comparator delay and clock quantization) must be measured and subtracted from the $3^1/_2$ digit result. This is accomplished by multiplying the residue by a factor of 10, then integrating and reference de-integrating the error. This error is subtracted from the $3^1/_2$ digit result, yielding a $4^1/_2$ digit accurate result. The error remaining from this step is then multiplied by 10 and subtracted, and the process is repeated a third time to achieve an internal accuracy of $6^1/_2$ digits. This result is rounded to $5^1/_2$ digits and transferred to the holding register, where it can be accessed by the user through one of the three communications modes.

Conversion Types

The HI-7159A offers the user a choice of three different conversion types. They are: (1) the converter's internal off-set voltage, measured by internally connecting $V_{IN\ HI}$ and $V_{IN\ LO}$ to A_{GND} and doing a conversion (Error Only Mode); (2) the input voltage ($V_{IN\ HI}$ minus $V_{IN\ LO}$) including the converter's internal offset (Uncompensated Mode); and (3) the input voltage including internal offset errors, minus the internal offset errors (Compensated Mode). This last measurement is a digital subtraction of an Error Only conversion from an Uncompensated conversion, and is the default conversion type. Since a Compensated conversion consists of two conversions, it takes twice as long to perform as the first two types.

Under some conditions, it may be desirable to increase the conversion rate without loss of resolution or accuracy. Since the short term drift of the internal offset error is slight when temperature is controlled, it is not always necessary to convert the error voltage once for every input voltage conversion. It is possible for the host processor to do an error conversion periodically, store the result, and subtract the error from a stream of uncompensated input conversions with its own internal ALU. In this way the conversion rate can be effectively doubled.

Communication Modes

The HI-7159A A/D converter receives instructions from and transmits data to the user host processor through one of four communication modes. The modes are: parallel microprocessor (Parallel); synchronous serial (Serial Mode 0); serial non-addressed (Serial Mode 1); and serial addressed (Serial Mode 2). The mode is determined by the states of the SEL, SMS0, and SMS1 pins as shown in Table 1.

The parallel mode allows the converter to be attached directly to a microprocessor data bus. Data is read and written to the device under control of the microprocessor's $\overline{RD}$, $\overline{WR}$ and $\overline{CS}$ signals. Serial Mode 0 permits high speed serial data transfer at up to 1 megabits/sec. Serial Mode 1 reads and writes industry standard serial data packets consisting of 1 start bit, 8 data bits, 1 parity bit (EVEN), and 1 stop bit, at one of 4 hardware selectable baud rates. Serial Mode 2 is identical to Serial Mode 1 with the addition of addressing capabilities which allow up to 32 HI-7159As to share the same serial line, with each assigned a unique address.

TABLE 1. COMMUNICATION MODE SELECTION

COMMUNICATION MODE	SEL PIN 28	SM S0 PIN 18	SM S1 PIN19
Parallel	V_{CC}	N/A	N/A
Serial 0	D_{GND}	D_{GND}	D_{GND}
Serial 1	D_{GND}	D_{GND}	V_{CC}
Serial 2	D_{GND}	V_{CC}	D_{GND}

All four modes follow the same interface protocol: a request or a command is sent from the host to the HI-7159A, and the converter responds with the requested data and, in the case of a command, begins a new conversion.

Parallel Mode Operation

The parallel communication mode (Figure 3) is selected when SEL (pin 28) is high. Pins 18-25 become the eight bi-directional data bits, P0-P7. Pins 15, 16, and 17 respectively become read ($\overline{RD}$), write ($\overline{WR}$), and chip select ($\overline{CS}$). Timing parameters for the parallel mode are shown in Figure 1.

Serial Mode 0

Serial Mode 0 is the high speed synchronous serial interface, directly compatible with the MCS-51 series of microcontrollers. It is enabled by tying SEL (pin 28), SMS0 (pin 18) and SMS1 (pin 19) low (Figure 4A). Pin 16 is the bi-direction serial data path, and pin 15 is the data clock input. Data sent to the HI-7159A is latched on the rising edge of the serial clock. See Figure 2A for detailed timing information.

Only 8 databits are used in this mode-no start, stop, or parity bits are transmitted or received. $\overline{CS}$ must either be tied to D_{GND} or pulled low to access the device. The SAD0 - SAD3 and BRS0 - BRS1 pins are unused in this mode and should be tied high.

Serial Mode 1

Serial Mode 1 is selected by tying SMS0 (pin 18) low, SMS1 (pin 19) high, and SEL (pin 28) low (Figure 4B). In this mode the HI-7159A interface emulates a UART, reading and writing data in serial data packets of 1 start bit, 8 data bits, 1 parity bit (EVEN), and 1 stop bit. The baud rate is determined by the state of BRS0 and BRS1 (pins 24 and 25) as shown in Table 2. Pin 15 becomes the serial receiver pin (RXD) and pin 16 the serial transmitter pin (TXD). $\overline{CS}$ (pin 17) remains a chip select and must either be tied to D_{GND} or pulled low (see Figure 2B) to access the device. SAD0-SAD3 (pins 20-23) are unused in this mode and should be tied high.

TABLE 2. BAUD RATE SELECTION FOR MODES 1 AND 2

BRS0 PIN 24	BRS1 PIN 25	BAUD RATE (f_{XTAL} = 2.4576MHz)	BAUD RATE vs f_{XTAL}
D_{GND}	D_{GND}	300	$f_{XTAL}/8192$
D_{GND}	V_{CC}	1200	$f_{XTAL}/2048$
V_{CC}	D_{GND}	9600	$f_{XTAL}/256$
V_{CC}	V_{CC}	19200	$f_{XTAL}/128$

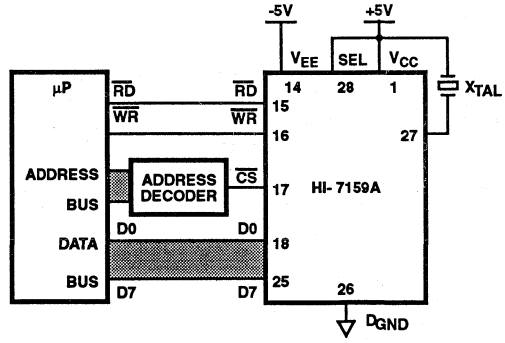


FIGURE 3. PARALLEL MODE CONFIGURATION

Design Hints for Operating in the Parallel Mode

1. Always read the status byte twice to make sure that it is cleared.
2. Make sure the status byte is cleared before issuing a command to change modes.
3. Read each digit pair five times before reading the next byte to ensure that the output data is correct.
4. Use a watchdog timer to monitor conversion time. If conversion time is either too long or too short, re-issue the conversion command.

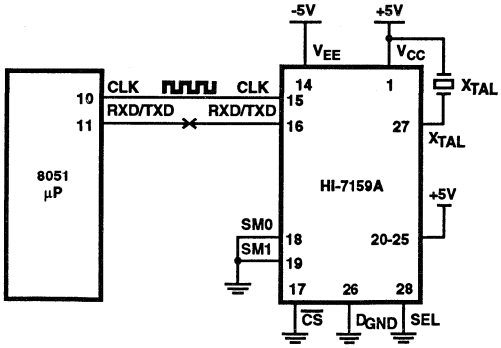


FIGURE 4A. SERIAL MODE 0

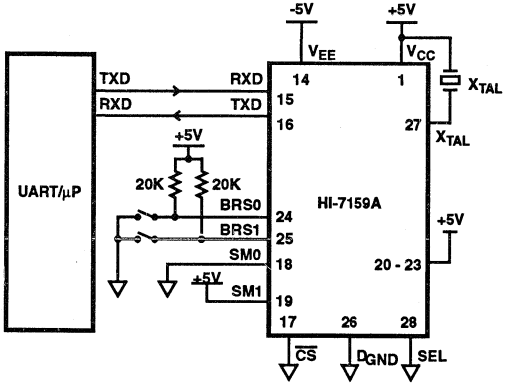


FIGURE 4B. SERIAL MODE 1

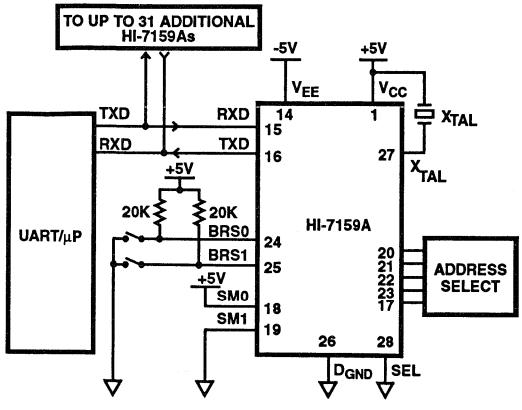


FIGURE 4C. SERIAL MODE 2

FIGURE 4. SERIAL MODE CONFIGURATIONS

Serial Mode 2

Serial Mode 2 is selected by tying SEL (pin 28) low, SMS0 (pin 18) high, and SMS1 (pin 19) low, as shown in Figure 4C. This mode of operation is identical to Serial Mode 1, except that each device now has one of 32 unique addresses determined by the state of pins 20-23 and 17, as shown in Table 3. This allows multiple HI-7159As to be attached to the same pair of serial lines.

When the microprocessor sends out an Address Byte (Table 4) that matches one of the HI-7159As' hardwired addresses, that particular HI-7159A is selected for all further I/O until another Address Byte with a different address is transmitted.

TABLE 3. HARDWARE ADDRESS SELECTION FOR MODE 2

PIN 17	PIN 23	PIN 22	PIN 21	PIN 20
B4 (MSB)	B3	B2	B1	B0 (LSB)

Reading the HI-7159A

Despite the wide variety of interface options available on the HI-7159A, the procedure for communicating with it is essentially the same in all four modes. (Serial Mode 2 differs from the rest in two respects: the chip to be communicated with must first be sent an address byte to select it, and the digit bytes are sent one by one, for a total of six bytes, instead of in pairs.) There are two types of bytes that can be sent to the converter, commands and requests. A command byte (Table 5) sets the parameters of and initiates a conversion. Those parameters are: continuity of the conversion (single or continuous), resolution ($5^1/_2$ or $4^1/_2$ digits), and type of conversion (Compensated, Uncompensated, or Error Only). Bit D0 = 0 indicates that this is a command byte and a new conversion(s) should be started.

A request byte (Table 6) asks for either the status of the converter or the result of a conversion. All bits of a request should be set to 0 except D3, D2, and D0. D3 and D2 determine the type of request (status or digit pair), and D0 = 1 indicates to the HI-7159A that this is a request byte. Serial Mode 2 uses a slightly modified request byte, shown in Table 7, allowing it to individually select each of the six digit bytes.

Upon receipt of a request, the HI-7159A will respond with either a status or a digit byte. The status byte (Table 8) returns the current state of the converter. Bit D6 = 1 indicates that a new conversion has been completed since the last time the status byte was read. Bit D6 is cleared after it is read. Bit D4 shows the current continuity (single or continuous). Bit D3 indicates the resolution ($5^1/_2$ or $4^1/_2$ digits) of the conversion, and bits D2 and D1 indicate the type (Compensated, Uncompensated, or Error Only). Bit D0 = 0 indicates that there was no parity error detected in the last request byte.

The three digit bytes (Table 9) each contain two nibbles representing two digits of the conversion. The sixth nibble contains the MSD (most significant digit), polarity (1 = positive) and overrange (1 = overrange) information. In Serial Mode 2 the digits (Table 10) are requested and received individually, so a total of six requests and six reads is necessary to obtain all $5^1/_2$ digits.

TABLE 4. SERIAL MODE 2 ADDRESS BYTE FORMAT (SENT TO HI-7159A)

ADDRESS BIT	(RESERVED)		(MSB)				(LSB)
D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	B4	B3	B2	B1	B0

TABLE 5. COMMAND BYTE FORMAT (SENT TO HI-7159A)

(RESERVED)			CONTINUITY		RESOLUTION		CONVERSION TYPE			COMMAND BIT
D7	D6	D5		D4		D3		D2	D1	D0
0	0	0	Single	0	$5^1/_2$	1	Comp	1	1	0
			Continuous	1	$4^1/_2$	0	Uncomp	1	0	
							Error Only	0	1	

TABLE 6. REQUEST BYTE FORMAT, PARALLEL AND SERIAL MODE 1 (SENT TO HI-7159A)

(RESERVED)				BYTE REQUEST			(RESERVED)	REQUEST BIT
D7	D6	D5	D4		D3	D2	D1	D0
0	0	0	0	Digit Pair 0, 1	0	0	0	1
				Digit Pair 2, 3	0	1		
				Digit Pair 4, 5	1	0		
				Converter Status	1	1		

TABLE 7. REQUEST BYTE FORMAT, SERIAL MODE 2 (SENT TO HI-7159A)

(RESERVED)				BYTE REQUEST				REQUEST BIT
D7	D6	D5	D4		D3	D2	D1	D0
0	0	0	0	Digit 0	0	0	0	1
				Digit 1	0	0	1	
				Digit 2	0	1	0	
				Digit 3	0	1	1	
				Digit 4	1	0	0	
				Digit 5	1	0	1	
				Converter Status	1	1	0	

TABLE 8. STATUS BYTE FORMAT (RECEIVED FROM HI-7159A)

(*)	CONVERTER UPDATE STATUS		(*)	CONTINUITY		RESOLUTION		CONVERSION TYPE			PARITY ERROR	
D7		D6	D5		D4		D3		D2	D1		D0
0	No Update	0	0	Single	0	$5^1/_2$	1	Comp	1	1	No	0
	Updated	1		Continuous	1	$4^1/_2$	0	Uncomp	1	0	Yes	1
								Error	0	1		

(* = Reserved)

TABLE 9. DIGIT BYTE FORMAT, PARALLEL AND SERIAL MODE 1 (RECEIVED FROM HI-7159A)

DIGIT BYTE	D7	D6	D5	D4	D3	D2	D1	D0
Digit Pair 0, 1	MSB1			LSB1	MSB0			LSB0
Digit Pair 2, 3	MSB3			LSB3	MSB2			LSB2
Digit Pair 4, 5	Polarity (1 = POS)	Overrange (1 = OR)	MSB5	LSB5	MSB4			LSB4

TABLE 10. DIGIT BYTE FORMAT, SERIAL MODE 2 (RECEIVED FROM HI-7159A)

DIGIT BYTE	D7	D6	D5	D4	D3	D2	D1	D0
Digits 0 - 4	0	0	1	1	MSB		LSB	
Digit 5	0	0	1	1	Polarity (1 = POS)	Overrange (1 = OR)	MSB	LSB

Single Conversion Mode

The suggested algorithm for reading the HI-7159A in its single conversion mode of operation is shown in Figure 5. Essentially it consists of initiating a conversion, waiting until the conversion is complete, and then reading the results. Since no further conversions take place, the data may be read out at any time and at any speed. This is the most straightforward method of reading the HI-7159A.

Continuous Conversion Mode

Once a command byte is sent to the HI-7159A initiating the continuous conversion mode, the output data registers will be updated continuously after every conversion. This makes obtaining a valid reading more difficult, since the possibility exists that the current data could be overwritten by a new conversion before all the digit bytes are read. To prevent this, the status byte should be read before and after the data is read from the converter, to ensure that the converter has not updated during the reads. This is demonstrated in Figure 6.

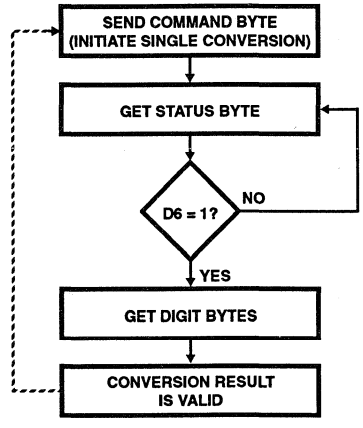


FIGURE 5. READING THE HI-7159A IN THE SINGLE CONVERSION MODE

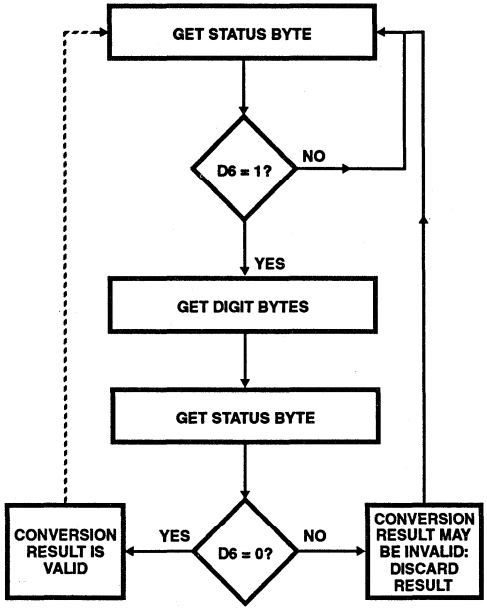


FIGURE 6. READING THE HI-7159A IN THE CONTINUOUS CONVERSION MODE

Due to the wide range of baud rates available in the serial modes, some of the lower baud rates will take longer to transfer the output data than it takes to perform a conversion. In these cases the continuous mode should not be used. Table 11 shows the percentage of the total conversion time that it takes to read all the data from the converter for the two serial modes. These are best case numbers, assuming that the bytes are transmitted and received end-to-end. An asterisk indicates that it is impossible to get all the data out within one conversion. Percentages in the 20-50% range indicate that it is possible to get valid data out with very tight code. In all cases the status byte should be checked before and after the reading to ensure data integrity.

TABLE 11. SERIAL MODES $^1/_2$

BAUD RATE	CONVERSION TYPE			
	$5^1/_2$ COMP	$5^1/_2$ UNCOMP	$4^1/_2$ COMP	$4^1/_2$ UNCOMP
300	*/*	*/*	*/*	*/*
1200	54%/*	*/*	*/*	*/*
9600	7%/13%	14%/25%	27%/50%	54%/*
19200	4%/7%	7%/13%	14%/25%	27%/50%

Crystal Oscillator

The HI-7159A uses a single pin crystal oscillator design (Figure 7). The crystal is connected between pin 27 and VCC; no load capacitors or other components are necessary. The user has a choice of crystal frequencies: 2.4576MHz or 2.4MHz. An off-the-shelf 2.4576MHz crystal works well and provides baud rates of exactly 19.2k, 9600, 1200, and 300. However its total integration period will be 16.28ms, or 0.39ms shorter than a 60Hz cycle. This effectively reduces the normal mode AC rejection.

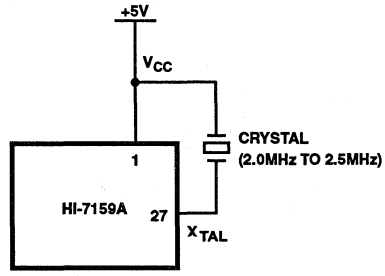


FIGURE 7. SINGLE-PIN OSCILLATOR

A 2.4MHz crystal results in an integration period of 16.67ms, exactly the length of one 60Hz AC cycle. Normal mode AC rejection is greatest at this frequency. At 2.4MHz, however, the Baud rates will be off by -2.34%. This error is not large enough to cause any errors with most peripherals, and only applies to operation in Serial Modes 1 and 2. Communication in Serial Mode 0 and the Parallel Mode is independent of the crystal frequency. For this mode a 2.4MHz crystal is recommended.

While the oscillator was designed to operate at 2.0MHz - 2.5MHz, the HI-7159A itself will operate reliably down to less than 600kHz when driven with an external clock. Benefits at lower clock frequencies include reduced rollover error (gain error for negative input voltages) and lower noise. The baud rates mentioned throughout this datasheet correspond to a crystal frequency of 2.4576MHz. At 1.2MHz, the actual baud rates will be half the speed they were at 2.4MHz, i.e. 9600, 4800, 600 and 150 baud. At 600kHz they will be one-fourth.

It may also be possible to directly program the host's serial hardware for operation at nonstandard baud rates, allowing HI-7159A operation at any arbitrary frequency. For example: 50Hz AC rejection requires a 2.00MHz clock. At this frequency the "9600" baud rate becomes 7812.5 baud. The host's UART must be programmed with the proper divider to operate at this baud rate. The data clock (see Figure 2) is defined as 16 times the baud rate, so the data clock of this configuration would be 125kHz. The data clock can also be determined by dividing the oscillator (clock) frequency by the correct divider from Table 12.

TABLE 12. CRYSTAL DIVIDER RATIOS

BAUD RATE SELECTED	CRYSTAL DIVIDER
"300"	512
"1200"	128
"9600"	16
"19200"	8

The following equation determines the divider needed to operate the HI-7159A at any given crystal frequency:

$$\frac{f_{CLOCK}\,(7159A)}{\text{Divider (7159A)}} = \frac{f_{CRYSTAL}\,(\text{Host UART})}{\text{Divider (Host UART)}} = \text{Data Clock}$$

Once determined, the new divider must be written directly to the Host's UART. Most PC compatibles use an 8250 UART with a 1.8432MHz crystal, so the proper divider for the 2MHz exampie given above would be 15. Again, these considerations apply only to Serial Modes 1 and 2. Parallel and Serial Mode 0 communication rates are independent of crystal frequency.

Conversion Time

The conversion time of the HI-7159A is a function of the crystal frequency and the type of conversion being made. The conversion times for f_{CLOCK} = 2.4MHz are shown in Table 13. At other clock frequencies the times may be calculated from the following formula:

$$t_{CONV} = \frac{C}{f_{CLOCK}}$$

where the constant C is determined from Table 13.

TABLE 13. CONVERSION TIMES

	CONVERSION TYPE			
	$5^1/_2$ COMP	$5^1/_2$ UNCOMP	$4^1/_2$ COMP	$4^1/_2$ UNCOMP
f = 2.4MHz	133ms	66.7ms	33.3ms	16.7ms
C	320,000	160,000	80,000	40,000

Component Selection

Three external passive components must be chosen for the HI-7159A: the integrating capacitor (C_{INT}), the integrating resistor (R_{INT}), and the reference capacitor (C_{REF}). They are chosen based on the crystal frequency, the reference voltage (V_{REF}), and the desired integrating current. Figure 8 illustrates the analog components necessary for the HI-7159A to function.

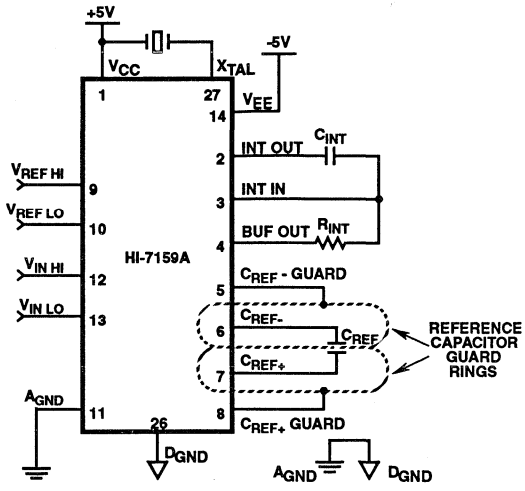


FIGURE 8. ANALOG COMPONENTS AND INPUTS

TABLE 14. RECOMMENDED COMPONENT VALUES vs CLOCK FREQUENCY

f_{CLOCK}	R_{INT}	C_{INT}	C_{REF}
2.4MHz	400kΩ	0.01µF	1.0µF
1.2MHz	360kΩ	0.022µF	2.2µF
600kHz	330kΩ	0.047µF	4.7µF

NOTE: C_{INT} MUST be a high quality polypropylene capacitor or performance may be degraded.

The reference capacitor and integrating components can either be selected from Table 14, or calculated from the following equations.

C_{REF} acts as a voltage source at different times during a conversion. Its value is determined by two considerations: it must be small enough to be fully charged from its discharged state at power-on; yet it also must be large enough to supply current to the circuit during conversion without significantly drooping from its initial value. For 2.4MHz operation, a 1µF capacitor is recommended. The equation for other frequencies is:

$$C_{REF} = \frac{2.5}{f_{CLOCK}}$$

The values of R_{INT} and C_{INT} are selected by choosing the maximum integration current and the maximum integrator output voltage swing. The maximum integration current and voltage swing occurs when V_{IN} = full scale = 2 X V_{REF}. The recommended integration current for the HI-7159A is 5mA - 10mA. This will help determine the value of R_{INT}, since

$$I_{INT} = \frac{V_{IN}}{R_{INT}} \quad \text{so} \quad R_{INT} = \frac{V_{IN}}{I_{INT}}$$

where $V_{IN} = V_{IN\,HI} - V_{IN\,LO} = 2 \times V_{REF}$.

Therefore values of R_{INT} should be between 200kΩ and 400kΩ. The exact value of R_{INT} may be altered to get the exact integrator swing desired after choosing a standard capacitor value for C_{INT}.

The most critical component in any integrating A/D converter is the integrating capacitor, C_{INT}. For a converter of this resolution, it is imperative that this component perform as closely to an ideal capacitor as possible. Any amount of leakage or dielectric absorption will manifest itself as linearity errors. For this reason C_{INT} must be a high quality polypropylene capacitor. Use of any other type may degrade performance. The value of C_{INT} is determined by the magnitude of the desired maximum integrator output voltage swing as shown below:

$$V_{SWING} = \frac{(V_{IN})\ (t_{INT})}{(R_{INT})\ (C_{INT})}$$

Solving for C_{INT} yields:

$$C_{INT} = \frac{(V_{IN})\ (t_{INT})}{(R_{INT})\ (V_{SWING})}$$

where V_{SWING} is the maximum output voltage swing of the integrator, V_{IN} is the full scale input voltage ($V_{IN\ HI}$ - $V_{IN\ LO}$) to the converter (equal to 2 X V_{REF}), and t_{INT} is the time in which V_{IN} is integrated. The best results are achieved when the maximum integrator output voltage is made as large as possible, yet still less than the nonlinear region in the vicinity of the power supply limit. A full scale output swing of about 3.0V provides the greatest accuracy and linearity.

NOTE: The integrator is auto-zeroed to the voltage at $V_{IN\ LO}$. If $V_{IN\ LO}$ is negative with respect to A_{GND}, the integrator will have | $V_{IN\ LO}$ | less headroom for positive input voltages (inputs where $V_{IN\ HI}$ - $V_{IN\ LO}$ > 0). If $V_{IN\ LO}$ is positive with respect to A_{GND}, the integrator will have | $V_{IN\ LO}$ | less headroom for negative input voltages (inputs where $V_{IN\ HI}$ - $V_{IN\ LO}$ < 0). In most applications $V_{IN\ LO}$ is at or near A_{GND} and the above equations will be adequate. In applications where $V_{IN\ LO}$ may be more than 0.1V away from A_{GND}, it should be included in the integrator swing considerations. The following formula combines all the above considerations:

$$\left| V_{IN\ LO} - \frac{(V_{IN\ HI} - V_{IN\ LO})\ (10,000)}{(R_{INT})\ (C_{INT})\ (f_{OSC})} \right| \leq 3.0V$$

Gain Error Adjustments

While the HI-7159A has a very linear transfer characteristic in both the positive and negative directions, the slope of the line is slightly greater for negative inputs than for positive. This results in the transfer characteristic shown in Figure 9. One end point of this curve, typically the positive side, can be adjusted to zero error by trimming the reference voltage. The other (negative) side will have a fixed gain error. This error can be removed in software by multiplying all negative readings by a scale factor, determined by dividing the ideal full scale reading (-200,000 counts) by the actual full scale reading when V_{IN} = -2.00000V.

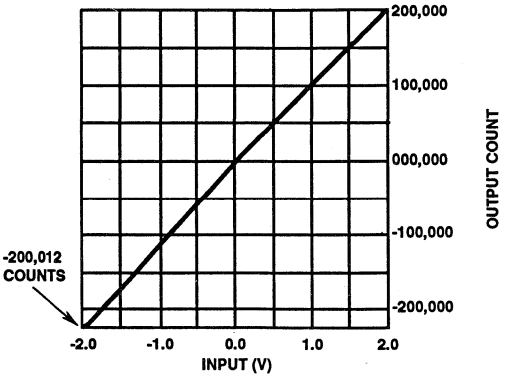


FIGURE 9. TYPICAL HI-7159A TRANSFER CHARACTERISTIC

C_{REF} Guard Pins

Depending on the polarity of the input signal, either the negative or the positive terminal of the reference capacitor will be connected to A_{GND} to provide the correct polarity for reference deintegration. In systems where $V_{REF\ LO}$ is tied to analog ground, the reference capacitor is effectively shifted down by | V_{REF} | for positive input voltages, and is not shifted at all for negative input voltages. This shift can cause some charge on the reference capacitor to be lost due to stray capacitance between the reference capacitor leads and ground traces or other fixed potentials on the board. The reference voltage will now be slightly smaller for positive inputs. This difference in reference voltages for positive and negative inputs appears as rollover error.

The HI-7159A provides two guard ring outputs to minimize this effect. Each guard ring output is a buffered version of the voltage at its respective C_{REF} pin. If the traces going to the C_{REF} pins and under C_{REF} itself are surrounded by their corresponding guard rings, no charge will be lost as C_{REF} is moved. Figure 10 shows two slightly different patterns.The first one is for capacitors of symmetrical construction, the second is for capacitors with outside foils (one end of the capacitor is the entire outside.

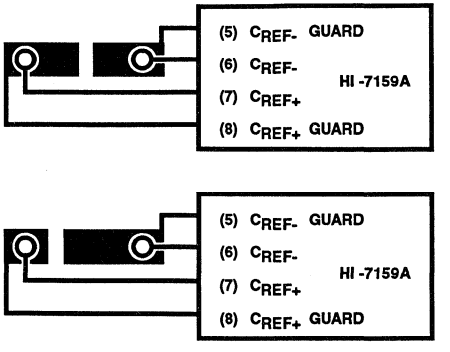


FIGURE 10. TYPICAL GUARD RING LAYOUT

Die Characteristics

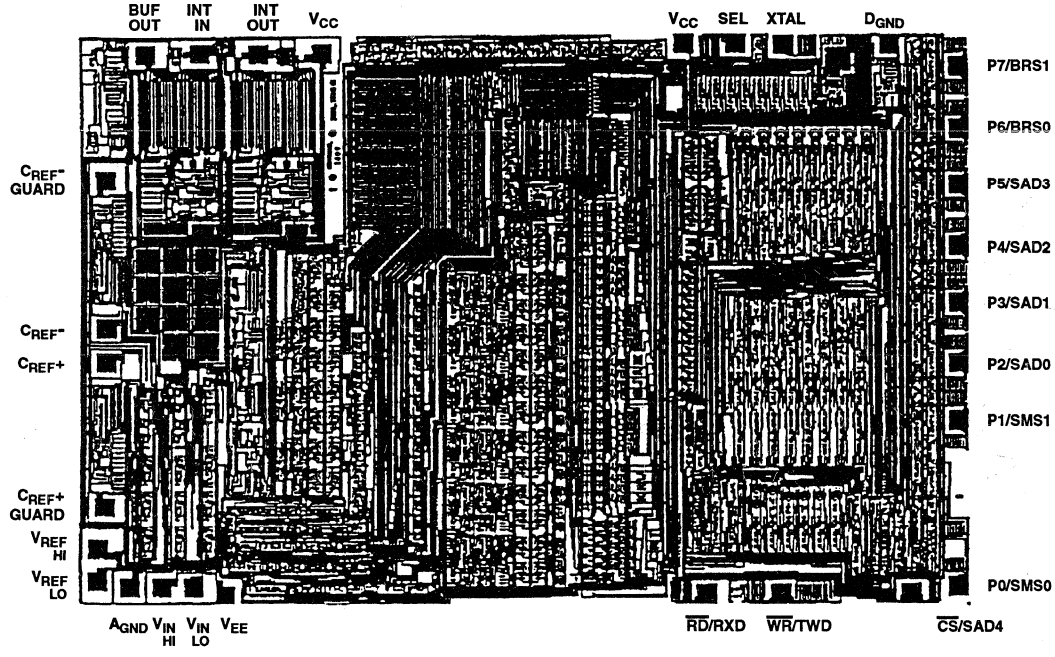
DIE DIMENSIONS:
5817µm x 3988µm

METALLIZATION:
Type: SiAl
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
Thickness: 15kÅ ± 1kÅ

Metallization Mask Layout

HI-7159A



ICL7109

December 1993

12-Bit Microprocessor Compatible A/D Converter

Features

- **12 Bit Binary (Plus Polarity and Overrange) Dual Slope Integrating Analog-to-Digital Converter**
- **Byte-Organized TTL Compatible Tri-State Outputs and UART Handshake Mode for Simple Parallel or Serial Interfacing to Microprocessor Systems**
- **RUN/$\overline{\text{HOLD}}$ Input and STATUS Output Can Be Used to Monitor and Control Conversion Timing**
- **True Differential Input and Differential Reference**
- **Low Noise - Typically 15μV_{P-P}**
- **1pA Typical Input Current**
- **Operates At Up to 30 Conversions/Sec**
- **On-Chip Oscillator Operates with Inexpensive 3.58MHz TV Crystal Giving 7.5 Conversions/Sec for 60Hz Rejection. May Also Be Used with An RC Network Oscillator for Other Clock Frequencies**

Description

The ICL7109 is a high performance, CMOS, low power integrating A/D converter designed to easily interface with microprocessors.

The output data (12 bits, polarity and overrange) may be directly accessed under control of two byte enable inputs and a chip select input for a single parallel bus interface. A UART handshake mode is provided to allow the ICL7109 to work with industry-standard UARTs in providing serial data transmission. The RUN/$\overline{\text{HOLD}}$ input and STATUS output allow monitoring and control of conversion timing.

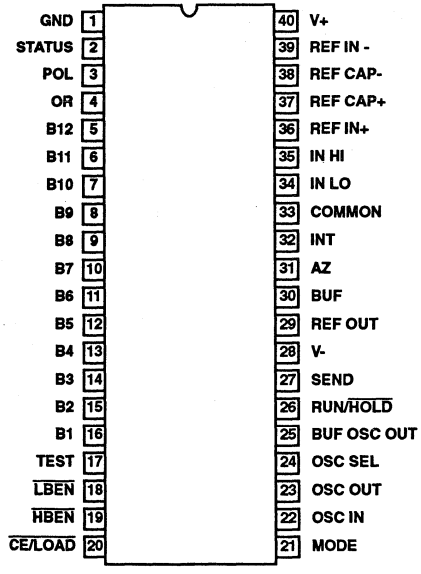
The ICL7109 provides the user with the high accuracy, low noise, low drift versatility and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, drift of less than 1$\mu V/^{o}C$, maximum input bias current of 10pA, and typical power consumption of 20mW make the ICL7109 an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7109MDL	-55°C to +125°C	40 Lead Side Brazed Ceramic DIP
ICL7109IDL	-25°C to +85°C	40 Lead Side Brazed Ceramic DIP
ICL7109IJL	-25°C to +85°C	40 Lead Ceramic DIP
ICL7109CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7109MDL/883B	-55°C to +125°C	40 Lead Side Brazed Ceramic DIP
ICL7109IPL	-25°C to +85°C	40 Lead Plastic DIP

Pinout

ICL7109
(CDIP, PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3092**

Absolute Maximum Ratings

Positive Supply Voltage (GND to V+) ..... +6.2V
Negative Supply Voltage (GND to V-) ..... -9V
Analog Input Voltage (Either Input) (Note 1) ..... V+ to V-
Reference Input Voltage (Either Input) (Note 1) ..... V+ to V-
Digital Input Voltage ..... (V+) +0.3V
Pins 2-27 (Note 2) ..... GND -0.3V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s Max) ..... +300°C
Junction Temperature (PDIP Package) ..... +150°C
(CDIP Package) ..... +175°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CDIP Package	45°C/W	8°C/W
CDIP Package (ICL7109IJL)	45°C/W	15°C/W
PDIP Package	50°C/W	-

Operating Temperature Range
M Suffix ..... -55°C to +125°C
I Suffix ..... -25°C to +85°C
C Suffix ..... 0°C to +75°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Analog Electrical Specifications

$V+ = +5V$, $V- = -5V$, GND = 0V, $T_A = +25°C$, $f_{CLK} = 3.58MHz$, Unless Otherwise Specified

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Oscillator Output Current					
High, O_{OH}	$V_{OUT} = 2.5V$	-	1	-	mA
Low, O_{OL}	$V_{OUT} = 2.5V$	-	1.5	-	mA
Buffered Oscillator Output Current					
High, BO_{OH}	$V_{OUT} = 2.5V$	-	2	-	mA
Low, BO_{OL}	$V_{OUT} = 2.5V$	-	5	-	mA
Zero Input Reading	$V_{IN} = 0.0000V$, $V_{REF} = 204.8mV$	-0000	±0000	+0000	Counts
Ratiometric Error	$V_{IN} = V_{REF}$, $V_{REF} = 204.8mV$ (Note 7)	-3	-	0	Counts
Non-Linearity	Full Scale = 409.6mV to 2.048mV Maximum Deviation from Best Straight Line Fit, Over Full Operating Temperature Range (Notes 4 and 6)	-1	±0.2	+1	Counts
Rollover Error	Full Scale = 409.6mV to 2.048V Difference in Reading for Equal Positive and Negative Inputs Near Full-Scale (Notes 5 and 6), $R_1 = 0\Omega$	-1	±0.2	+1	Counts
Linearity	Full-Scale = 200mV or Full-Scale = 2V Maximum Deviation from Best Straight Line Fit (Note 4)	-	±0.2	±1	Counts
Common Mode Rejection Ratio, CMRR	$V_{CM} = ±1V$, $V_{IN} = 0V$, Full-Scale = 409.6mV	-	50	-	µV/V
Input Common Mode Range, VCMR	Input HI, Input LO, Common (Note 4)	(V-) +2.0	-	(V+) -2.0	V
Noise, eN	$V_{IN} = 0V$, Full-Scale = 409.6mV (P-P Value Not Exceeded 95% of Time)	-	15	-	µV
Leakage Current Input, I_{ILK}	$V_{IN} = 0V$, All Devices at +25°C (Note 4)	-	1	10	pA
ICL7109CPL	$0°C \le T_A \le +70°C$ (Note 4)	-	20	100	pA
ICL7109IDL	$-25°C \le T_A \le +85°C$ (Note 4)	-	100	250	pA
ICL7109MDL	$-55°C \le T_A \le +125°C$	-	2	100	nA
Zero Reading Drift	$V_{IN} = 0V$, R_1 - 0Ω (Note 4)	-	0.2	1	µV/°C
Scale Factor Temperature Coefficient	$V_{IN} = 408.9mV = > 7770_8$ Reading Ext. Ref. 0ppm/°C (Note 4)	-	1	5	ppm/°C

Analog Electrical Specifications V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, f_{CLK} = 3.58MHz, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE VOLTAGE					
Ref Out Voltage, V_{REF}	Referred to V+, 25kΩ Between V+ and REF OUT	-2.4	-2.8	-3.2	V
Ref Out Temperature Coefficient	25kΩ Between V+ and REF OUT (Note 4)	-	80	-	ppm/°C
POWER SUPPLY CHARACTERISTICS					
Supply Current V+ to GND, I+	V_{IN} = 0V, Crystal Osc 3.58MHz Test Circuit	-	700	1500	µA
Supply Current V+ to V-, I_{SUPP}	Pins 2 - 21, 25, 26, 27, 29; Open	-	700	1500	µA

Digital Electrical Specifications V+ = +5V, V- = -5V, GND = 0V, T_A = +25°C, Unless Otherwise Specified.

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{OUT} = 100µA Pins 2 - 16, 18, 19, 20	3.5	4.3	-	V
Output Low Voltage, V_{OL}	I_{OUT} = 1.6mA Pins 2 - 16, 18, 19, 20	-	±0.20	±0.40	V
Output Leakage Current	Pins 3 - 16 High Impedance	-	±0.01	±1	µA
Control I/O Pullup Current	Pins 18, 19, 20 V_{OUT} = V+ -3V MODE Input at GND (Note 4)	-	5	-	µA
Control I/O Loading	$\overline{HBEN}$ Pin 19 $\overline{LBEN}$ Pin 18 (Note 4)	-	–	50	pF
DIGITAL INPUTS					
Input High Voltage, V_{IH}	Pins 18 - 21, 26, 27 Referred to GND	3.0	-	-	V
Input Low Voltage, V_{IL}	Pins 18 - 21, 26, 27 Referred to GND	-	-	1	V
Input Pull-Up Current	Pins 26, 27 V_{OUT} = (V+) -3V	-	5	-	µA
Input Pull-Up Current	Pins 17, 24 V_{OUT} = (V+) -3V	-	25	-	µA
Input Pull-Down Current	Pin 21 V_{OUT} = GND +3V	-	5	-	µA
TIMING CHARACTERISTICS					
MODE Input Pulse Width, t_W	(Note 4)	50	-	-	ns

NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to ±100µA.
2. Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources other than the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.
3. This limit refers to that of the package and will not be obtained during normal operation.
4. This parameter is not production tested, but is guaranteed by design.
5. Roll-over error for T_A = -55°C to +125°C is ±10 counts maximum.
6. A full scale voltage of 2.048V is used because a full scale voltage of 4.096V exceeds the devices Common Mode Voltage Range.
7. For Cerdip package the Ratiometric error can be -4 (Minimum).

Pin Description

PIN	SYMBOL	DESCRIPTION		
1	GND	Digital Ground, 0V. Ground return for all digital logic.		
2	STATUS	Output High during integrate and deintegrate until data is latched. Output Low when analog section is in Auto-Zero configuration.		
3	POL	Polarity - HI for positive input.		Tri-State output data bits
4	OR	Overrange - HI if overranged.		Tri-State output data bits
5	B12	Bit 12	(Most Significant Bit)	Tri-State output data bits
6	B11	Bit 11	High = True	Tri-State output data bits
7	B10	Bit 10	High = True	Tri-State output data bits
8	B9	Bit 9	High = True	Tri-State output data bits
9	B8	Bit 8	High = True	Tri-State output data bits
10	B7	Bit 7	High = True	Tri-State output data bits
11	B6	Bit 6	High = True	Tri-State output data bits
12	B5	Bit 5	High = True	Tri-State output data bits
13	B4	Bit 4	High = True	Tri-State output data bits
14	B3	Bit 3	High = True	Tri-State output data bits
15	B2	Bit 2	High = True	Tri-State output data bits
16	B1	Bit 1	(Least Significant Bit)	Tri-State output data bits
17	TEST	Input High - Normal Operation. Input Low - Forces all bit outputs high. Note: This input is used for test purposes only. Tie high if not used.		
18	$\overline{\text{LBEN}}$	Low Byte Enable - With Mode (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates low order byte outputs B1 through B8. With Mode (Pin 21) high, this pin serves as a low byte flag output used in handshake mode. See Figures 7, 8, 9.		
19	$\overline{\text{HBEN}}$	High Byte Enable - With Mode (Pin 21) low, and $\overline{\text{CE/LOAD}}$ (Pin 20) low, taking this pin low activates high order byte outputs B9 through B12, POL, OR. With Mode (Pin 21) high, this pin serves as a high byte flag output used in handshake mode. See Figures 7, 8, 9.		
20	$\overline{\text{CE/LOAD}}$	Chip Enable Load - With Mode (Pin 21) low. $\overline{\text{CE/LOAD}}$ serves as a master output enable. When high, B1 through B12, POL, OR outputs are disabled. With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode. See Figures 7, 8, 9.		
21	MODE	Input Low - Direct output mode where $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19) and $\overline{\text{LBEN}}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High - Causes immediate entry into handshake mode and output of data as in Figure 9. Input High - Enables $\overline{\text{CE/LOAD}}$ (Pin 20), $\overline{\text{HBEN}}$ (Pin 19), and $\overline{\text{LBEN}}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversion completion.		
22	OSC IN	Oscillator Input		
23	OSC OUT	Oscillator Output		

Pin Description (Continued)

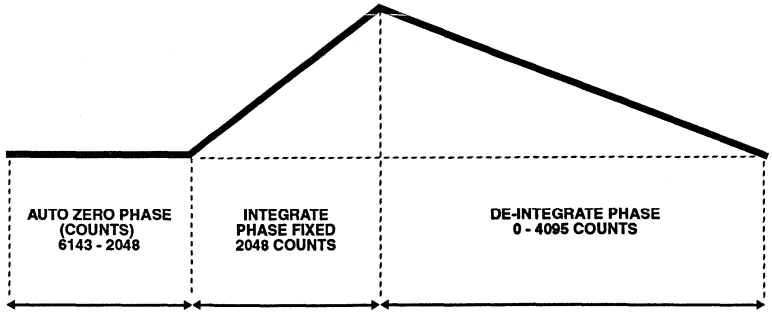
PIN	SYMBOL	DESCRIPTION
24	OSC SEL	Oscillator Select - Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator - clock will be same phase and duty cycle as BUF OSC OUT. Input low configures OSC IN, OSC OUT for crystal oscillator - clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN/$\overline{\text{HOLD}}$	Input High - Conversions continuously performed every 8192 clock pulses. Input Low - Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input - Used in hndshake mode to indicate ability of an external device to accept data. Connect to +5V if not used.
28	V-	Analog Negative Supply - Nominally -5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output - Nominally 2.8V down from V+ (Pin 40).
30	BUFFER	Buffer Amplifier Output.
31	AUTO-ZERO	Auto-Zero Node - Inside foil of C_{AZ}.
32	INTEGRATOR	Integrator Output - Outside foil of C_{INT}.
33	COMMON	Analog Common - System is Auto-Zeroed to COMMON.
34	INPUT LO	Differential Input Low Side.
35	INPUT HI	Differential Input High Side.
36	REF IN +	Differential Reference Input Positive.
37	REF CAP +	Reference Capacitor Positive.
38	REF CAP-	Reference Capacitor Negative.
39	REF IN-	Differential Reference Input Negative.
40	V+	Positive Supply Voltage - Nominally +5V with respect to GND (Pin1).

NOTE: All digital levels are positive true.

Design Information Summary Sheet

- **OSCILLATOR FREQUENCY**
  $f_{OSC} = 0.45/RC$
  $C_{OSC} > 50pF$; $R_{OSC} > 50K\Omega$
  f_{OSC} Typ. = 60kHz
  or
  f_{OSC} Typ. = 3.58MHz Crystal
- **OSCILLATOR PERIOD**
  $t_{OSC} = RC/0.45$
  $t_{OSC} = 1/3.58MHz$ (Crystal)
- **INTEGRATION CLOCK FREQUENCY**
  $f_{CLOCK} = f_{OSC}$ (RC Mode)
  $f_{CLOCK} = f_{OSC}/58$ (Crystal)
  $t_{CLOCK} = 1/f_{CLOCK}$
- **INTEGRATION PERIOD**
  $t_{INT} = 2048 \times t_{CLOCK}$
- **60/50Hz REJECTION CRITERION**
  t_{INT}/t_{60Hz} or t_{INT}/t_{50Hz} = Integer
- **OPTIMUM INTEGRATION CURRENT**
  $I_{INT} = 20.0\mu A$
- **FULL-SCALE ANALOG INPUT VOLTAGE**
  V_{INFS} Typically = 200mV or 2.0V
- **INTEGRATE RESISTOR**
  $$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$
- **INTEGRATE CAPACITOR**
  $$C_{INT} = \frac{(t_{INT})\ (I_{INT})}{V_{INT}}$$
- **INTEGRATOR OUTPUT VOLTAGE SWING**
  $$V_{INT} = \frac{(t_{INT})\ (I_{INT})}{C_{INT}}$$
- **V_{INT} MAXIMUM SWING**
  $(V- + 0.5V) < V_{INT} < (V+ - 0.5V)$
  V_{INT} Typically = 2.0V
- **DISPLAY COUNT**
  $$COUNT = 2048 \times \frac{V_{IN}}{V_{REF}}$$
- **CONVERSION CYCLE**
  $t_{CYC} = t_{CLOCK} \times 8192$
  (In Free Run Mode, Run/$\overline{HOLD}$ = 1)
  when f_{CLOCK} = 60kHz, t_{CYC} = 133ms
- **COMMON MODE INPUT VOLTAGE**
  $(V- + 2.0V) < V_{IN} < (V+ - 2.0V)$
- **AUTO-ZERO CAPACITOR**
  $0.01\mu F < C_{AZ} < 1.0\mu F$
- **REFERENCE CAPACITOR**
  $0.1\mu F < C_{REF} < 1.0\mu F$
- **V_{REF}**
  Biased between V+ and V-
  $V_{REF} \cong V+ - 2.8V$
  Regulation lost when V+ to V- ≤ 6.4V.
  If V_{REF} is not used, float output pin.
- **POWER SUPPLY: DUAL ±5.0V**
  V+ = +5.0 to GND
  V- = -5.0 to GND
- **OUTPUT TYPE**
  Binary Amplitude with Polarity and Overrange Bits
  Tips: Always tie TEST pin HIGH.
  Don't leave any inputs floating.

Typical Integrator Amplifier Output Waveform (INT Pin)



TOTAL CONVERSION TIME = 8192 x t_{CLOCK} (IN FREE-RUN MODE)

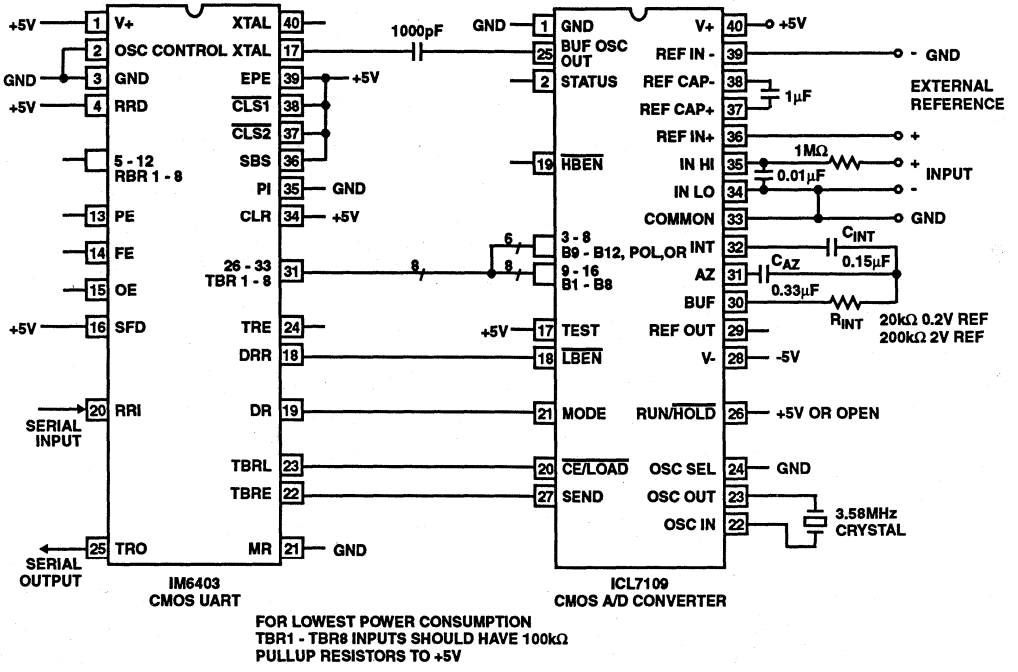


FIGURE 1A. TYPICAL CONNECTION DIAGRAM UART INTERFACE-TO TRANSMIT LATEST RESULT, SEND ANY WORD TO UART

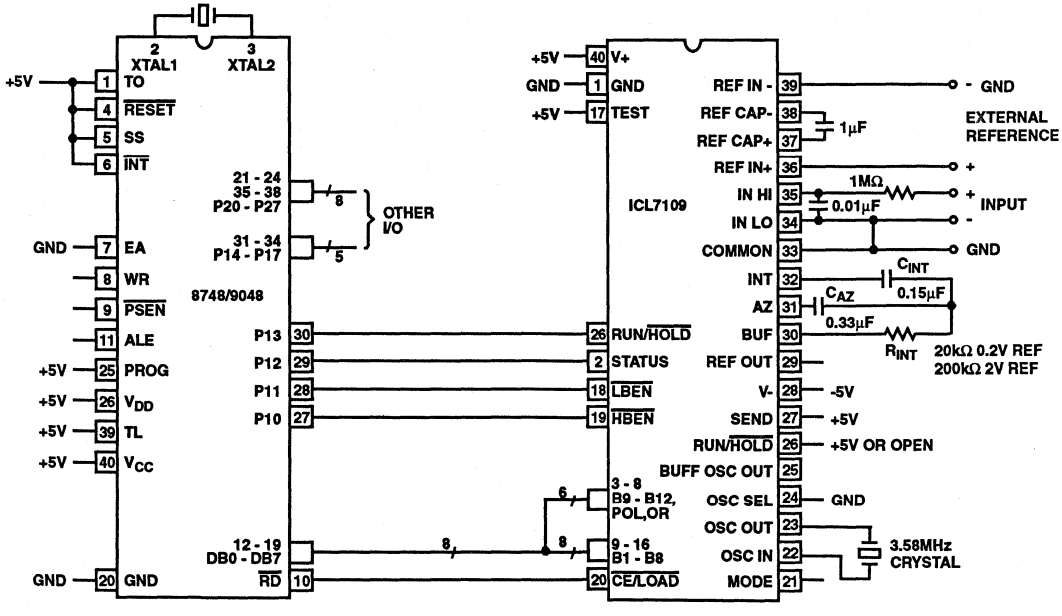


FIGURE 1B. TYPICAL CONNECTION DIAGRAM PARALLEL INTERFACE WITH 8048 MICROCOMPUTER

FIGURE 1.

Detailed Description

Analog Section

Figure 2 shows the equivalent circuit of the Analog Section for the ICL7109. When the RUN/$\overline{\text{HOLD}}$ input is left open or connected to V+, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases as shown in Figure 3. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) de-integrate (DE).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range of the inputs. At the end of this phase, the polarity of the integrated signal is determined.

De-Integrate Phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged (during auto-zero) reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero crossing (established in Auto-Zero) with a fixed slope. The time required for the output to return to zero is proportional to the input signal.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier, or specifically from 1.0V below the positive supply to 1.5V above the negative supply. In this range, the system has a CMRR of 86dB typical. However, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator output swing can be reduced to less than the recommended 4V full-scale swing with little loss of accuracy. The integrator output can swing to within 0.3V of either supply without loss of linearity.

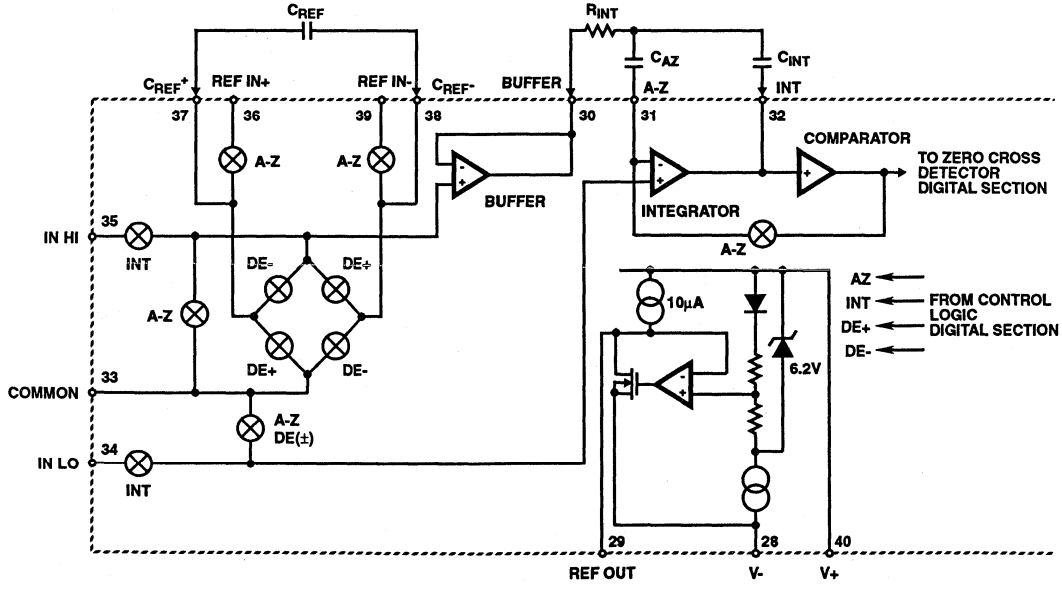


FIGURE 2. ANALOG SECTION OF ICL7109

The ICL7109 has, however, been optimized for operation with analog common near digital ground. With power supplies of +5V and -5V, this allows a 4V full scale integrator swing positive or negative thus maximizing the performance of the analog section.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for positive or negative input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count worst case. (See Component Value Selection.)

The roll-over error from these sources is minimized by having the reference common mode voltage near or at analog COMMON.

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

The most important consideration is that the integrator output swing (for full-scale input) be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the normal integrator output swing at full scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly affecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common mode range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and roll-over will be slightly worse than in the ±4V case. For larger common mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and roll-over errors. To improve the performance, supplies of ±6V may be used.

Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100µA of quiescent current. They supply 20µA of drive current with negligible nonlinearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 409.6mV full-scale, 200kΩ is near optimum and similarly a 20kΩ for a 409.6mV scale. For other values of full scale voltage, R_{INT} should be chosen by the relation

$$R_{INT} = \frac{\text{full scale voltage}}{20\mu A} .$$

Integrating Capacitor

The integrating capacitor C_{INT} should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approximately. 0.3V from either supply). For the ICL7109 with ±5V supplies and analog common connected to GND, a ±3.5V to ±4V integrator output swing is nominal. For $7^1/_2$ conversions per second (61.72kHz clock frequency) as provided by the crystal oscillator, nominal values for C_{INT} and C_{AZ} are 0.15µF and 0.33µF, respectively. If different clock frequencies are used, these values should be changed to maintain the integrator output swing. In general, the value C_{INT} is given by

$$C_{INT} = \frac{(2048 \times \text{clock period})\ (20\mu A)}{\text{integrator output voltage swing}} .$$

An additional requirement of the integrating capacitor is that it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at The integrating capacitor should have a low dielectric absorption to prevent roll-over errors. While other types may be adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost up to +85°C. Teflon® capacitors are recommended for the military temperature range. While their dielectric absorption characteristics vary somewhat from unit to unit, selected devices should give less than 0.5 count of error due to dielectric absorption.

Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system: a smaller physical size and a larger capacitance value lower the overall system noise. However, C_{AZ} cannot be increased without limits since it, in parallel with the integrating capacitor forms an R-C time constant that determines the speed of recovery from overloads and the error that exists at the end of an auto-zero cycle. For 409.6mV full scale where noise is very important and the integrating resistor small, a value of C_{AZ} twice C_{INT} is optimum. Similarly for 4.096V full scale where recovery is more important than noise, a value of C_{AZ} equal to half of C_{INT} is recommended.

For optimal rejection of stray pickup, the outer foil of C_{AZ} should be connected to the R-C summing junction and the inner foil to pin 31. Similarly the outer foil of C_{INT} should be connected to pin 32 and the inner foil to the R-C summing junction. Teflon, or equivalent, capacitors are recommended above +85°C for their low leakage characteristics.

Reference Capacitor

A 1µF capacitor gives good results in most applications. However, where a large reference common mode voltage exists (i.e., the reference low is not at analog common) and a 409.6mV scale is used, a large value is required to prevent roll-over error. Generally 10µF will hold the roll-over error to 0.5 count in this instance. Again, Teflon, or equivalent capacitors should be used for temperatures above +85°C for their low leakage characteristics.

Reference Voltage

The analog input required to generate a full scale output of 4096 counts is $V_{IN} = 2V_{REF}$. For normalized scale, a reference of 2.048V should be used for a 4.096V full scale, and 204.8mV should be used for a 0.4096V full scale. However, in many applications where the A/D is sensing the output of a transducer, there will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of driving the input down to 409.6mV, the input voltage should be measured directly and a reference voltage of 0.341V should be used. Suitable values for integrating resistor and capacitor are 33kΩ and 0.15μF. This avoids a divider on the input. Another advantage of this system occurs when a zero reading is desired for non-zero input. Temperature and weight measurements with an offset or tare are examples. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. However, in processor-based systems using the ICL7109, it may be more efficient to perform this type of scaling or tare subtraction digitally using software.

Reference Sources

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7109 at 12 bits is one part in 4096, or 244ppm. Thus if the reference has a temperature coefficient of 80ppm/°C (onboard reference) a temperature difference of 3°C will introduce a one-bit absolute error.

For this reason, it is recommended that an external high-quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

The ICL7109 provides a REFerence OUTput (pin 29) which may be used with a resistive divider to generate a suitable reference voltage. This output will sink up to about 20mA without significant variation in output voltage, and is provided with a pullup bias device which sources about 10μA. The output voltage is nominally 2.8V below V+, and has a temperature coefficient of ±80ppm/°C typ. When using the onboard reference, REF OUT (pin 29) should be connected to REF- (pin 39), and REF+ should be connected to the wiper of a precision potentiometer between REF OUT and V+. The circuit for a 204.8mV reference is shown in the test circuit. For a 2.048mV reference, the fixed resistor should be removed, and a 25kΩ precision potentiometer between REF OUT and V+ should be used.

Note that if pins 29 and 39 are tied together and pins 39 and 40 accidentally shorted (e.g., during testing), the reference supply will sink enough current to destroy the device. This can be avoided by placing a 1kΩ resistor in series with pin 39.

Detailed Description

Digital Section

The digital section includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible tri-state output drivers, polarity, overrange and control logic, and UART handshake logic, as shown in Figure 4.

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined in the Electrical Specifications Table. For minimum power consumption, all inputs should swing from GND (low) to V+ (high). Inputs driven from TTL gates should have 3-5kΩ pullup resistors added for maximum noise immunity.

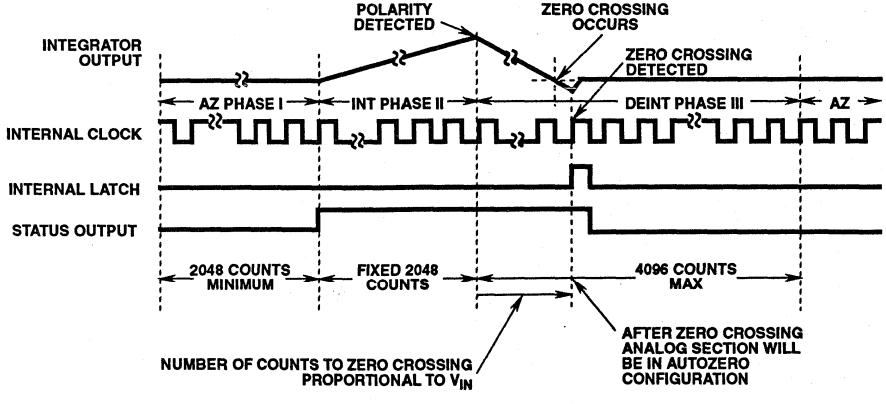


FIGURE 3. CONVERSION TIMING (RUN/$\overline{\text{HOLD}}$ PIN HIGH)

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is low or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3 for of this timing. This signal may be used as a "data valid" flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the converter.

RUN/$\overline{\text{HOLD}}$ Input

When the RUN/$\overline{\text{HOLD}}$ input is high, or left open, the circuit will continuously perform conversion cycles, updating the output latches after zero crossing during the Deintegrate (Phase III)

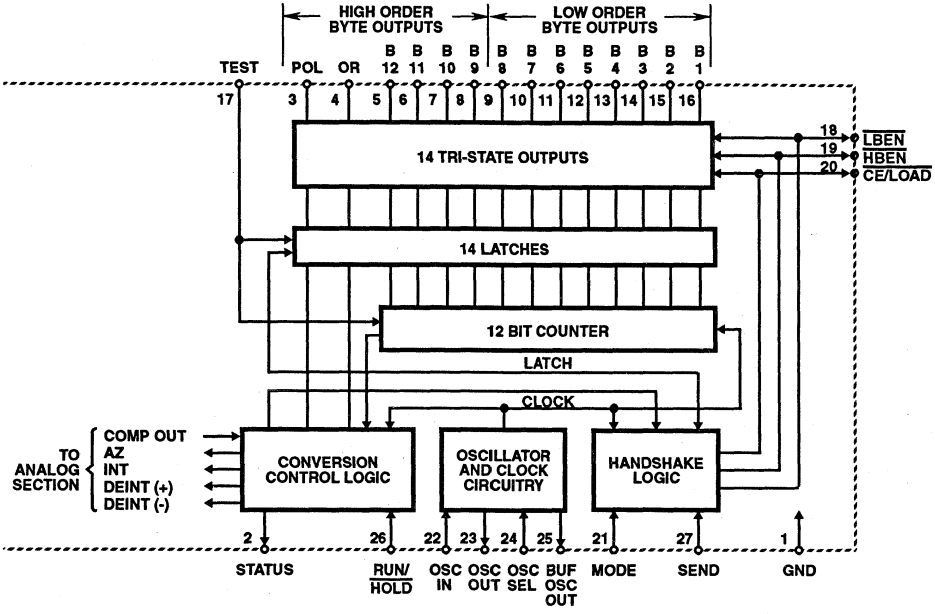


FIGURE 4. DIGITAL SECTION

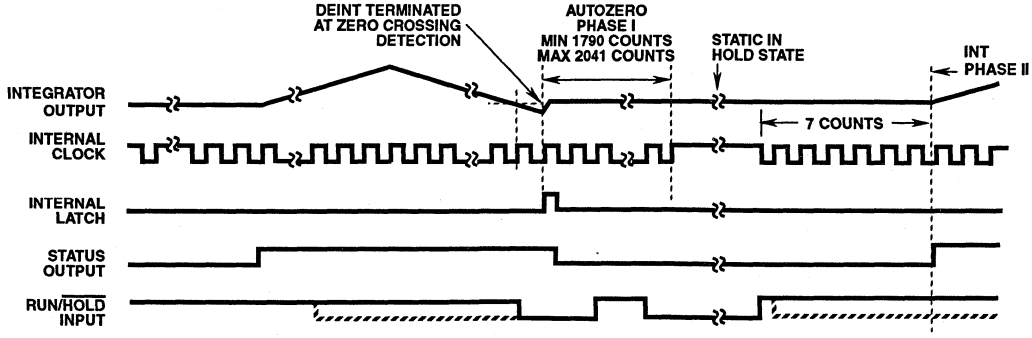


FIGURE 5. RUN/$\overline{\text{HOLD}}$ OPERATION

portion of the conversion cycle (See Figure 3). In this mode of operation, the conversion cycle will be performed in 8192 clock periods, regardless of the resulting value.

If RUN/$\overline{\text{HOLD}}$ goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If RUN/$\overline{\text{HOLD}}$ stays or goes low, the converter will ensure minimum Auto-Zero time, and then wait in Auto-Zero until the RUN/$\overline{\text{HOLD}}$ input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STATUS output will go high) seven clock periods after the high level is detected at RUN/$\overline{\text{HOLD}}$. See Figure 5 for details.

Using the RUN/$\overline{\text{HOLD}}$ input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in auto-zero with RUN/$\overline{\text{HOLD}}$ low. When RUN/$\overline{\text{HOLD}}$ goes high the conversion is started, and when the STATUS output goes low the new data is valid (or transferred to the UART; see Handshake Mode). RUN/$\overline{\text{HOLD}}$ may now be taken low which terminates deintegrate and ensures a minimum Auto-Zero time before the next conversion.

Alternately, RUN/$\overline{\text{HOLD}}$ can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the RUN/$\overline{\text{HOLD}}$ input can be provided by connecting it to the Buffered Oscillator Output. In this mode the conversion time is dependent on the input value measured. Also refer to Harris Application Note AN032 for a discussion of the effects this will have on Auto-Zero performance.

If the RUN/$\overline{\text{HOLD}}$ input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for RUN/$\overline{\text{HOLD}}$ to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and over-range high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip enable input is low, taking a byte enable input low will allow the outputs of that byte to become active (tri-stated on). This allows a variety of parallel data accessing techniques to be used, as shown in the section entitled "Interfacing." The timing requirements for these outputs are shown in Figure 6 and Table 1.

It should be noted that these control inputs are asynchronous with respect to the converter clock - the data may be accessed at any time. Thus it is possible to access the latches while they are being updated, which could lead to erroneous data. Synchronizing the access of the latches with the conversion cycle by monitoring the STATUS output will prevent this. Data is never updated while STATUS is low.

TABLE 1. DIRECT MODE TIMING REQUIREMENTS
(See Note 4 of Electrical Specifications)

DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNITS
Byte Enable Width	t_{BEA}	350	220	-	ns
Data Access Time from Byte Enable	t_{DAB}	-	210	350	ns
Data Hold Time from Byte Enable	t_{DHB}	-	150	300	ns
Chip Enable Width	t_{CEA}	400	260	-	ns
Data Access Time from Chip Enable	t_{DAC}	-	260	400	ns
Data Hold Time from Chip Enable	t_{DHC}	-	240	400	ns

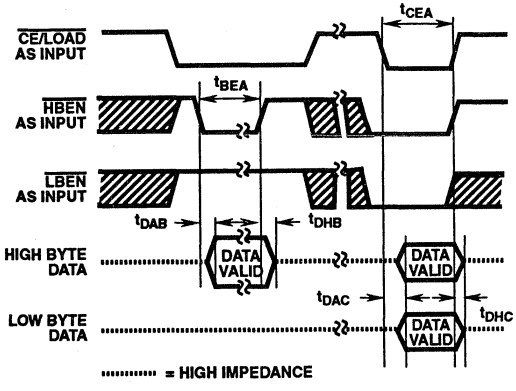


FIGURE 6. DIRECT MODE OUTPUT TIMING

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7109 to digital systems where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode is specifically designed to allow a direct interface between the ICL7109 and industry-standard UARTs (such as the Harris IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7109 provides all the control and flag signals necessary to sequentially transfer two bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission.

Entry into the handshake mode is controlled by the MODE pin. When the MODE terminal is held high, the ICL7109 will enter the handshake mode after new data has been stored in the output latches at the end of a conversion (See Figures 7 and 8). The MODE terminal may also be used to trigger entry into the handshake mode on demand. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. While the converter is in the handshake mode, the MODE input is ignored, and although conversions will still be performed, data updating will be inhibited (See Figure 9) until the converter completes the output cycle and clears the handshake mode.

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte enable terminals become TTL-compatible outputs which provide the control signals for the output cycle (See Figures 7, 8, and 9).

In handshake mode, the SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data.

Figure 7 shows the sequence of the output cycle with SEND held high. The handshake mode (Internal MODE high) is entered after the data latch pulse, and since MODE remains high the $\overline{CE/LOAD}$, $\overline{LBEN}$ and $\overline{HBEN}$ terminals are active as outputs. The high level at the SEND input is sensed on the same high to low internal clock edge that terminates the data latch pulse. On the next low to high internal clock edge the $\overline{CE/LOAD}$ and the $\overline{HBEN}$ outputs assume a low level, and the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled. The $\overline{CE/LOAD}$ output remains low for one full internal clock period only, the data outputs remain active for $1^1/_2$ internal clock periods, and the high byte enable remains low for two clock periods. Thus the $\overline{CE/LOAD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using $\overline{CE/LOAD}$ and $\overline{LBEN}$ while the low order byte outputs (bits 1 through 8) are activated. The handshake mode is terminated when both bytes are sent.

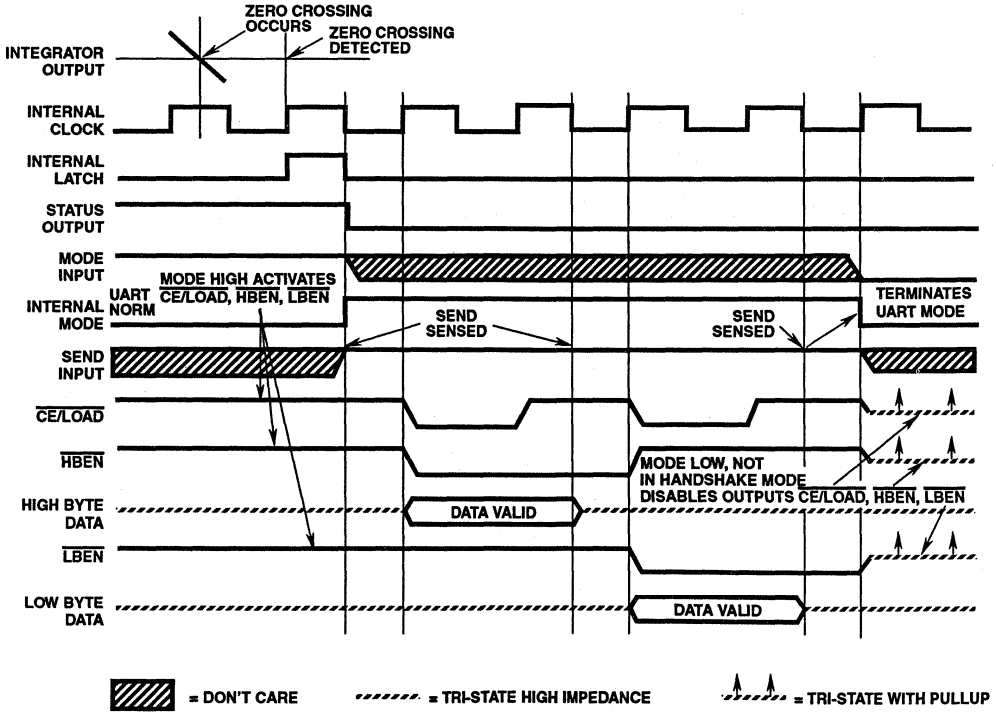


FIGURE 7. HANDSHAKE WITH SEND HELD HIGH

Figure 8 shows an output sequence where the SEND input is used to delay portions of the sequence, or handshake to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEND input to the ICL7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{\text{CE/LOAD}}$ terminal of the ICL7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. The $\overline{\text{CE/LOAD}}$ and $\overline{\text{HBEN}}$ terminals will go low after SEND is sensed, and the high order byte outputs become active. When $\overline{\text{CE/LOAD}}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{\text{HBEN}}$ output low, and the high order byte outputs active. When the UART has transferred that data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7109 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{\text{HBEN}}$ output returns high. At the same time, the $\overline{\text{CE/LOAD}}$ and $\overline{\text{LBEN}}$ outputs go low, and the low order byte outputs become active. Similarly, when the $\overline{\text{CE/LOAD}}$ returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7109 internal clock high to low edge, disabling the data outputs. One-half internal clock later, the handshake mode will be cleared, and the $\overline{\text{CE/LOAD}}$, $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ terminals return high and stay inactive (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 9 shows a handshake output sequence triggered by such an edge. In addition, the SEND input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence for the first (high order) byte is similar to the sequence for the second byte. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STATUS output and RUN/$\overline{\text{HOLD}}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

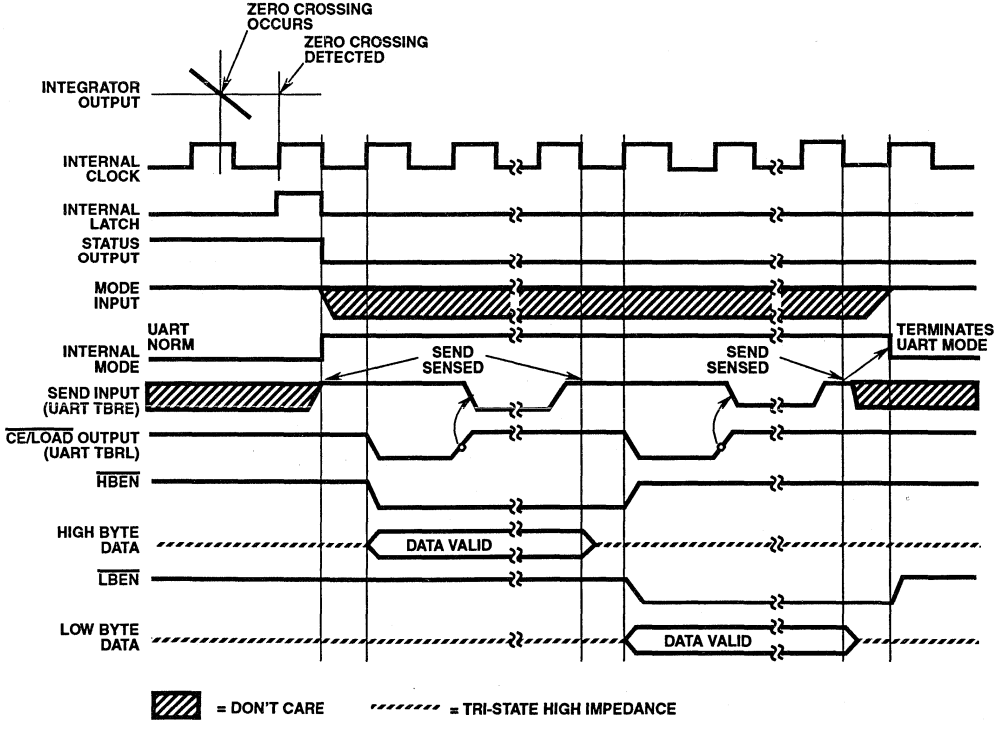


FIGURE 8. HANDSHAKE - TYPICAL UART INTERFACE TIMING

Oscillator

The ICL7109 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated with an RC network or crystal. The OSCILLATOR SELECT input changes the internal configuration of the oscillator to optimize it for RC or crystal operation.

When the OSCILLATOR SELECT input is high or left open (the input is provided with a pullup resistor), the oscillator is configured for RC operation, and the internal clock will be of the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. The resistor and capacitor should be connected as in Figure 10. The circuit will oscillate at a frequency given by f=0.45/RC. A 100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 2048 clock periods is close to an integral multiple of the 60Hz period (but should not be less than 50pF).

When the OSCILLATOR SELECT input is low a feedback device and output and input capacitors are added to the oscillator. In this configuration, as shown in Figure 11, the oscillator will operate with most crystals in the 1MHz to 5MHz range with no external components. Taking the OSCILLATOR SELECT input low also inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. Using an inexpensive 3.58MHz TV crystal, this division ratio provides an integration time given by:

T_{INT} = (2048 clock periods) x (T_{CLOCK}) = 33.18ms where

$$T_{CLOCK} = \frac{58}{3.58MHZ}$$

This time is very close to two 60Hz periods or 33ms. The error is less than one percent, which will give better than 40dB 60Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, which corresponds to a clock frequency of 245.8kHz.

If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the OSCILLATOR INPUT, and the OSCILLATOR OUTPUT should be left open. The internal clock will be of the same frequency, duty cycle, and phase as the input signal when OSCILLATOR SELECT is left open. When OSCILLATOR SELECT is at GND, the clock will be a factor of 58 below the input frequency.

When using the ICL7109 with the IM6403 UART, it is possible to use one 3.58MHz crystal for both devices. The BUFFERED OSCILLATOR OUTPUT of the ICL7109 may be used to drive the OSCILLATOR INPUT of the UART, saving the need for a second crystal. However, the BUFFERED OSCILLATOR OUTPUT does not have a great deal of drive capability, and when driving more than one slave device external buffering should be used.

Test Input

When the TEST input is taken to a level halfway between V+ and GND, the counter output latches are enabled, allowing the counter contents to be examined anytime.

When the RUN/$\overline{HOLD}$ is low and the TEST input is connected to GND, the counter outputs are all forced into the high state, and the internal clock is disabled. When the RUN/$\overline{HOLD}$ returns high and the TEST input returns to the $^1/_2$ (V+ - GND) voltage (or to V+) and one clock is applied, all the counter outputs will be clocked to the low state. This allows easy testing of the counter and its outputs.

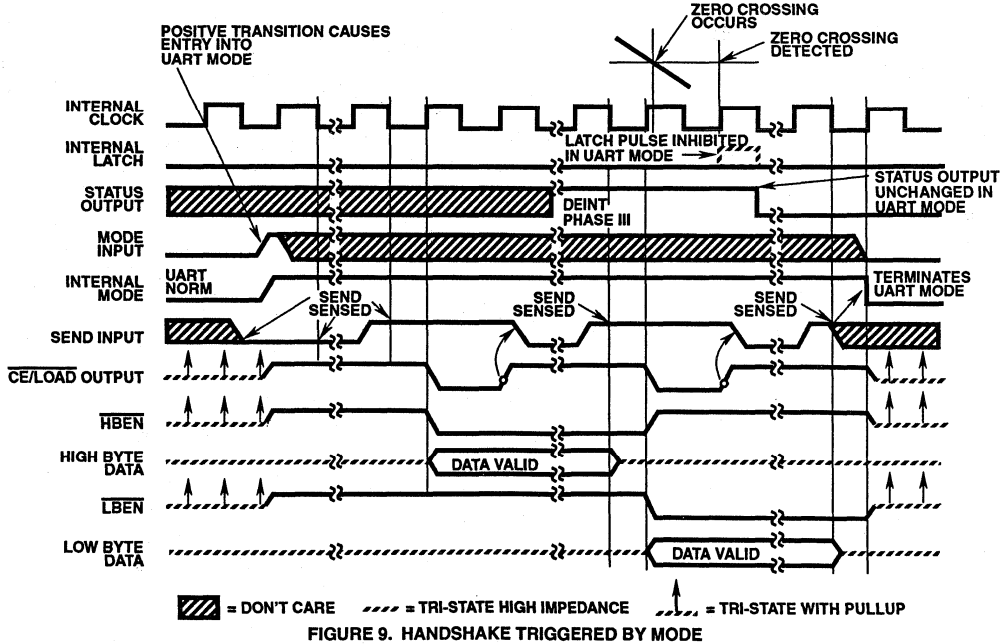


FIGURE 9. HANDSHAKE TRIGGERED BY MODE

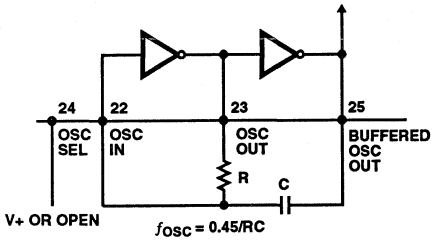


FIGURE 10. RC OSCILLATOR

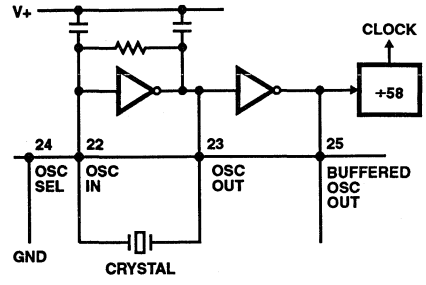


FIGURE 11. CRYSTAL OSCILLATOR

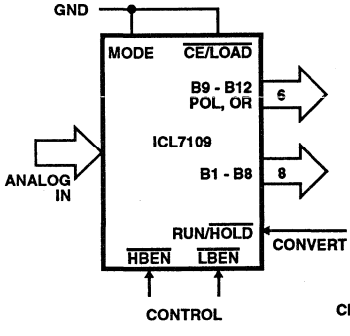


FIGURE 12A.

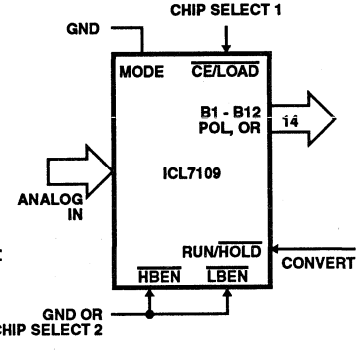


FIGURE 12B.

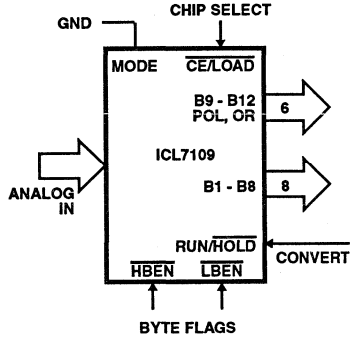


FIGURE 12C.

FIGURE 12. DIRECT MODE CHIP AND BYTE ENABLE COMBINATIONS

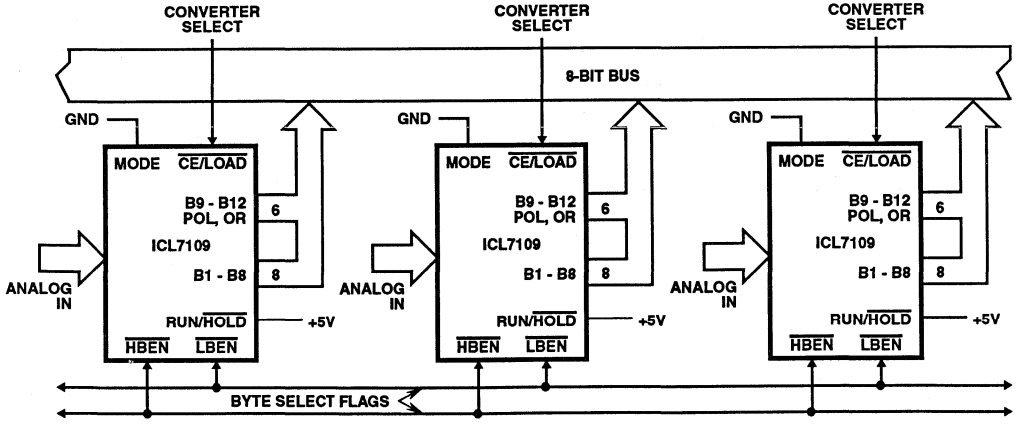


FIGURE 13. TRI-STATE SEVERAL ICL7109'S TO A SMALL BUS

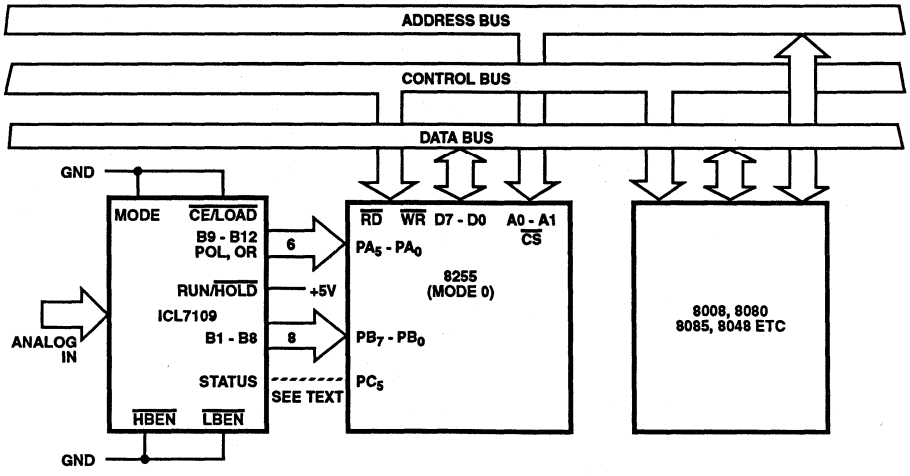


FIGURE 14. FULL-TIME PARALLEL INTERFACE TO 8040/80/85 MICROPROCESSORS

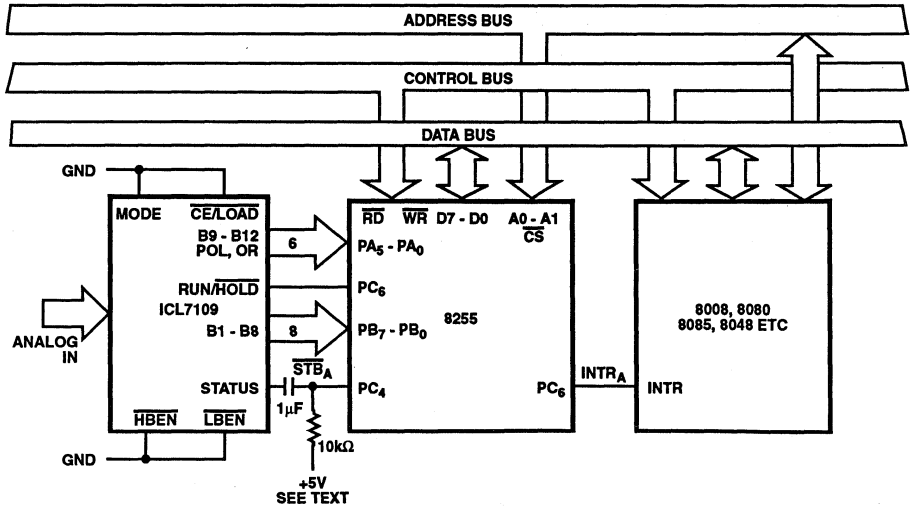
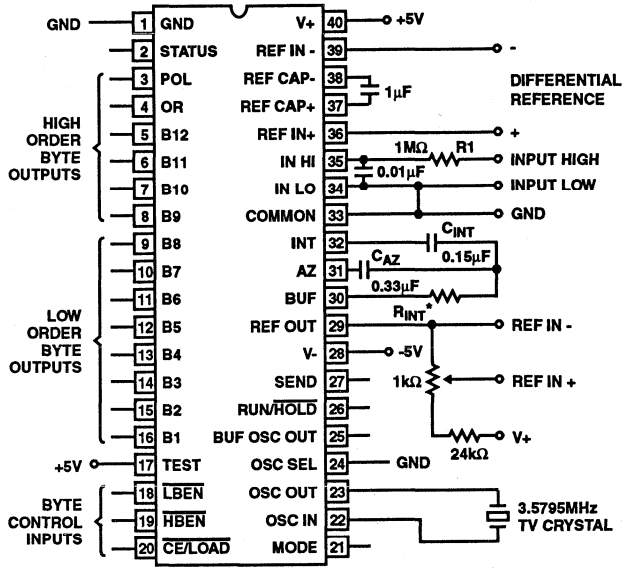


FIGURE 15. FULL-TIME PARALLEL INTERFACE TO 8048/80/85 MICROPROCESSORS WITH INTERRUPT

Test Circuit



*R_{INT} = 20kΩ FOR 0.2V REF
= 200kΩ FOR 2.0V REF

Typical Applications

Direct Mode Interfacing

Figure 12 shows some of the combinations of chip enable and byte enable control signals which may be used when interfacing the ICL7109 to parallel data lines. The $\overline{CE/LOAD}$ input may be tied low, allowing either byte to be controlled by its own enable as in Figure 12A. Figure 12B shows a configuration where the two byte enables are connected together. In this configuration, the $\overline{CE/LOAD}$ serves as a chip enable, and the $\overline{HBEN}$ and $\overline{LBEN}$ may be connected to GND or serve as a second chip enable. The 14 data outputs will all be enabled simultaneously. Figure 12C shows the $\overline{HBEN}$ and $\overline{LBEN}$ as flag inputs, and $\overline{CE/LOAD}$ as a master enable, which could be the READ strobe available from most microprocessors.

Figure 13 shows an approach to interfacing several ICL7109s to a bus, connecting the $\overline{HBEN}$ and $\overline{LBEN}$ signals of several converters together, and using the $\overline{CE/LOAD}$ inputs (perhaps decode from an address) to select the desired converter.

Some practical circuits utilizing the parallel tri-state output capabilities of the ICL7109 are shown in Figures 14 through 19. Figure 14 shows a straightforward application to the Intel 8048/80/85 microprocessors via an 8255PPI, where the ICL7109 data outputs are active at all times. The I/O ports of an 8155 may be used in the same way. This interface can be used in a read-anytime mode, although a read performed while the data latches are being updated will lead to scrambled data. This will occur very rarely, in the proportion of set-up skew times to conversion time. One way to overcome this is to read the STATUS output as well, and if it is high, read the data again after a delay of more than $^1/_2$ converter clock period. If STATUS is now low, the second reading is correct, and if it is still high, the first reading is correct. Alternatively, this timing problem is completely avoided by using a read-after-update sequence, as shown in Figure 15. Here the high to low transition of the STATUS output drives an interrupt to the microprocessor causing it to access the data latches. This application also shows the RUN/$\overline{HOLD}$ input being used to initiate conversions under software control.

A similar interface to Motorola MC6800 or Rockwell R650X systems is shown in Figure 16. The high to low transition of the STATUS output generates an interrupt via the Control Register B CB1 line. Note that CB2 controls the RUN/$\overline{HOLD}$ pin through Control Register B, allowing software-controlled initiation of conversions in this system as well.

The tri-state output capability of the ICL7109 allows direct interfacing to most microprocessor busses. Examples of this are shown in Figures 17 and 18. It is necessary to carefully consider the system in this type of interface, to be sure that requirements for setup and hold times, and minimum pulse widths are met. Note also the drive limitations on long buses. Generally this type of interface is only favored if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can also require many additional components, and using an interface device will usually simplify the system in this case.

Handshake Mode Interfacing

The handshake mode allows ready interface with a wide variety of external devices. For instance, external latches may be clocked by the rising edge of $\overline{CE/LOAD}$, and the byte enables may be used as byte identification flags or as load enables.

Figure 19 shows a handshake interface to Intel microprocessors again using an 8255PPI. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ICL7109, and using the $\overline{CE/LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be sent in MODE 1 for the port used. If the ICL7109 is in handshake mode and the 8255 IBF flag is low, the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enable byte outputs active. The PPI will generate an interrupt which when executed will result in the data being

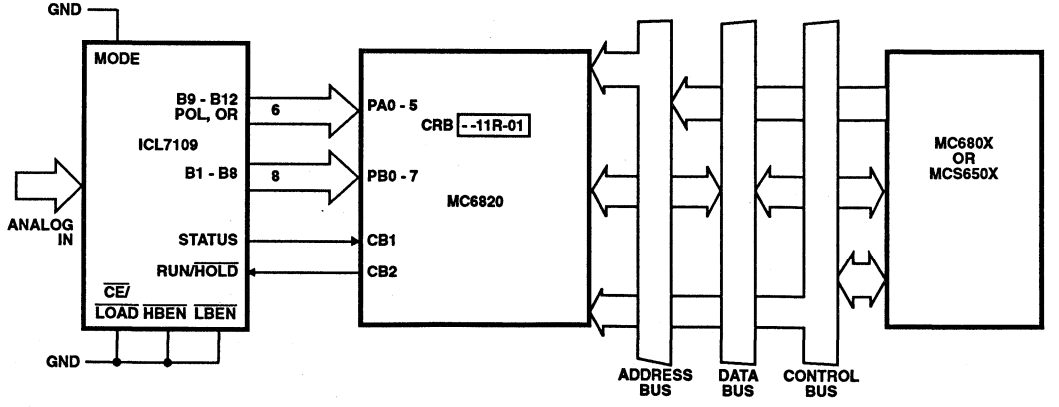


FIGURE 16. FULL-TIME PARALLEL INTERFACE TO MC680X OR MCS650X MICROPROCESSORS

read. When the byte is read, the IBF will be reset low, which causes the ICL7109 to sequence into the next byte. This figure shows the MODE input to the ICL7109 connected to a control line on the PPI. If this output is left high, or tied high separately, the data from every conversion (provided the data access takes less time than a conversion) will be sequenced in two bytes into the system.

If this output is made to go from low to high, the output sequence can be obtained on demand, and the interrupt may be used to reset the MODE bit. Note that the RUN/$\overline{\text{HOLD}}$ input to the ICL7109 may also be obtained on command under software control. Note that one port of the 8255 is not used, and can service another peripheral device. the same arrangement can also be used with the 8155.

Figure 20 shows a similar arrangement with the MC6800 or MCS650X microprocessors, except that both MODE and RUN/$\overline{\text{HOLD}}$ are tied high to save port outputs.

The handshake mode is particularly convenient for directly interfacing to industry standard UARTs (such as the Harris IM6402 or Western Digital TR1602) providing a minimum component count means of serially transmitting converted data. A typical UART connection is shown in Figure 1A. In this circuit, any word received by the UART causes the UART DR (Data Ready) output to go high. This drives the MODE input to the ICL7109 high, triggering the ICL7109 into handshake mode. The high order byte is output to the UART first, and when the UART has transferred the data to the Transmitter Register, TBRE (SEND) goes high again, $\overline{\text{LBEN}}$ will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the ICL7109 to the UART.

Figure 21 shows an extension of the one converter one UART scheme to several ICL7109s with one UART. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. With no external components, this scheme will allow up to eight ICL7109s to interface with one UART. Using a few more components to decode the received word will allow up to 256 converters to be accessed on one serial line.

The applications of the ICL7109 are not limited to those shown here. The purposes of these examples are to provide a starting point for users to develop useful systems and to show some of the variety of interfaces and uses of the combination. In particular the uses of the STATUS, RUN/$\overline{\text{HOLD}}$, and MODE signals may be mixed.

The following application notes contain very useful information on understanding and applying this part and are available from Harris Semiconductor.

Application Notes

A016 "Selecting A/D Converters"

A017 "The Integrating A/D Converter"

A018 "Do's and Don'ts of Applying A/D Converters"

A030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors"

A032 "Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7/9 Family"

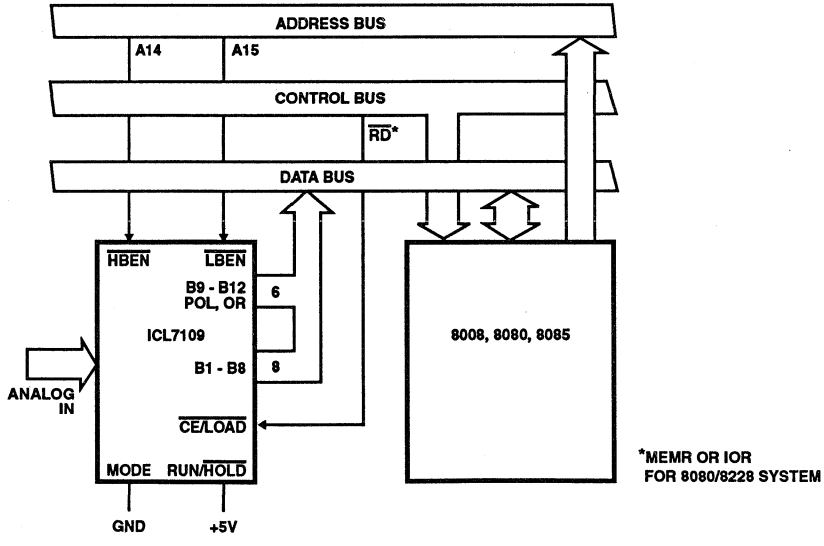


FIGURE 17. DIRECT INTERFACE - ICL7109 TO 8080/8085

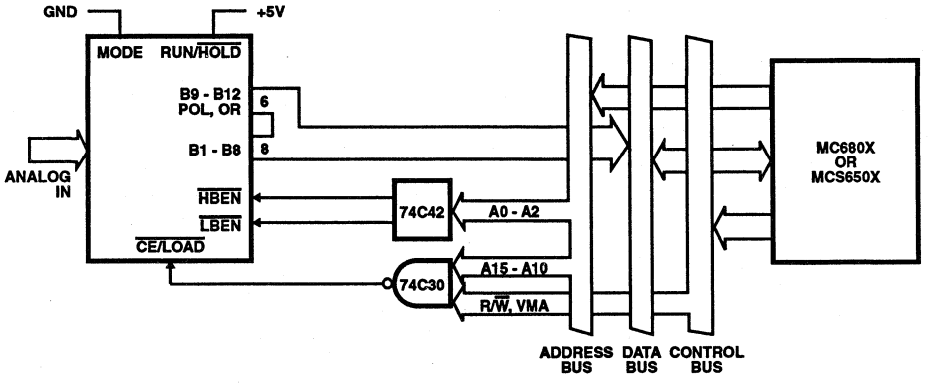


FIGURE 18. DIRECT ICL7109 - MC680X BUS INTERFACE

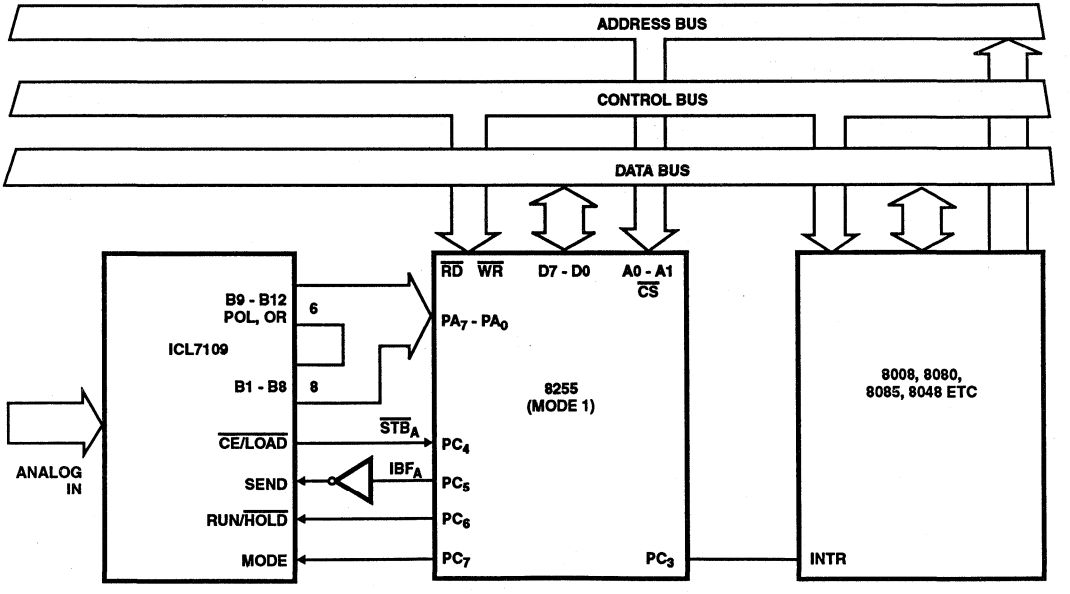


FIGURE 19. HANDSHAKE INTERFACE - ICL7109 TO 8048, 80/85

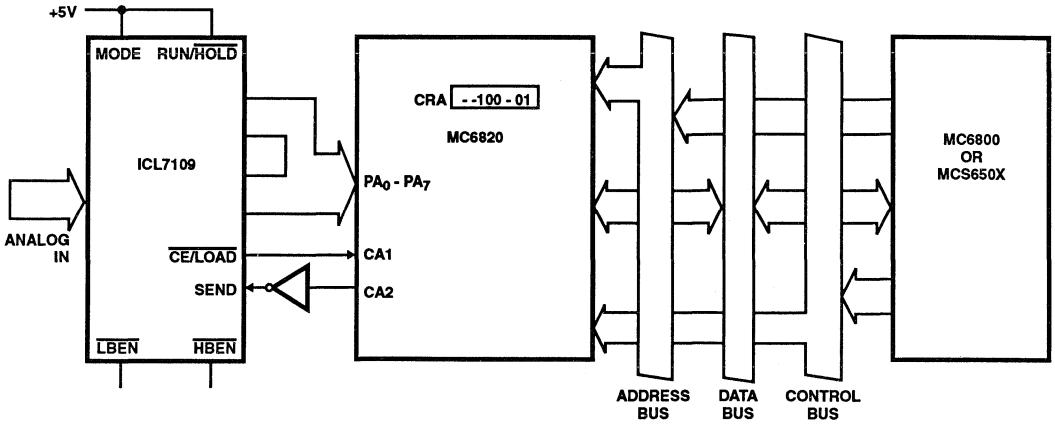


FIGURE 20. HANDSHAKE INTERFACE - ICL7109 TO MC6800, MCS650X

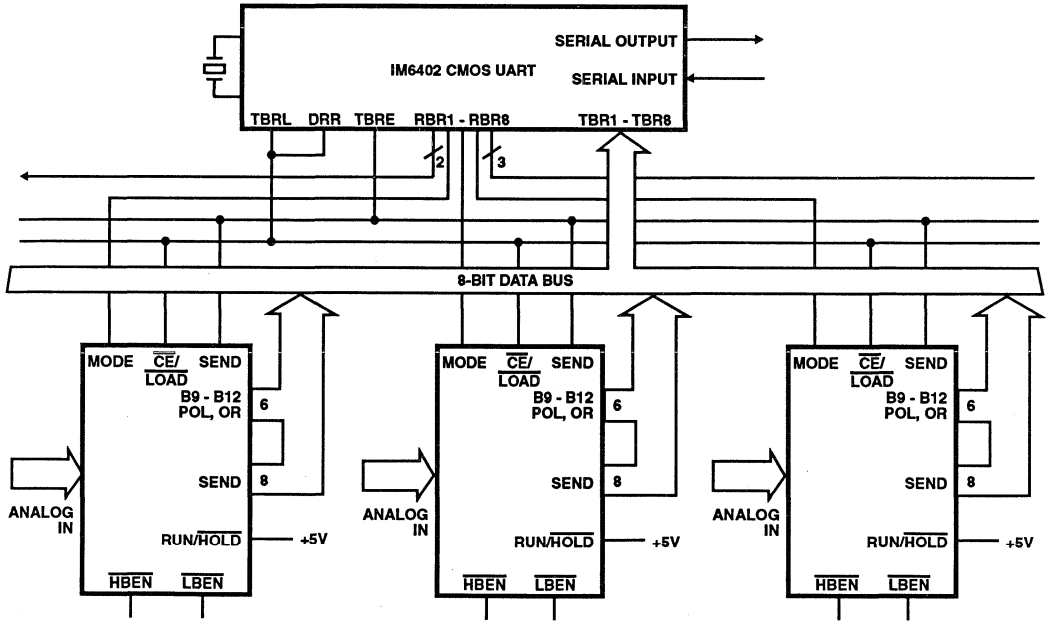


FIGURE 21. MULTIPLEXING CONVERTERS WITH MODE INPUT

Die Characteristics

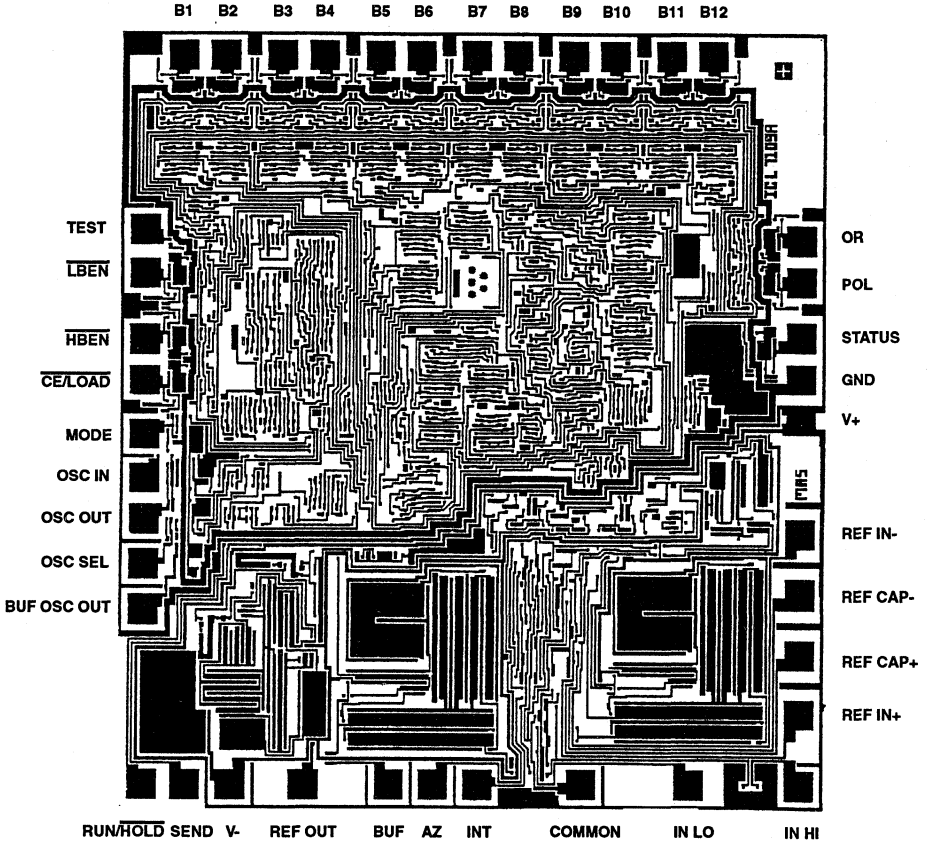
DIE DIMENSIONS:
(122 x 135)mils x 525µm ± 25µm Thick

METALLIZATION:
Type: Alum
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride/Silox Sandwich
Thickness: 8kÅ Nitride over 7kÅ Silox

Metallization Mask Layout

ICL7109



HARRIS SEMICONDUCTOR

ICL7135

$4^1/_2$ Digit BCD Output A/D Converter

December 1993

Features

- Accuracy Guaranteed to ±1 Count Over Entire ±20000 Counts (2.0000V Full Scale)
- Guaranteed Zero Reading for 0V Input
- 1pA Typical Input Leakage Current
- True Differential Input
- True Polarity at Zero Count for Precise Null Detection
- Single Reference Voltage Required
- Overrange and Underrange Signals Available for Auto-Range Capability
- All Outputs TTL Compatible
- Blinking Outputs Gives Visual Indication of Overrange
- Six Auxiliary Inputs/Outputs are Available for Interfacing to UARTs, Microprocessors, or Other Circuitry
- Multiplexed BCD Outputs

Description

The Harris ICL7135 precision A/D converter, with its multiplexed BCD output and digit drivers, combines dual-slope conversion reliability with ±1 in 20,000 count accuracy and is ideally suited for the visual display DVM/DPM market. The 2.0000V full scale capability, auto-zero, and auto-polarity are combined with true ratiometric operation, almost ideal differential linearity and true differential input. All necessary active devices are contained on a single CMOS IC, with the exception of display drivers, reference, and a clock.

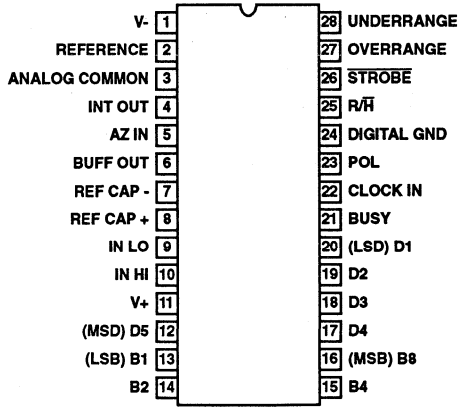
The ICL7135 brings together an unprecedented combination of high accuracy, versatility, and true economy. It features auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA max., and rollover error of less than one count. The versatility of multiplexed BCD outputs is increased by the addition of several pins which allow it to operate in more sophisticated systems. These include $\overline{\text{STROBE}}$, OVERRANGE, UNDERRANGE, RUN/$\overline{\text{HOLD}}$ and BUSY lines, making it possible to interface the circuit to a microprocessor or UART.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL7135CPI	0°C to +70°C	28 Lead Plastic DIP

Pinout

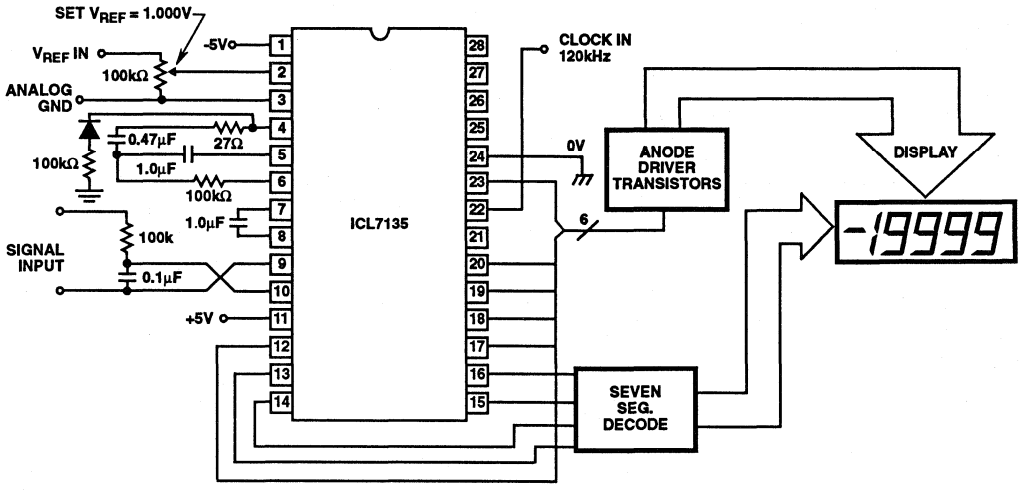
ICL7135
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3093

Typical Application Schematic



Absolute Maximum Ratings

Supply Voltage V+ ..... +6V
V- ..... -9V
Analog Input Voltage (Either Input) (Note 1) ..... V+ to V-
Reference Input Voltage (Either Input) ..... V+ to V-
Clock Input Voltage ..... GND to V+
Lead Temperature (Soldering 10s Max) ..... +300°C

Thermal Information

Thermal Resistance θ_{JA}
28 Lead Plastic Package ..... 55°C/W
Maximum Power Dissipation (Note 2) 800mW
Operating Temperature Range ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +5V$, $V- = -5V$, $T_A = +25°C$, f_{CLK} Set for 3 Readings/s, Unless Otherwise Specified

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG (Notes 3, 4)					
Zero Input Reading	$V_{IN} = 0V$, $V_{REF} = 1.000V$	-00000	+00000	+00000	Counts
Ratiometric Error (Note 4)	$V_{IN} = V_{REF} = 1.000V$	-3	-1	0	Counts
Linearity Over ± Full Scale (Error of Reading from Best Straight Line)	$-2V \le V_{IN} \le +2V$	-	0.5	1	LSB
Differential Linearity (Difference Between Worse Case Step of Adjacent Counts and Ideal Step)3	$-2V \le V_{IN} \le +2V$	-	0.01	-	LSB
Rollover Error (Difference in Reading for Equal Positive and Negative Voltage Near Full Scale)	$-V_{IN} \equiv +V_{IN} \approx 2V$	-	0.5	1	LSB
Noise (P-P Value Not Exceeded 95% of Time), eN	$V_{IN} = 0V$, Full scale = 2.000V	-	15	-	µV
Input Leakage Current, I_{ILK}	$V_{IN} = 0V$	-	1	10	pA
Zero Reading Drift (Note 7)	$V_{IN} = 0V$, $0° \le T_A \le +70°C$	-	0.5	2	µV/°C
Scale Factor Temperature Coefficient, TC (Notes 5 and 7)	$V_{IN} = +2V$, $0° \le T_A \le +70°C$ Ext. Ref. 0ppm/°C	-	2	5	ppm/°C
DIGITAL INPUTS					
Clock In, Run/$\overline{Hold}$ (See Figure 2)					
V_{INH}		2.8	2.2	-	V
V_{INL}		-	1.6	0.8	V
I_{INL}	$V_{IN} = 0V$	-	0.02	0.1	mA
I_{INH}	$V_{IN} = +5V$	-	0.1	10	µA
DIGITAL OUTPUTS					
All Outputs, V_{OL}	$I_{OL} = 1.6mA$	-	0.25	0.40	V
B_1, B_2, B_4, B_8, D_1, D_2, D_3, D_4, D_5, V_{OH}	$I_{OH} = -1mA$	2.4	4.2	-	V
BUSY, $\overline{STROBE}$, OVERRANGE, UNDERRANGE, POLARITY, V_{OH}	$I_{OH} = -10µA$	4.9	4.99	-	V
SUPPLY					
+5V Supply Range, V+		+4	+5	+6	V
-5V Supply Range, V-		-3	-5	-8	V
+5V Supply Current, I+	$f_C = 0$	-	1.1	3.0	mA
-5V Supply Current, I-	$f_C = 0$	-	0.8	3.0	mA
Power Dissipation Capacitance, C_{PD}	vs Clock Frequency	-	40	-	pF
CLOCK					
Clock Frequency (Note 6)		DC	2000	1200	kHz

NOTES:

1. Input voltages may exceed the supply voltages provided the input current is limited to +100µA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. Tested in $4^1/_2$ digit (20.000 count) circuit shown in Figure 3. (Clock frequency 120kHz.)
4. Tested with a low dielectric absorption integrating capacitor, the 27W INT. OUT resistor shorted, and RINT = 0. See Component Value Selection Discussion.
5. The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the ICL7135.
6. This specification relates to the clock frequency range over which the ICL7135 will correctly perform its various functions See "Max Clock Frequency" section for limitations on the clock frequency range in a system.
7. Parameter guaranteed by design or characterization. Not production tested.

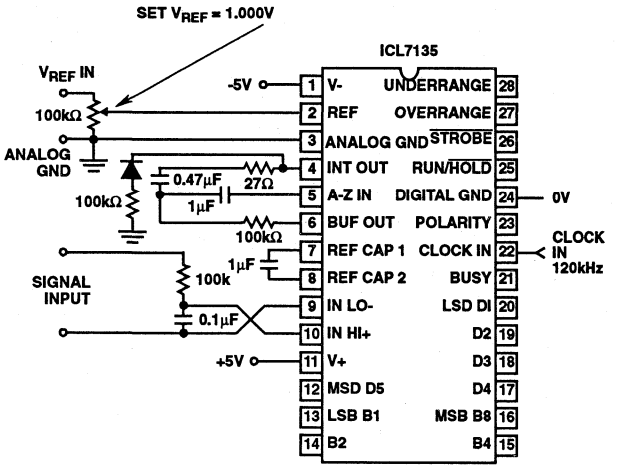


FIGURE 1. ICL7135 TEST CIRCUIT

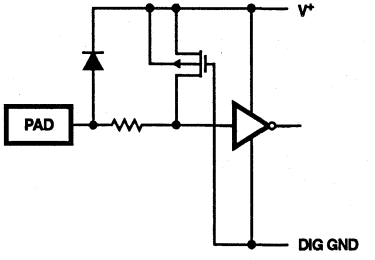


FIGURE 2. ICL7135 DIGITAL LOGIC INPUT

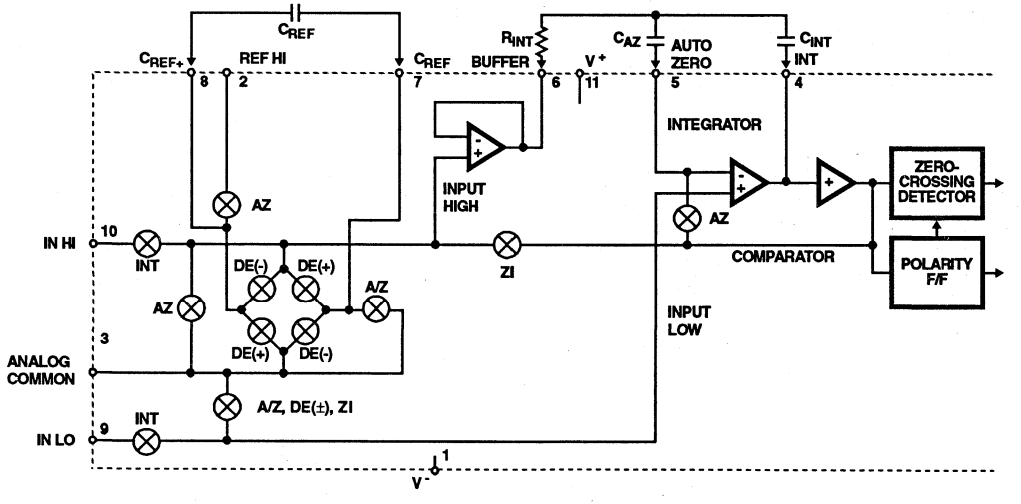


FIGURE 3. ANALOG SECTION OF ICL7135

Detailed Description

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7135. Each measurement cycle is divided into four phases. They are (1) auto-zero (AZ), (2) signal-integrate (INT), (3) de-integrate (DE) and (4) zero-integrator (ZI).

Auto-Zero Phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog COMMON. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

Signal Integrate Phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between IN HI and IN LO for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, IN LO can be tied to analog COMMON to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is latched into the polarity F/F.

De-Integrate Phase

The third phase is de-integrate or reference integrate. Input low is internally connected to analog COMMON and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is:

$$\text{OUTPUT COUNT} = 10{,}000 \left(\frac{V_{IN}}{V_{REF}}\right)$$

Zero Integrator Phase

The final phase is zero integrator. First, input low is shorted to analog COMMON. Second, a feedback loop is closed around the system to input high to cause the integrator output to return to zero. Under normal condition, this phase lasts from 100 to 200 clock pulses, but after an overrange conversion, it is extended to 6200 clock pulses.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5V below the positive supply to 1V above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale swing with some loss of accuracy. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog COMMON

Analog COMMON is used as the input low return during auto-zero and de-integrate. If IN LO is different from analog COMMON, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in most applications IN LO will be set at a fixed known voltage (power supply common for instance). In this application, analog COMMON should be tied to the same point, thus removing the common mode voltage from the converter. The reference voltage is referenced to analog COMMON.

Reference

The reference input must be generated as a positive voltage with respect to COMMON, as shown in Figure 4.

Digital Section

Figure 5 shows the Digital Section of the ICL7135. The ICL7135 includes several pins which allow it to operate conveniently in more sophisticated systems. These include:

Run/$\overline{\text{HOLD}}$ (Pin 25)

When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,002 clock pulses. If taken low, the converter will continue the full measurement cycle that it is doing and then hold this reading as long as R/$\overline{\text{H}}$ is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle, beginning with between 1 and 10,001 counts of auto zero. If the pulse occurs before the full measurement cycle (40,002 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is doing. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 101 counts after the end of this cycle. Thus, if Run/$\overline{\text{HOLD}}$ is low and has been low for at least 101 counts, the converter is holding and ready to start a new measurement when pulsed high.

$\overline{\text{STROBE}}$ (Pin 26)

This is a negative going output pulse that aids in transferring the BCD data to external latches, UARTs, or microprocessors. There are 5 negative going $\overline{\text{STROBE}}$ pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 101 clock pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 201 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first $\overline{\text{STROBE}}$ pulse goes negative for 1/2 clock pulse width. Similarly, after digit 5, digit 4 goes high (for 200 clock pulses) and 100 pulses later the $\overline{\text{STROBE}}$ goes negative for the second time. This continues through digit 1

(LSD) when the fifth and last $\overline{\text{STROBE}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was overrange) but no additional $\overline{\text{STROBE}}$ pulses will be sent until a new measurement is available.

BUSY (Pin 21)

BUSY goes high at the beginning of signal integrate and stays high until the first clock pulse after zerocrossing (or after end of measurement in the case of an overrange). The internal latches are enabled (i.e., loaded) during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY, so it may also be considered a $\overline{(ZI + AZ)}$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001 counts from the number of pulses received - as mentioned previously there is one "NO-count" pulse in each reference integrate cycle.

OVERRANGE (Pin 27)

This pin goes positive when the input signal exceeds the range (20,000) of the converter. The output F/F is set at the end of BUSY and is reset to zero at the beginning of reference integrate in the next measurement cycle.

UNDERRANGE (Pin 28)

This pin goes positive when the reading is 9% of range or less. The output F/F is set at the end of BUSY (if the new reading is 1800 or less) and is reset at the beginning of signal integrate of the next reading.

POLARITY (Pin 23)

This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal frequency of (+) and (-) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is revalidated for the next measurement.

Digit Drives (Pins 12,17,18,19 and 20)

Each digit drive is a positive going signal that lasts for 200 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2, and D_1 (LSD). All five digits are scanned and this scan is continuous unless an overrange occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when D_5 will start the scan again. This can give a blinking display as a visual indication of overrange.

BCD (Pins 13, 14, 15 and 16)

The Binary coded Decimal bits B_8, B_4, B_2,and B_1 are positive logic signals that go on simultaneously with the digit driver signal.

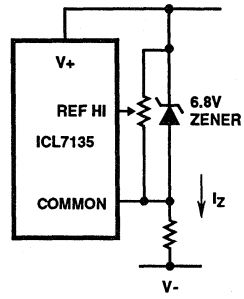


FIGURE 4A.

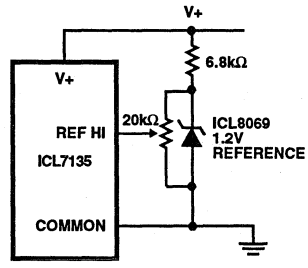


FIGURE 4B.

FIGURE 4. USING AN EXTERNAL REFERENCE

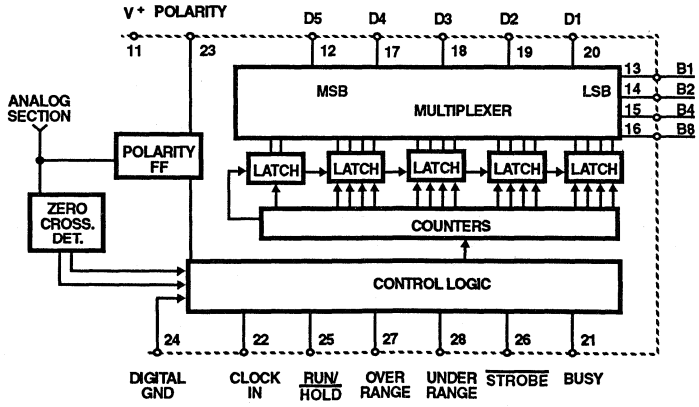


FIGURE 5. DIGITAL SECTION OF THE ICL7135

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. Values of 5μA to 40μA give good results, with a nominal of 20μA, and the exact value of integrating resistor may be chosen by

$$R_{INT} = \frac{\text{full scale voltage}}{20\,\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor should be selected to give the maximum voltage swing which ensures that the tolerance built-up will not saturate the integrator swing (approx. 0.3V from either supply). For ±5V supplies and analog COMMON tied to supply ground, a ±3.5V to ±4V full scale integrator swing is fine, and 0.47μF is nominal. In general, the value of C_{INT} is given by

$$C_{INT} = \left(\frac{[10{,}000 \times \text{clock period}] \times I_{INT}}{\text{integrator output voltage swing}}\right)$$

$$= \frac{(10{,}000)\,(\text{clock period})\,(20\,\mu A)}{\text{integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it has low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 0.9999, and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The physical size of the auto-zero capacitor has an influence on the noise of the system. A larger capacitor value reduces system noise. A larger physical size increases system noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full-scale output is $V_{IN} = 2V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. For this reason, it is recommended that a high quality reference be used where high-accuracy absolute measurements are being made.

Rollover Resistor and Diode

A small rollover error occurs in the ICL7135, but this can be easily corrected by adding a diode and resistor in series between the INTegrator OUTput and analog COMMON or ground. The value shown in the schematics is optimum for the recommended conditions, but if integrator swing or clock frequency is modified, adjustment may be needed. The diode can be any silicon diode such as 1N914. These components can be eliminated if rollover error is not important and may be altered in value to correct other (small) sources of rollover as needed.

Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. The comparator in this circuit follows the integrator ramp with a 3μs delay, and at a clock frequency of 160kHz (6μs period) half of the first reference integrate clock period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50μV input, 1 to 2 with a 150μV input, 2 to 3 with a 250μV input, etc. This transition at mid-point is considered desirable by most users; however, if the clock frequency is increased appreciably above 160kHz, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always of one polarily, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, clock rates of up to ~1MHz may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be constant and can be subtracted out digitally.

The clock frequency may be extended above 160kHz without this error, however, by using a low value resistor in series with the integrating capacitor. The effect of the resistor is to introduce a small pedestal voltage on to the integrator output at the beginning of the reference integrate phase. By careful selection of the ratio between this resistor and the integrating resistor (a few tens of ohms in the recommended circuit), the comparator delay can be compensated and the maximum clock frequency extended by approximately a factor of 3. At higher frequencies, ringing and second order breaks will cause significant non-linearities in the first few counts of the instrument. See Application Note AN017.

The minimum clock frequency is established by leakage on the auto-zero and reference caps. With most devices, measurement cycles as long as 10sec give no measurable leakage error.

To achieve maximum rejection of 60Hz pickup, the signal integrate cycle should be a multiple of 60Hz. Oscillator frequencies of 300kHz, 200kHz, 150kHz, 120kHz, 100kHz, 40kHz, 33-1/3kHz, etc. should be selected. For 50Hz rejection, oscillator frequencies of 250kHz, 166-2/3kHz, 125kHz, 100kHz, etc. would be suitable. Note that 100kHz (2.5 readings/second) will reject both 50Hz and 60Hz.

The clock used should be free from significant phase or frequency jitter. Several suitable low-cost oscillators are shown in the Typical Applications section. The multiplexed output means that if the display takes significant current from the logic supply, the clock should have good PSRR.

Zero-Crossing Flip-Flop

The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. False zero-crossings caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by up to one count in every instance, and if a correction were not made, the display would always be one count too high. Therefore, the counter is disabled for one clock pulse at the beginning of phase 3. This one-count delay compensates for the delay of the zero-crossing flip-flop, and allows the correct number to be latched into the display. Similarly, a one-count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2, so that true ratiometric readings result.

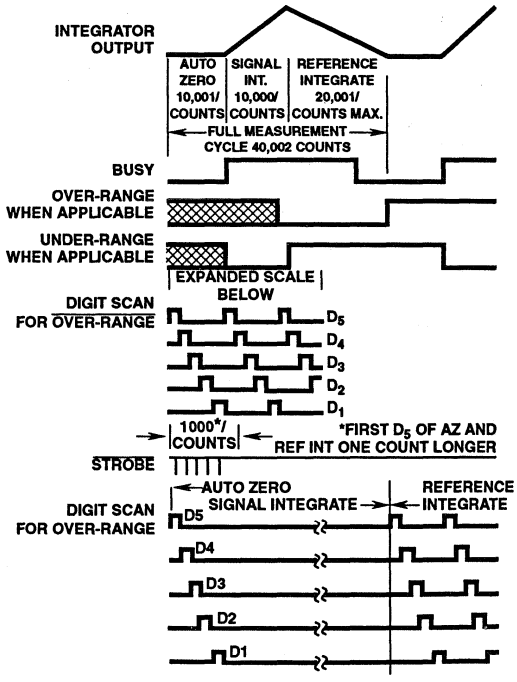


FIGURE 6. TIMING DIAGRAM FOR OUTPUTS

Evaluating The Error Sources

Errors from the "ideal" cycle are caused by:

1. Capacitor droop due to leakage.
2. Capacitor voltage change due to charge "suck-out" (the reverse of charge injection) when the switches turn off.
3. Non-linearity of buffer and integrator.
4. High-frequency limitations of buffer, integrator, and comparator.
5. Integrating capacitor non-linearity (dielectric absorption).
6. Charge lost by C_{REF} in charging C_{STRAY}.
7. Charge lost by C_{AZ} and C_{INT} to charge C_{STRAY}.

Each error is analyzed for its error contribution to the converter in application notes listed on the back page, specifically Application Note AN017 and Application Note AN032.

Noise

The peak-to-peak noise around zero is approximately 15µV (pk-to-pk value not exceeded 95% of the time). Near full scale, this value increases to approximately 30µV. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

Analog And Digital Grounds

Extreme care must be taken to avoid ground loops in the layout of ICL7135 circuits, especially in high-sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line.

Power Supplies

The ICL7135 is designed to work from ±5V supplies. However, in selected applications no negative supply is required. The conditions to use a single + 5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5V.

See "differential input" for a discussion of the effects this will have on the integrator swing without loss of linearity.

Typical Applications

The circuits which follow show some of the wide variety of possibilities and serve to illustrate the exceptional versatility of this A/D converter.

Figure 7 shows the complete circuit for a $4^1/_2$ digit (±2.000V) full scale) A/D with LED readout using the ICL8069 as a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to 50µA. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower, or the filter deleted completely. The 1/2 digit LED is

driven from the 7 segment decoder, with a zero reading blanked by connecting a D_5 signal to RBI input of the decoder. The 2-gate clock circuit should use CMOS gates to maintain good power supply rejection.

A suitable circuit for driving a plasma-type display is shown in Figure 8. The high voltage anode driver buffer is made by Dionics. The 3 AND gales and caps driving "BI" are needed for interdigit blanking of multiple-digit display elements, and can be omitted if not needed. The 2.5kΩ & 3kΩ resistors set the current levels in the display. A similar arrangement can be used with Nixie® tubes.

The popular LCD displays can be interfaced to the outputs of the ICL7135 with suitable display drivers, such as the ICM7211A as shown in Figure 9. A standard CMOS 4030 QUAD XOR gate is used for displaying the 1/2 digit, the polarity, and an "overrange" flag. A similar circuit can be used with the ICL7212A LED driver and the ICM7235A vacuum fluorescent driver with appropriate arrangements made for the "extra" outputs. Of course, another full driver circuit could be ganged to the one shown if required. This would be useful if additional annunciators were needed. The Figure shows the complete circuit for a $4^1/_2$ digit (±2.000V) A/D.

Figure 10 shows a more complicated circuit for driving LCD displays. Here the data is latched into the ICM7211 by the $\overline{\text{STROBE}}$ signal and "Overrange" is indicated by blanking the 4 full digits.

A problem sometimes encountered with both LED and plasma-type display driving is that of clock source supply line variations. Since the supply is shared with the display, any variation in voltage due to the display reading may cause clock supply voltage modulation. When in overrange the display alternates between a blank display and the 0000 overrange indication. This shift occurs during the reference integrate phase of conversion causing a low display reading just after overrange recovery. Both of the above circuits have considerable current flowing in the digital supply from drivers, etc. A clock source using an LM311 voltage comparator with positive feedback (Figure 11) could minimize any clock frequency shift problem.

The ICL7135 is designed to work from ±5V supplies. However, if a negative supply is not available, it can be generated with an ICL7660 and two capacitors (Figure 12).

Interfacing with UARTs and Microprocessors

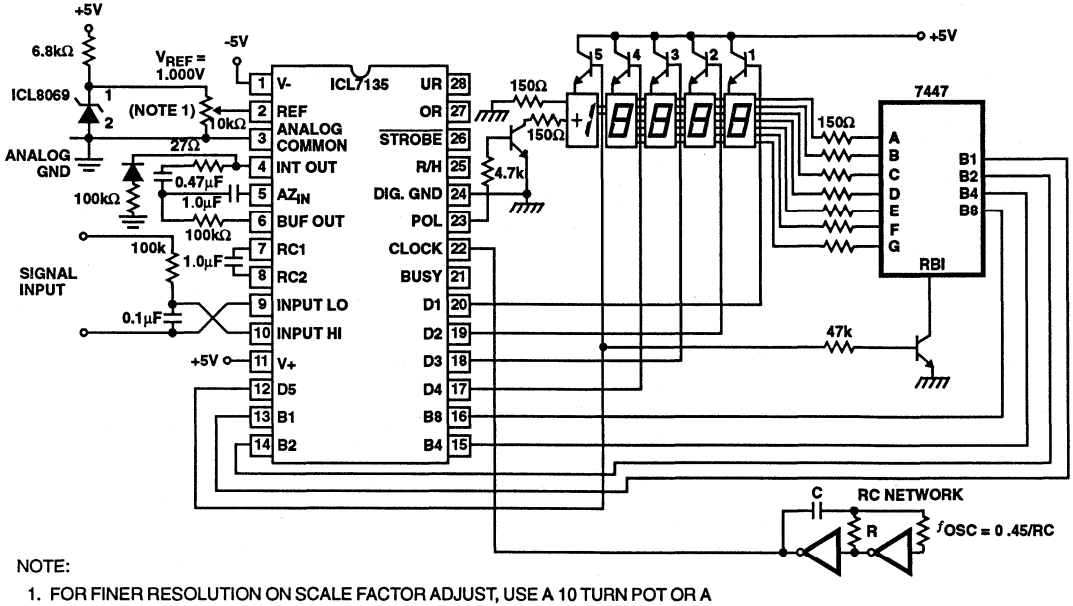
Figure 13 shows a very simple interface between a free- running ICL7135 and a UART. The five $\overline{\text{STROBE}}$ pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative. A complex arrangement is shown in Figure 14. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The $\overline{\text{BUSY}}$ signal resets the Data Ready Reset (DRR). Again $\overline{\text{STROBE}}$ starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

For correct operation it is important that the UART clock be fast enough that each word is transmitted before the next $\overline{\text{STROBE}}$ pulse arrives. Parity is locked into the UART at load time but does not change in this connection during an output stream.

Circuits to interface the ICL7135 directly with three popular microprocessors are shown in Figure 15 and Figure 16. The 8080/8048 and the MC6800 groups with 8 bit buses need to have polarity, over-range and under-range multiplexed onto the Digit 5 Sword - as in the UART circuit. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

Application Notes

A016	"Selecting A/D Converters"
A017	"The Integrating A/D Converters"
A018	"Do's and Don'ts of Applying A/D Converters"
A023	"Low Cost Digital Panel Meter Designs"
A028	"Building an Auto-Ranging DMM Using the 8052A/ 7103A A/D Converter Pair"
A030	"The ICL7104 - A Binary Output A/D Converter for Microprocessors"
A032	"Understanding the Auto-Zero and Common Mode Performance of the ICL7106 Family"
R005	"Interfacing Data Converters & Microprocessors"



NOTE:

1. FOR FINER RESOLUTION ON SCALE FACTOR ADJUST, USE A 10 TURN POT OR A SMALL POT IN SERIES WITH A FIXED RESISTOR.

FIGURE 7. $4^1/_2$ DIGIT A/D CONVERTER WITH A MULTIPLEXED COMMON ANODE LED DISPLAY

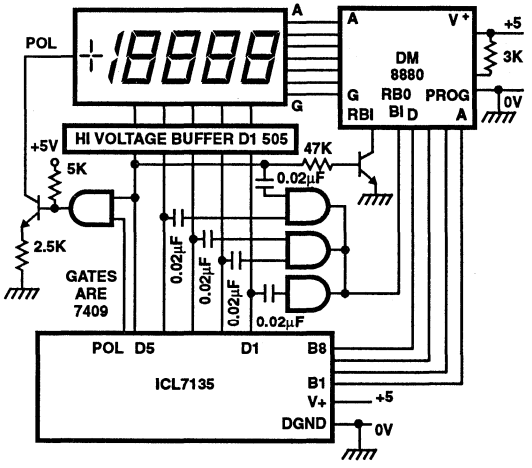


FIGURE 8. ICL7135 PLASMA DISPLAY CIRCUIT

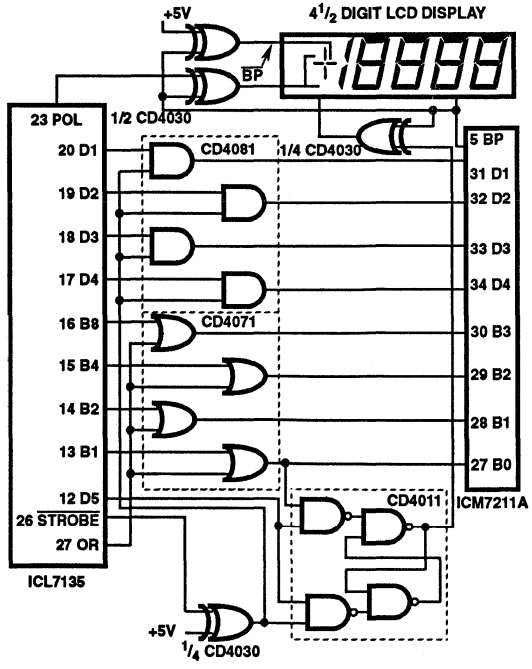


FIGURE 9. LCD DISPLAY WITH DIGIT BLANKING ON OVERRANGE

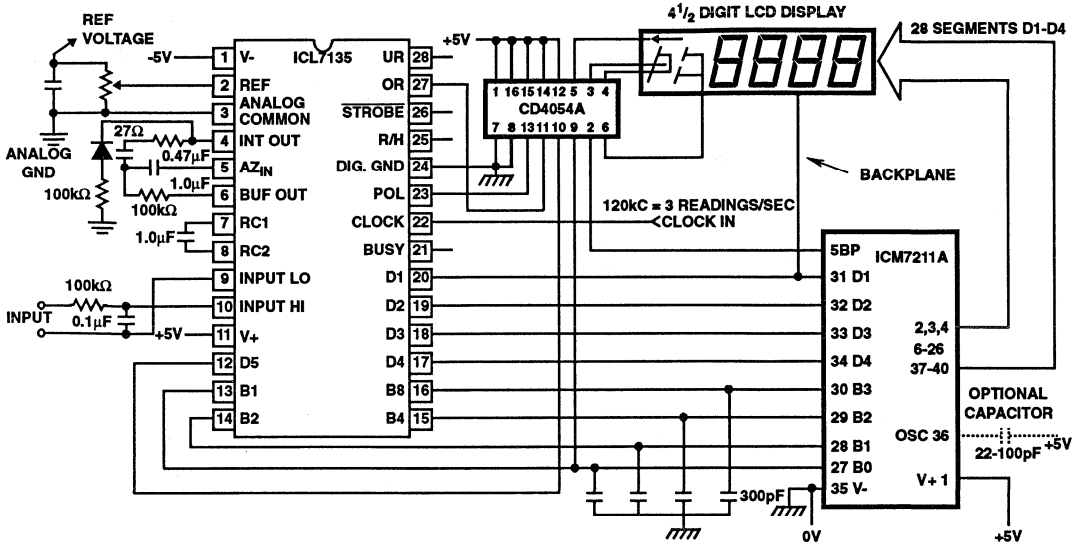


FIGURE 10. DRIVING LCD DISPLAYS

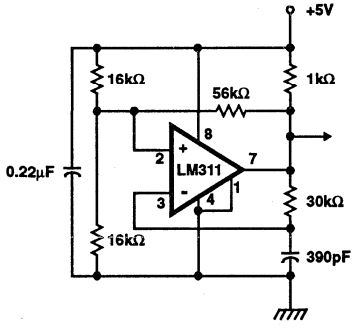


FIGURE 11. LM311 CLOCK SOURCE

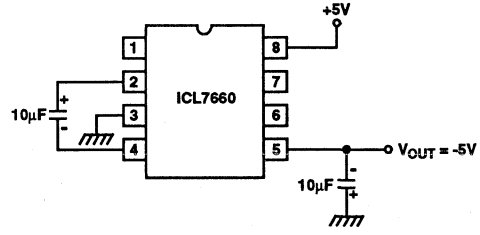


FIGURE 12. GENERATING A NEGATIVE SUPPLY FROM +5V

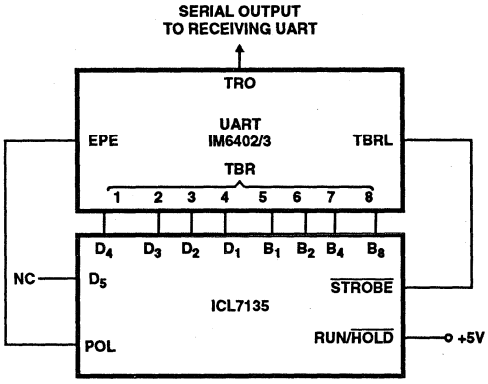


FIGURE 13. ICL7135 TO UART INTERFACE

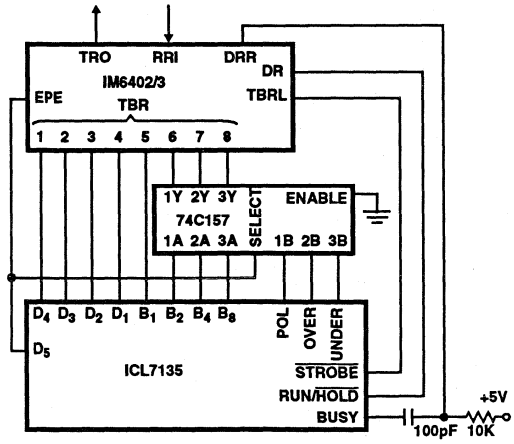


FIGURE 14. COMPLEX ICL7135 TO UART INTERFACE

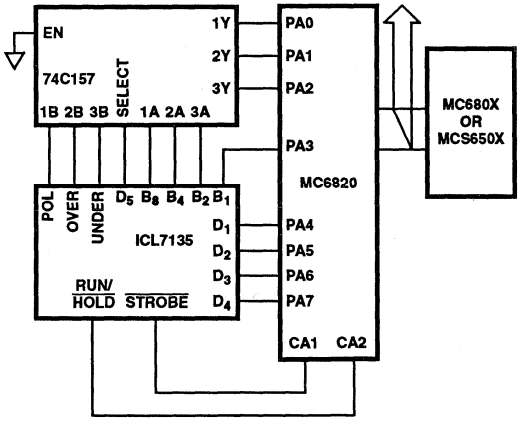


FIGURE 15. ICL7135 TO MC6800, MCS650X INTERFACED

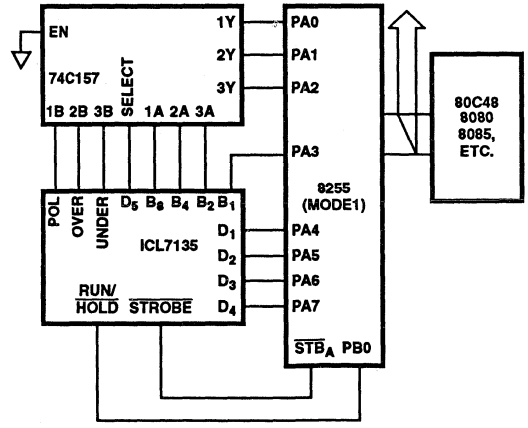


FIGURE 16. ICL7135 TO MCS-48, -80, 85 INTERFACE

Design Information Summary Sheet

- **CLOCK INPUT**
  The ICL7135 does not have an internal oscillator. It requires an external clock.
  f_{CLOCK} typ = 120KHz
- **CLOCK PERIOD**
  $t_{CLOCK} = 1/f_{CLOCK}$
- **INTEGRATION PERIOD**
  $t_{INT} = 10{,}000 \times t_{CLOCK}$
- **60/50Hz REJECTION CRITERION**
  t_{INT}/t_{60Hz} or t_{INT}/t_{50Hz} = Interger
- **OPTIMUM INTEGRATION CURRENT**
  $I_{INT} = 20.0\mu A$
- **FULL-SCALE ANALOG INPUT VOLTAGE**
  V_{INFS} Typically = 200mV or 2.0V
- **INTEGRATE RESISTOR**

$$R_{INT} = \frac{V_{INFS}}{I_{INT}}$$

- **INTEGRATE CAPACITOR**

$$C_{INT} = \frac{(t_{INT})\ (I_{INT})}{V_{INT}}$$

- **INTEGRATOR OUTPUT VOLTAGE SWING**

$$V_{INT} = \frac{(t_{INT})\ (I_{INT})}{C_{INT}}$$

V_{INT} MAXIMUM SWING:

$(V- + 0.5) < V_{INT} < (V+ - 0.5V)$
V_{INT} Typically = 2.7V

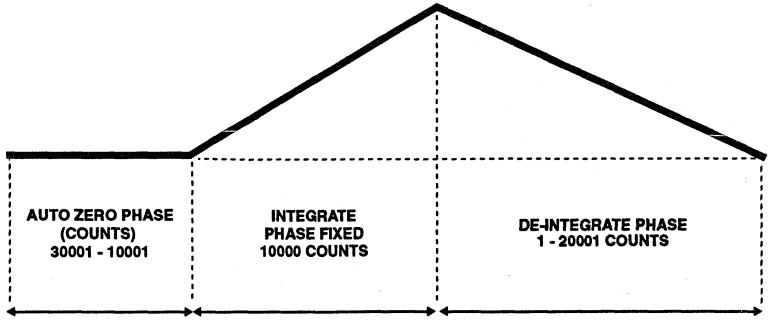
- **DISPLAY COUNT**

$$COUNT = 10{,}000 \times \frac{V_{IN}}{V_{REF}}$$

- **CONVERSION CYCLE**
  $t_{CYC} = t_{CLOCK} \times 40002$
  when f_{CLOCK} = 120kHz, t_{CYC} = 333ms
- **COMMON MODE INPUT VOLTAGE**
  $(V- + 1.0V) < V_{IN} < (V+ - 0.5V)$
- **AUTO-ZERO CAPACITOR**
  $0.01\mu F < C_{AZ} < 1.0\mu F$
- **REFERENCE CAPACITOR**
  $0.1\mu F < C_{REF} < 1.0\mu F$
- **POWER SUPPLY: DUAL ±5.0V**
  V+ = +5.0 to GND
  V- = -5.0 to GND
- **OUTPUT TYPE**
  4 BCD Nibbles with Polarity and Overrange Bits

There is no internal reference available on the ICL7135. An external reference is required due to the ICL7135's $4^1/_2$ digit resolution.

Typical Integrator Amplifier Output Waveform (INT Pin)



Die Characteristics

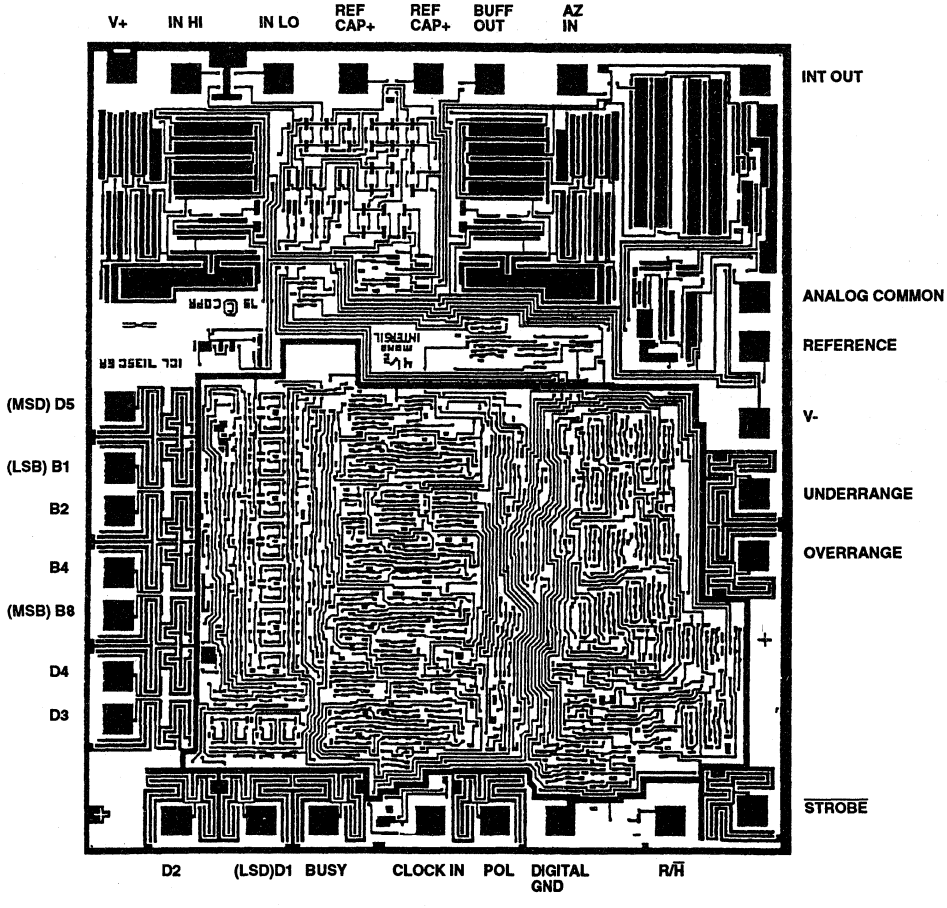
DIE DIMENSIONS:
(120 x 130mils) x 525 ± 25µm

METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride/Silox Sandwich
Thickness: 8k Nitride over 7k Silox

Metallization Mask Layout

ICL7135



DATA ACQUISITION 4

A/D CONVERTERS - SIGMA-DELTA

NOTE: Bold Type Designates a New Product from Harris.

HARRIS SEMICONDUCTOR

HI7190

ADVANCE INFORMATION

December 1993

24-Bit High Precision Sigma-Delta A/D Converter

Features

- 24-Bit Resolution with No Missing Code
- 0.0007% Integral Non-Linearity
- 20mV to ±2.5V Full Scale Input Ranges
- Dual ±5V, Single +5V, or Battery Operation
- Internal PGIA with Gains of 1X-128X
- Serial Data I/O Interface
- Differential Analog and Reference Input
- Internal or System Auto-Calibration
- -120dB Rejection of 60Hz

Applications

- Weigh Scales
- Medical Patient Monitoring
- Seismic Monitoring
- Part Counting Scales
- Motion Control
- Magnetic Field Monitoring
- Intruder Detection
- Laboratory Instrumentation
- Process Control and Measurement

Description

The Harris HI7190 is a monolithic instrumentation A/D converter that uses a Sigma-Delta modulation technique. Both the signal and reference inputs are fully differential for maximum flexibility and performance. An internal Programmable Gain Instrumentation Amplifier (PGIA) provides input gains up to 128X, eliminating the need for external pre-amplifiers. The on-demand converter auto-calibrate function is capable of removing offset and gain errors existing in external and internal circuitry. The device can operate from 5V supplies and from a single +5V supply and can operate from a battery. The on-board, user programmable digital filter provides over 120dB of 60Hz noise rejection and allows fine tuning of resolution and conversion speed.

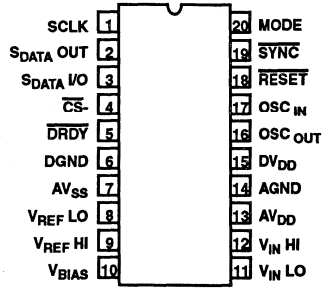
The HI7190 contains a serial I/O port, and is compatible with most synchronous transfer formats, including both the Motorola/Harris 6805/11 series SPI and Intel 8051 series SSR protocols. A sophisticated set of commands gives the user control over calibration, PGIA gain, device selection, sleep mode, and other options.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI7190IP	-40°C to +85°C	20 Lead Plastic DIP
HI7190IJ	-40°C to +85°C	20 Lead Ceramic DIP
HI7190IB	-40°C to +85°C	20 Lead Small Outline Package (SOIC)

Pinout

HI7190
(PDIP, CDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3612

DATA ACQUISITION 5

A/D CONVERTERS - SAR

NOTE: Bold Type Designates a New Product from Harris.

HARRIS SEMICONDUCTOR

ADC0802, ADC0803 ADC0804

8-Bit µP Compatible A/D Converters

December 1993

Features

- 80C48 and 80C80/85 Bus Compatible - No Interfacing Logic Required
- Conversion Time < 100µs
- Easy Interface to Most Microprocessors
- Will Operate in a "Stand Alone" Mode
- Differential Analog Voltage Inputs
- Works with Bandgap Voltage References
- TTL Compatible Inputs and Outputs
- On-Chip Clock Generator
- 0V to 5V Analog Voltage Input Range (Single + 5V Supply)
- No Zero-Adjust Required

Description

The ADC0802 family are CMOS 8-Bit successive approximation A/D converters which use a modified potentiometric ladder and are designed to operate with the 8080A control bus via three-state outputs. These converters appear to the processor as memory locations or I/O ports, and hence no interfacing logic is required.

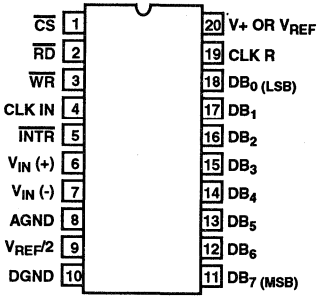
The differential analog voltage input has good common-mode-rejection and permits offsetting the analog zero-input-voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8-Bits of resolution.

Ordering Information

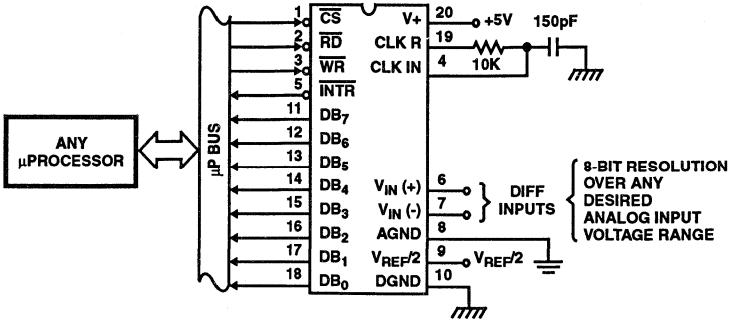
PART NUMBER	ERROR	EXTERNAL CONDITIONS	TEMPERATURE RANGE	PACKAGE
ADC0802LCN	$\pm 1/2$ LSB	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	0°C to +70°C	20 Lead Plastic DIP
ADC0802LCD	$\pm 3/4$ LSB		-40°C to +85°C	20 Lead Ceramic DIP
ADC0802LD	±1 LSB		-55°C to +125°C	20 Lead Ceramic DIP
ADC0803LCN	$\pm 1/2$ LSB	$V_{REF}/2$ Adjusted for Correct Full-Scale Reading	0°C to +70°C	20 Lead Plastic DIP
ADC0803LCD	$\pm 3/4$ LSB		-40°C to +85°C	20 Lead Ceramic DIP
ADC0802LCWM	±1 LSB		-40°C to +85°C	20 Lead SOIC (W)
ADC0803LD	±1 LSB		-55°C to +125°C	20 Lead Ceramic DIP
ADC0804LCN	±1 LSB	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	0°C to +70°C	20 Lead Plastic DIP
ADC0804LCD	±1 LSB		-40°C to +85°C	20 Lead Ceramic DIP

Pinout

ADC0802, ADC0803, ADC0804
(PDIP, CDIP)
TOP VIEW



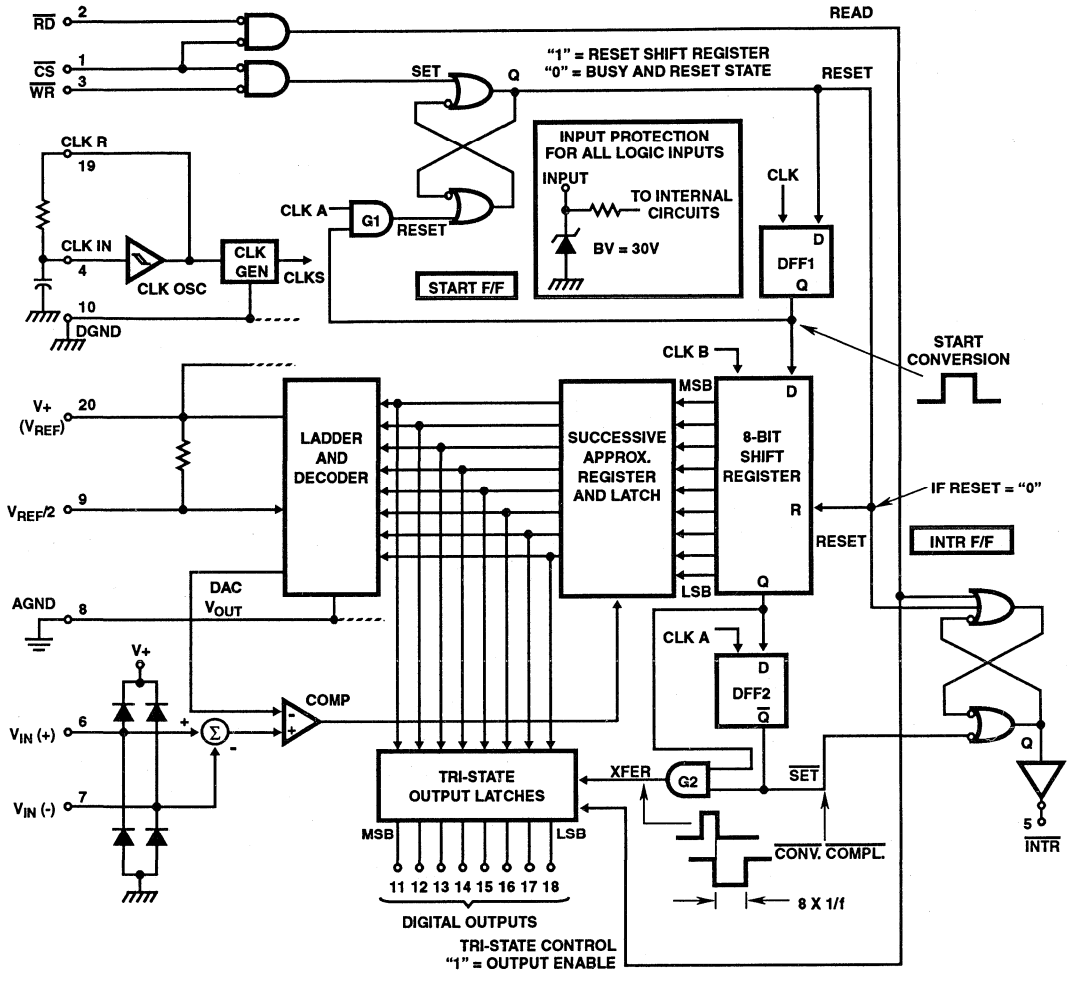
Typical Application Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3094

Functional Diagram



Absolute Maximum Ratings

Supply Voltage 6.5V
Voltage at Any Input ..... -0.3V to (V^+ +0.3V)
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	125°C/W	-
Ceramic DIP Package	70°C/W	20°C/W
SOIC Package	120°C/W	-

Operating Temperature Range
ADC0802/03LD ..... -55°C to +125°C
ADC0802/03/04LCD ..... -40°C to +85°C
ADC0802/03/04LCN ..... 0°C to +70°C
ADC0803LCWM ..... -40°C to +85°C
Junction Temperature
Ceramic Package ..... +175°C
Plastic Package ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications (Notes 1, 7)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CONVERTER SPECIFICATIONS	V+ = 5V, T_A = +25°C and f_{CLK} = 640kHz, Unless Otherwise Specified				
Total Unadjusted Error					
ADC0802	$V_{REF}/2$ = 2.500V	-	-	$\pm^1/_2$	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full-Scale Reading	-	-	$\pm^1/_2$	LSB
ADC0804	$V_{REF}/2$ = 2.500V	-	-	±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm^1/_{16}$	$\pm^1/_8$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm^1/_{16}$	$\pm^1/_8$	LSB
CONVERTER SPECIFICATIONS	V+ = 5V, 0°C ≤ T_A ≤ +70°C and f_{CLK} = 640kHz, Unless Otherwise Specified				
Total Unadjusted Error					
ADC0802	$V_{REF}/2$ = 2.500V	-	-	$\pm^1/_2$	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full-Scale Reading	-	-	$\pm^1/_2$	LSB
ADC0804	$V_{REF}/2$ = 2.500V	-	-	±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm^1/_8$	$\pm^1/_4$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm^1/_{16}$	$\pm^1/_8$	LSB
CONVERTER SPECIFICATIONS	V+ = 5V, -25°C ≤ T_A ≤ +85°C and f_{CLK} = 640kHz, Unless Otherwise Specified				
Total Unadjusted Error					
ADC0802	$V_{REF}/2$ = 2.500V	-	-	$\pm^3/_4$	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full-Scale Reading	-	-	$\pm^3/_4$	LSB
ADC0804	$V_{REF}/2$ = 2.500V	-	-	±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm^1/_8$	$\pm^1/_4$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm^1/_{16}$	$\pm^1/_8$	LSB

Electrical Specifications (Notes 1, 7) **(Continued)**

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CONVERTER SPECIFICATIONS V+ = 5V, -55°C ≤ T_A ≤ +125°C and f_{CLK} = 640kHz, Unless Otherwise Specified					
Total Unadjusted Error					
ADC0802	$V_{REF}/2$ = 2.500V	-	-	±1	LSB
ADC0803	$V_{REF}/2$ Adjusted for Correct Full-Scale Reading	-	-	±1	LSB
$V_{REF}/2$ Input Resistance	Input Resistance at Pin 9	1.0	1.3	-	kΩ
Analog Input Voltage Range	(Note 2)	GND-0.05	-	(V+) + 0.05	V
DC Common-Mode Rejection	Over Analog Input Voltage Range	-	$\pm^1/_8$	$\pm^1/_4$	LSB
Power Supply Sensitivity	V+ = 5V ±10% Over Allowed Input Voltage Range	-	$\pm^1/_8$	$\pm^1/_4$	LSB
AC TIMING SPECIFICATIONS V+ = 5V, and T_A = +25°C, Unless Otherwise Specified					
Clock Frequency, f_{CLK}	V+ = 6V (Note3)	100	640	1280	kHz
	V+ = 5V	100	640	800	kHz
Clock Periods per Conversion (Note 4), t_{CONV}		62	-	73	clocks/conv
Conversion Rate In Free-Running Mode, CR	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0V, f_{CLK} = 640kHz	-	-	8888	conv/s
Width of $\overline{WR}$ Input (Start Pulse Width), $t_{W(WR)I}$	$\overline{CS}$ = 0V (Note 5)	100	-	-	ns
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid), t_{ACC}	C_L = l00pF (Use Bus Driver IC for larger C_L)	-	135	200	ns
Tri-State Control (Delay from Rising Edge of $\overline{RD}$ to HI-Z State), t_{1H}, t_{0H}	C_L = l0pF, R_L= 10k (See Tri-State Test Circuits)	-	125	250	ns
Delay from Falling Edge of $\overline{WR}$ to Reset of $\overline{INTR}$, t_{WI}, t_{RI}		-	300	450	ns
Input Capacitance of Logic Control Inputs, C_{IN}		-	5	-	pF
Tri-State Output Capacitance (Data Buffers), C_{OUT}		-	5	-	pF
DC DIGITAL LEVELS AND DC SPECIFICATIONS V+ = 5V, and $T_{MIN} \le T_A \le T_{MAX}$, Unless Otherwise Specified					
CONTROL INPUTS (Note 6)					
Logic "1" Input Voltage (Except Pin 4 CLK IN), V_{INH}	V+ = 5.25V	2.0	-	V+	V
Logic "0" Input Voltage (Except Pin 4 CLK IN), V_{INL}	V+ = 4.75V	-	-	0.8	V
CLK IN (Pin 4) Positive Going Threshold Voltage, $V+_{CLK}$		2.7	3.1	3.5	V
CLK IN (Pin 4) Negative Going Threshold Voltage, $V-_{CLK}$		1.5	1.8	2.1	V
CLK IN (Pin 4) Hysteresis, V_H		0.6	1.3	2.0	V
Logic "1" Input Current (All Inputs), I_{INHI}	V_{IN} = 5V	-	0.005	1	µA
Logic "0" Input Current (All Inputs), I_{INLO}	V_{IN} = 0V	-1	-0.005	-	µA
Supply Current (Includes Ladder Current), I+	f_{CLK} = 640kHz, T_A = +25°C and $\overline{CS}$ = HI	-	1.3	2.5	mA

Electrical Specifications (Notes 1, 7) **(Continued)**

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DC DIGITAL LEVELS AND DC SPECIFICATIONS V+ = 5V, and $T_{MIN} \le T_A \le T_{MAX}$, Unless Otherwise Specified **(Continued)**					
DATA OUTPUTS AND $\overline{INTR}$					
Logic "0" Output Voltage, V_{OL}	I_O = 1.6mA V+ = 4.75V	-	-	0.4	V
Logic "1" Output Voltage, V_{OH}	I_O = -360µA V+ = 4.75V	2.4	-	-	V
Tri-State Disabled Output Leakage (All Data Buffers), I_{LO}	V_{OUT} = 0V	-3	-	-	µA
	V_{OUT} = 5V	-	-	3	µA
Output Short Circuit Current, I_{SOURCE}	V_{OUT} Short to Gnd T_A = +25°C	4.5	6	-	mA
Output Short Circuit Current, I_{SINK}	V_{OUT} Short to V + T_A = +25°C	9.0	16	-	mA

NOTES:

1. All voltages are measured with respect to GND, unless otherwise specified. The separate AGND point should always be wired to the DGND, being careful to avoid ground loops.
2. For $V_{IN(-)} \ge V_{IN(+)}$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see Block Diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V+ supply. Be careful, during testing at low V+ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct-especially at elevated temperatures, and cause errors for analog inputs near full-scale. As long as the analog V_{IN} does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over temperature variations, initial tolerance and loading.
3. With V+ = 6V, the digital logic interfaces are no longer TTL compatible.
4. With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process.
5. The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input so that timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see Timing Diagrams).
6. CLK IN (pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately.
7. None of these A/Ds requires a zero-adjust. However, if an all zero code is desired for an analog input other than 0.0V, or if a narrow full-scale span exists (for example: 0.5V to 4.0V full-scale) the $V_{IN(-)}$ input can be adjusted to achieve this. See Zero Error on page 13 of this data sheet.

Timing Waveforms

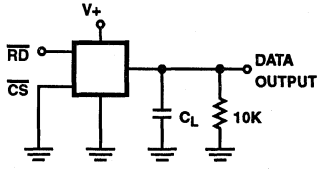


FIGURE 1A. t_{1H}

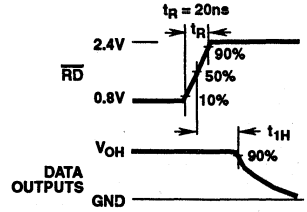


FIGURE 1B. t_{1H}, C_L = 10pF

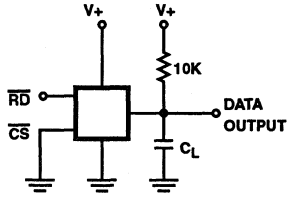


FIGURE 1C. t_{0H}

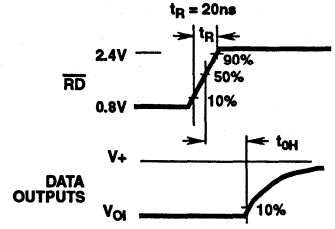


FIGURE 1D. t_{0H}, C_L = 10pF

FIGURE 1. TRI-STATE CIRCUITS AND WAVEFORMS

Typical Performance Curves

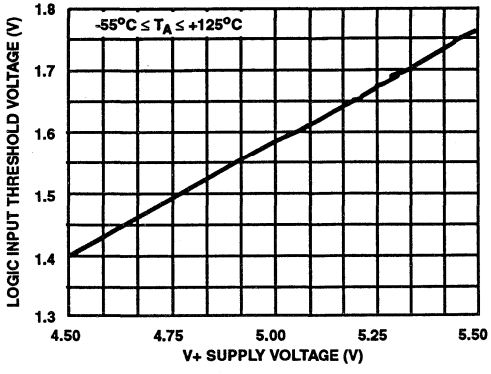


FIGURE 2. LOGIC INPUT THRESHOLD VOLTAGE vs SUPPLY VOLTAGE

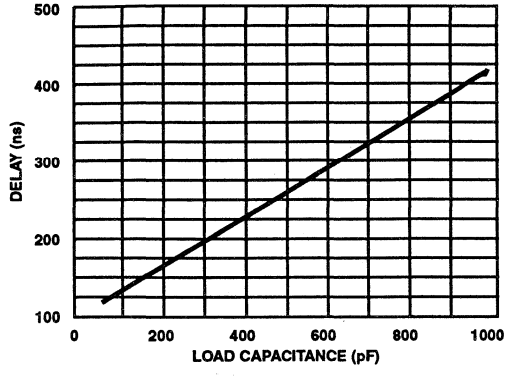


FIGURE 3. DELAY FROM FALLING EDGE OF $\overline{RD}$ TO OUTPUT DATA VALID vs LOAD CAPACITANCE

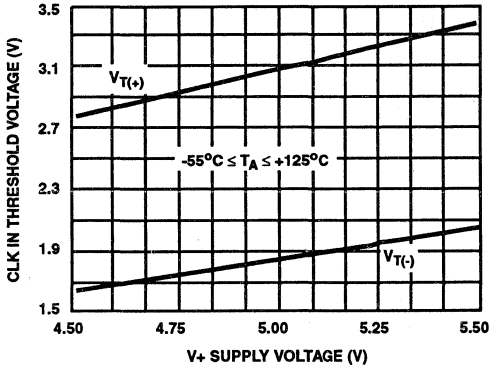


FIGURE 4. CLK IN SCHMITT TRIP LEVELS vs SUPPLY VOLTAGE

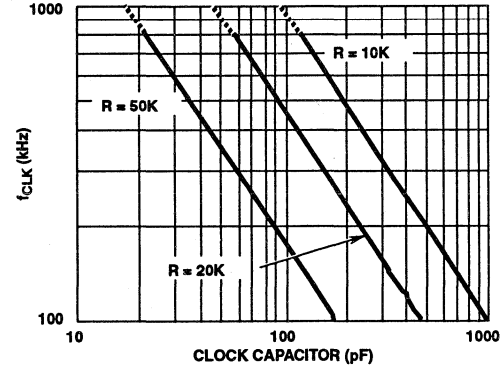


FIGURE 5. f_{CLK} vs CLOCK CAPACITOR

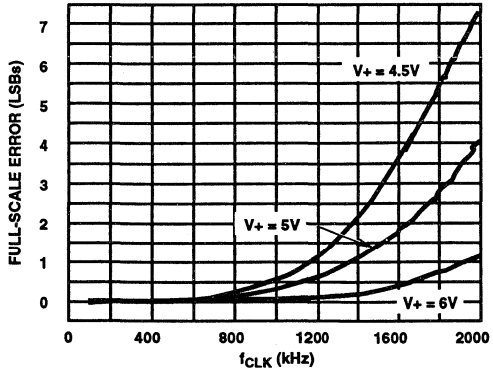


FIGURE 6. FULL SCALE ERROR vs f_{CLK}

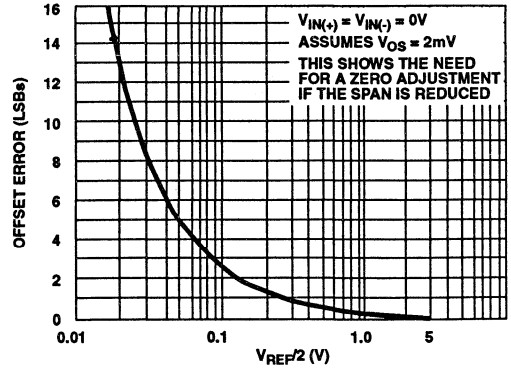


FIGURE 7. EFFECT OF UNADJUSTED OFFSET ERROR

Typical Performance Curves (Continued)

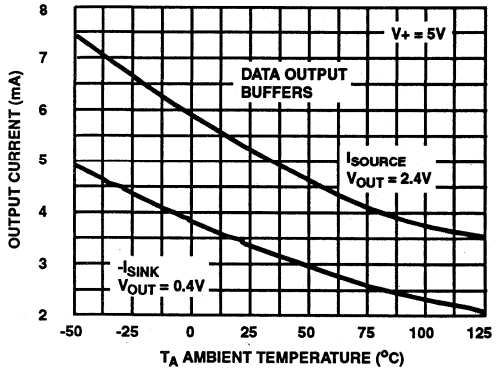


FIGURE 8. OUTPUT CURRENT vs TEMPERATURE

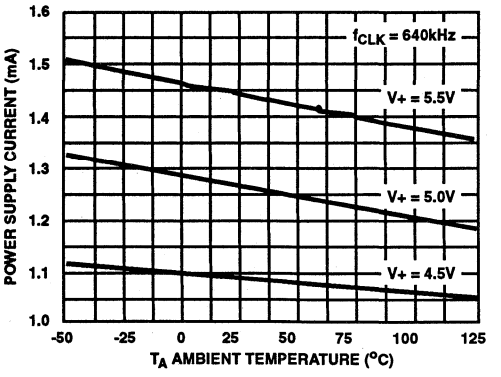


FIGURE 9. POWER SUPPLY CURRENT vs TEMPERATURE

Timing Diagrams

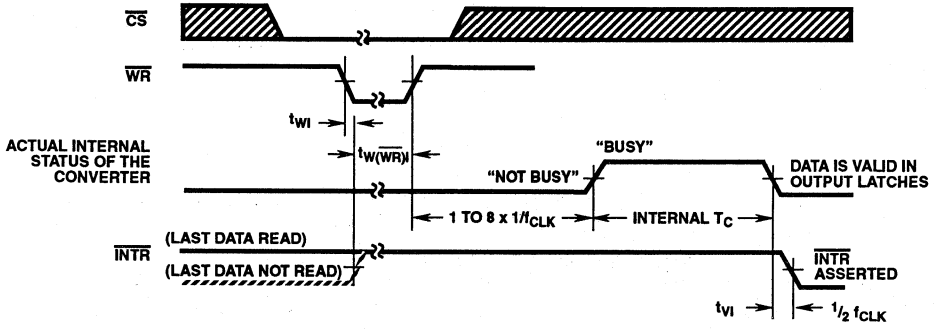


FIGURE 10A. START CONVERSION

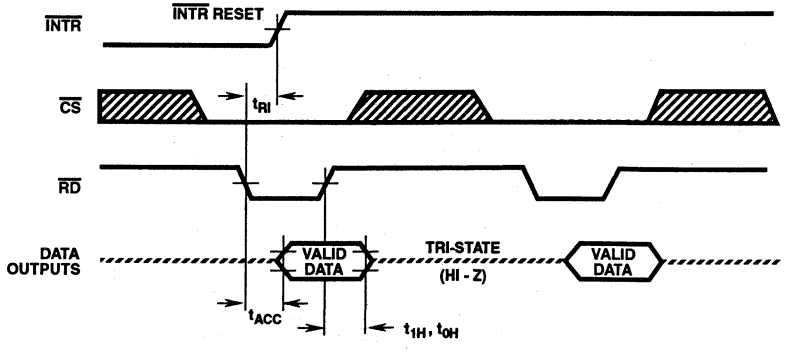


FIGURE 10B. OUTPUT ENABLE AND RESET INTR

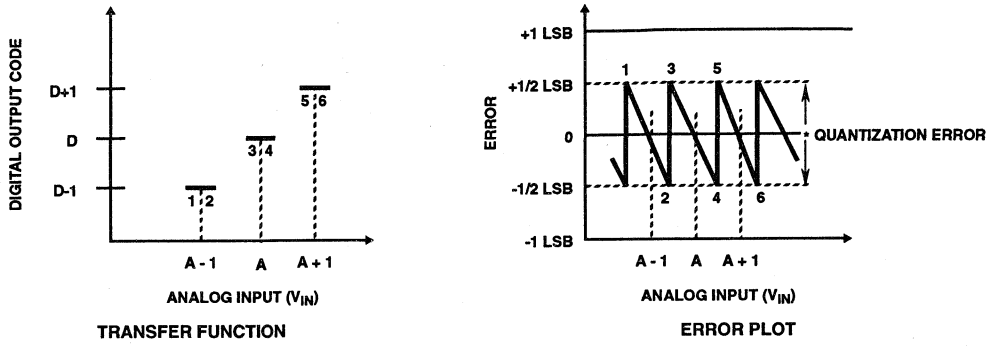


FIGURE 11A. ACCURACY = ±0 LSB; PERFECT A/D

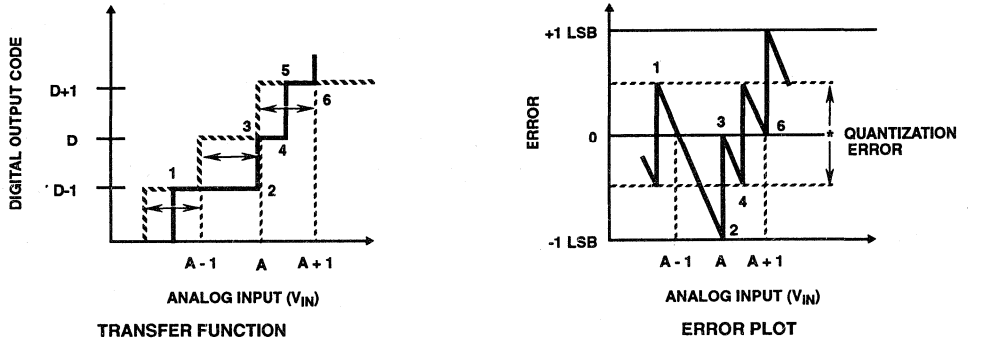


FIGURE 11B. ACCURACY = $\pm^1/_2$ LSB

FIGURE 11. CLARIFYING THE ERROR SPECS OF AN A/D CONVERTER

Understanding A/D Error Specs

A perfect A/D transfer characteristic (staircase wave-form) is shown in Figure 11A. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes which correspond to these inputs are shown as D-1, D, and D+1. For the perfect A/D, not only will center-value (A - 1, A, A + 1, . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located $\pm^1/_2$ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages which extend $\pm^1/_2$ LSB from the ideal center-values. Each tread (the range of analog input voltage which provides the same digital output code) is therefore 1 LSB wide.

The error curve of Figure 11B shows the worst case transfer function for the ADC0802. Here the specification guarantees that if we apply an analog input equal to the LSB analog voltage center-value, the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Notice that the error includes the quantization uncertainty of the A/D. For example, the error at point 1 of Figure 11A is $+^1/_2$ LSB because the digital code appeared $^1/_2$ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude, unless the device has missing codes.

Detailed Description

The functional diagram of the ADC0802 series of A/D converters operates on the successive approximation principle (see Application Notes AN016 and AN020 for a more detailed description of this principle). Analog switches are closed sequentially by successive-approximation logic until the analog differential input voltage $[V_{IN(+)} - V_{IN(-)}]$ matches a voltage derived from a tapped resistor string across the reference voltage. The most significant bit is tested first and after 8 comparisons (64 clock cycles), an 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch.

The normal operation proceeds as follows. On the high-to-low transition of the $\overline{WR}$ input, the internal SAR latches and the shift-register stages are reset, and the $\overline{INTR}$ output will be set high. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition. After the requisite number of

clock pulses to complete the conversion, the $\overline{INTR}$ pin will make a high-to-low transition. This can be used to interrupt a processor, or otherwise signal the availability of a new conversion. A $\overline{RD}$ operation (with $\overline{CS}$ low) will clear the $\overline{INTR}$ line high again. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ = 0. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle. A conversion-in-process can be interrupted by issuing a second start command.

Digital Operation

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flip-flop, DFF1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of DFF1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1"), the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This allows for asynchronous or wide $\overline{CS}$ and $\overline{WR}$ signals.

After the "1" is clocked through the 8-bit shift register (which completes the SAR operation) it appears as the input to DFF2. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the Tri-State output latches. When DFF2 is subsequently clocked, the $\overline{Q}$ output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ output signal.

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the tri-state output latches will be enabled to provide the 8-bit digital outputs.

Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard TTL logic voltage levels. These signals are essentially equivalent to the standard A/D Start and Output Enable control signals, and are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function obtained by an active low pulse at the $\overline{WR}$ input (pin 3). The Output Enable function is achieved by an active low pulse at the $\overline{RD}$ input (pin 2).

Analog Operation

The analog comparisons are performed by a capacitive charge summing circuit. Three capacitors (with precise ratioed values) share a common node with the input to an auto-zeroed comparator. The input capacitor is switched between $V_{IN(+)}$ and $V_{IN(-)}$, while two ratioed reference capacitors are switched between taps on the reference voltage divider string. The net charge corresponds to the weighted difference between the input and the current total value set by the successive approximation register. A correction is made to offset the comparison by $^1/_2$ LSB (see Figure 11A).

Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D gains considerable applications flexibility from the analog differential voltage input. The $V_{IN(-)}$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4mA - 20mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN(+)}$ and $V_{IN(-)}$ is 4 $^1/_2$ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_E(MAX) = (V_P)(2\pi f_{CM})\left[\frac{4.5}{f_{CLK}}\right]$$

where:

ΔV_E is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{CM} is the common-mode frequency

For example, with a 60Hz common-mode frequency, f_{CM}, and a 640kHz A/D clock, f_{CLK}, keeping this error to $^1/_4$ LSB (~5mV) would allow a common-mode voltage, V_P, given by:

$$V_P = \frac{\left[\Delta V_{E(MAX)}(f_{CLK})\right]}{(2\pi f_{CM})(4.5)}$$

or

$$V_P = \frac{(5\times10^{-3})(640\times10^{3})}{(6.28)(60)(4.5)} \cong 1.9V$$

The allowed range of analog input voltage usually places more severe restrictions on input common-mode voltage levels than this.

An analog input voltage with a reduced span and a relatively large zero offset can be easily handled by making use of the differential input (see Reference Voltage Span Adjust).

Analog Input Current

The internal switching action causes displacement currents to flow at the analog inputs. The voltage on the on-chip capacitance to ground is switched through the analog differential input voltage, resulting in proportional currents entering the $V_{IN(+)}$ input and leaving the $V_{IN(-)}$ input. These current transients occur at the leading edge of the internal clocks. They rapidly decay and do not inherently cause errors as the on-chip comparator is strobed at the end of the clock period.

Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN(+)}$ input voltage

at full-scale. For a 640kHz clock frequency with the $V_{IN(+)}$ input at 5V, this DC current is at a maximum of approximately 5μA. Therefore, **bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$** pin for high resistance sources (>1kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the effects of the voltage drop across this input resistance, due to the average value of the input current, can be compensated by a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage at a constant conversion rate.

Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used will not cause errors since the input currents settle out prior to the comparison time. If a low-pass filter is required in the system, use a low-value series resistor (≤ 1kΩ) for a passive RC section or add an op amp RC active low-pass filter. For low-source-resistance applications (≤ 1kΩ), a 0.1μF bypass capacitor at the inputs will minimize EMI due to the series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor (both the R and C are placed outside the feedback loop) from the output of an op amp, if used.

Stray Pickup

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible to minimize stray signal pickup (EMI). Both EMI and undesired digital-clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5kΩ. Larger values of source resistance can cause undesired signal pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate this pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see Analog Input Current). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be compensated by a full-scale adjustment of the A/D (see Full-Scale Adjustment) with the source resistance and input bypass capacitor in place, and the desired conversion rate.

Reference Voltage Span Adjust

For maximum application flexibility, these A/Ds have been designed to accommodate a 5V, 2.5V or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 12.

Notice that the reference voltage for the IC is either $^1/_2$ of the voltage which is applied to the V+ supply pin, or is equal to the voltage which is externally forced at the $V_{REF}/2$ pin. This allows for a pseudo-ratiometric voltage reference using, for the V+ supply, a 5V reference voltage. Alternatively, a voltage less than 2.5V can be applied to the $V_{REF}/2$ input. The internal gain to the $V_{REF}/2$ input is 2 to allow this factor of 2 reduction in the reference voltage.

Such an adjusted reference voltage can accommodate a reduced span or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5V to 3.5V, instead of 0V to 5V, the span would be 3V. With 0.5V applied to the $V_{IN(-)}$ pin to absorb the offset, the reference voltage can be made equal to $^1/_2$ of the 3V span or 1.5V. The A/D now will encode the $V_{IN(+)}$ signal from 0.5V to 3.5V with the 0.5V input corresponding to zero and the 3.5V input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range. The requisite connections are shown in Figure 13. For expanded scale inputs, the circuits of Figures 14 and 15 can be used.

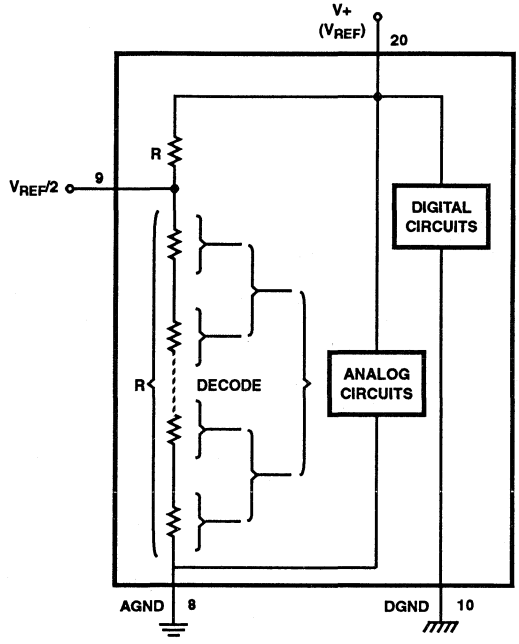


FIGURE 12. THE $V_{REFERENCE}$ DESIGN ON THE IC

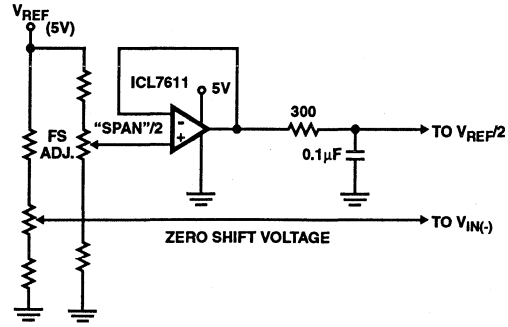


FIGURE 13. OFFSETTING THE ZERO OF THE ADC0802 AND PERFORMING AN INPUT RANGE (SPAN) ADJUSTMENT

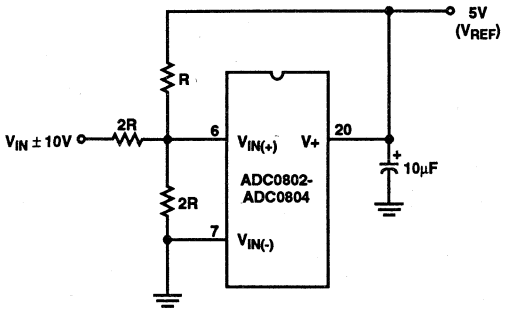


FIGURE 14. HANDLING ±10V ANALOG INPUT RANGE

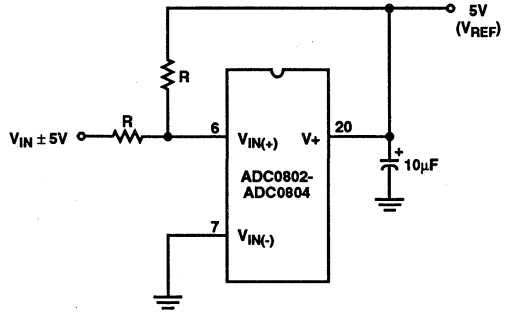


FIGURE 15. HANDLING ±5V ANALOG INPUT RANGE

Reference Accuracy Requirements

The converter can be operated in a pseudo-ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important accuracy factors in the operation of the A/D converter. For $V_{REF}/2$ voltages of 2.5V nominal value, initial errors of ±10mV will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20mV (5V span) to 10mV and 1 LSB at the $V_{REF}/2$ input becomes 5mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive.

Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN(-)}$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN(-)}$ input and applying a small magnitude positive voltage to the $V_{IN(+)}$ input. Zero error is the difference between the actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal $^1/_2$ LSB value ($^1/_2$ LSB = 9.8mV for $V_{REF}/2$ = 2.500V).

Full-Scale Adjust

The full-scale adjustment can be made by applying a differential input voltage which is $1^1/_2$ LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9) for a digital output code which is just changing from 1111 1110 to 1111 1111. When offsetting the zero and using a span-adjusted $V_{REF}/2$ voltage, the full-scale adjustment is made by inputting V_{MIN} to the $V_{IN(-)}$ input of the A/D and applying a voltage to the $V_{IN(+)}$ input which is given by:

$$V_{IN(+)}{}^{f}SADJ = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

V_{MAX} = the high end of the analog input range

and

V_{MIN} = the low end (the offset zero) of the analog range. (Both are ground referenced.)

Clocking Option

The clock for the A/D can be derived from an external source such as the CPU clock or an external RC network can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 16.

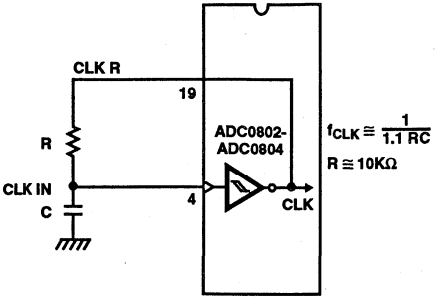


FIGURE 16. SELF-CLOCKING THE A/D

Heavy capacitive or DC loading of the CLK R pin should be avoided as this will disturb normal converter operation. Loads less than 50pF, such as driving up to 7 A/D converter clock inputs from a single CLK R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the CLK R pin (do not use a standard TTL buffer).

Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in progress is not completed. The data from the previous conversion remain in this latch.

Continuous Conversions

In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to insure circuit operation. See Figure 17 for details.

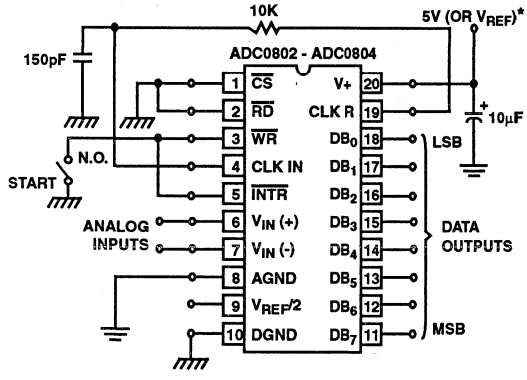


FIGURE 17. FREE-RUNNING CONNECTION

Driving the Data Bus

This CMOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in tri-state (high-impedance mode). Back plane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see Typical Performance Curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock-extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be tri-state buffers (low power Schottky is recommended, such as the 74LS240 series) or special higher-drive-current products which are designed as bus drivers. High-current bipolar bus drivers with PNP inputs are recommended.

Power Supplies

Noise spikes on the V+ supply line can cause conversion errors as the comparator will respond to this noise. A low-inductance tantalum filter capacitor should be used close to the converter V+ pin, and values of 1μF or greater are recommended. If an unregulated voltage is available in the system, a separate 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the V+ supply. An ICL7663 can be used to regulate such a supply from an input as low as 5.2V.

Wiring and Hook-Up Precautions

Standard digital wire-wrap sockets are not satisfactory for breadboarding with this A/D converter. Sockets on PC boards can be used. All logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup; therefore, shielded leads may be necessary in many applications.

A single-point analog ground should be used which is separate from the logic ground points. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of $^1/_4$ LSB can usually be traced to improper board layout and wiring (see Zero Error for measurement). Further information can be found in Application Note AN018.

Testing the A/D Converter

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 18.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560V and a V+ supply voltage of 5.12V should be used. This provides an LSB value of 20mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090V (5.120 - $1^1/_2$ LSB) should be applied to the $V_{IN(+)}$ pin with the $V_{IN(-)}$ pin grounded. The value of the $V_{REF}/2$ input voltage should be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital-output LED display can be decoded by dividing the 8 bits into 2 hex characters, one with the 4 most-significant bits (MS) and one with the 4 least-significant bits (LS). The output is then interpreted as a sum of fractions times the full-scale voltage:

$$V_{OUT} = \left(\frac{MS}{16} + \frac{LS}{256}\right)(5.12)\,V.$$

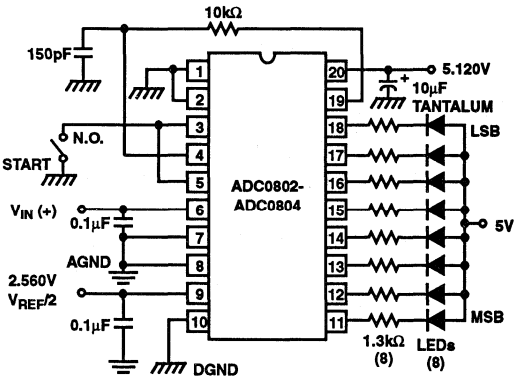


FIGURE 18. BASIC TESTER FOR THE A/D

For example, for an output LED display of 1011 0110, the MS character is hex B (decimal 11) and the LS character is hex (and decimal) 6, so

$$V_{OUT} = (\frac{11}{16} + \frac{6}{256})(5.12) = 3.64V$$

Figures 19 and 20 show more sophisticated test circuits.

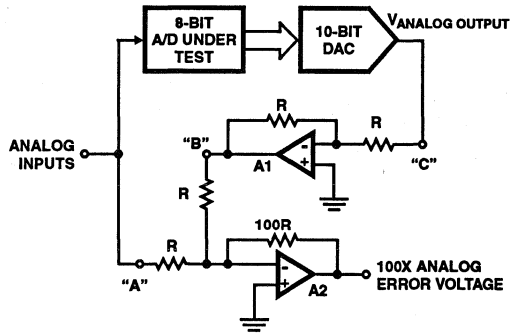


FIGURE 19. A/D TESTER WITH ANALOG ERROR OUTPUT. THIS CIRCUIT CAN BE USED TO GENERATE "ERROR PLOTS" OF FIGURE 11.

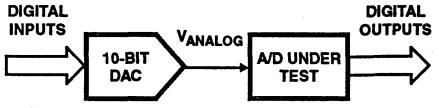


FIGURE 20. BASIC "DIGITAL" A/D TESTER

Typical Applications

Interfacing 8080/85 or Z-80 Microprocessors

This converter has been designed to directly interface with 8080/85 or Z-80 Microprocessors. The tri-state output capability of the A/D eliminates the need for a peripheral interface device, although address decoding is still required to generate the appropriate $\overline{CS}$ for the converter. The A/D can be mapped into memory space (using standard memory-address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/OR}$ and $\overline{I/OW}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15, since they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder, but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. See AN020 for more discussion of memory-mapped vs I/O-mapped interfaces. An example of an A/D in I/O space is shown in Figure 21.

The standard control-bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D, since the bus timing requirements, to allow both starting the converter, and outputting the data onto the data bus, are met. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100pF.

It is useful to note that in systems where the A/D converter is 1 of 8 or fewer I/O-mapped devices, no address-decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs, one for each I/O device.

Interfacing the Z-80 and 8085

The Z-80 and 8085 control buses are slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals have to be combined with the generalized strobes to provide the appropriate signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 22. By using $\overline{MREQ}$ in place of $\overline{IORQ}$, a memory-mapped configuration results.

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

The 8085 also provides a generalized $\overline{RD}$ and $\overline{WR}$ strobe, with an IO/$\overline{M}$ line to distinguish I/O and memory requests. The circuit of Figure 22 can again be used, with IO/$\overline{M}$ in place of $\overline{IORQ}$ for a memory-mapped interface, and an extra inverter (or the logic equivalent) to provide $\overline{IO}$/M for an I/O-mapped connection.

Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived from the $\phi 2$ clock. All I/O devices are memory-mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 23 shows an interface schematic where the A/D is memory-mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using $^1/_2$ DM8092. Note that in many 6800 systems, an already decoded $\overline{4/5}$ line is brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HEX ADDR: 4XXX or 5XXX.

In Figure 24 the ADC0802 series is interfaced to the MC6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory-mapped in the MC6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

Application Notes

Some applications bulletins that may be found useful are listed here:

AN016 "Selecting A/D Converters"

AN018 "Do's and Don'ts of Applying A/D Converters"

AN020 "A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing"

AN030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors"

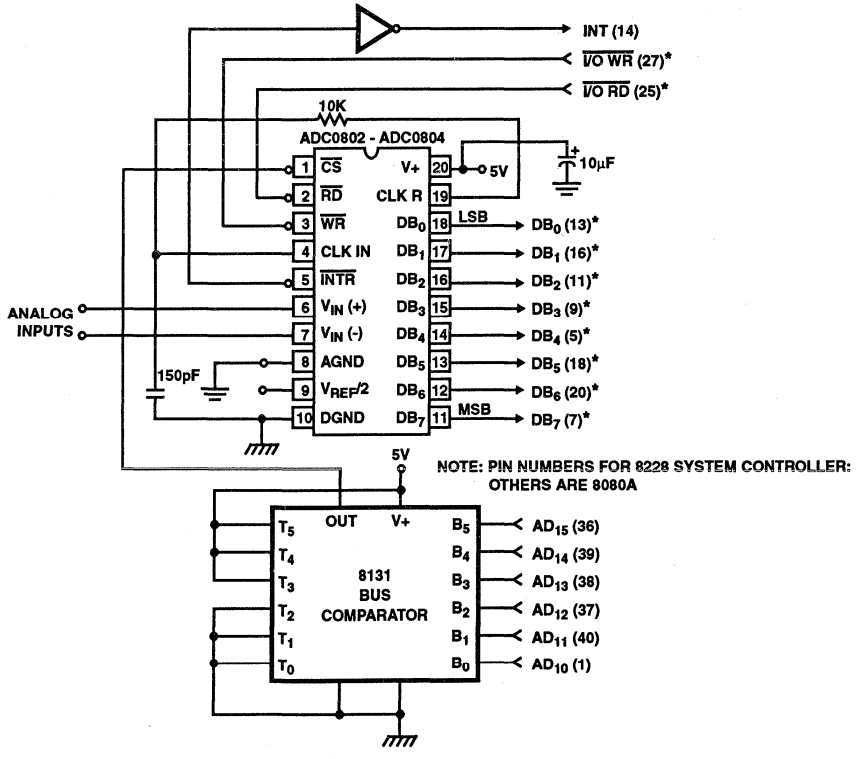


FIGURE 21. ADC0802 TO 8080A CPU INTERFACE

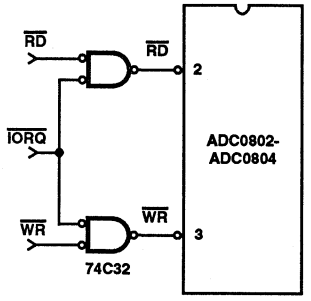
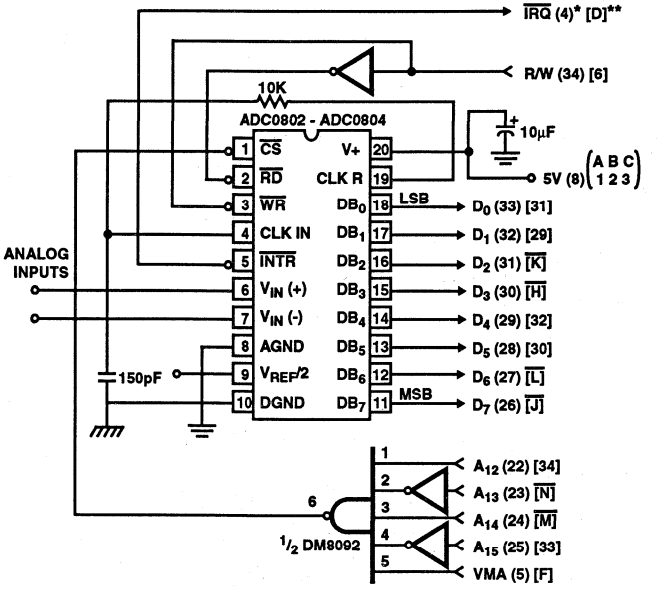


FIGURE 22. MAPPING THE A/D AS AN I/O DEVICE FOR USE WITH THE Z-80 CPU



* NUMBERS IN PARENTHESES REFER TO MC6800 CPU PINOUT.
** NUMBERS OR LETTERS IN BRACKETS REFER TO STANDARD MC6800 SYSTEM COMMON BUS CODE.

FIGURE 23. ADC0802 TO MC6800 CPU INTERFACE

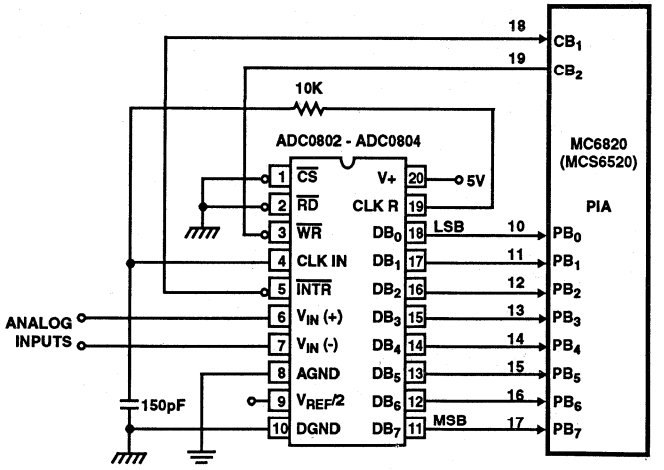


FIGURE 24. ADC0802 TO MC6820 PIA INTERFACE

Die Characteristics

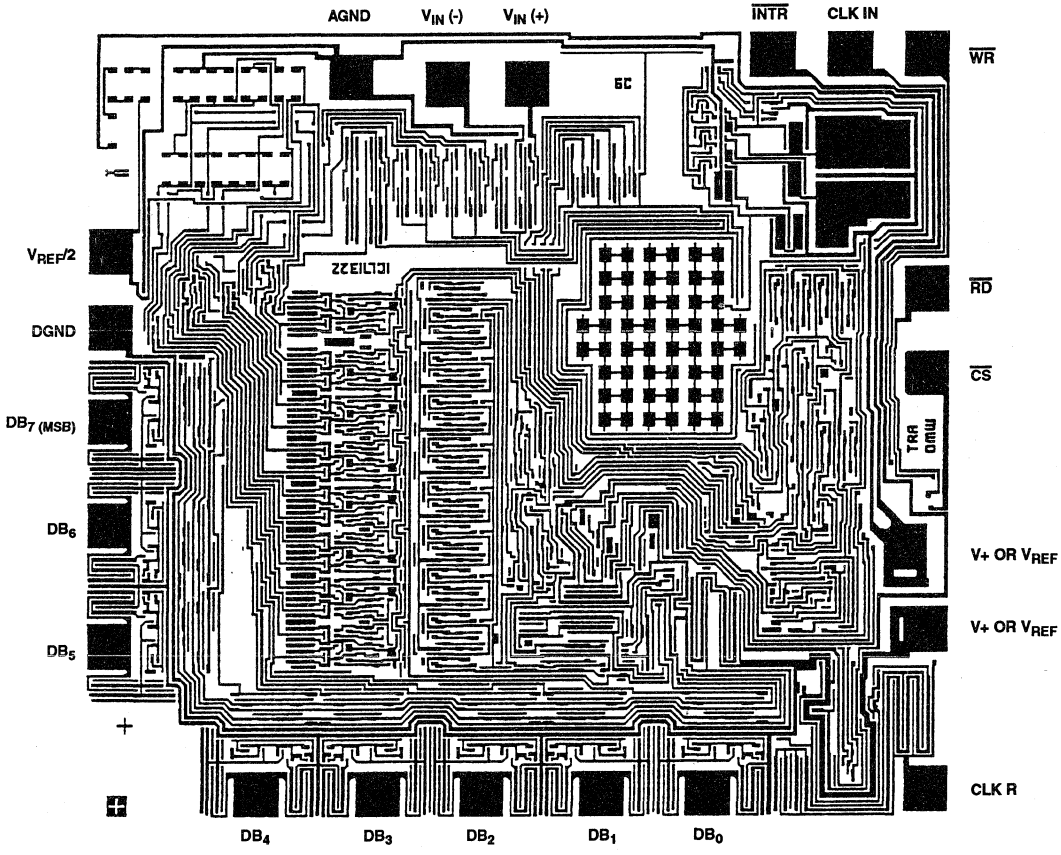
DIE DIMENSIONS:
(101 x 93mils) x 525 x 25µm

METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride over Silox
Nitride Thickness: 8kÅ
Silox Thickness: 7kÅ

Metallization Mask Layout

ADC0802, ADC0803, ADC0804



CA3310, CA3310A

CMOS 10-Bit A/D Converter with Internal Track and Hold

December 1993

Features

- CMOS Low Power (15mW Typ.)
- Single Supply Voltage (3V to 6V)
- 13μs Conversion Time
- Built-In Track and Hold
- Rail-to-Rail Input Range
- Latched Tri-state Output Drivers
- Microprocessor-Compatible Control Lines
- Internal or External Clock

Applications

- Fast, No-Droop, Sample and Hold
- Voice Grade Digital Audio
- DSP Modems
- Remote Low Power Data Acquisition Systems
- μP Controlled Systems

Description

The Harris CA3310 is a fast, low power, 10-bit successive approximation analog-to-digital converter, with microprocessor-compatible outputs. It uses only a single 3V to 6V supply and typically draws just 3mA when operating at 5V. It can accept full rail-to-rail input signals, and features a built-in track and hold. The track and hold will follow high bandwidth input signals, as it has only a 100ns (typical) input time constant.

The ten data outputs feature full high-speed CMOS tri-state bus driver capability, and are latched and held through a full conversion cycle. Separate 8 MSB and 2 LSB enables, a data ready flag, and conversion start and ready reset inputs complete the microprocessor interface.

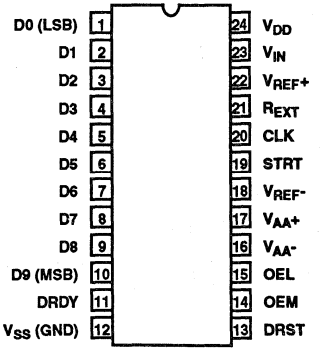
An internal, adjustable clock is provided and is available as an output. The clock may also be driven from an external source.

Ordering Information

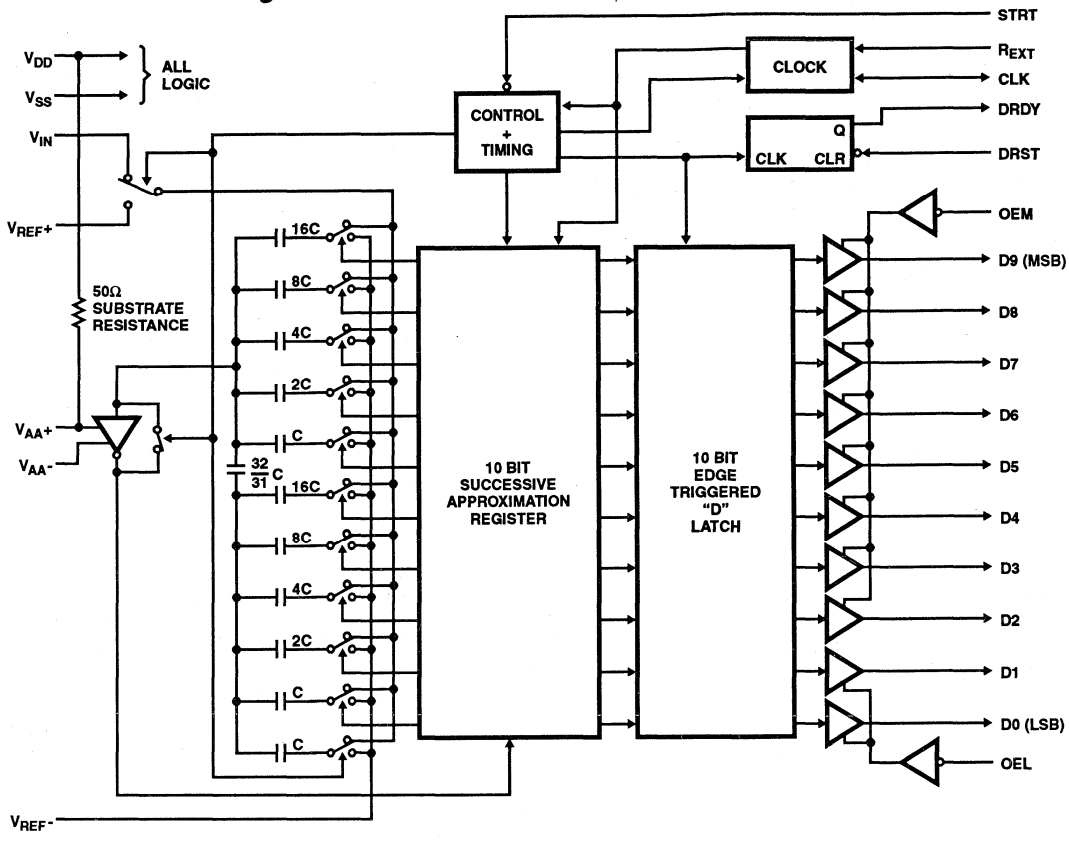
PART NUMBER	LINEARITY (INL, DNL)	TEMPERATURE RANGE	PACKAGE
CA3310E	±0.75 LSB	-40°C to +85°C	24 Lead Plastic DIP
CA3310AE	±0.5 LSB	-40°C to +85°C	24 Lead Plastic DIP
CA3310M	±0.75 LSB	-40°C to +85°C	24 Lead Plastic SOIC
CA3310AM	±0.5 LSB	-40°C to +85°C	24 Lead Plastic SOIC
CA3310D	±0.75 LSB	-55°C to +125°C	24 Lead Ceramic DIP
CA3310AD	±0.5 LSB	-55°C to +125°C	24 Lead Ceramic DIP

Pinout

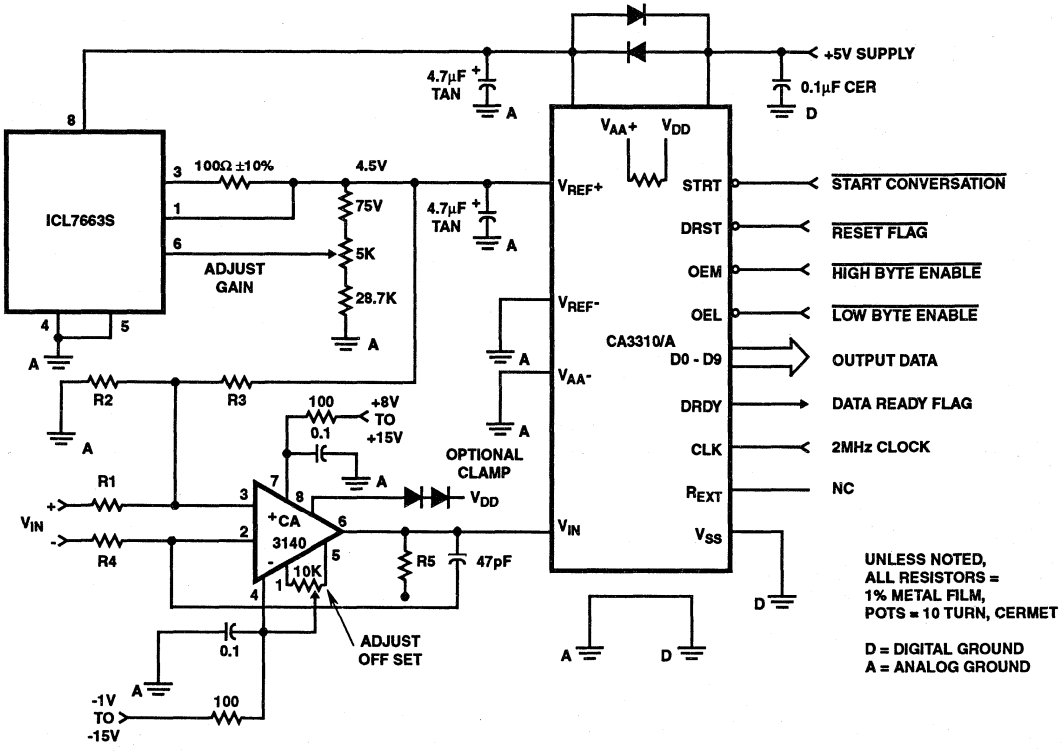
CA3310, CA3310A
(PDIP, CERAMIC DIP, SOIC)
TOP VIEW



Functional Block Diagram



Typical Application Schematics



INPUT RANGE	R1	R2	R3	R4	R5
0V TO 2.5V	4.99K	9.09K	OPEN	4.99K	9.09K
0V TO 5V	4.99K	4.53K	OPEN	4.99K	4.53K
0V TO 10V	10K	4.53K	OPEN	10K	4.53K
-2.5V TO +2.5V	4.99K	9.09K	9.09K	4.99K	4.53K
-5V TO +5V	10K	9.09K	9.09K	10K	4.53K

Absolute Maximum Ratings

Digital Supply Voltage V_{DD} ..... V_{SS} -0.5V to V_{SS} +7V
Analog Supply Voltage (V_{AA}+) ..... V_{DD} ±0.5V
Any Other Terminal ..... V_{SS} -0.5V to V_{DD} + 0.5V
DC Input Current or Output (Protection Diode) Current ..... ±20mA
DC Output Drain Current, per Output ..... ±35mA
Total DC Supply or Ground Current ..... ±70mA
Operating Temperature Range (T_A)
Package Type D ..... -55°C to +125°C
Package Type E, M ..... -40°C to +85°C
Storage Temperature (T_{STG}) ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +265°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic Package	75°C/W	-
Ceramic DIP Package	58°C/W	11C/W
SOIC Package	75°C/W	-

Junction Temperature
Plastic Package ..... +150°C
Sidebrazed Package ..... +175°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V_{DD} = V_{AA}+ = 5V, V_{REF}+ = 4.608V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = External 1MHz (Unless Otherwise Specified.)

PARAMETER		TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
ACCURACY: SEE TEXT FOR DEFINITIONS						
Resolution			10	-	-	Bits
Differential Linearity Error	CA3310		-	±0.5	±0.75	LSB
	CA3310A		-	±0.25	±0.5	LSB
Integral Linearity Error	CA3310		-	±0.5	±0.75	LSB
	CA3310A		-	±0.25	±0.5	LSB
Gain Error	CA3310		-	±0.25	±0.5	LSB
	CA3310A		-	-	±0.25	LSB
Offset Error	CA3310		-	±0.25	±0.5	LSB
	CA3310A		-	-	±0.25	LSB
ANALOG OUTPUT						
Input Resistance		In Series with Input Sample Capacitors	-	330	-	Ω
Input Capacitance		During Sample State	-	300	-	pF
Input Capacitance		During Hold State	-	20	-	pF
Input Current		At V_{IN} = V_{REF}+ = 5V	-	-	+300	µA
		At V_{IN} = V_{REF}- = 0V	-	-	-100	µA
Static Input Current		STRT = V+, CLK = V+ At V_{IN} = V_{REF}+ = 5V	-	-	1	µA
		At V_{IN} = V_{REF}- = 0V	-	-	-1	µA
Input + Full-Scale Range		(Note 2)	V_{REF}- +1	-	V_{DD} +0.3	V
Input - Full-Scale Range		(Note 2)	V_{SS} -0.3	-	V_{REF}+ -1	V
Input Bandwidth		From Input RC Time Constant	-	1.5	-	MHz
DIGITAL INPUTS: DRST, OEL, OEM, STRT, CLK						
High-Level Input Voltage		Over V_{DD} = 3V to 6V (Note 2)	70	-	-	% of V_{DD}

Electrical Specifications T_A = +25°C, V_{DD} = V_{AA}+ = 5V, V_{REF}+ = 4.608V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = External 1MHz (Unless Otherwise Specified.) **(Continued)**

PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Low-Level Input Voltage	Over V_{DD} = 3V to 6V (Note 2)	-	-	30	% of V_{DD}
Input Leakage Current	Except CLK	-	-	±1	µA
Input Capacitance	(Note 2)	-	-	10	pF
Input Current	CLK Only (Note 2)	-	-	±400	µA
DIGITAL OUTPUTS: D0 - D9, DRDY					
High-Level Output Voltage	I_{SOURCE} = -4mA	4.6	-	-	V
Low-Level Output Voltage	I_{SINK} = 6mA	-	-	0.4	V
Tri-state Leakage	Except DRDY	-	-	±1	µA
Output Capacitance	Except DRDY (Note 2)	-	-	20	pF
CLK OUTPUT					
High-Level Output Voltage	I_{SOURCE} = 100µA (Note 2)	4	-	-	V
Low-Level Output Voltage	I_{SINK} = 100µA (Note 2)	-	-	1	V
TIMING					
Clock Frequency	Internal, CLK and R_{EXT} Open	200	300	400	kHz
	Internal, CLK Shorted to R_{EXT}	600	800	1000	kHz
	External, Applied to CLK: (Note 2) Max.	-	4	2	MHz
	Min.	100	10	-	kHz
Clock Pulse Width, T_{LOW}, T_{HIGH}	External, Applied to CLK: See figure 1 (Note 2)	100	-	-	ns
Conversion Time		13	-	-	µs
Aperture Delay, T_D APR	See Figure 1	-	100	-	ns
Clock to Data Ready Delay, T_{D1} DRDY	See Figure 1	-	150	-	ns
Clock to Data Ready Delay, T_{D2} DRDY	See Figure 1	-	250	-	ns
Clock to Data Delay, T_D Data	See Figure 1	-	200	-	ns
Start Removal Time, T_R STRT	See Figures 3 and 4 (Note 1)	-	-120	-	ns
Start Setup Time, T_{SU} STRT	See Figure 4	-	160	-	ns
Start Pulse Width, T_W STRT	See Figures 3 and 4	-	10	-	ns
Start to Data Ready Delay, T_{D3} DRDY	See Figures 3 and 4	-	170	-	ns
Clock Delay from Start, T_D CLK	See Figure 3	-	200	-	ns
Ready Reset Removal Time, T_R DRST	See Figure 50 (Note 1)	-	-80	-	ns
Ready Reset Pulse Width, T_W DRST	See Figure 5	-	10	-	ns
Ready Reset to Data Ready Delay, T_{D4} DRDY	See Figure 5	-	35	-	ns
Output Enable Delay, T_{EN}	See Figure 2	-	40	-	ns

Electrical Specifications T_A = +25°C, V_{DD} = V_{AA}+ = 5V, V_{REF}+ = 4.608V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = External 1MHz (Unless Otherwise Specified.) **(Continued)**

PARAMETER	TEST CONDITIONS	LIMITS			UNITS
		MIN	TYP	MAX	
Output Disable Delay, T_{DIS}	See Figure 2	-	50	-	ns
SUPPLIES					
Supply Operating Range, V_{DD} or V_{AA}	(Note 2)	3	-	6	V
Supply Current, I_{DD} + I_{AA}	See Figures 14, 15	-	3	8	mA
Supply Standby Current	Clock Stopped During Cycle 1	-	3.5	-	mA
Analog Supply Rejection	At 120Hz, See Figure 13	-	25	-	mV/V
Reference Input Current	See Figure 10	-	160	-	µA
TEMPERATURE DEPENDENCY					
Offset Drift	At 0 to 1 Code Transition	-	-4	-	µV/°C
Gain Drift	At 1022 to 1023 Code Transition	-	-6	-	µV/°C
Internal Clock Speed	See Figure 7	-	-0.5	-	%/°C

NOTE:

1. A (-) removal time means the signal can be removed after the reference signal.
2. Parameter not tested, but guaranteed by design or characterization.

Timing Diagrams

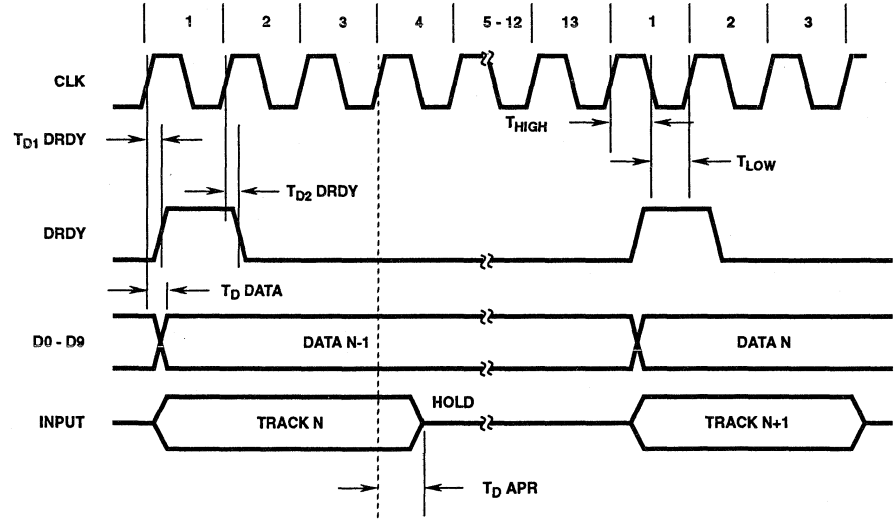


FIGURE 1. FREE RUNNING, STRT TIED LOW, DRST TIED HIGH

Timing Diagrams (Continued)

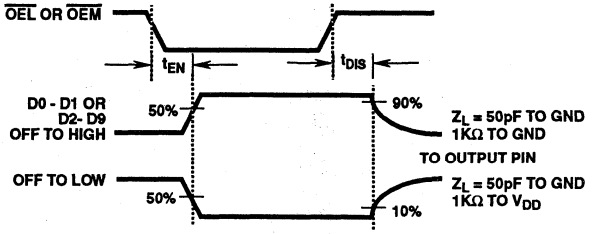


FIGURE 2. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

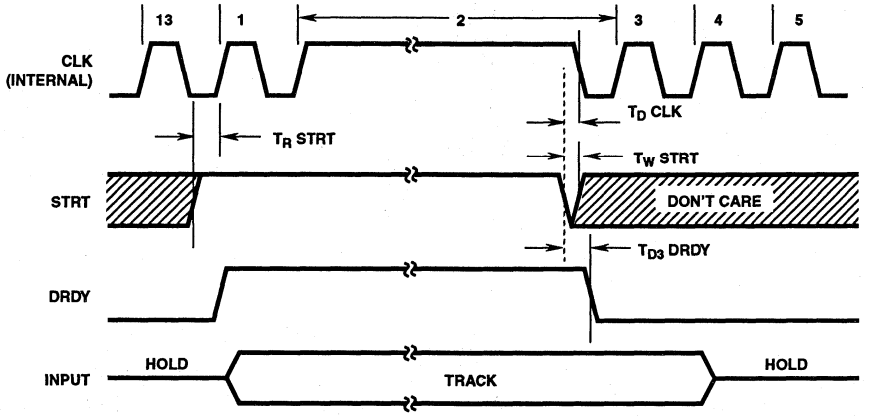


FIGURE 3. STRT PULSED LOW, DRST TIED HIGH, INTERNAL CLOCK

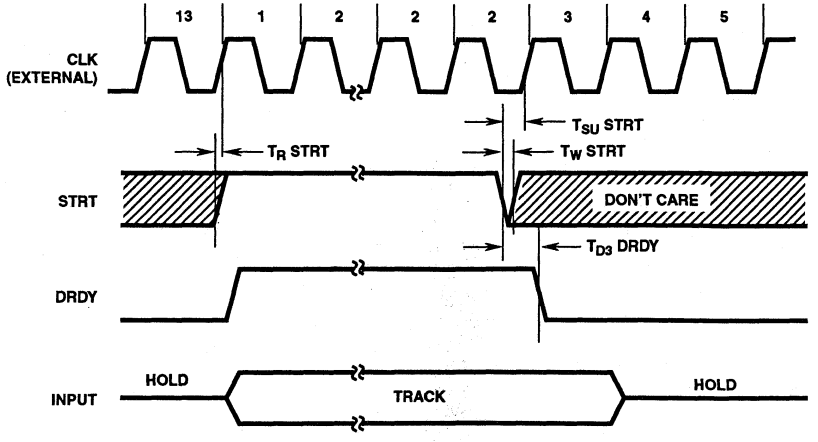


FIGURE 4. STRT PULSED LOW, DRST TIED HIGH, EXTERNAL CLOCK

Timing Diagrams (Continued)

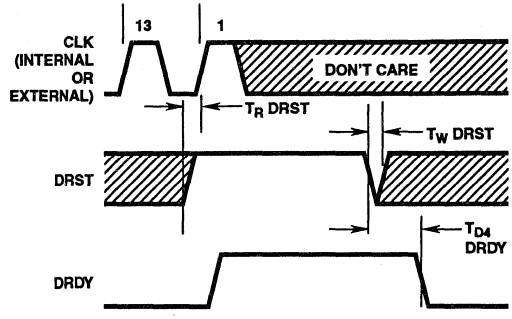


FIGURE 5. DRST PULSED LOW, STRT TIED HIGH

Typical Performances Curves

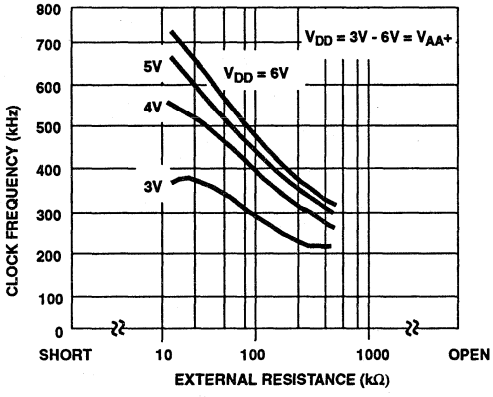


FIGURE 6. INTERNAL CLOCK FREQUENCY vs EXTERNAL RESISTANCE

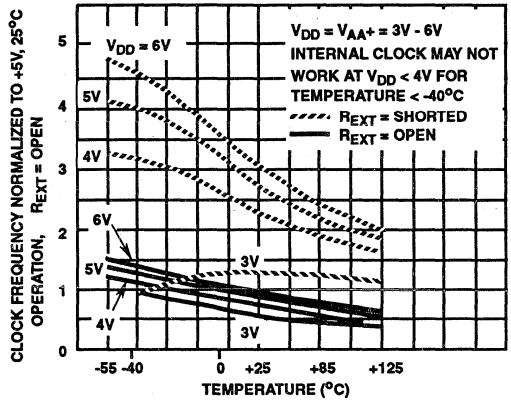


FIGURE 7. INTERNAL CLOCK FREQUENCY vs TERMPERATURE AND SUPPLY VOLTAGE

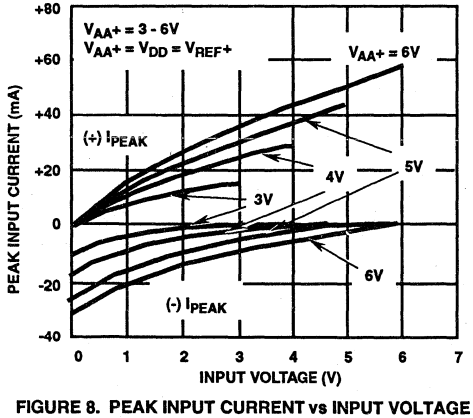


FIGURE 8. PEAK INPUT CURRENT vs INPUT VOLTAGE

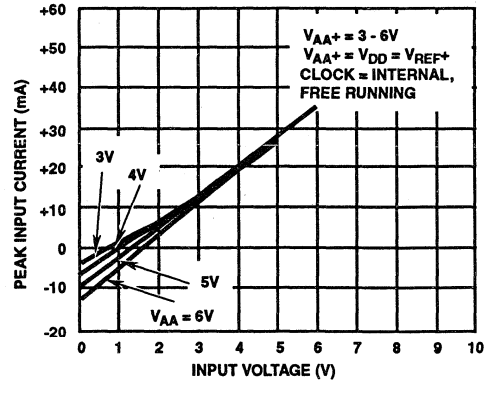


FIGURE 9. AVERAGE INPUT CURRENT vs INPUT VOLTAGE

Typical Performances Curves (Continued)

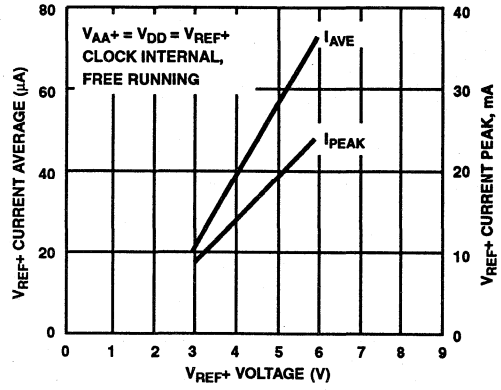


FIGURE 10. $V_{REF}+$ CURRENT vs $V_{REF}+$ VOLTAGE

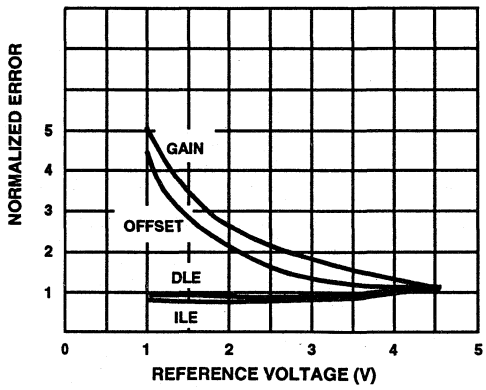


FIGURE 11. NORMALIZED GAIN, OFFSET, INTEGRAL AND DIFFERENTIAL LINEARITY ERRORS vs REFERENCE VOLTAGE

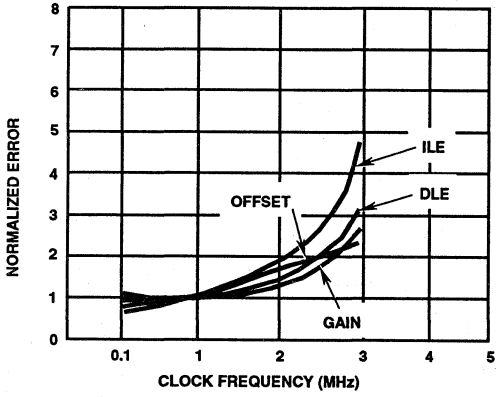


FIGURE 12. NORMALIZED GAIN, OFFSET, INTEGRAL AND DIFFERENTIAL LINEARITY ERRORS vs CLOCK SPEED

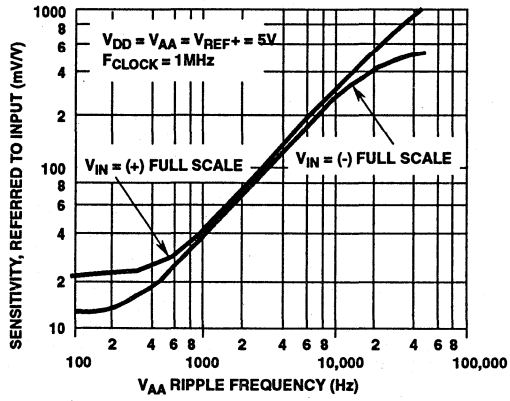


FIGURE 13. V_{AA} SUPPLY SENSITIVITY

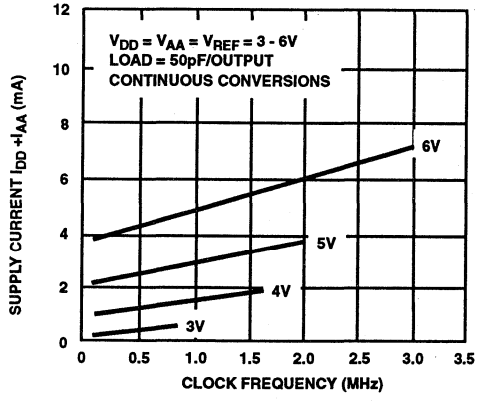


FIGURE 14. SUPPLY CURRENT vs CLOCK FREQUENCY

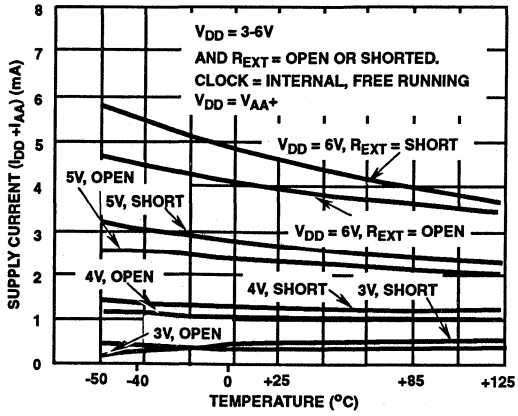


FIGURE 15. SUPPLY CURRENT vs TEMPERATURE

TABLE 1. PIN DESCRIPTION

PIN NUMBER	NAME	DESCRIPTION
1-10	D0 - D9	Tri-state outputs for data bits representing 2^0 (LSB) through 2^9 (MSB).
11	DRDY	Output flag signifying new data is available. Goes high at end of clock period 13, goes low when new conversion started. Also reset asynchronously by DRST.
12	V_{SS}	Digital ground.
13	DRST	Active low input, resets DRDY.
14	OEM	Active low input, tri-state enable of D2 - D9.
15	OEL	Active low input, tri-state enable of D0, D1.
16	V_{AA}-	Analog ground.
17	V_{AA}+	Analog + supply.
18	V_{REF}-	Reference input voltage, sets 0 code (-) end of input range.
19	STRT	Active low start conversion input. Recognized after end of clock period 13.
20	CLK	Clock input or output. Conversion functions are synchronous to high-going edge.
21	R_{EXT}	Clock adjust input when using internal clock.
22	V_{REF}+	Reference input voltage, set 1023 code (+) end of input range.
23	V_{IN}	Analog input.
24	V_{DD}	Digital + supply.

TABLE 2. OUTPUT CODES

CODE DESCRIPTION $LSB = \frac{(V_{REF+} - V_{REF-})}{1024}$	INPUT VOLTAGE (NOTE 1) $(V_{REF+} - V_{REF-}) = 4.608V$ (V)	BINARY OUTPUT CODE MSB D9	D8	D7	D6	D5	D4	D3	D2	D1	LSB D0	DECIMAL COUNT
Zero	0.000	0	0	0	0	0	0	0	0	0	0	0
1 LSB	0.0045	0	0	0	0	0	0	0	0	0	1	1
$^1/_4$ (V_{REF}+ - V_{REF}-)	1.152	0	1	0	0	0	0	0	0	0	0	256
$^1/_2$ (V_{REF}+ - V_{REF}-)	2.304	1	0	0	0	0	0	0	0	0	0	512
$^3/_4$ (V_{REF}+ - V_{REF}-)	3.456	1	1	0	0	0	0	0	0	0	0	768
(V_{REF}+ - V_{REF}-) - 1 LSB	4.6035	1	1	1	1	1	1	1	1	1	1	1023

NOTE:

1. The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Device Operation

The CA3310 is a CMOS 10-bit analog-to-digital converter that uses capacitor-charge balancing to successively approximate the analog input. A binarily weighted capacitor network forms the D-to-A "Heart" of the device. See the Functional Diagram of the CA3310.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, $V_{REF}+$ or $V_{REF}-$.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input. The comparator is being auto-balanced at its trip point, thus setting the voltage at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input, the one representing the MSB (D9) is connected to the $V_{REF}+$ terminal, and the remaining capacitors to $V_{REF}-$. The capacitor-common node, after the charges balance out, will represent whether the input was above or below $^1/_2$ of ($V_{REF}+ - V_{REF}-$).

At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to $V_{REF}+$ (if the comparator was high) or returned to $V_{REF}-$. This allows the next comparison to be at either $^3/_4$ or $^1/_4$ of ($V_{REF}+ - V_{REF}-$).

At the end of periods 5 through 12, capacitors representing the next to MSB (D8) through the next to LSB (D1) are tested, the result stored, and each capacitor either left at $V_{REF}+$ or at $V_{REF}-$.

At the end of the 13th period, when the LSB (D0) capacitor is tested, D0 and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data-ready output goes active. The conversion cycle is now complete.

Clock

The CA3310 can operate either from its internal clock or from one externally supplied. The CLK pin functions either as the clock output or input. All converter functions are synchronous with the rising edge of the clock signal.

Figure 16 shows the configuration of the internal clock. The clock output drive is low power: if used as an output, it should not have more than 1 CMOS gate load applied, and wiring capacitance should be kept to a minimum.

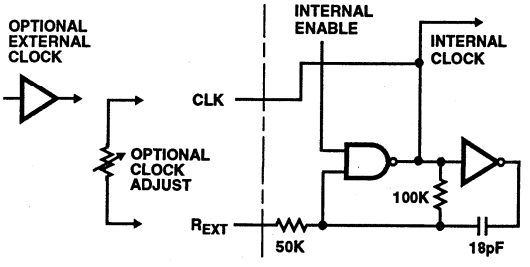


FIGURE 16. CLOCK CIRCUITRY

The R_{EXT} pin allows adjusting of the internal clock frequency by connecting a resistor between R_{EXT} and CLK. Figure 6 shows the typical relationship between the resistor and clock speed, while Figure 7 shows clock speed versus temperature and supply voltage.

The internal clock will shut down if the A/D is not restarted after a conversion. This is described under Control Timing. The clock could also be shut down with an open collector driver applied to the CLK pin. This should only be done during the sample portion (the first three periods) of a conversion cycle, and might be useful for using the device as a digital sample and hold: this is described further under Applications.

If an external clock is supplied to the CLK pin, it must have sufficient drive to overcome the internal clock source. The external clock can be shut off, but again only during the sample portion of a conversion cycle. At other times, it must be above the minimum frequency shown in the specifications.

If the internal or external clock was shut off during the conversion time (clock cycles 4 through 13) of the A/D, the output might be invalid due to balancing capacitor droop.

An external clock must also meet the minimum T_{LOW} and T_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

Control Signals

The CA3310 may be synchronized from an external source by using the STRT (Start Conversion) input to initiate conversions, or if STRT is tied low, may be allowed to free-run. In the free-running mode, illustrated in Figure 1, each conversion takes 13 clock periods.

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by T_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by T_{D1} DRDY) after the start of clock period 1, and returns low (specified by T_{D2} DRDY) after the start of clock period 2. DRDY may also be asynchronously reset by a low on DRST (to be discussed later).

If the output data is to be latched externally by the DRDY signal, the trailing edge of DRDY should be used: there is no guaranteed set-up time to the leading edge.

The 10 output data bits are available in parallel on three-state bus driver outputs. When low, the OEM input enables the most significant byte (D2 through D9) while the OEL input enables the two least significant bits (D0, D1). TEN and T_{DIS} specify the output enable and disable times, respectively. See Figure 2.

When the STRT input is used to initiate conversions, operation is slightly different depending on whether an internal or external clock is used.

Figure 3 illustrates operation with an internal clock. If the STRT signal is removed (at least T_R STRT) before clock period 1, and is not reapplied during that period, the clock will shut off after entering period 2. The input will continue to track the DRDY output will remain high during this time.

A low signal applied to STRT (at least T_W STRT wide) can now initiate a new conversion. The STRT signal (after a delay of T_{D3} DRDY) will cause the DRDY flag to drop, and (after a delay of T_D CLK) cause the clock to restart.

Depending on how long the clock was shut off, the low portion of clock period 2 may be longer than during the remaining cycles.

The input will continue to track until the end of period 3, the same as when free-running.

Figure 4 illustrates the same operation as above, but with an external clock. If STRT is removed (at least T_R STRT) before clock period 1, and not reapplied during that period, the clock will continue to cycle in period 2. A low signal applied to STRT will drop the DRDY flag as before, and with the first positive-going clock edge that meets the T_{SU} STRT set-up time, the converter will continue with clock period 3.

The DRDY flag output, as described previously, goes active at the start of period 1, and drops at the start of period 2 or upon a new STRT command, whichever is later. It may also be controlled with the DRST (Data Ready Reset) input. Figure 5 depicts this operation.

DRST must be removed (at least T_R DRST) before the start of period 1 to allow DRDY to go high. A low level on DRST (at least T_W DRST wide) will (after a delay of T_{D4} DRDY) drop DRDY.

Analog Input

The analog input pin is a predominantly capacitive load that changes between the track and hold periods of a conversion cycle. During hold, clock period 4 through 13, the input loading is leakage and stray capacitance, typically less than 0.1µA and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the charge by the end of the tracking period. The amount of charge is dependent on supply and input voltages. Figure 8 shows typical peak input currents for various supply and input voltages, while Figure 9 shows typical average input currents. The average current is also proportional to clock frequency, and should be scaled accordingly.

During tracking, the input appears as approximately a 300pF capacitor in series with 330Ω, for a 100ns time constant. A full-scale input swing would settle to $^1/_2$ LSB ($^1/_{2048}$) in 7RC time constants. Doing continuous conversions with a 1MHz clock provides 3µs of tracking time, so up to 1000Ω of external source impedance (400ns time constant) would allow proper settling of a step input.

If the clock was slower, or the converter was not restarted immediately (causing a longer sample lime), a higher source impedance could be used.

The CA3310s low-input time constant also allows good tracking of dynamic input waveforms. The sampling rate with a 1MHz clock is approximately 80kHz. A Nyquist rate ($f_{SAMPLE}/2$) input sine wave of 40kHz would have negligible attenuation and a phase lag of only 1.5 degrees.

Accuracy Specifications

The CA3310 accepts an analog input between the values of V_{REF}- and V_{REF}+, and quantizes it into one of 2^{10} or 1024 output codes. Each code should exist as the input is varied through a range of $^1/_{1024}$ X (V_{REF}+ - V_{REF}-), referred to as 1 LSB of input voltage. A differential linearity error, illustrated in Figure 17, occurs if an output code occurs over other than the ideal (1 LSB) input range. Note that as long as the error does not reach -1 LSB, the converter will not miss any codes.

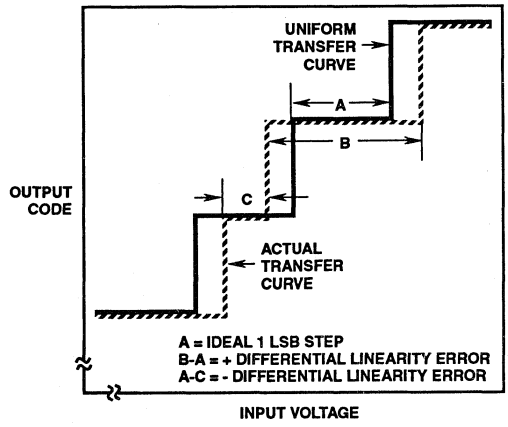


FIGURE 17. DIFFERENTIAL LINEARITY ERROR

The CA3310 output should change from a code of 000_{16} to 001_{16} at an input voltage of (V_{REF}- +1 LSB). It should also change from a code of $3FE_{16}$ to $3FF_{16}$ at an input of (V_{REF}+ -1 LSB). Any differences between the actual and expected input voltages that cause these transitions are the offset and gain errors, respectively. Figure 18 illustrates these errors.

As the input voltage is increased linearly from the point that causes the 000_{16} to 001_{16} transition to the point that causes the $3FE_{16}$ to $3FF_{16}$ transition, the output code should also increase linearly. Any deviation from this input- to-output correspondence is integral linearity error, illustrated in Figure 19.

Note that the integral linearity is referenced to a straight line drawn through the actual end points, not the ideal end points. For absolute accuracy to be equal to the integral linearity, the gain and offset would have to be adjusted to ideal.

Offset and Gain Adjustments

The V_{REF}+ and V_{REF}- pins, references for the two ends of the analog input range, are the only means of doing offset or gain adjustments. In a typical system, the V_{REF}- might be returned to a clean ground, and offset adjustment done on an input amplifier. V_{REF}+ would then be adjusted for gain.

V_{REF}- could be raised from ground to adjust offset or to accommodate an input source that can't drive down to ground. There are current pulses that occur, however, during the successive approximation part of a conversion cycle, as the charge-balancing capacitors are switched between V_{REF}-

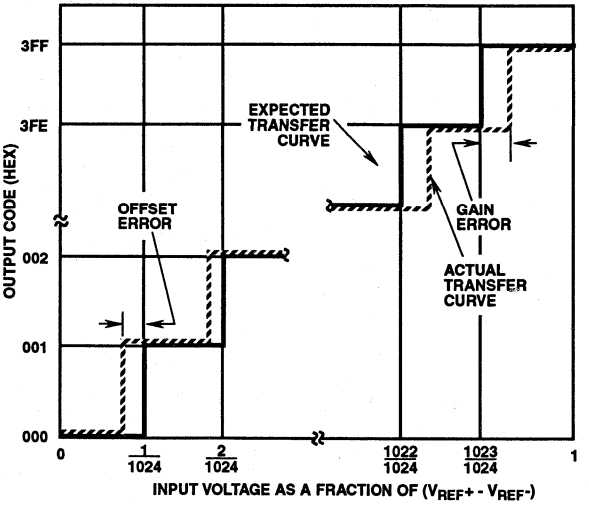


FIGURE 18. GAIN AND OFFSET ERROR

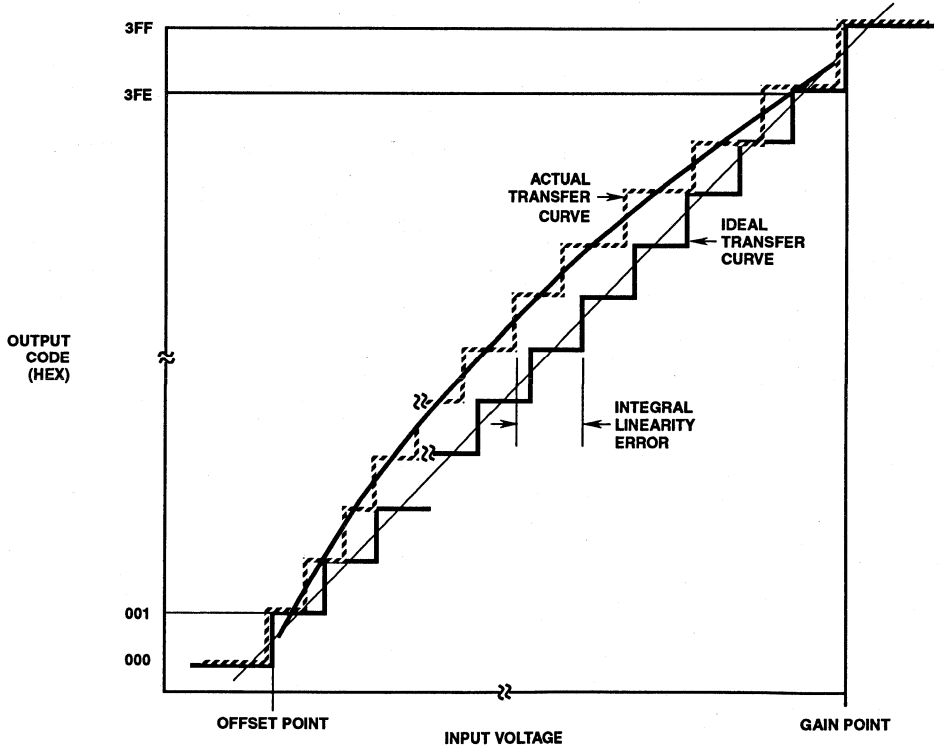


FIGURE19. NORMALIZED GAIN, OFFSET, INTEGRAL AND DIFFERENTIAL LINEARITY ERRORS vs REFERENCE VOLTAGE

and V_{REF}+. For that reason, V_{REF}- and V_{REF}+ should be well bypassed. Figure 10 shows peak and average V_{REF}+ current.

Other Accuracy Effects

Linearity, offset, and gain errors are dependent on the magnitude of the full-scale input range, V_{REF}+ - V_{REF}-. Figure 11 shows how these errors vary with full-scale range.

The clocking speed is a second factor that affects conversion accuracy. Figure 12 shows the typical variation of linearity, offset, and gain errors versus clocking speed.

Gain and offset drift due to temperature are kept very low by means of auto-balancing the comparator. The specifications show typical offset and gain dependency on temperature.

There is also very little linearity change with temperature, only that caused by the slight slowing of CMOS with increasing temperature. At +85°C, for instance, the ILE and DLE would be typically those for a 20% faster clock than at +25°C.

Power Supplies and Grounding

V_{DD}(+) and V_{SS}(GND) are the digital supply pins: they operate all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for V_{DD}+, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}: input transients above V_{DD} or below V_{SS} will get steered to the digital supplies. Current on these pins must be limited by external means to the values specified under maximum ratings.

The V_{AA}+ and V_{AA}- terminals supply the charge-balancing comparator only. Because the comparator is autobalanced between conversions, it has good low frequency supply rejection. It does not reject well at high frequencies, however: V_{AA}- should be returned to a clean analog ground, and V_{AA}+ should be RC decoupled from the digital supply.

There is approximately 50Ω of substrate impedance between V_{DD} and V_{AA}+. This can be used, for example, as part of a low-pass RC filter to attenuate switching supply noise. A 10pF capacitor from V_{AA}+ to ground would attenuate 30kHz noise by approximately 40dB. Note that back-to-back diodes should be placed from V_{DD} to V_{AA}+ to handle supply to capacitor turn-on or turn-off current spikes.

Figure 16 shows V_{AA}+ supply rejection versus frequency. Note that the frequency to be rejected scales with the clock: the 100Hz rejection with a 100kHz clock would be roughly equivalent to the 1kHz rejection with a 1MHz clock.

The supply current for the CA3310 is dependent on clock frequency, supply voltage, and temperature. Figure 14 shows the typical current versus frequency and voltage, while Figure 15 shows it versus temperature and voltage. Note that if stopped in auto-balance, the supply current is typically somewhat higher than if free-running. See Specifications.

Applications Circuits

Differential Input A/D System

As the CA3310 accepts a unipolar positive-analog input, the accommodation of other ranges requires additional circuitry. The input capacitance and the input energy also force using a low-impedance source for all but slow speed use. Figure 20 shows the CA3310 with a reference, input amplifier, and input-scaling resistors for several input ranges.

The ICL7663S regulator was chosen as the reference, as it can deliver less than 0.25V input-to-output (dropout) voltage and uses very little power. As high a reference as possible is generally desirable, resulting in the best linearity and rejection of noise at the CA3310.

The tantalum capacitor sources the V_{REF} current spikes during a conversion cycle. This relieves the response and peak current requirements of the reference.

The CA3140 operational amplifier provides good slewing capability for high bandwidth input signals and can quickly settle the energy that the CA3310 outputs at its V_{IN} terminal. It can also drive close to the negative supply rail.

If system supply sequencing or an unknown input voltage is likely to cause the operational amplifier to drive above the V_{DD} supply, a diode clamp can be added from pin 8 of the operational amplifier to the V_{DD} supply. The minus drive current is low enough not to require protection.

With a 2MHz clock (~150kHz sampling), Nyquist criteria would give a maximum input bandwidth of 75kHz. The resistor values chosen are low enough to not seriously degrade system bandwidth (an operational amplifier settling) at that clock frequency. If A/D clock frequency and bandwidth requirements are lower, the resistor values (and input impedance) can be made correspondingly higher.

The A/D system would generally be calibrated by tying V_{IN}- to ground and applying a voltage to V_{IN}+ that is 0.5 LSB ($^1/_{2048}$ of full-scale range) above ground. The operational amplifier offset should be adjusted for an output code dithering between 000_{16} and 001_{16} for unipolar use, or 100_{16} and 101_{16} for bipolar use. The gain would then be adjusted by applying a voltage that is 1.5 LSB below the positive full scale input, and adjusting the reference for an output dithering between $3FE_{16}$ and $3FF_{16}$.

Note that RI through R5 should be very well matched, as they affect the common-mode rejection of the A/D system. Also, if R2 and R3 are not matched, the offset adjust of the operational amplifier may not have enough adjustment range in bipolar systems.

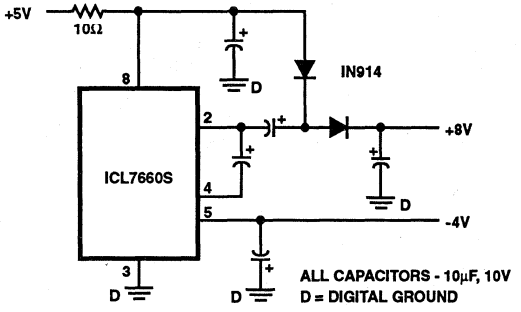
The common-mode input range of the system is set by the supply voltage available to the operational amplifier. The range that can be applied to the V_{IN}- terminal can be calculated by:

$(\frac{R4}{R5} + 1)$ V_{IN}- for the most negative

$(\frac{R4}{R5} + 1)$ (VIN+ -2.5V) - $(\frac{R4}{R5})V_{REF}$+ for the most positive

Single +5V Supply

If only a single +5V supply is available, an ICL7660 can be used to provide approximately +8V and -4V to the operational amplifier. Figure 20 shows this approach. Note that the converter and associated capacitors should be grounded to the digital supply. The 100Ω in series with each supply at the operational amplifier isolates digital and analog grounds.



Digital Sample and Hold

With a minimum of external logic, the CA3310 can be made to wait at the verge of ending a sample. A start pulse will then, after the internal aperture delay, capture the input and finish the conversion cycle. Figure 21 illustrates this application.

The CA3310 is connected as if to free run. The Data Ready signal is shifted through a CD74HC175, and at the low-going clock edge just before the sample would end, is used to hold the clock low.

The same signal, active high, is available to indicate the CA3310 is ready to convert. A low pulse to reset the CD74HC175 will now release the clock, and the sample will end as it goes positive. Ten cycles later, the conversion will be complete, and DRDY will go active.

Operating and Handling Considerations

1. Handling

All inputs and outputs of Harris CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6526, "Guide to Better Handling and Operation of CMOS Integrated Circuits".

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} - V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} +0.3V nor less than V_{SS} -0.3V. Input currents must not exceed 20mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused Input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

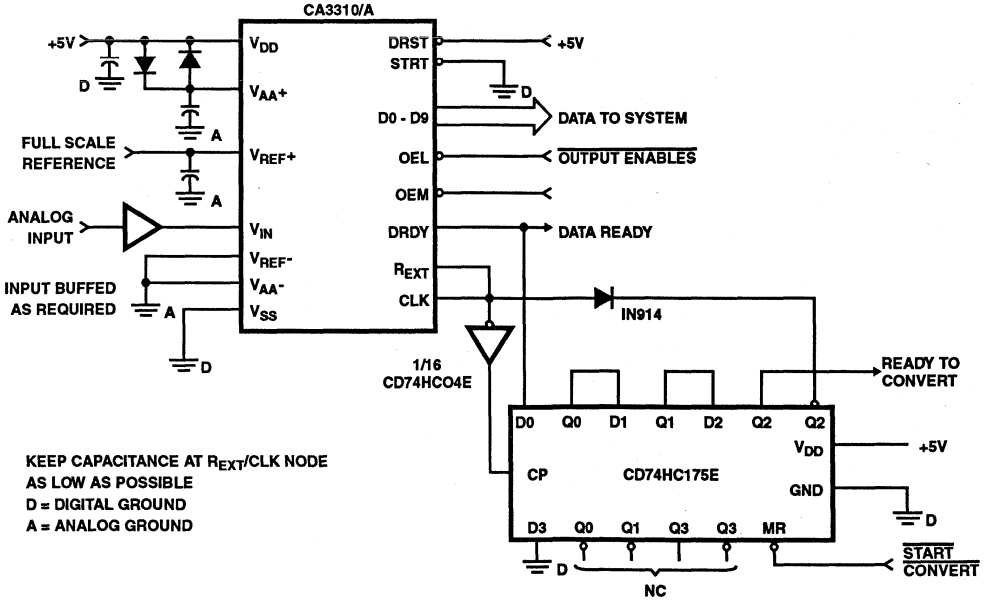


FIGURE 21. DIGITAL TRACK-AND-HOLD BLOCK DIAGRAM

HI-574A, HI-674A HI-774

Complete 12-Bit A/D Converter with Microprocessor Interface

December 1993

Features

- Complete 12-Bit A/D Converter with Reference and Clock
- Full 8-, 12- or 16-Bit Microprocessor Bus Interface
- 150ns Bus Access Time
- No Missing Codes Over Temperature
- Minimal Setup Time for Control Signals
- Fast Conversion Times
  - 25µs Max (HI-574A)
  - 15µs Max (HI-674A)
  - 9µs Max (HI-774)
- Digital Error Correction (HI-774)
- Low Noise, via Current-Mode Signal Transmission Between Chips
- Byte Enable/Short Cycle (A_0 Input)
  - Guaranteed Break-Before-Make Action, Eliminating Bus Contention During Read Operation. Latched by Start Convert Input (To Set the Conversion Length)
- ±12V to ±15V Operation

Applications

- Military and Industrial Data Acquisition Systems
- Electronic Test and Scientific Instrumentation
- Process Control Systems

Description

The HI-X74(A) is a complete 12-bit Analog-to-Digital Converter, including a +10V reference clock, tri-state outputs and a digital interface for microprocessor control. Successive approximation conversion is performed by two monolithic dice housed in a 28 lead package. The bipolar analog die features the Harris Dielectric Isolation process, which provides enhanced AC performance and freedom from latch-up.

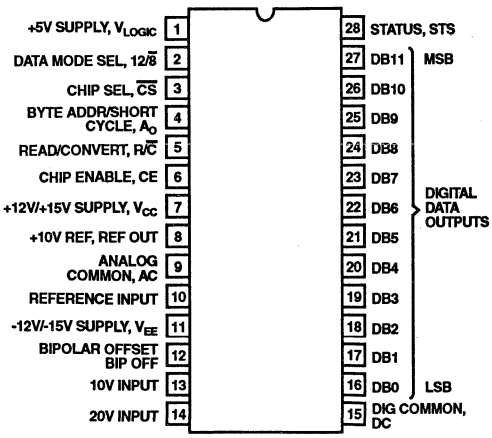
Custom design of each IC (bipolar analog and CMOS digital) has yielded improved performance over existing versions of this converter. The voltage comparator features high PSRR plus a high speed current-mode latch, and provides precise decisions down to 0.1 LSB of input overdrive. More than 2X reduction in noise has been achieved by using current instead of voltage for transmission of all signals between the analog and digital IC's. Also, the clock oscillator is current controlled for excellent stability over temperature.

The HI-X74(A) offers standard unipolar and bipolar input ranges, laser trimmed for specified linearity, gain and offset accuracy. The low noise buried zener reference circuit is trimmed for minimum temperature coefficient.

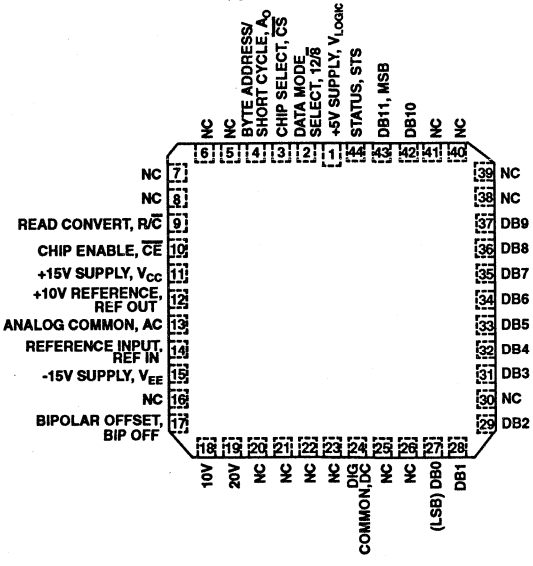
Power requirements are +5V and ±12V to ±15V, with typical dissipation of 385mW (HI-574A/674A) and 390mW (HI-774) at 12V. All models are available in sidebrazed DIP, PDIP, and LCC. For additional HI-Rel screening including 160 hour burn-in, specify "-8" suffix. For MIL-STD-883 compliant parts, request HI-574A/883, HI-674A/883, and HI-774/883 data

Pinouts

(PDIP AND CERAMIC DIP)
TOP VIEW



(LCC)
TOP VIEW



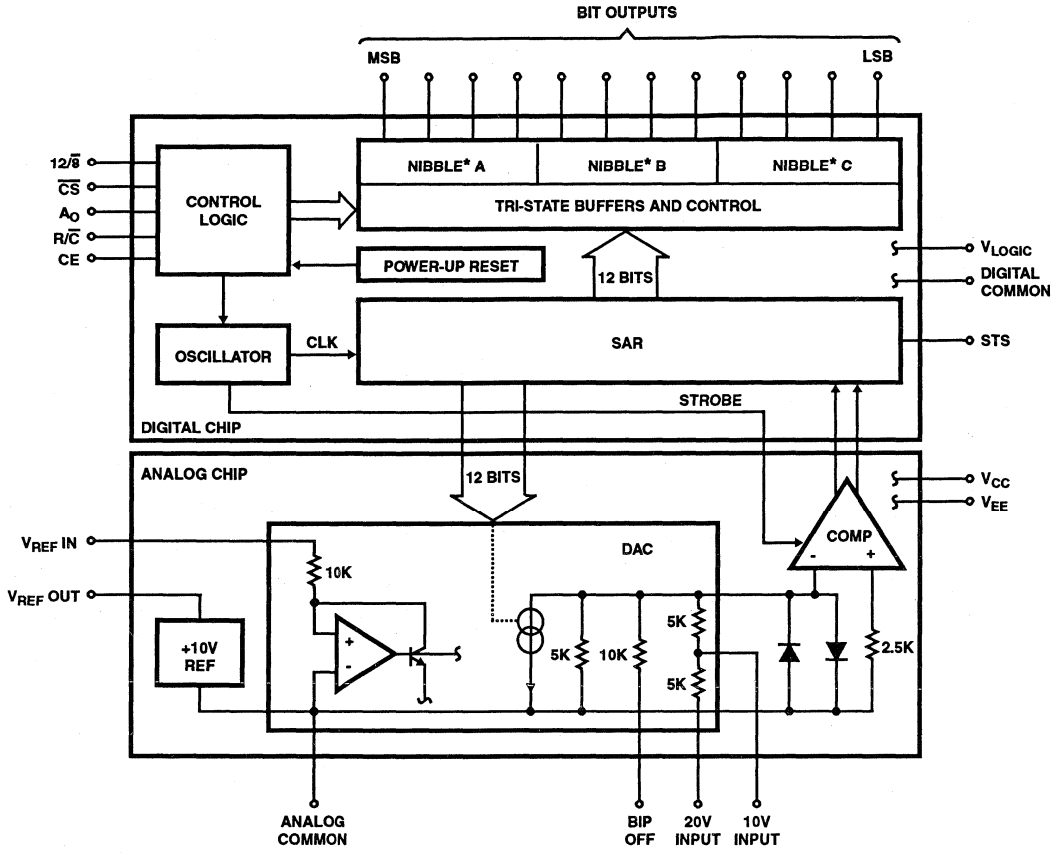
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3096.3**

Ordering Information

PART NUMBER	INL	TEMPERATURE RANGE	PACKAGE
HI3-574AJN-5	±1.0 LSB	0°C to +75°C	28 Lead Plastic DIP
HI3-574AKN-5	±0.5 LSB	0°C to +75°C	28 Lead Plastic DIP
HI3-574ALN-5	±0.5 LSB	0°C to +70°C	28 Lead Plastic DIP
HI1-574AJD-5	±1.0 LSB	0°C to +75°C	28 Lead Ceramic DIP
HI1-574AKD-5	±0.5 LSB	0°C to +75°C	28 Lead Ceramic DIP
HI1-574ALD-5	±0.5 LSB	0°C to +75°C	28 Lead Ceramic DIP
HI1-574ASD-2	±1.0 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-574ATD-2	±0.5 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-574AUD-2	±0.5 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-574ASD/883	±1.0 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-574ATD/883	±0.5 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-574AUD/883	±0.5 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI4-574ASE/883	±1.0 LSB	-55°C to +125°C	44 Lead Ceramic LCC
HI4-574ATE/883	±0.5 LSB	-55°C to +125°C	44 Lead Ceramic LCC
HI4-574AUE/883	±0.5 LSB	-55°C to +125°C	44 Lead Ceramic LCC
HI3-674AJN-5	±1.0 LSB	0°C to +75°C	28 Lead Plastic DIP
HI3-674AKN-5	±0.5 LSB	0°C to +75°C	28 Lead Plastic DIP
HI3-674ALN-5	±0.5 LSB	0°C to +75°C	28 Lead Plastic DIP
HI1-674AJD-5	±1.0 LSB	0°C to +75°C	28 Lead Ceramic DIP
HI1-674AKD-5	±0.5 LSB	0°C to +75°C	28 Lead Ceramic DIP
HI1-674ALD-5	±0.5 LSB	0°C to +75°C	28 Lead Ceramic DIP
HI1-674ASD-2	±1.0 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-674ATD-2	±0.5 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-674AUD-2	±0.5 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-674ASD/883	±1.0 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-674ATD/883	±0.5 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-674AUD/883	±0.5 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI4-674ASE/883	±1.0 LSB	-55°C to +125°C	44 Lead Ceramic LCC
HI4-674ATE/883	±0.5 LSB	-55°C to +125°C	44 Lead Ceramic LCC
HI4-674AUE/883	±0.5 LSB	-55°C to +125°C	44 Lead Ceramic LCC
HI3-774J-5	±1.0 LSB	0°C to +75°C	28 Lead Plastic DIP
HI3-774K-5	±0.5 LSB	0°C to +75°C	28 Lead Plastic DIP
HI1-774J-5	±1.0 LSB	0°C to +75°C	28 Lead Ceramic DIP
HI1-774K-5	±0.5 LSB	0°C to +75°C	28 Lead Ceramic DIP
HI1-774L-5	±0.5 LSB	0°C to +75°C	28 Lead Ceramic DIP
HI1-774S-2	±1.0 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-774T-2	±0.5 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-774U-2	±0.5 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-774S/883	±1.0 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-774T/883	±0.5 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI1-774U/883	±0.5 LSB	-55°C to +125°C	28 Lead Ceramic DIP
HI4-774S/883	±1.0 LSB	-55°C to +125°C	44 Lead Ceramic LCC
HI4-774T/883	±0.5 LSB	-55°C to +125°C	44 Lead Ceramic LCC
HI4-774U/883	±0.5 LSB	-55°C to +125°C	44 Lead Ceramic LCC

Functional Block Diagram



* "Nibble" is a 4 bit digital word

Absolute Maximum Ratings

Supply Voltage
- V_{CC} to Digital Common ..... 0V to +16.5V
- V_{EE} to Digital Common ..... 0V to -16.5V
- V_{LOGIC} to Digital Common ..... 0V to +7V
- Analog Common to Digital Common ..... ±1V

Control Inputs
- (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to Digital Common ..... -0.5V to V_{LOGIC}+0.5V

Analog Inputs
- (REFIN, BIPOFF, 10VIN) to Analog Common ..... ±16.5V
- 20VIN to Analog Common ..... ±24V

REFOUT ..... Indefinite short to Common, momentary short to V_{CC}

Operating Temperature Range
- HI3-574AxN-5, HI1-574AxD-5 ..... 0°C to +75°C
- HI3-674AxN-5, HI1-674AxD-5 ..... 0°C to +75°C
- HI3-774xN-5, HI1-774xD-5 ..... 0°C to +75°C
- HI1-574AxD-2, HI1-674AxD-2, HI1-774xD-2 ... -55°C to +125°C

Storage Temperature Range
- HI3-574AxN-5 ..... $-40°C < T_A < +85°C$
- HI3-674AxN-5 ..... $-40°C < T_A < +85°C$
- HI3-774xN-5 ..... $-40°C < T_A < +85°C$
- HI1-574AxD-2, HI1-574AxD-5 ..... $-65°C < T_A < +150°C$
- HI1-674AxD-2, HI1-674AxD-5 ..... $-65°C < T_A < +150°C$
- HI1-774xD-2, HI1-774xD-5 ..... $-65°C < T_A < +150°C$

Lead Temperature (Soldering, 10s) ..... 300°C

Thermal Information

Thermal Resistance	θ_{JA}
HI3-574AxN-5	65°C/W
HI3-674AxN-5	65°C/W
HI3-774xN-5	65°C/W
Power Dissipation at +75°C (Note 1)	
HI3-574AxN-5	1000mW
HI3-674AxN-5	1000mW
HI3-774xN-5	1000mW
HI1-574AxD-x	2080mW
HI1-674AxD-2, HI1-674AxD-5	2083mW
HI1-774xD-2, HI1-774xD-5	2083mW
HI4-574AxE-x	2270mW
Transistor Count	
HI-574A, HI-674A	1117
HI-774	2117
Junction Temperature	
HI3-574AxN-5, HI3-674AxN-5, HI3-774xN-5	+150°C
HI1-574AxD-2, HI1-574AxD-5	+175°C
HI1-674AxD-2, HI1-674AxD-5	+175°C
HI1-774xD-2, HI1-774xD-5	+175°C

DC and Transfer Accuracy Specifications

Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified

PARAMETERS		TEMPERATURE RANGE -5 (0°C to +75°C) J SUFFIX	K SUFFIX	L SUFFIX	UNITS
DYNAMIC CHARACTERISTICS					
Resolution (Max)		12	12	12	Bits
Linearity Error					
+25°C (Max)		±1	±1/2	±1/2	LSB
0°C to +75°C (Max)		±1	±1/2	±1/2	LSB
Max resolution for which no missing codes is guaranteed					
+25°C	HI-574A, HI-674A	12	12	12	Bits
	HI-774	11	12	12	Bits
T_{MIN} to T_{MAX}	HI-574A, HI-674A	11	12	12	Bits
	HI-774	11	12	12	Bits
Unipolar Offset (Max)					
Adjustable to Zero		±2	±1.5	±1	LSB
Bipolar Offset (Max)					
V_{IN} = 0V (Adjustable to Zero)		±4	±4	±3	LSB
V_{IN} = -10V		±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error					
+25°C (Max), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to Zero)		±0.25	±0.25	±0.15	% of F.S.
T_{MIN} to T_{MAX} (No adjustment at +25°C)		±0.475	±0.375	±0.20	% of F.S.
T_{MIN} to T_{MAX} (With adjustment to zero +25°C)		±0.22	±0.12	±0.05	% of F.S.

DC and Transfer Accuracy Specifications Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified **(Continued)**

PARAMETERS		TEMPERATURE RANGE -5 (0°C to +75°C) J SUFFIX	K SUFFIX	L SUFFIX	UNITS
Temperature Coefficients Guaranteed Max change, T_{MIN} to T_{MAX} (Using internal reference)					
Unipolar Offset	HI-574A, HI-674A	±2	±1	±1	LSB
	HI-774	±2	±1	±1	LSB
Bipolar Offset	HI-574A, HI-674A	±2	±1	±1	LSB
	HI-774	±2	±2	±1	LSB
Full Scale Calibration	HI-574A, HI-674A	±9	±2	±2	LSB
	HI-774	±9	±5	±2	LSB
Power Supply Rejection Max change in Full Scale Calibration					
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V		±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V		±1/2	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V		±2	±1	±1	LSB
ANALOG INPUTS					
Input Ranges					
Bipolar		-5 to +5			V
		-10 to +10			V
Unipolar		0 to +10			V
		0 to +20			V
Input Impedance					
10V Span		5K, ±25%			Ω
20V Span		10K, ±25%			Ω
POWER SUPPLIES					
Operating Voltage Range					
V_{LOGIC}		+4.5 to +5.5			V
V_{CC}		+11.4 to +16.5			V
V_{EE}		-11.4 to -16.5			V
Operating Current					
I_{LOGIC}		7 Typ, 15 Max			mA
I_{CC} +15V Supply		11 Typ, 15 Max			mA
I_{EE} -15V Supply		21 Typ, 28 Max			mA
Power Dissipation					
±15V, +15V		515 Typ, 720 Max			mW
±12V, +5V		385 Typ			mW
Internal Reference Voltage					
T_{MIN} to T_{MAX}		+10.00 ±0.05 Max			V
Output current, available for external loads (External load should not change during conversion).		2.0 Max			mA

DC and Transfer Accuracy Specifications Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified

PARAMETERS		TEMPERATURE RANGE -2 (-55°C to +125°C) S SUFFIX	T SUFFIX	U SUFFIX	UNITS
DYNAMIC CHARACTERISTICS					
Resolution (Max)		12	12	12	Bits
Linearity Error					
+25°C		±1	±1/2	±1/2	LSB
-55°C to +125°C (Max)		±1	±1	±1	LSB
Max resolution for which no missing codes is guaranteed					
+25°C	HI-574A, HI-674A	12	12	12	Bits
	HI-774	11	12	12	Bits
T_{MIN} to T_{MAX}	HI-574A, HI-674A	11	12	12	Bits
	HI-774	11	12	12	Bits
Unipolar Offset (Max)					
Adjustable to Zero	HI-574A, HI-674A	±2	±1.5	±1	LSB
	HI-774	±2	±2	±1	LSB
Bipolar Offset (Max)					
V_{IN} = 0V (Adjustable to Zero)		±4	±4	±3	LSB
V_{IN} = -10V		±0.15	±0.1	±0.1	% of F.S.
Full Scale Calibration Error					
+25°C (Max), with fixed 50Ω resistor from REF OUT to REF IN (Adjustable to Zero)		±0.25	±0.25	±0.15	% of F.S.
T_{MIN} to T_{MAX} (No adjustment at +25°C)		±0.75	±0.50	±0.275	% of F.S.
T_{MIN} to T_{MAX} (With adjustment to zero +25°C)		±0.50	±0.25	±0.125	% of F.S.
Temperature Coefficients Guaranteed Max change, T_{MIN} to T_{MAX} (Using internal reference)					
Unipolar Offset		±2	±1	±1	LSB
Bipolar Offset		±2	±2	±1	LSB
Full Scale Calibration		±20	±10	±5	LSB
Power Supply Rejection Max change in Full Scale Calibration					
+13.5V < V_{CC} < +16.5V or +11.4V < V_{CC} < +12.6V		±2	±1	±1	LSB
+4.5V < V_{LOGIC} < +5.5V		±1/2	±1/2	±1/2	LSB
-16.5V < V_{EE} < -13.5V or -12.6V < V_{EE} < -11.4V		±2	±1	±1	LSB
ANALOG INPUTS					
Input Ranges					
Bipolar		-5 to +5			V
		-10 to +10			V
Unipolar		0 to +10			V
		0 to +20			V

DC and Transfer Accuracy Specifications Typical at +25°C with V_{CC} = +15V or +12V, V_{LOGIC} = +5V, V_{EE} = -15V or -12V, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEMPERATURE RANGE -2 (-55°C to +125°C)			UNITS
	S SUFFIX	T SUFFIX	U SUFFIX	
Input Impedance				
10V Span	5K, ±25%			Ω
20V Span	10K, ±25%			Ω
POWER SUPPLIES				
Operating Voltage Range				
V_{LOGIC}	+4.5 to +5.5			V
V_{CC}	+11.4 to +16.5			V
V_{EE}	-11.4 to -16.5			V
Operating Current				
I_{LOGIC}	7 Typ, 15 Max			mA
I_{CC} +15V Supply	11 Typ, 15 Max			mA
I_{EE} -15V Supply	21 Typ, 28 Max			mA
Power Dissipation				
±15V, +15V	515 Typ, 720 Max			mW
±12V, +5V	385 Typ			mW
Internal Reference Voltage				
T_{MIN} to T_{MAX}	+10.00 ±0.05 Max			V
Output current, available for external loads (External load should not change during conversion).	2.0 Max			mA

Digital Specifications All Models, Over Full Temperature Range

PARAMETERS	MIN	TYP	MAX
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, A_0, 412/$\overline{8}$)			
Logic "1"	+2.4V	-	+5.5V
Logic "0"	-0.5V	-	+0.8V
Current	-	±0.1µA	±5µA
Capacitance	-	5pF	-
Logic Outputs (DB11-DB0, STS)			
Logic "0" (I_{SINK} - 1.6mA)	-	-	+0.4V
Logic "1" (I_{SOURCE} - 500µA)	+2.4V	-	-
Logic "1" (I_{SOURCE} - 10µA)	+4.5V	-	-
Leakage (High Z State, DB11-DB0 Only)	-	±0.1µA	±5µA
Capacitance	-	5pF	-

Timing Specifications (HI-574A) +25°C, Note 2, Unless Otherwise Specified

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
CONVERT MODE						
t_{DSC}	STS Delay from CE		-	-	200	ns
t_{HEC}	CE Pulse Width		50	-	-	ns
t_{SSC}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{HSC}	$\overline{CS}$ Low During CE High		50	-	-	ns
t_{SRC}	R/$\overline{C}$ to CE Setup		50	-	-	ns
t_{HRC}	R/$\overline{C}$ Low During CE High		50	-	-	ns
t_{SAC}	A_0 to CE Setup		0	-	-	ns
t_{HAC}	A_0 Valid During CE High		50	-	-	ns
t_C	Conversion Time	12-Bit Cycle T_{MIN} to T_{MAX}	15	20	25	µs
		8-Bit Cycle T_{MIN} to T_{MAX}	10	13	17	µs
READ MODE						
t_{DD}	Access Time from CE		-	75	150	ns
t_{HD}	Data Valid After CE Low		25	-	-	ns
t_{HL}	Output Float Delay		-	100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{SRR}	R/$\overline{C}$ to CE Setup		0	-	-	ns
t_{SAR}	A_0 to CE Setup		50	-	-	ns
t_{HSR}	$\overline{CS}$ Valid After CE Low		0	-	-	ns
t_{HRR}	R/$\overline{C}$ High After CE Low		0	-	-	ns
t_{HAR}	A_0 Valid After CE Low		50	-	-	ns
t_{HS}	STS Delay After Data Valid		300	-	1200	ns

Timing Specifications (HI-674A) +25°C, Note 2, Unless Otherwise Specified

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
CONVERT MODE						
t_{DSC}	STS Delay from CE		-	-	200	ns
t_{HEC}	CE Pulse Width		50	-	-	ns
t_{SSC}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{HSC}	$\overline{CS}$ Low During CE High		50	-	-	ns
t_{SRC}	R/$\overline{C}$ to CE Setup		50	-	-	ns
t_{HRC}	R/$\overline{C}$ Low During CE High		50	-	-	ns
t_{SAC}	A_0 to CE Setup		0	-	-	ns
t_{HAC}	A_0 Valid During CE High		50	-	-	ns
t_C	Conversion Time	12-Bit Cycle T_{MIN} to T_{MAX}	9	12	15	µs
		8-Bit Cycle T_{MIN} to T_{MAX}	6	8	10	µs
READ MODE						
t_{DD}	Access Time from CE		-	75	150	ns
t_{HD}	Data Valid After CE Low		25	-	-	ns
t_{HL}	Output Float Delay		-	100	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup		50	-	-	ns
t_{SRR}	R/$\overline{C}$ to CE Setup		0	-	-	ns
t_{SAR}	A_0 to CE Setup		50	-	-	ns
t_{HSR}	$\overline{CS}$ Valid After CE Low		0	-	-	ns
t_{HRR}	R/$\overline{C}$ High After CE Low		0	-	-	ns
t_{HAR}	A_0 Valid After CE Low		50	-	-	ns
t_{HS}	STS Delay After Data Valid		25	-	850	ns

Timing Specifications (HI-774) +25°C, Into a load with R_L = 3kΩ and C_L = 50pF, Note 2, Unless Otherwise Specified

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS
CONVERT MODE						
t_{DSC}	STS Delay from CE		-	100	200	ns
t_{HEC}	CE Pulse Width		50	30	-	ns
t_{SSC}	$\overline{CS}$ to CE Setup		50	20	-	ns
t_{HSC}	$\overline{CS}$ Low During CE High		50	20	-	ns
t_{SRC}	R/$\overline{C}$ to CE Setup		50	0	-	ns
t_{HRC}	R/$\overline{C}$ Low During CE High		50	20	-	ns
t_{SAC}	A_0 to CE Setup		0	0	-	ns
t_{HAC}	A_0 Valid During CE High		50	30	-	ns
t_C	Conversion Time	12-Bit Cycle T_{MIN} to T_{MAX} (-5)	-	8.0	9	µs
		8-Bit Cycle T_{MIN} to T_{MAX} (-5)	-	6.4	6.8	µs
		12-Bit Cycle T_{MIN} to T_{MAX} (-2)	-	9	11	µs
		8-Bit Cycle T_{MIN} to T_{MAX} (-2)	-	6.8	8.3	µs
READ MODE						
t_{DD}	Access Time from CE		-	75	150	ns
t_{HD}	Data Valid After CE Low		25	35	-	ns
t_{HL}	Output Float Delay		-	70	150	ns
t_{SSR}	$\overline{CS}$ to CE Setup		50	0	-	ns
t_{SRR}	R/$\overline{C}$ to CE Setup		0	0	-	ns
t_{SAR}	A_0 to CE Setup		50	25	-	ns
t_{HSR}	CS Valid After CE Low		0	0	-	ns
t_{HRR}	R/$\overline{C}$ High After CE Low		0	0	-	ns
t_{HAR}	A_0 Valid After CE Low		50	25	-	ns
t_{HS}	STS Delay After Data Valid		-	90	300	ns

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

Pin Description

PIN	SYMBOL	DESCRIPTION
1	V_{LOGIC}	Logic supply pin (+5V)
2	12/$\overline{8}$	Data Mode Select - Selects between 12-bit and 8-bit output modes.
3	$\overline{CS}$	Chip Select - Chip Select high disables the device.
4	A_0	Byte Address/Short Cycle - See Table 1 for operation.
5	R/$\overline{C}$	Read/Convert - See Table 1 for operation.
6	CE	Chip Enable - Chip Enable low disables the device.
7	V_{CC}	Positive Supply (+12V/+15V)
8	REF OUT	+10V Reference
9	AC	Analog Common
10	REF IN	Reference Input
11	V_{EE}	Negative Supply (-12V/-15V).
12	BIP OFF	Bipolar Offset
13	10V Input	10V Input - Used for 0V to 10V and -5V to +5V input ranges.
14	20V Input	20V Input - Used for 0V to 20V and -10V to +10V input ranges.
15	DC	Digital Common
16	DB0	Data Bit 0 (LSB)
17	DB1	Data Bit 1
18	DB2	Data Bit 2
19	DB3	Data Bit 3
20	DB4	Data Bit 4
21	DB5	Data Bit 5
22	DB6	Data Bit 6
23	DB7	Data Bit 7
24	DB8	Data Bit 8
25	DB9	Data Bit 9
26	DB10	Data Bit 10
27	DB11	Data Bit 11 (MSB)
28	STS	Status Bit - Status high implies a conversion is in progress.

Definitions of Specifications

Linearity Error

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale". The point used as "zero" occurs $^1/_2$ LSB (1.22mV for 10V span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level $1^1/_2$ LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HI-X74(A)K and L grades are guaranteed for maximum nonlinearity of $\pm^1/_2$ LSB. For these grades, this means that an analog value which falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HI-X74(A)J is guaranteed to ±1 LSB max error. For this grade, an analog value which falls within a given code width will result in either the correct code for that region or either adjacent one.

Note that the linearity error is not user-adjustable.

Differential Linearity Error (No Missing Codes)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HI-X74(A)K and L grades, which guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HI-X74(A)J grade guarantees no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11 bits must be present; in practice very few of the 12-bit codes are missing.

Unipolar Offset

The first transition should occur at a level $^1/_2$ LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with or without external adjustment.

Bipolar Offset

Similarly, in the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value $^1/_2$ LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

Full Scale Calibration Error

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value $1^1/_2$ LSB below the nominal full scale (9.9963V for 10.000V full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which is typically 0.05 to 0.1% of full scale, can be trimmed out as shown in Figures 2 and 3. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10V reference.

Temperature Coefficients

The temperature coefficients for full-scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (+25°C) value to the value at T_{MIN} or T_{MAX}.

Power Supply Rejection

The standard specifications for the HI-X74A assume use of +5.00 and ±15.00 or ±12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

Code Width

A fundamental quantity for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to 1 least significant bit (LSB) of the full scale range or 2.44mV out of 10V for a 12-bit ADC.

Quantization Uncertainty

Analog-to-digital converters exhibit an inherent quantization uncertainty of $\pm^1/_2$ LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of given resolution.

Left-justified Data

The data format used in the HI-X74(A) is left-justified. This means that the data represents the analog input as a fraction of full-scale, ranging from 0 to $\frac{4095}{4096}$. This implies a binary point to the left of the MSB.

Applying the HI-X74(A)

For each application of this converter, the ground connections, power supply bypassing, analog signal source, digital timing and signal routing on the circuit board must be optimized to assure maximum performance. These areas are reviewed in the following sections, along with basic operating modes and calibration requirements.

Physical Mounting and Layout Considerations

Layout

Unwanted, parasitic circuit components, (L, R, and C) can make 12 bit accuracy impossible, even with a perfect A/D converter. The best policy is to eliminate or minimize these parasitics through proper circuit layout, rather than try to quantify their effects.

The recommended construction is a double-sided printed circuit board with a ground plane on the component side. Other techniques, such as wire-wrapping or point-to-point wiring on vector board, will have an unpredictable effect on accuracy.

In general, sensitive analog signals should be routed between ground traces and kept well away from digital lines. If analog and digital lines must cross, they should do so at right angles.

Power Supplies

Supply voltages to the HI-X74(A) (+15V, -15V and +5V) must be "quiet" and well regulated. Voltage spikes on these lines can affect the converter's accuracy, causing several LSBs to flicker when a constant input is applied. Digital noise and spikes from a switching power supply are especially troublesome. If switching supplies must be used, outputs should be carefully filtered to assure "quiet" DC voltage at the converter terminals.

Further, a bypass capacitor pair on each supply voltage terminal is necessary to counter the effect of variations in supply current. Connect one pair from pin 1 to 15 (V_{LOGIC} supply), one from pin 7 to 9 (V_{CC} to Analog Common) and one from pin 11 to 9 (V_{EE} to Analog Common). For each capacitor pair, a 10µF tantalum type in parallel with a 0.1µF ceramic type is recommended.

Ground Connections

Pins 9 and 15 should be tied together at the package to guarantee specified performance for the converter. In addition, a wide PC trace should run directly from pin 9 to (usually) +15V common, and from pin 15 to (usually) the +5V Logic Common. If the converter is located some distance from the system's "single point" ground, make only these connections to pins 9 and 15: Tie them together at the package, and back to the system ground with a single path. This path should have low resistance. (Code dependent currents flow in the V_{CC}, V_{EE} and V_{LOGIC} terminals, but not through the HI-X74(A)'s Analog Common or Digital Common).

Analog Signal Source

HI-574A and HI-674A

The device chosen to drive the HI-X74A analog input will see a nominal load of 5kΩ (10V range) or 10kΩ (20V range). However, the other end of these input resistors may change ±400mV with each bit decision, creating abrupt changes in current at the analog input. Thus, the signal source must maintain its output voltage while furnishing these step changes in load current, which occur at 1.6µs and 950ns intervals for the HI-574A and HI-674A respectively. This requires low output impedance and fast settling by the signal source.

The output impedance of an op amp, for example, has an open loop value which, in a closed loop, is divided by the loop gain available at a frequency of interest. The amplifier should have acceptable loop gain at 600KHz for use with the HI-X74A. To check whether the output properties of a signal source are suitable, monitor the HI-X74A's input (pin 13 or 14) with an oscilloscope while a conversion is in progress. Each of the twelve disturbances should subside in 1µs or less for the HI-574A and 500ns or less for the HI-674A. (The comparator decision is made about 1.5µs and 850ns after each code change from the SAR for the HI-574A and HI-674A, respectively.)

If the application calls for a Sample/Hold to precede the converter, it should be noted that not all Sample/Holds are compatible with the HI-574A in the manner described above. These will require an additional wideband buffer amplifier to lower their output impedance. A simpler solution is to use the Harris HA-5320 Sample/Hold, which was designed for use with the HI-574A.

HI-774

The device driving the HI-774 analog input will see a nominal load of 5kΩ (10V range) or 10kΩ (20V range). However, the other end of these input resistors may change as much as ±400mV with each bit decision. These input disturbances are caused by the internal DAC changing codes which causes a glitch on the summing junction. This creates abrupt changes in current at the analog input causing a "kick back" glitch from the input. Because the algorithm starts with the MSB, the first glitches will be the largest and get smaller as the conversion proceeds. These glitches can occur at 350ns intervals so an op amp with a low output impedance and fast settling is desirable. Ultimately the input must settle to within the window of Figure 1 at the bit decision points in order to achieve 12 bit accuracy.

The HI-774 differs from the most high-speed successive approximation type ADC's in that it does not require a high performance buffer or sample and hold. With error correction the input can settle while the conversion is underway, but only during the first 4.8µs. The input must be within 10.76% of the final value when the MSB decision is made. This occurs approximately 650ns after the conversion has been initiated. Digital error correction also loosens the bandwidth requirements of the buffer or sample and hold. As long as the input "kick back" disturbances settle within the window of Figure 1 the device will remain accurate. The combined effect of settling and the "kick back" disturbances must remain in the Figure 1 window.

If the design is being optimized for speed, the input device should have closed loop bandwidth to 3MHz, and a low output impedance (calculated by dividing the open loop output resistance by the open loop gain). If the application requires a high speed sample and hold the Harris HA-5330 or HA-5320 are recommended.

In any design the input (pin 13 or 14) should be checked during a conversion to make sure that the input stays within the correctable window of Figure 1.

Digital Error Correction

HI-774

The HI-774 features the smart successive approximation register (SSAR ™) which includes digital error correction. This has the advantage of allowing the initial input to vary within a +31 to -32 LSB window about the final value. The input can move during the first 4.8µs, after which it must remain stable within $\pm^1/_2$ LSB. With this feature a conversion can start before the input has settled completely; however, it must be within the window as described in Figure 1.

The conversion cycle starts by making the first 8-bit decisions very quickly, allowing the internal DAC to settle only to 8-bit accuracy. Then the converter goes through two error correction cycles. At this point the input must be stable within $\pm^1/_2$ LSB. These cycles correct the 8-bit word to 12-bit accuracy for any errors made (up to +16 or -32 LSBs). This is up one count or down two counts at 8-bit resolution. The converter then continues to make the 4 LSB decisions, settling out to 12-bit accuracy. The last four bits can adjust the code in the positive direction by up to 15 LSBs. This results in a total correction range of +31 to -32 LSBs. When an 8-bit conversion is performed, the input must settle to within $\pm^1/_2$ LSB at 8 bit resolution (which equals ±8 LSBs at 12-bit resolution).

With the HI-774 a conversion can be initiated before the input has completely settled, as long as it meets the constraints of the Figure 1 window. This allows the user to start conversion up to 4.8µs earlier than with a typical analog to digital converter. A typical successive approximation type ADC must have a constant input during a conversion because once a bit decision is made it is locked in and cannot change.

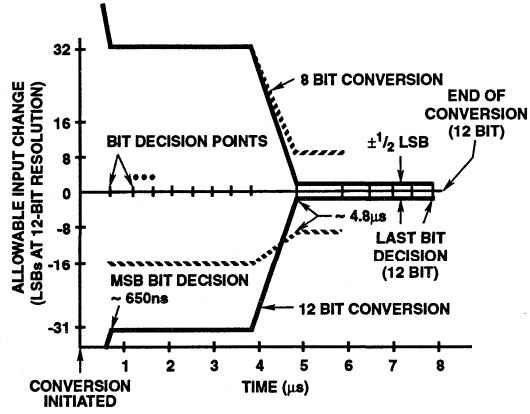
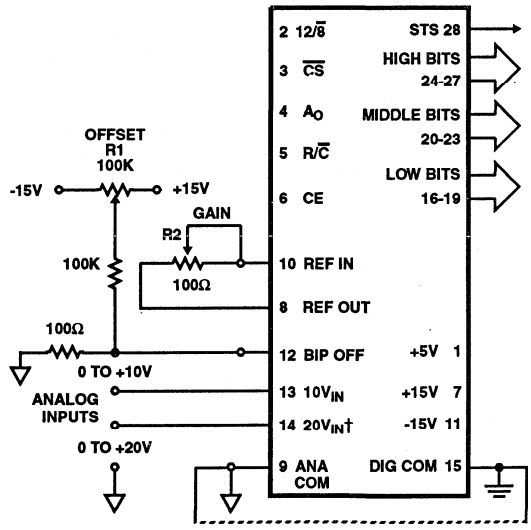
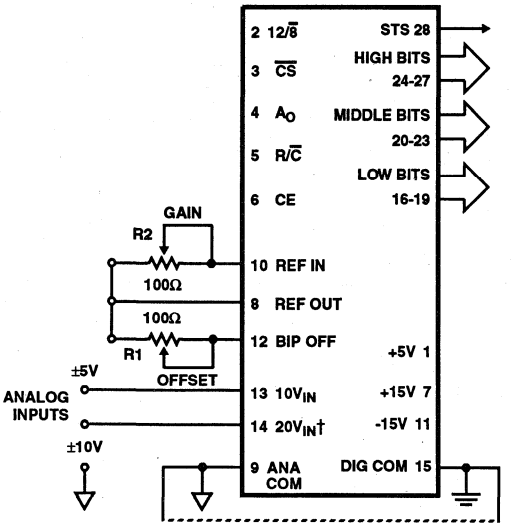


FIGURE 1. HI-774 ERROR CORRECTION WINDOW vs TIME



†When driving the 20V (pin 14) input, minimize capacitance on pin 13.

FIGURE 2. UNIPOLAR CONNECTIONS



†When driving the 20V (pin 14) input, minimize capacitance on pin 13.

FIGURE 3. BIPOLAR CONNECTIONS

Range Connections and Calibration Procedures

The HI-X74(A) is a "complete" A/D converter, meaning it is fully operational with addition of the power supply voltages, a Start Convert signal, and a few external components as shown in Figure 2 and Figure 3. Nothing more is required for most applications.

Whether controlled by a processor or operating in the stand-alone mode, the HI-X74(A) offers four standard input ranges: 0V to +10V, 0V to +20V, ±5V and ±10V. The maximum errors for gain and offset are listed under Specifications. If required, however, these errors may be adjusted to zero as explained below. Power supply and ground connections have been discussed in an earlier section.

Unipolar Connections and Calibration

Refer to Figure 2. The resistors shown* are for calibration of offset and gain. If this is not required, replace R2 with a 50Ω, 1% metal film resistor and remove the network on pin 12. Connect pin 12 to pin 9. Then, connect the analog signal to pin 13 for the 0V to 10V range, or to pin 14 for the 0V to 20V range. Inputs to +20V (5V over the power supply) are no problem - the converter operates normally.

Calibration consists of adjusting the converter's most negative output to its ideal value (offset adjustment), then, adjusting the most positive output to its ideal value (gain adjustment). To understand the procedure, note that in principle, one is setting the output with respect to the midpoint of an increment of analog input, as denoted by two adjacent code changes. Nominal value of an increment is one LSB. However, this approach is impractical because nothing "happens" at a midpoint to indicate that an adjustment is complete. Therefore, calibration is performed in terms of the observable code changes instead of the midpoint between code changes.

For example, midpoint of the first LSB increment should be positioned at the origin, with an output code of all 0's. To do this, apply an input of $+^1/_2$ LSB (+1.22mV for the 10V range; +2.44mV for the 20V range). Adjust the Offset potentiometer R1 until the first code transition flickers between 0000 0000 0000 and 0000 0000 0001.

Next, perform a Gain Adjust at positive full scale. Again, the ideal input corresponding to the last code change is applied. This is $1^1/_2$ LSB's below the nominal full scale (+9.9963V for 10V range; +19.9927V for 20V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

Bipolar Connections and Calibration

Refer to Figure 3. The gain and offset errors listed under Specifications may be adjusted to zero using potentiometers R1 and R2*. If this isn't required, either or both pots may be replaced by a 50Ω, 1% metal film resistor.

Connect the Analog signal to pin 13 for a ±5V range, or to pin 14 for a ±10V range. Calibration of offset and gain is similar to that for the unipolar ranges as discussed above. First apply a DC input voltage $^1/_2$ LSB above negative full scale (i.e., -4.9988V for the ±5V range, or -9.9976V for the ±10V range). Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage $1^1/_2$ LSB's below positive full scale (+4.9963V for ±5V range; +9.9927V for ±10V range). Adjust the Gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

*The 100Ω potentiometer R2 provides Gain Adjust for the 10V and 20V ranges. In some applications, a full scale of 10.24V (LSB equals 2.5mV) or 20.48V (LSB equals 5.0mV) is more convenient. For these, replace R2 by a 50Ω, 1% metal film resistor. Then, to provide Gain Adjust for the 10.24V range, add a 200Ω potentiometer in series with pin 13. For the 20.48V range, add a 500Ω potentiometer in series with pin 14.

Controlling the HI-X74(A)

The HI-X74(A) includes logic for direct interface to most microprocessor systems. The processor may take full control of each conversion, or the converter may operate in the "stand-alone" mode, controlled only by the R/$\overline{C}$ input. Full control consists of selecting an 8 or 12 bit conversion cycle, initiating the conversion, and reading the output data when ready-choosing either 12 bits at once or 8 followed by 4, in a left-justified format. The five control inputs are all TTL/CMOS-compatible: (12/$\overline{8}$, $\overline{CS}$, A_0, R/$\overline{C}$ and CE). Table 1 illustrates the use of these inputs in controlling the converter's operations. Also, a simplified schematic of the internal control logic is shown in Figure 7.

"Stand-Alone Operation"

The simplest control interface calls for a singe control line connected to R/$\overline{C}$. Also, CE and 12/$\overline{8}$ are wired high, $\overline{CS}$ and A_0 are wired low, and the output data appears in words of 12 bits each.

The R/$\overline{C}$ signal may have any duty cycle within (and including) the extremes shown in Figures 8 and 9. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress. Timing parameters particular to this mode of operation are listed below under "Stand-Alone Mode Timing".

HI-574A STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	-	-	ns
t_{DS}	STS Delay from R/$\overline{C}$	-	-	200	ns
t_{HDR}	Data Valid after R/$\overline{C}$ Low	25	-	-	ns
t_{HS}	STS Delay after Data Valid	300	-	1200	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	-	-	ns
t_{DDR}	Data Access Time	-	-	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

HI-674A STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	-	-	ns
t_{DS}	STS Delay from R/$\overline{C}$	-	-	200	ns
t_{HDR}	Data Valid after R/$\overline{C}$ Low	25	-	-	ns
t_{HS}	STS Delay after Data Valid	25	-	850	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	-	-	ns
t_{DDR}	Data Access Time	-	-	150	ns

Time is measured from 50% level of digital transitions. Tested with a 50pF and 3kΩ load.

HI-774 STAND-ALONE MODE TIMING

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
t_{HRL}	Low R/$\overline{C}$ Pulse Width	50	-	-	ns
t_{DS}	STS Delay from R/$\overline{C}$	-	-	200	ns
t_{HDR}	Data Valid after R/$\overline{C}$ Low	20	-	-	ns
t_{HS}	STS Delay after Data Valid	-	-	850	ns
t_{HRH}	High R/$\overline{C}$ Pulse Width	150	-	-	ns
t_{DDR}	Data Access Time	-	-	150	ns

Conversion Length

A Convert Start transition (see Table 1) latches the state of A_0, which determines whether the conversion continues for 12 bits (A_0 low) or stops with 8-bits (A_0 high). If all 12-bits are read following an 8-bit conversion, the last three LSB's will read ZERO and DB3 will read ONE. A_0 is latched because it is also involved in enabling the output buffers (see "Reading the Output Data"). No other control inputs are latched.

TABLE 1. TRUTH TABLE FOR HI-X74(A) CONTROL INPUTS

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

Conversion Start

A conversion may be initiated as shown in Table 1 by a logic transition on any of three inputs: CE, $\overline{CS}$ or R/$\overline{C}$. The last of the three to reach the correct state starts the conversion, so one, two or all three may be dynamically controlled. The nominal delay from each is the same, and if necessary, all three may change state simultaneously. To assure that a particular input controls the start of conversion, the other two should be set up at least 50ns earlier, however. See the HI-774 Timing Specifications, Convert mode.

This variety of HI-X74(A) control modes allows a simple interface in most system applications. The Convert Start timing relationships are illustrated in Figure 4.

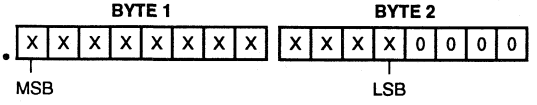
The output signal STS indicates status of the converter by going high only while a conversion is in progress. While STS is high, the output buffers remain in a high impedance state and data cannot be read. Also, an additional Start Convert will not reset the converter or reinitiate a conversion while STS is high.

Reading the Output Data

The output data buffers remain in a high impedance state until four conditions are met: R/$\overline{C}$ high, STS low, CE high and $\overline{CS}$ low. At that time, data lines become active according to the state of inputs 12/$\overline{8}$ and A_0. Timing constraints are illustrated in Figure 5.

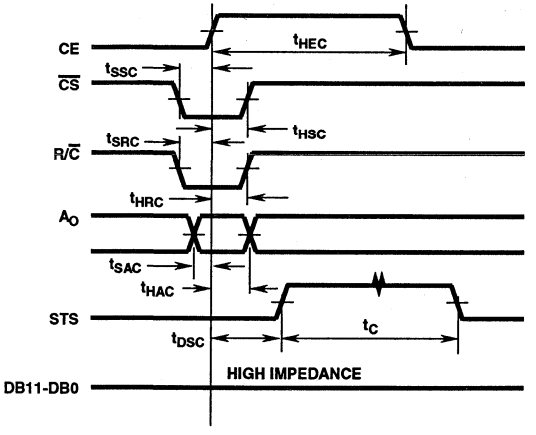
The 12/$\overline{8}$ input will be tied high or low in most applications, though it is fully TTL/CMOS-compatible. With 12/$\overline{8}$ high, all 12 output lines become active simultaneously, for interface to a 12-bit or 16-bit data bus. The A_0 input is ignored.

With 12/$\overline{8}$ low, the output is organized in two 8-bit bytes, selected one at a time by A_0. This allows an 8-bit data bus to be connected as shown in Figure 6. A_0 is usually tied to the least significant bit of the address bus, for storing the HI-X74(A) output in two consecutive memory locations. (With A_0 low, the 8 MSB's only are enabled. With A_0 high, 4 MSB's are disabled, bits 4 through 7 are forced low, and the 4 LSB's are enabled). This two byte format is considered "left justified data", for which a decimal (or binary!) point is assumed to the left of byte 1:



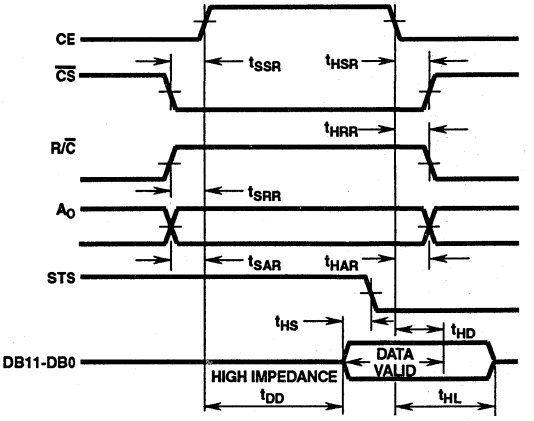
Further, A_0 may be toggled at any time without damage to the converter. Break-before-make action is guaranteed between the two data bytes, which assures that the outputs strapped together in Figure 6 will never be enabled at the same time.

A read operation usually begins after the conversion is complete and STS is low. For earliest access to the data however, the read should begin no later than (t_{DD} + t_{HS}) before STS goes low. See Figure 5.



See HI-774 Timing Specifications for more information.

FIGURE 4. CONVERT START TIMING



See HI-774 Timing Specifications for more information.

FIGURE 5. READ CYCLE TIMING

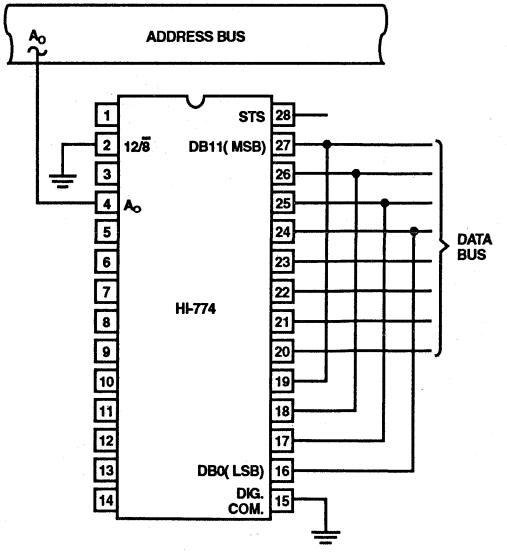


FIGURE 6. INTERFACE TO AN 8 BIT DATA BUS

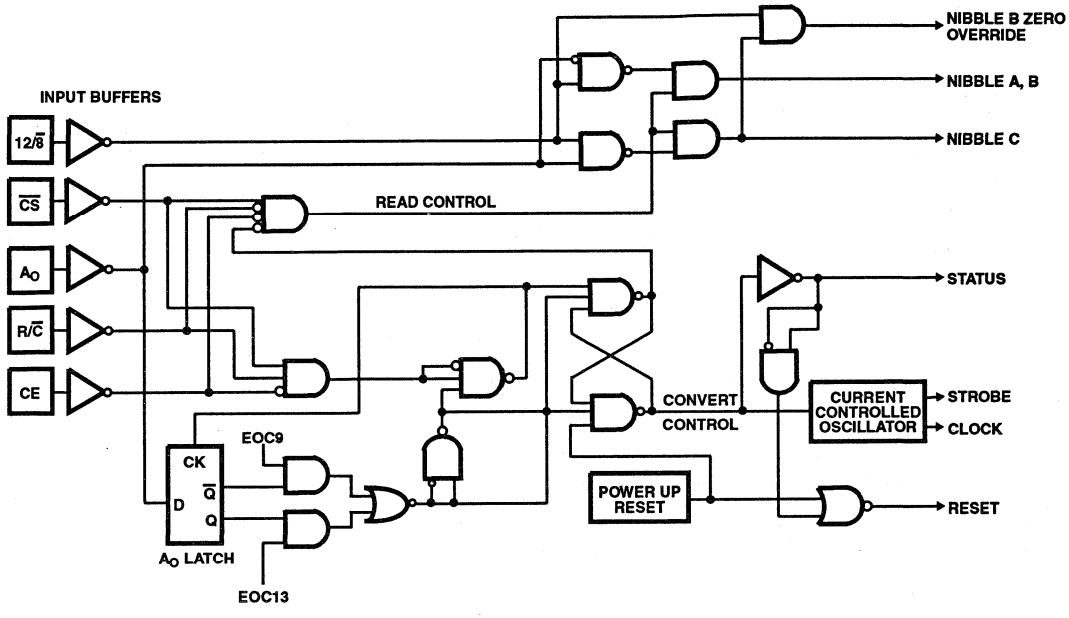


FIGURE 7. HI-774 CONTROL LOGIC

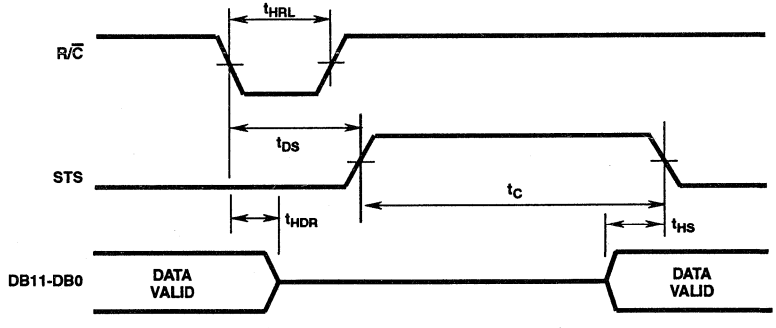


FIGURE 8. LOW PULSE FOR R/C - OUTPUTS ENABLED AFTER CONVERSION

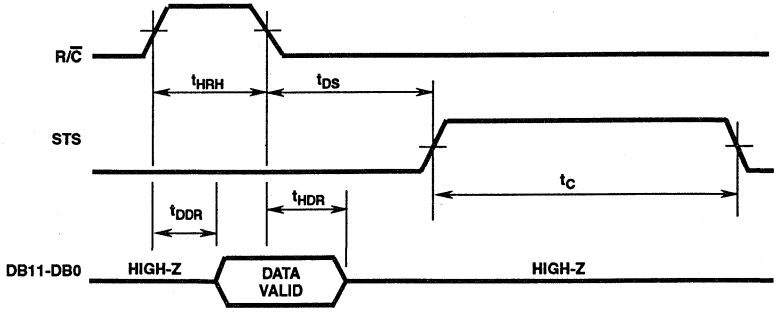


FIGURE 9. HIGH PULSE FOR R/C - OUTPUTS ENABLED WHILE R/C HIGH, OTHERWISE HIGH-Z

Die Characteristics

DIE DIMENSIONS:
Analog: 3070mm x 4610mm
Digital: 1900mm x 4510mm

METALLIZATION:
Digital Type: Nitrox
Thickness: 10kÅ ± 2kÅ

Metal 1: AL Si Cu
Thickness: 8kÅ ± 1kÅ

Metal 2: AlSiCu
Thickness: 16kÅ ± 2kÅ

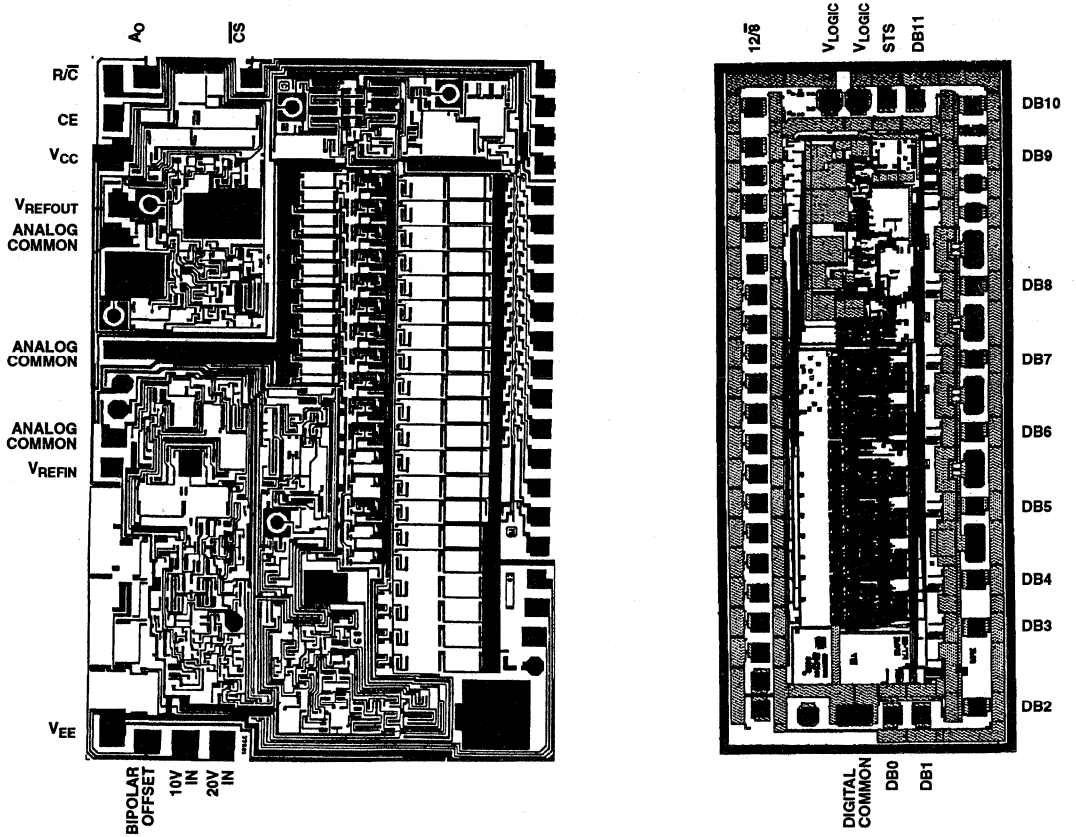
AnalogType: Al
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ± 0.5kÅ
Silox Thickness: 12kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:
1.3×10^5 A/cm^2

Metallization Mask Layout

HI-574A, HI-674A, HI-774



HARRIS SEMICONDUCTOR

HI5810

CMOS 10µs 12-Bit Sampling A/D Converter with Internal Track and Hold

December 1993

Features

- 10µs Conversion Time
- 100KSPS Throughput Rate
- Built-In Track and Hold
- Single +5V Supply Voltage
- 40mW Maximum Power Consumption
- Internal or External Clock
- 1MHz Input Bandwidth -3dB

Applications

- Remote Low Power Data Acquisition Systems
- Digital Audio
- DSP Modems
- General Purpose DSP Front End
- µP Controlled Measurement Systems
- Process Controls
- Industrial Controls

Description

The HI5810 is a fast, low power, 12-bit successive approximation analog-to-digital converter. It can operate from a single 3V to 6V supply and typically draws just 1.9mA when operating at 5V. The HI5810 features a built-in track and hold. The conversion time is as low as 10µs with a 5V supply.

The twelve data outputs feature full high speed CMOS tri-state bus driver capability, and are latched and held through a full conversion cycle. The output is user selectable: (i.e.), 12-bit, 8-bit (MSBs), and/or 4-bit (LSBs). A data ready flag, and conversion-start input complete the digital interface.

An internal clock is provided and is available as an output. The clock may also be over-driven by an external source.

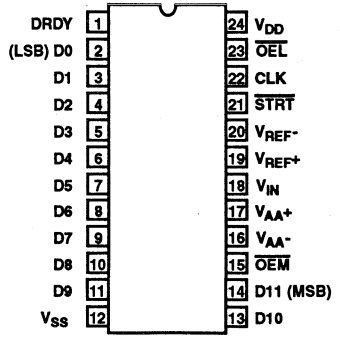
The HI5810 is rated over the full industrial temperature range and is offered in 24 lead narrow body Plastic DIP, narrow body Ceramic DIP, and Plastic SOIC packages.

Ordering Information

PART NUMBER	INL (LSB) (MAX OVER TEMP.)	TEMP. RANGE	PACKAGE
HI5810JIP	±2.5	-40°C to +85°C	24 Lead Plastic DIP
HI5810KIP	±2.0	-40°C to +85°C	24 Lead Plastic DIP
HI5810JIB	±2.5	-40°C to +85°C	24 Lead Plastic SOIC
HI5810KIB	±2.0	-40°C to +85°C	24 Lead Plastic SOIC
HI5810JIJ	±2.5	-40°C to +85°C	24 Lead Ceramic DIP
HI5810KIJ	±2.0	-40°C to +85°C	24 Lead Ceramic DIP

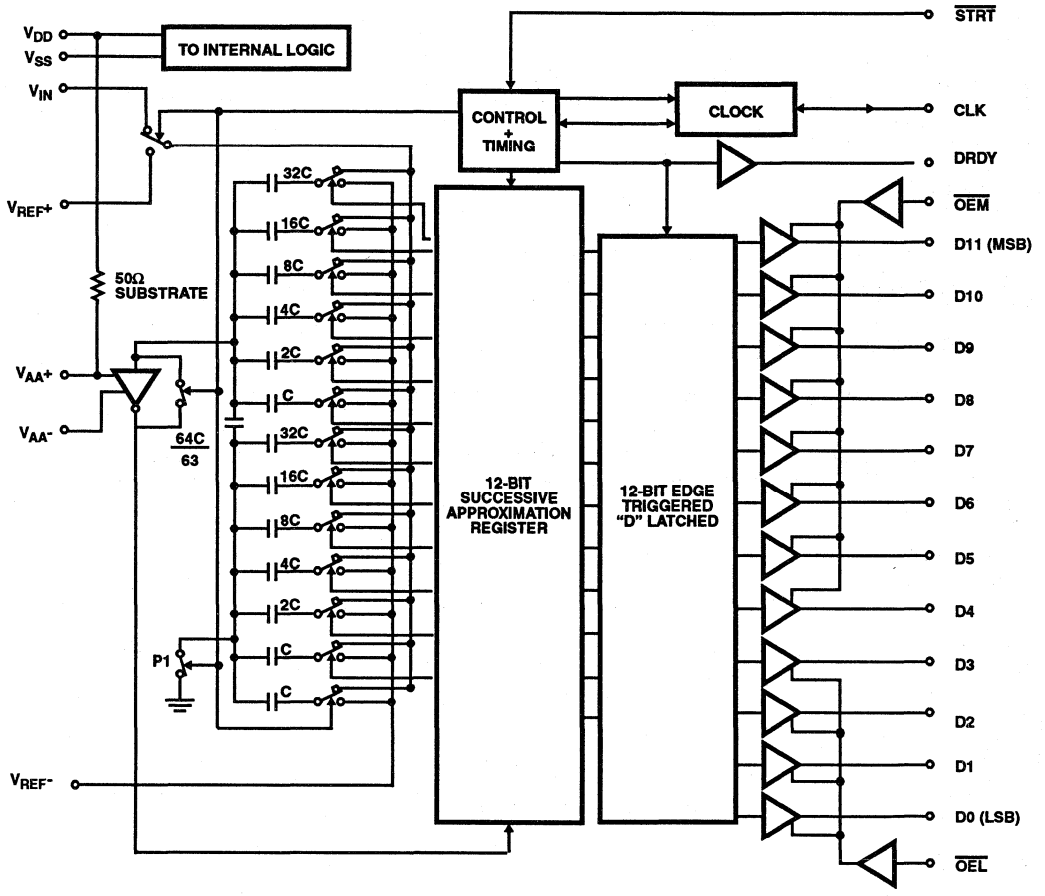
Pinout

HI5810
(PDIP, CDIP, SOIC)
TOP VIEW



File Number 3633

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage
- V_{DD} to V_{SS} ..... (V_{SS} -0.5V) < V_{DD} < +6.5V
- V_{AA}+ to V_{AA}- ..... (V_{SS} -0.5V) to (V_{SS} +6.5V)
- V_{AA}+ to V_{DD} ..... ±0.3V

Analog and Reference Inputs
- V_{IN}, V_{REF}+, V_{REF}- ..... (V_{SS} -0.3V) < V_{INA} < (V_{DD} +0.3V)

Digital I/O Pins ..... (V_{SS} -0.3V) < VI/O < (V_{DD} +0.3V)

Operating Temperature Range
- Plastic DIP, Plastic SOIC, and Ceramic DIP ..... -40°C to +85°C

Junction Temperature
- Plastic DIP and Plastic SOIC ..... +150°C
- Ceramic DIP ..... +175°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}
Plastic DIP	80°C/W
Plastic SOIC	75°C/W

Power Dissipation at +85°C (Note 1)
- Plastic DIP 0.810W
- Plastic SOIC 0.870W

Power Dissipation Derating Factor above +85°C
- Plastic DIP ..... 12mW/°C
- Plastic SOIC ..... 13mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = V_{AA}+ = 5V, V_{REF}+ = +4.608V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = External 1.5MHz, Unless Otherwise Specified.

PARAMETER		TEST CONDITION	+25°C MIN	+25°C TYP	+25°C MAX	-40°C TO +85°C MIN	-40°C TO +85°C MAX	UNITS
ACCURACY								
Resolution			12	-	-	12	-	Bits
Integral Linearity Error, INL (End Point)	J		-	-	±2.5	-	±2.5	LSB
	K		-	-	±2.0	-	±2.0	LSB
Differential Linearity Error, DNL	J		-	-	±2.0	-	±2.0	LSB
	K		-	-	±2.0	-	±2.0	LSB
Gain Error, FSE (Adjustable to Zero)	J		-	-	±3.5	-	±3.5	LSB
	K		-	-	±2.5	-	±2.5	LSB
Offset Error, VOS (Adjustable to Zero)	J		-	-	±2.5	-	±2.5	LSB
	K		-	-	±1.5	-	±1.5	LSB
DYNAMIC CHARACTERISTICS								
Signal to Noise Ratio, SINAD = RMS Signal / RMS Noise + Distortion	J	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	68.8 62.1	-	-	-	dB dB
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	71.0 63.6	-	-	-	dB dB
Signal to Noise Ratio, SNR = RMS Signal / RMS Noise	J	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	70.5 63.2	-	-	-	dB dB
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	71.5 65.0	-	-	-	dB dB
DYNAMIC CHARACTERICS (Continued)								
Total Harmonic Distortion, THD	J	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	-73.9 -68.4	-	-	-	dBc dBc
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	-80.3 69.7	-	-	-	dBc dBc

Electrical Specifications $V_{DD} = V_{AA}+ = 5V$, $V_{REF}+ = +4.608V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = External 1.5MHz, Unless Otherwise Specified. **(Continued)**

PARAMETER		TEST CONDITION	+25°C MIN	+25°C TYP	+25°C MAX	-40°C TO +85°C MIN	-40°C TO +85°C MAX	UNITS
Spurious Free Dynamic Range, SFDR	J	f_S =Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	75.4 69.2	-	-	-	dB dB
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 1.5MHz, f_{IN} = 1kHz	-	80.9 70.7	-	-	-	dB dB
ANALOG INPUT								
Input Current, Dynamic		At $V_{IN} = V_{REF}+, 0V$	-	±125	±150	-	±150	µA
Input Current, Static		Conversion Stopped	-	±0.6	±10	-	±10	µA
Input Bandwidth -3dB			-	1	-	-	-	MHz
Reference Input Current			-	160	-	-	-	µA
Input Series Resistance, R_S		In Series with Input C_{SAMPLE}	-	420	-	-	-	Ω
Input Capacitance, C_{SAMPLE}		During Sample State	-	380	-	-	-	pF
Input Capacitance, C_{HOLD}		During Hold State	-	20	-	-	-	pF
DIGITAL INPUTS $\overline{OEL}$, $\overline{OEM}$, $\overline{STRT}$								
High-Level Input Voltage, V_{IH}			2.4	-	-	2.4	-	V
Low-Level Input Voltage, V_{IL}			-	-	0.8	-	0.8	V
Input Leakage Current, I_{IL}		Except CLK, $V_{IN} = 0V, 5V$	-	-	±10	-	±10	µA
Input Capacitance, C_{IN}			-	10	-	-	-	pF
DIGITAL OUTPUTS								
High-Level Output Voltage, V_{OH}		I_{SOURCE} = -400µA	4.6	-	-	4.6	-	V
Low-Level Output Voltage, V_{OL}		I_{SINK} = 1.6mA	-	-	0.4	-	0.4	V
Tri-state Leakage, I_{OZ}		Except DRDY, $V_{OUT} = 0V, 5V$	-	-	±10	-	±10	µA
Output Capacitance, C_{OUT}		Except DRDY	-	20	-	-	-	pF
CLOCK								
High-Level Output Voltage, V_{OH}		I_{SOURCE} = -100µA (Note 2)	4	-	-	4	-	V
Low-Level Output Voltage, V_{OL}		I_{SINK} = 100µA (Note 2)	-	-	1	-	1	V
Input Current		CLK Only, $V_{IN} = 0V, 5V$	-	-	±5	-	±5	mA
TIMING								
Conversion Time ($t_{CONV} + t_{ACQ}$) (Includes Acquisition Time)			10	-	-	10	-	µs
Clock Frequency		Internal Clock, (CLK = Open)	200	300	400	150	500	kHz
		External CLK (Note 2)	0.05	-	2.0	-	-	MHz
Clock Pulse Width, t_{LOW}, t_{HIGH}		External CLK (Note 2)	100	-	-	100	-	ns

Electrical Specifications $V_{DD} = V_{AA}+ = 5V$, $V_{REF}+ = +4.608V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = External 1.5MHz, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITION	+25°C			-40°C TO +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
Aperture Delay, t_DAPR	(Note 2)	-	35	50	-	70	ns
Clock to Data Ready Delay, $t_{D1}DRDY$	(Note 2)	-	105	150	-	180	ns
Clock to Data Ready Delay, $t_{D2}DRDY$	(Note 2)	-	100	160	-	195	ns
Start Removal Time, $t_R\overline{STRT}$	(Note 2)	75	30	-	75	-	ns
Start Setup Time, $t_{SU}\overline{STRT}$	(Note 2)	85	60	-	100	-	ns
Start Pulse Width, $t_W\overline{STRT}$	(Note 2)	10	4	-	15	-	ns
Start to Data Ready Delay, t_{D3} DRDY	(Note 2)	-	65	105	-	120	ns
Clock Delay from Start, $t_D\overline{STRT}$	(Note 2)	-	60	-	-	-	ns
Output Enable Delay, t_{EN}	(Note 2)	-	20	30	-	50	ns
Output Disabled Delay, t_{DIS}	(Note 2)	-	80	95	-	120	ns
POWER SUPPLY CHARACTERISTICS							
Supply Current, $I_{DD} + I_{AA}$		-	2.6	8	-	8.5	mA

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Parameter guaranteed by design or characterization, not production tested.

Timing Diagrams

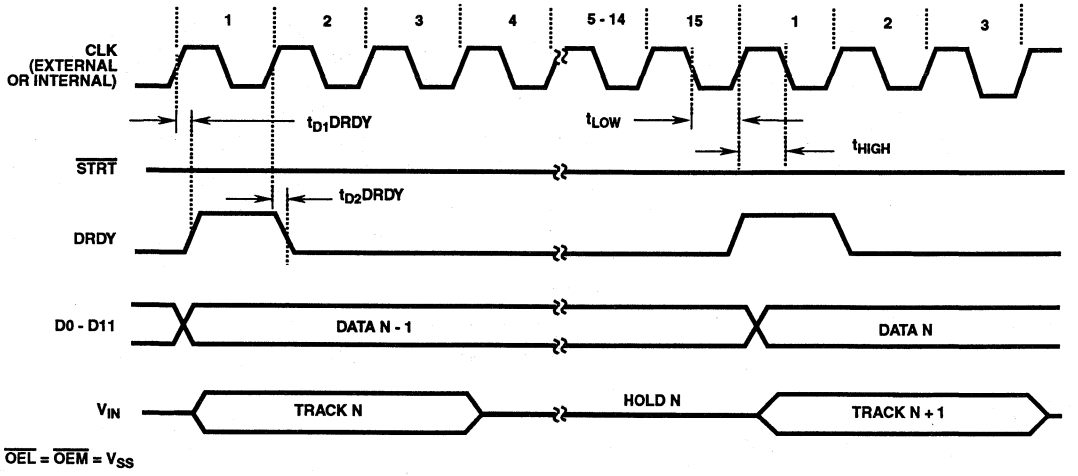


FIGURE 1. CONTINUOUS CONVERSION MODE

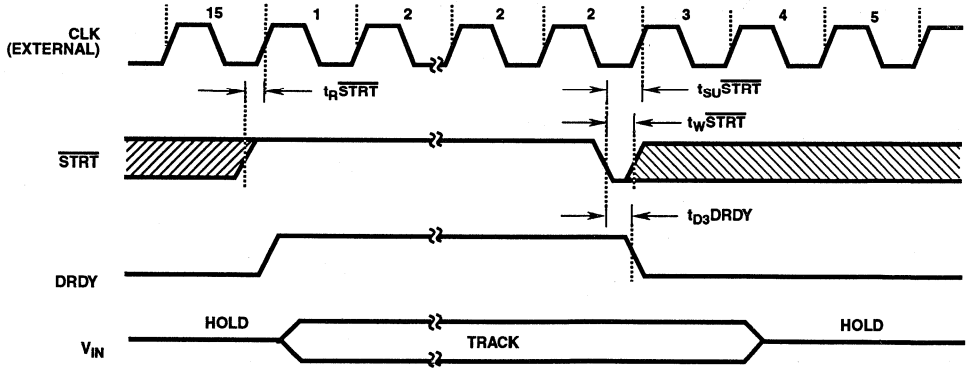


FIGURE 2. SINGLE SHOT MODE EXTERNAL CLOCK

Timing Diagrams (Continued)

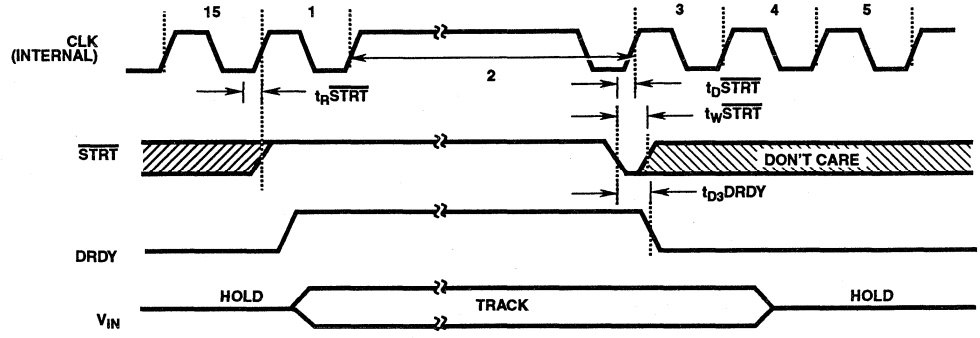


FIGURE 3. SINGLE SHOT MODE INTERNAL CLOCK

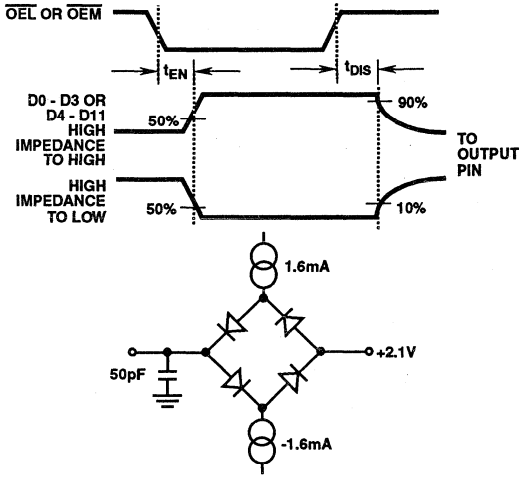


FIGURE 4. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

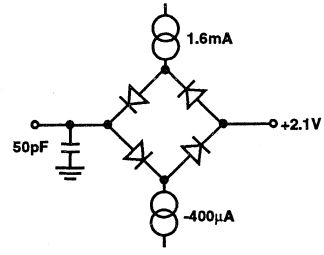


FIGURE 5. TIMING LOAD CIRCUIT

Typical Performance Curves

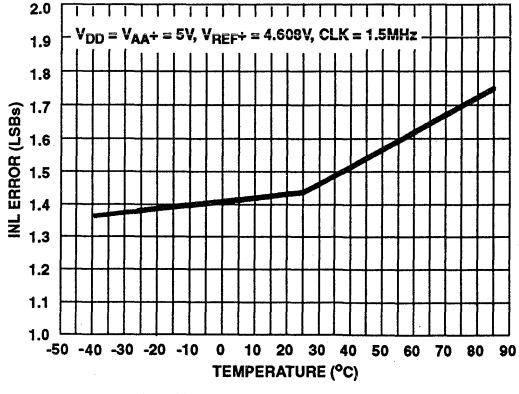


FIGURE 6. INL vs TEMPERATURE

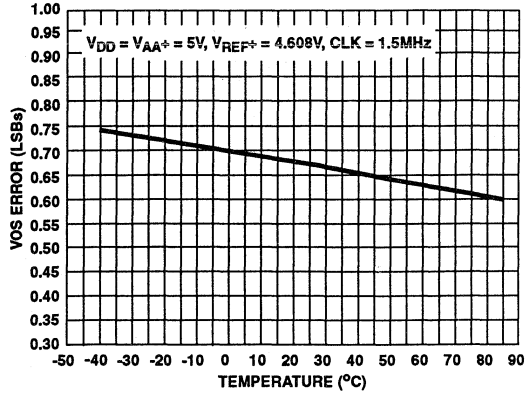


FIGURE 7. OFFSET ERROR vs TEMPERATURE

Typical Performance Curves (Continued)

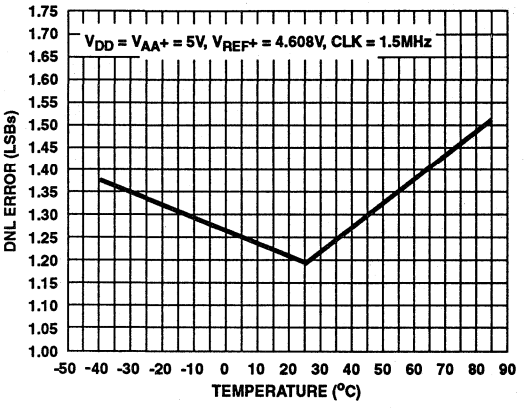


FIGURE 8. DNL vs TEMPERATURE

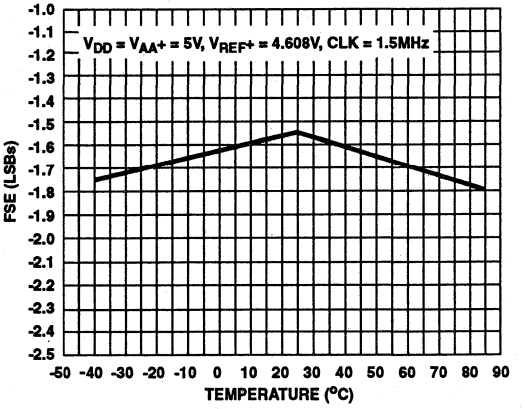


FIGURE 9. FULL SCALE ERROR vs TEMPERATURE

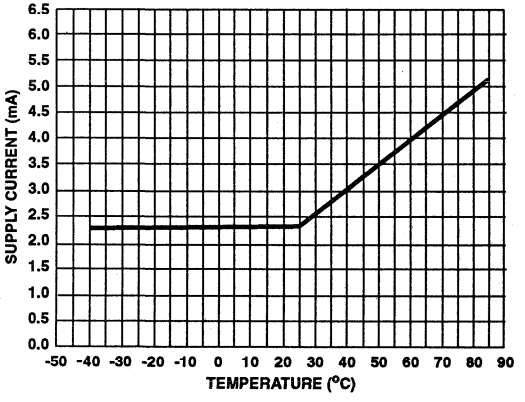


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

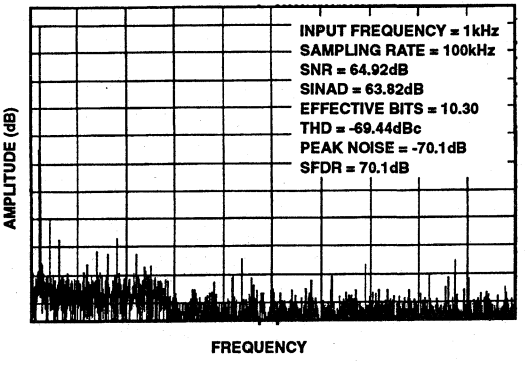


FIGURE 11. FFT SPECTRUM

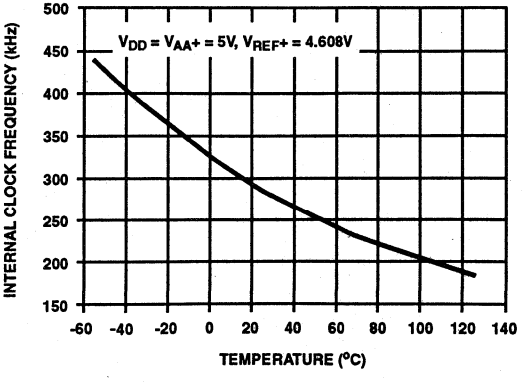


FIGURE 12. INTERNAL CLOCK FREQUENCY vs TEMPERATURE

TABLE 1. PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	DRDY	Output flag signifying new data is available. Goes high at end of clock period 15. Goes low when new conversion is started.
2	D0	Bit-0 (Least significant bit, LSB)
3	D1	Bit-1
4	D2	Bit-2
5	D3	Bit-3
6	D4	Bit-4
7	D5	Bit-5
8	D6	Bit-6
9	D7	Bit-7
10	D8	Bit-8
11	D9	Bit-9
12	V_{SS}	Digital ground, (0V).
13	D10	Bit-10
14	D11	Bit-11 (Most significant bit, MSB)
15	$\overline{OEM}$	Tri-state enable for D4-D11. Active low input.
16	V_{AA}-	Analog ground, (0V).
17	V_{AA}+	Analog positive supply. (+5V) (See text)
18	V_{IN}	Analog input.
19	V_{REF}+	Reference voltage positive input, sets 4095 code end of input range.
20	V_{REF}-	Reference voltage negative input, sets 0 code end of input range.
21	$\overline{STRT}$	Start conversion input active low, recognized after end of clock period 15.
22	CLK	CLK input or output. Conversion functions are synchronized to positive going edge. (See text)
23	$\overline{OEL}$	Tri-state enable for D0 D3. Active low input.
24	V_{DD}	Digital positive supply (+5V).

Theory of Operation

HI5810 is a CMOS 12-bit Analog-to-Digital Converter that uses capacitor charge balancing to successively approximate the analog input. A binarily weighted capacitor network forms the A/D heart of the device. See the block diagram for the HI5810.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, V_{REF}+ or V_{REF}-.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input and the comparator is being auto balanced at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input; the one representing the MSB (D11) is connected to the V_{REF}+ terminal; and the remaining capacitors to V_{REF}-. The capacitor common node, after the charges balance out, will indicate whether the input was above 1/2 of (V_{REF}+ - V_{REF}-). At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to V_{REF}+ (if the comparator was high) or returned to V_{REF}-. This allows the next comparison to be at either 3/4 or 1/4 of (V_{REF}+ - V_{REF}-).

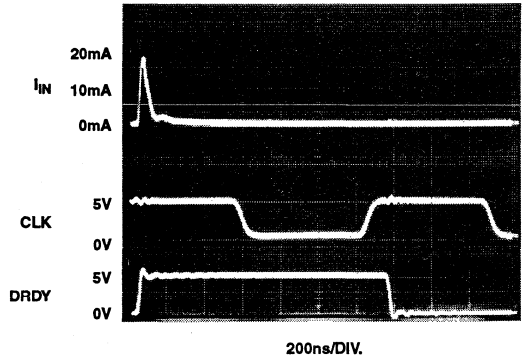
At the end of periods 5 through 14, capacitors representing D10 through D1 are tested, the result stored, and each capacitor either left at V_{REF}+ or at V_{REF}-.

At the end of the 15th period, when the LSB (D0) capacitor is tested, (D0) and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data ready output goes active. The conversion cycle is now complete.

Analog Input

The analog input pin is a predominately capacitive load that changes between the track and hold periods of the conversion cycle. During hold, clock period 4 through 15, the input loading is leakage and stray capacitance, typically less than 5µA and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the current spike by the end of the tracking period as shown in Figure 13. The amount of charge is dependent on supply and input voltages. The average current is also proportional to clock frequency.



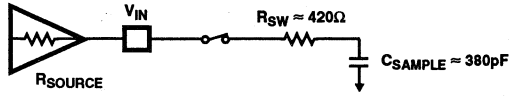
CONDITIONS: V_{DD} = V_{AA}+ = 5.0V, V_{REF}+ = 4.608V, V_{IN} = 4.608V, CLK = 750kHz, T_A = +25°C

FIGURE 13. TYPICAL ANALOG INPUT CURRENT

As long as these current spikes settle completely by end of the signal acquisition period, converter accuracy will be preserved. The analog input is tracked for 3 clock cycles. With an external clock of 1.5MHz the track period is 2µs.

A simplified analog input model is presented in Figure 14. During tracking, the A/D input (V_{IN}) typically appears as a 380pF capacitor being charged through a 420Ω internal switch resistance. The time constant is 160ns. To charge this capacitor from an external "zero Ω" source to 0.5 LSB (1/8192), the charging time must be at least 9 time constants or 1.4µs. The maximum source impedance (R_{SOURCE} Max) for a 2µs acquisition time settling to within 0.5 LSB is 164Ω.

If the clock frequency was slower, or the converter was not restarted immediately (causing a longer sample time), a higher source impedance could be tolerated.



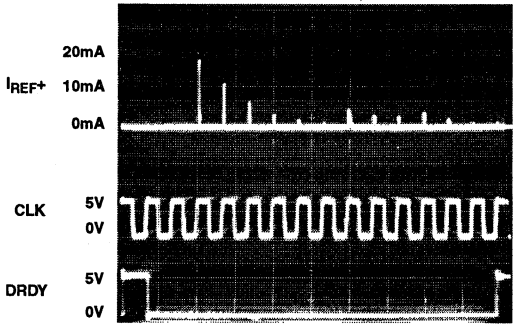
$$R_{SOURCE\ (MAX)} = \frac{-t_{ACQ}}{C_{SAMPLE} \ln [2^{-(N+1)}]} - R_{SW}$$

FIGURE 14. ANALOG INPUT MODEL IN TRACK MODE

Reference Input

The reference input $V_{REF}+$ should be driven from a low impedance source and be well decoupled.

As shown in Figure 15, current spikes are generated on the reference pin during each bit test of the successive approximation part of the conversion cycle as the charge balancing capacitors are switched between $V_{REF}-$ and $V_{REF}+$ (clock periods 5 - 14). These current spikes must settle completely during each bit test of the conversion to not degrade the accuracy of the converter. Therefore $V_{REF}+$ and $V_{REF}-$ should be well bypassed. Reference input $V_{REF}-$ is normally connected directly to the analog ground plane. If $V_{REF}-$ is biased for nulling the converters offset it must be stable during the conversion cycle.



CONDITIONS: $V_{DD} = V_{AA}+ = 5.0V$, $V_{REF}+ = 4.608V$, $V_{IN} = 2.3V$, CLK = 750kHz, $T_A = +25°C$

FIGURE 15. TYPICAL REFERENCE INPUT CURRENT

The HI5810 is specified with a 4.608V reference, however, it will operate with a reference down to 3V having a slight degradation in performance.

Full Scale and Offset Adjustment

In many applications the accuracy of the HI5810 would be sufficient without any adjustments. In applications where accuracy is of utmost importance full scale and offset errors may be adjusted to zero.

The $V_{REF}+$ and $V_{REF}-$ pins reference the two ends of the analog input range and may be used for offset and full scale adjustments. In a typical system the $V_{REF}-$ might be returned to a clean ground, and the offset adjustment done on an input amplifier. $V_{REF}+$ would then be adjusted to null out the full scale error. When this is not possible, the $V_{REF}-$ input can be adjusted to null the offset error, however, $V_{REF}-$ must be well decoupled.

Full scale and offset error can also be adjusted to zero in the signal conditioning amplifier driving the analog input (V_{IN}).

Control Signal

The HI5810 may be synchronized from an external source by using the $\overline{STRT}$ (Start Conversion) input to initiate conversion, or if $\overline{STRT}$ is tied low, may be allowed to free run. Each conversion cycle takes 15 clock periods.

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by T_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by T_{D1}DRDY) after the start of clock period 1, and returns low (specified by T_{D2}DRDY) after the start of clock period 2.

The 12 data bits are available in parallel on tri-state bus driver outputs. When low, the $\overline{OEM}$ input enables the most significant byte (D4 through D11) while the $\overline{OEL}$ input enables the four least significant bits (D0 - D3). T_{EN} and T_{DIS} specify the output enable and disable times.

If the output data is to be latched externally, either the trailing edge of data ready or the next falling edge of the clock after data ready goes high can be used.

When $\overline{STRT}$ input is used to initiate conversions, operation is slightly different depending on whether an internal or external clock is used.

Figure 3 illustrates operation with an internal clock. If the $\overline{STRT}$ signal is removed (at least $T_R\overline{STRT}$) before clock period 1, and is not reapplied during that period, the clock will shut off after entering period 2. The input will continue to track and the DRDY output will remain high during this time.

A low signal applied to $\overline{STRT}$ (at least $T_W\overline{STRT}$ wide) can now initiate a new conversion. The $\overline{STRT}$ signal (after a delay of ($T_D\overline{STRT}$)) causes the clock to restart.

Depending on how long the clock was shut off, the low portion of clock period 2 may be longer than during the remaining cycles.

The input will continue to track until the end of period 3, the same as when free running.

Figure 2 illustrates the same operation as above but with an external clock. If $\overline{STRT}$ is removed (at least $T_R\overline{STRT}$) before clock period 2, a low signal applied to $\overline{STRT}$ will drop the DRDY flag as before, and with the first positive going clock edge that meets the ($T_{SU}\overline{STRT}$) setup time, the converter will continue with clock period 3.

Clock

The HI5810 can operate either from its internal clock or from one externally supplied. The CLK pin functions either as the clock output or input. All converter functions are synchronized with the rising edge of the clock signal.

Figure 16 shows the configuration of the internal clock. The clock output drive is low power: if used as an output, it should not have more than 1 CMOS gate load applied, and stray wiring capacitance should be kept to a minimum.

The internal clock will shut down if the A/D is not restarted after a conversion. The clock could also be shut down with an open collector driver applied to the CLK pin. This should only be done during the sample portion (the first three clock periods) of a conversion cycle, and might be useful for using the device as a digital sample and hold.

If an external clock is supplied to the CLK pin, it must have sufficient drive to overcome the internal clock source. The external clock can be shut off, but again, only during the sample portion of a conversion cycle. At other times, it must be above the minium frequency shown in the specifications. In the above two cases, a further restriction applies in that the clock should not be shut off during the third sample period for more than 1ms. This might cause an internal charge pump voltage to decay.

If the internal or external clock was shut off during the conversion time (clock cycles 4 through 15) of the A/D, the output might be invalid due to balancing capacitor droop.

An external clock must also meet the minimum T_{LOW} and T_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

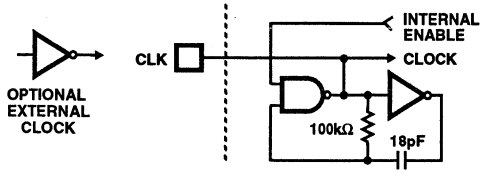


FIGURE 16. INTERNAL CLOCK CIRCUITRY

Power Supplies and Grounding

V_{DD} and V_{SS} are the digital supply pins: they power all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for V_{AA}+, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}. Input transients above V_{DD} or below V_{SS} will get steered to the digital supplies.

The V_{AA}+ and V_{AA}- terminals supply the charge balancing comparator only. Because the comparator is autobalanced between conversions, it has good low frequency supply rejection. It does not reject well at high frequencies however; V_{AA}- should be returned to a clean analog ground and V_{AA}+ should be RC decoupled from the digital supply as shown in Figure 17.

There is approximately 50Ω of substrate impedance between V_{DD} and V_{AA}+. This can be used, for example, as part of a low pass RC filter to attenuate switching supply noise. A 10µF capacitor from V_{AA}+ to ground would attenuate 30kHz noise by approximately 40dB. Note that back-to-back diodes should be placed from V_{DD} to V_{AA}+ to handle supply to capacitor turn-on or turn-off current spikes.

Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the A/D. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is than transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See typical performance characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured RMS signal to RMS sum of noise at a specified input and sampling frequency. The noise is the RMS sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76) dB. For an ideal 12-bit converter the SNR is 74dB. Differential and integral linearity errors will degrade SNR.

$$SNR = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Total Noise Power}}$$

Signal-To-Noise + Distortion Ratio

SINAD is the measured RMS signal to RMS sum of noise plus harmonic power and is expressed by the following.

$$SINAD = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (2nd - 6th)}}$$

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data;

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of the second through sixth harmonic components to the fundamental RMS signal for a specified input and sampling frequency.

$$THD = 10 \log \frac{\text{Total Harmonic Power (2nd - 6th Harmonic)}}{\text{Sinewave Signal Power}}$$

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

$$SFDR = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Highest Spurious Signal Power}}$$

TABLE 2. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE† V_{REF+} = 4.608V V_{REF-} = 0.0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB											LSB
			D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale (FS)	4.6069	4095	1	1	1	1	1	1	1	1	1	1	1	1
FS - 1 LSB	4.6058	4094	1	1	1	1	1	1	1	1	1	1	1	0
3/4 FS	3.4560	3072	1	1	0	0	0	0	0	0	0	0	0	0
1/2 FS	2.3040	2048	1	0	0	0	0	0	0	0	0	0	0	0
1/4 FS	1.1520	1024	0	1	0	0	0	0	0	0	0	0	0	0
1 LSB	0.001125	1	0	0	0	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0	0	0	0

†The voltages listed above represent the ideal lower transition of each output code shown as a function of the reference voltage.

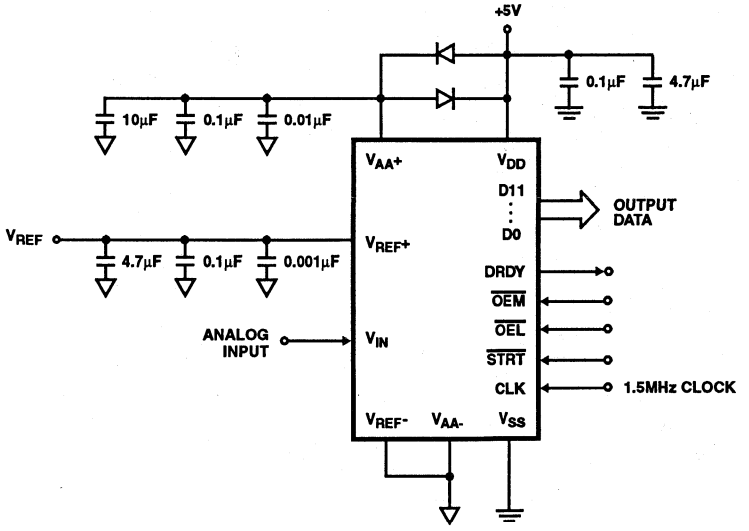


FIGURE 17. GROUND AND SUPPLY DECOUPLING

Die Characteristics

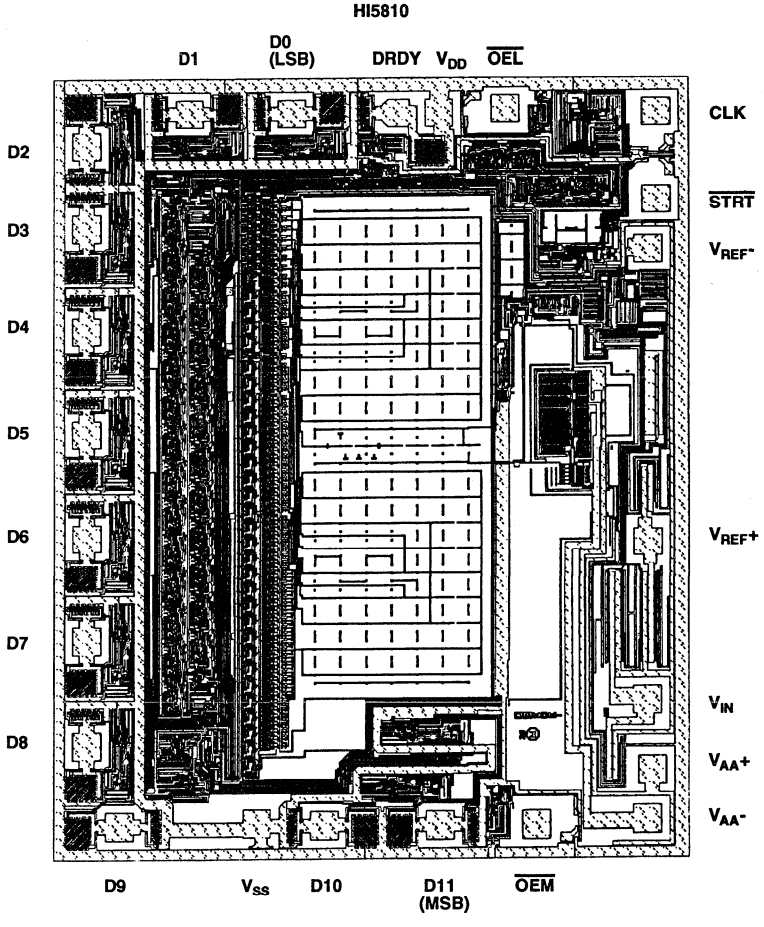
DIE DIMENSIONS:
3200µm x 3940µm

METALLIZATION:
Type: Al Si
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: PSG
Thickness: 13kÅ ± 2.5kÅ

WORST CASE CURRENT DENSITY:
1.84×10^5 A/cm^2

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HI5812

CMOS 20µs 12-Bit Sampling A/D Converter with Internal Track and Hold

December 1993

Features

- 20µs Conversion Time
- 50KSPS Throughput Rate
- Built-In Track and Hold
- Guaranteed No Missing Codes Over Temperature
- Single +5V Supply Voltage
- 25mW Maximum Power Consumption
- Internal or External Clock

Applications

- Remote Low Power Data Acquisition Systems
- Digital Audio
- DSP Modems
- General Purpose DSP Front End
- µP Controlled Measurement System
- Professional Audio Positioner/Fader

Description

The HI5812 is a fast, low power, 12-bit successive approximation analog-to-digital converter. It can operate from a single 3V to 6V supply and typically draws just 1.9mA when operating at 5V. The HI5812 features a built-in track and hold. The conversion time is as low as 15µs with a 5V supply.

The twelve data outputs feature full high speed CMOS tri-state bus driver capability, and are latched and held through a full conversion cycle. The output is user selectable: (i.e.) 12-bit, 8-bit (MSBs), and/or 4-bit (LSBs). A data ready flag, and conversion-start inputs complete the digital interface.

An internal clock is provided and is available as an output. The clock may also be over-driven by an external source.

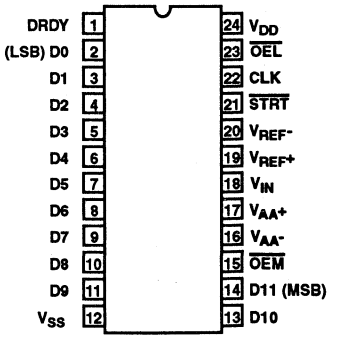
The HI5812 is rated over the full industrial temperature range and is offered in 24 lead narrow body Plastic DIP, narrow body Ceramic DIP, and Plastic SOIC packages.

Ordering Information

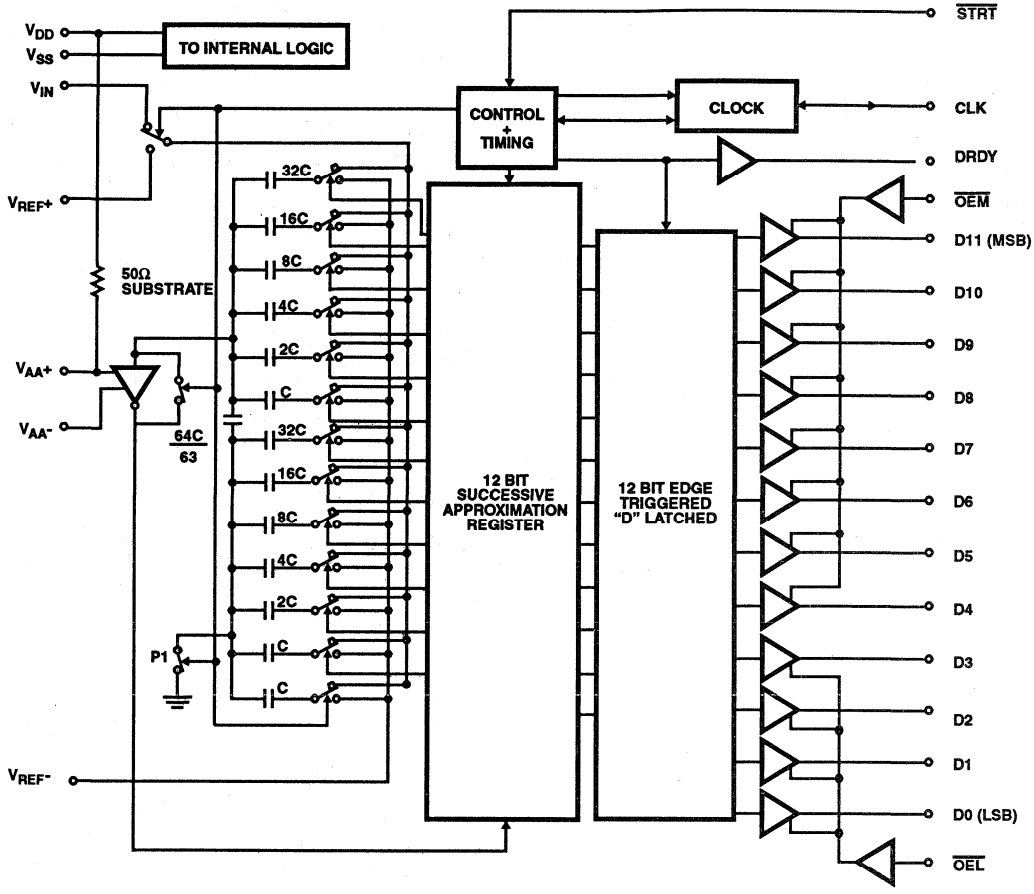
PART NUMBER	INL (LSB) (MAX OVER TEMP.)	TEMP. RANGE	PACKAGE
HI5812JIP	±1.5	-40°C to +85°C	24 Lead Plastic DIP
HI5812KIP	±1.0	-40°C to +85°C	24 Lead Plastic DIP
HI5812JIB	±1.5	-40°C to +85°C	24 Lead Plastic SOIC
HI5812KIB	±1.0	-40°C to +85°C	24 Lead Plastic SOIC
HI5812JIJ	±1.5	-40°C to +85°C	24 Lead Ceramic DIP
HI5812KIJ	±1.0	-40°C to +85°C	24 Lead Ceramic DIP

Pinout

HI5812 (PDIP, CDIP, SOIC)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage
- V_{DD} to V_{SS} ..... (V_{SS} -0.5V) < V_{DD} < +6.5V
- V_{AA}+ to V_{AA}- ..... (V_{SS} -0.5V) to (V_{SS} +6.5V)
- V_{AA}+ to V_{DD} ..... ±0.3V

Analog and Reference Inputs
- V_{IN}, V_{REF+}, V_{REF-} ..... (V_{SS} -0.3V) < V_{INA} < (V_{DD} +0.3V)

Digital I/O Pins ..... (V_{SS} -0.3V) < VI/O < (V_{DD} +0.3V)

Operating Temperature Range
- Plastic DIP, Plastic SOIC, and CERDIP ..... -40°C to +85°C

Junction Temperature
- Plastic Dip and Plastic SOIC ..... +150°C
- Ceramic DIP ..... +175°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}
Plastic DIP	80°C/W
Plastic SOIC	75°C/W
Package Power Dissipation at +85°C (Note 1)	
Plastic DIP	0.810W
Plastic SOIC	0.870W
Power Dissipation Derating Factor above +85°C	
Plastic DIP	12mW/°C
Plastic SOIC	13mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = V_{AA}+ = 5V, V_{REF}+ = +4.608V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = External 750kHz, Unless Otherwise Specified.

PARAMETER		TEST CONDITION	+25°C MIN	+25°C TYP	+25°C MAX	-40°C TO +85°C MIN	-40°C TO +85°C MAX	UNITS
ACCURACY								
Resolution			12	-	-	12	-	Bits
Integral Linearity Error, INL (End Point)	J		-	-	±1.5	-	±1.5	LSB
	K		-	-	±1.0	-	±1.0	LSB
Differential Linearity Error, DNL	J		-	-	±2.0	-	±2.0	LSB
	K		-	-	±1.0	-	±1.0	LSB
Gain Error, FSE (Adjustable to Zero)	J		-	-	±3.0	-	±3.0	LSB
	K		-	-	±2.5	-	±2.5	LSB
Offset Error, VOS (Adjustable to Zero)	J		-	-	±2.0	-	±2.0	LSB
	K		-	-	±1.0	-	±1.0	LSB
Power Supply Rejection, PSRR		V_{REF} = 4V	-	-	-	-	-	-
Offset Error PSRR		V_{DD} = V_{AA}+ = 5V ±5%		0.1	±0.5		±0.5	LSB
Gain Error PSRR		V_{DD} = V_{AA}+ = 5V ±5%		0.1	±0.5		±0.5	LSB
DYNAMIC CHARACTERISTICS								
Signal to Noise Ratio, SINAD = RMS Signal / RMS Noise + Distortion	J	f_S = Internal Clock, f_{IN} = 1kHz	-	68.8	-	-	-	dB
		f_S = 750kHz, f_{IN} = 1kHz		69.2				dB
	K	f_S = Internal Clock, f_{IN} = 1kHz	-	71.0	-	-	-	dB
		f_S = 750kHz, f_{IN} = 1kHz		71.5				dB
Signal to Noise Ratio, SNR = RMS Signal / RMS Noise	J	f_S = Internal Clock, f_{IN} = 1kHz	-	70.5	-	-	-	dB
		f_S = 750kHz, f_{IN} = 1kHz		71.1				dB
	K	f_S = Internal Clock, f_{IN} = 1kHz	-	71.5	-	-	-	dB
		f_S = 750kHz, f_{IN} = 1kHz		72.1				dB

Electrical Specifications $V_{DD} = V_{AA}+ = 5V$, $V_{REF}+ = +4.608V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = External 750kHz, Unless Otherwise Specified. **(Continued)**

PARAMETER		TEST CONDITION	+25°C MIN	+25°C TYP	+25°C MAX	-40°C TO +85°C MIN	-40°C TO +85°C MAX	UNITS
Total Harmonic Distortion, THD	J	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz	-	-73.9 -73.8	-	-	-	dBc dBc
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz		-80.3 -79.0	-	-	-	dBc dBc
Spurious Free Dynamic Range, SFDR	J	f_S =Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz	-	-75.4 -75.1	-	-	-	dB dB
	K	f_S = Internal Clock, f_{IN} = 1kHz f_S = 750kHz, f_{IN} = 1kHz	-	-80.9 -79.6	-	-	-	dB dB
ANALOG INPUT								
Input Current, Dynamic		At $V_{IN} = V_{REF}+$, 0V	-	±50	±100	-	±100	µA
Input Current, Static		Conversion Stopped	-	±0.4	±10	-	±10	µA
Input Bandwidth -3dB			-	1	-	-	-	MHz
Reference Input Current			-	160	-	-	-	µA
Input Series Resistance, R_S		In Series with Input C_{SAMPLE}	-	420	-	-	-	Ω
Input Capacitance, C_{SAMPLE}		During Sample State	-	380	-	-	-	pF
Input Capacitance, C_{HOLD}		During Hold State	-	20	-	-	-	pF
DIGITAL INPUTS $\overline{OEL}$, $\overline{OEM}$, $\overline{STRT}$								
High-Level Input Voltage, V_{IH}			2.4	-	-	2.4	-	V
Low-Level Input Voltage, V_{IL}			-	-	0.8	-	0.8	V
Input Leakage Current, I_{IL}		Except CLK, V_{IN} = 0V, 5V	-	-	±10	-	±10	µA
Input Capacitance, C_{IN}			-	10	-	-	-	pF
DIGITAL OUTPUTS								
High-Level Output Voltage, V_{OH}		I_{SOURCE} = -400µA	4.6	-	-	4.6	-	V
Low-Level Output Voltage, V_{OL}		I_{SINK} = 1.6mA	-	-	0.4	-	0.4	V
Tri-state Leakage, I_{OZ}		Except DRDY, V_{OUT}= 0V, 5V	-	-	±10	-	±10	µA
Output Capacitance, C_{OUT}		Except DRDY	-	20	-	-	-	pF
CLOCK								
High-Level Output Voltage, V_{OH}		I_{SOURCE} = -100µA (Note 2)	4	-	-	4	-	V
Low-Level Output Voltage, V_{OL}		I_{SINK} = 100µA (Note 2)	-	-	1	-	1	V
Input Current		CLK Only, V_{IN} = 0V, 5V	-	-	±5	-	±5	mA
TIMING								

Electrical Specifications $V_{DD} = V_{AA}+ = 5V$, $V_{REF}+ = +4.608V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = External 750kHz, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITION	+25°C			-40°C TO +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
Conversion Time ($t_{CONV} + t_{ACQ}$) (Includes Acquisition Time)		20	-	-	20	-	µs
Clock Frequency	Internal Clock, (CLK = Open)	200	300	400	150	500	kHz
	External CLK (Note 2)	0.05	2	1.5	0.05	1.5	MHz
Clock Pulse Width, t_{LOW}, t_{HIGH}	External CLK (Note 2)	100	-	-	100	-	ns
Aperture Delay, t_DAPR	(Note 2)	-	35	50	-	70	ns
Clock to Data Ready Delay, t_{D1}DRDY	(Note 2)	-	105	150	-	180	ns
Clock to Data Ready Delay, t_{D2}DRDY	(Note 2)	-	100	160	-	195	ns
Start Removal Time, $t_R\overline{STRT}$	(Note 2)	75	30	-	75	-	ns
Start Setup Time, $t_{SU}\overline{STRT}$	(Note 2)	85	60	-	100	-	ns
Start Pulse Width, $t_W\overline{STRT}$	(Note 2)	10	4	-	15	-	ns
Start to Data Ready Delay, t_{D3} DRDY	(Note 2)	-	65	105	-	120	ns
Clock Delay from Start, $t_D\overline{STRT}$	(Note 2)	-	60	-	-	-	ns
Output Enable Delay, t_{EN}	(Note 2)	-	20	30	-	50	ns
Output Disabled Delay, t_{DIS}	(Note 2)	-	80	95	-	120	ns
POWER SUPPLY CHARACTERISTICS							
Supply Current, $I_{DD} + I_{AA}$		-	1.9	5	-	8	mA

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Parameter guaranteed by design or characterization, not production tested.

Timing Diagrams

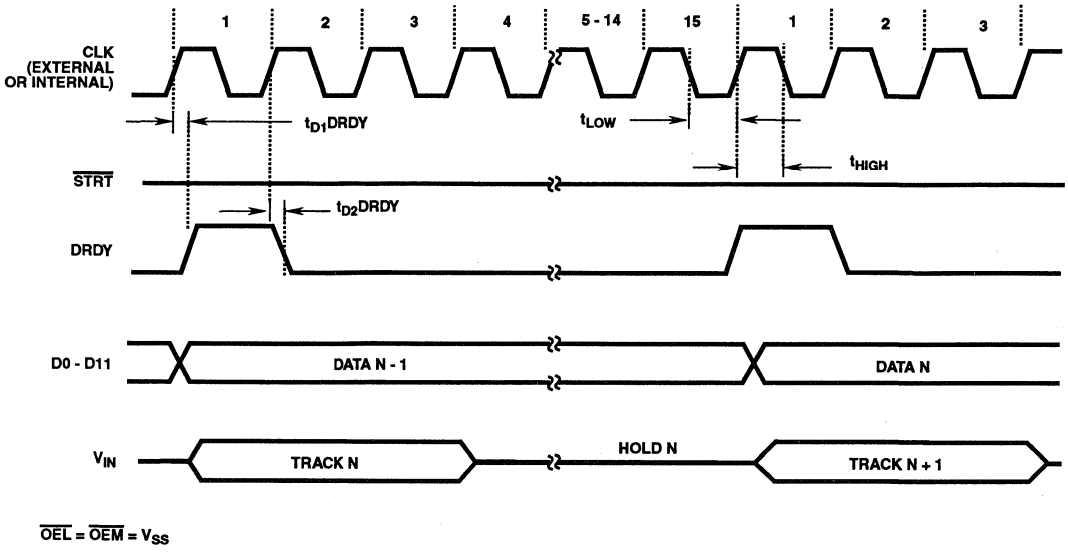


FIGURE 1. CONTINUOUS CONVERSION MODE

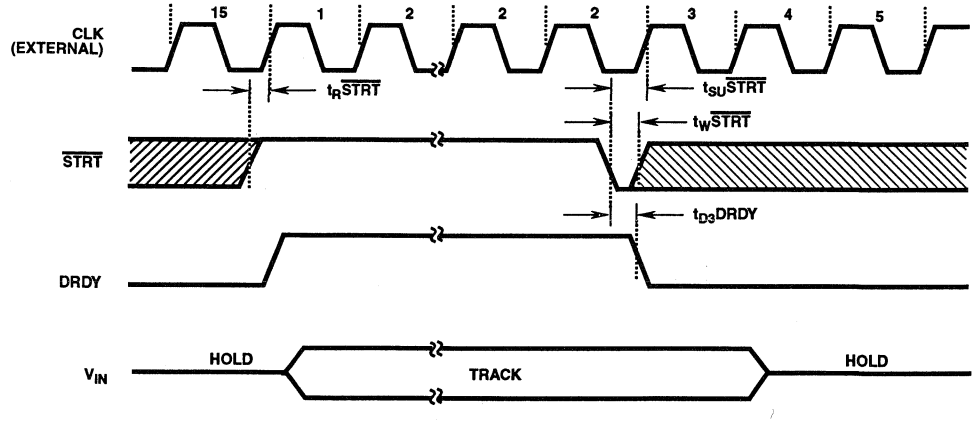


FIGURE 2. SINGLE SHOT MODE EXTERNAL CLOCK

Timing Diagrams (Continued)

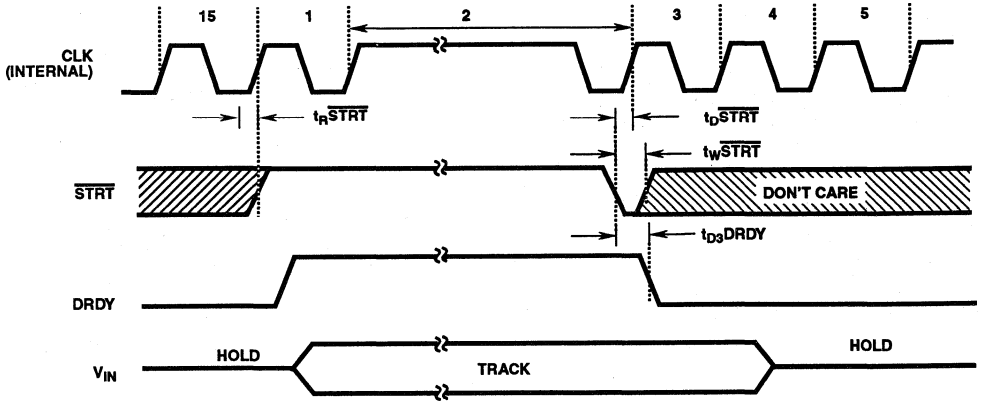


FIGURE 3. SINGLE SHOT MODE INTERNAL CLOCK

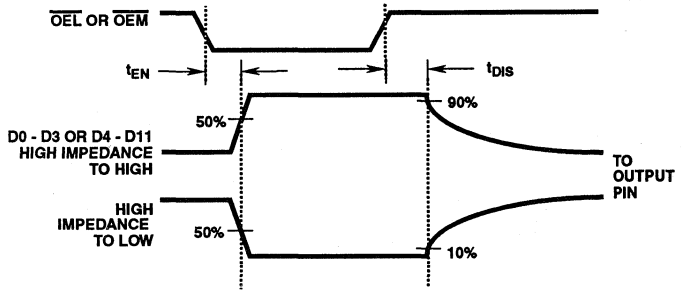


FIGURE 4A.

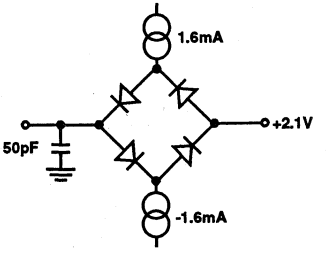


FIGURE 4B.

FIGURE 4. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

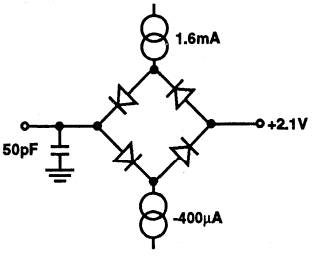


FIGURE 5. GENERAL TIMING LOAD CIRCUIT

Typical Performance Curves

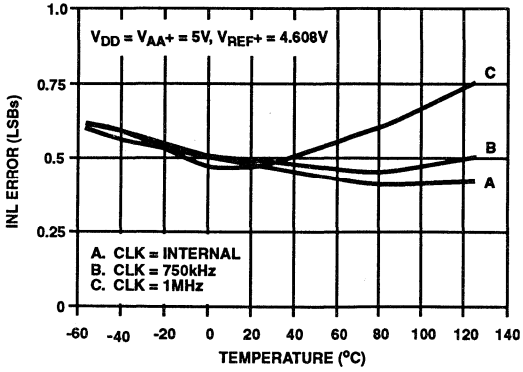


FIGURE 6. INL vs TEMPERATURE

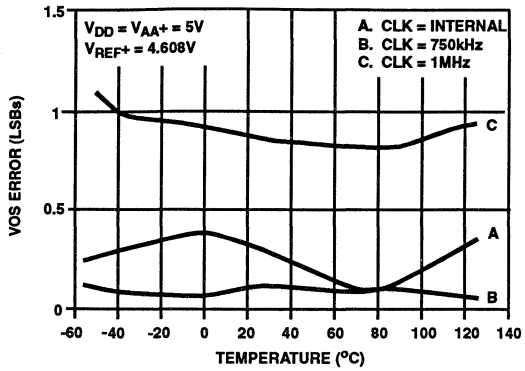


FIGURE 7. OFFSET VOLTAGE vs TEMPERATURE

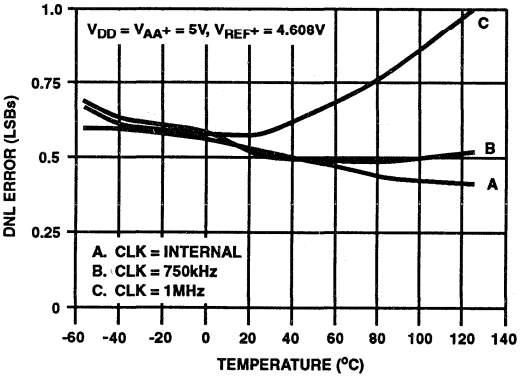


FIGURE 8. DNL vs TEMPERATURE

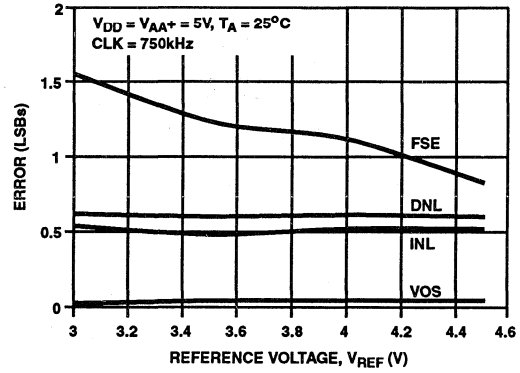


FIGURE 9. ACCURACY vs REFERENCE VOLTAGE

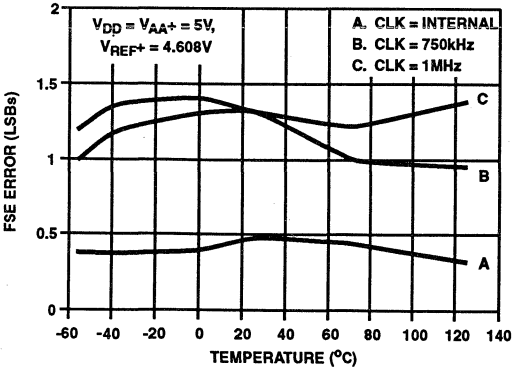


FIGURE 10. FULL SCALE ERROR vs TEMPERATURE

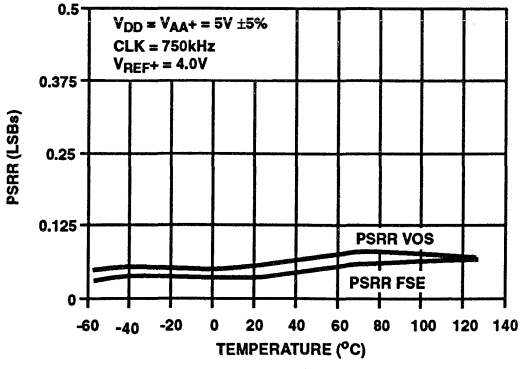


FIGURE 11. POWER SUPPLY REJECTION vs TEMPERATURE

Typical Performance Curves (Continued)

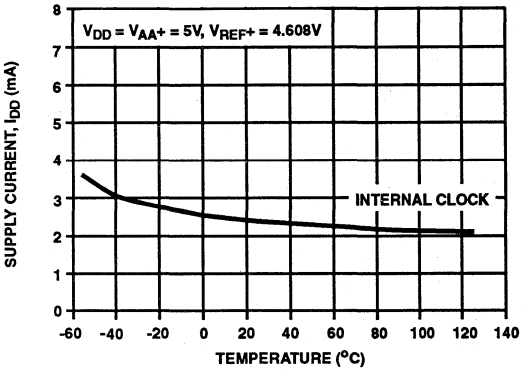


FIGURE 12. SUPPLY CURRENT vs TEMPERATURE

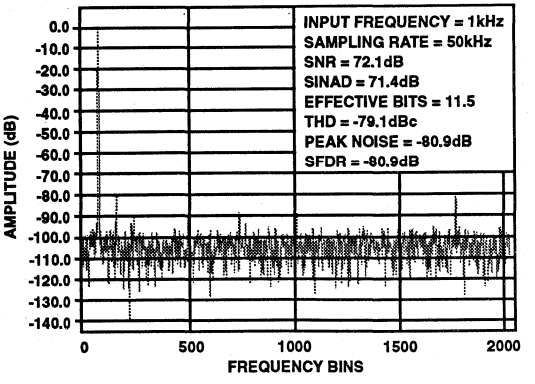


FIGURE 13. FFT SPECTRUM

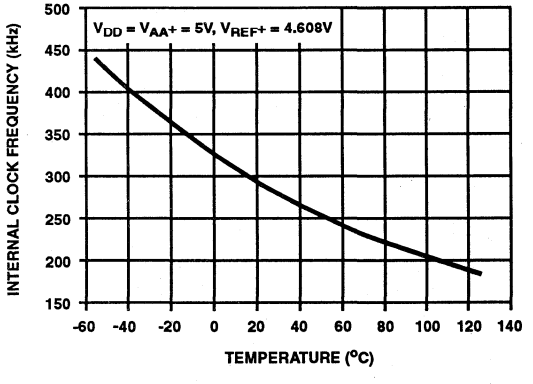
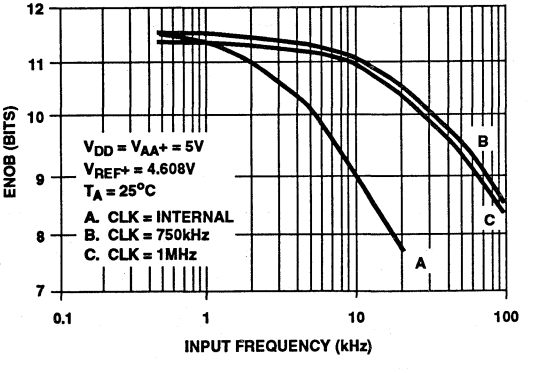


FIGURE 14. INTERNAL CLOCK FREQUENCY vs TEMPERATURE



FGURE 15. EFFECTIVE BITS vs INPUT FREQUENCY

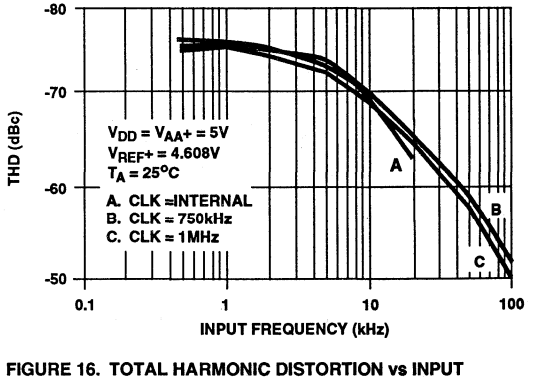


FIGURE 16. TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

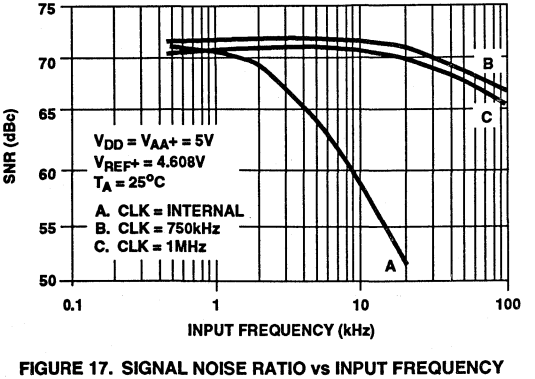


FIGURE 17. SIGNAL NOISE RATIO vs INPUT FREQUENCY

TABLE 1. PIN DESCRIPTION

PIN NO.	NAME	DESCRIPTION
1	DRDY	Output flag signifying new data is available. Goes high at end of clock period 15. Goes low when new conversion is started.
2	D0	Bit-0 (Least significant bit, LSB)
3	D1	Bit-1
4	D2	Bit-2
5	D3	Bit-3
6	D4	Bit-4
7	D5	Bit-5
8	D6	Bit-6
9	D7	Bit-7
10	D8	Bit-8
11	D9	Bit-9
12	V_{SS}	Digital ground, (0V).
13	D10	Bit-10
14	D11	Bit-11 (Most significant bit, MSB)
15	$\overline{OEM}$	Tri-state enable for D4-D11. Active low input.
16	V_{AA}-	Analog ground, (0V).
17	V_{AA}+	Analog positive supply. (+5V) (See text)
18	V_{IN}	Analog input.
19	V_{REF}+	Reference voltage positive input, sets 4095 code end of input range.
20	V_{REF}-	Reference voltage negative input, sets 0 code end of input range.
21	$\overline{STRT}$	Start conversion input active low, recognized after end of clock period 15.
22	CLK	CLK input or output. Conversion functions are synchronized to positive going edge. (See text)
23	$\overline{OEL}$	tri-state enable for D0 D3. Active low input.
24	V_{DD}	Digital positive supply (+5V).

Theory of Operation

HI5812 is a CMOS 12-Bit Analog-to-Digital Converter that uses capacitor-charge balancing to successively approximate the analog input. A binarily weighted capacitor network forms the A/D heart of the device. See the block diagram for the HI5812.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, V_{REF}+ or V_{REF}-.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input and the comparator is being auto-balanced at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input; the one representing the MSB (D11) is connected to the V_{REF}+ terminal; and the remaining capacitors to V_{REF}-. The capacitor-common node, after the charges balance out, will indicate whether the input was above $^1/_2$ of (V_{REF}+ - V_{REF}-). At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to V_{REF}+ (if the comparator was high) or returned to V_{REF}-. This allows the next comparison to be at either $^3/_4$ or $^1/_4$ of (V_{REF}+ - V_{REF}-).

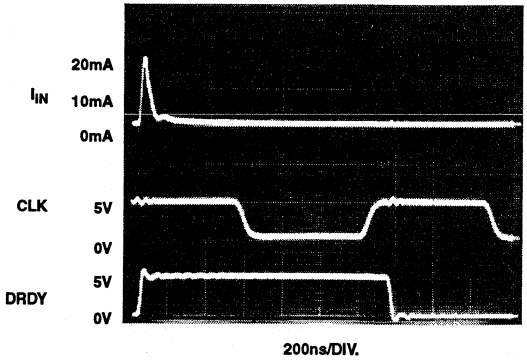
At the end of periods 5 through 14, capacitors representing D10 through D1 are tested, the result stored, and each capacitor either left at V_{REF}+ or at V_{REF}-.

At the end of the 15th period, when the LSB (D0) capacitor is tested, (D0) and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data-ready output goes active. The conversion cycle is now complete.

Analog Input

The analog input pin is a predominately capacitive load that changes between the track and hold periods of the conversion cycle. During hold, clock period 4 through 15, the input loading is leakage and stray capacitance, typically less than 5µA and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the current spike by the end of the tracking period as shown in Figure 18. The amount of charge is dependent on supply and input voltages. The average current is also proportional to clock frequency.



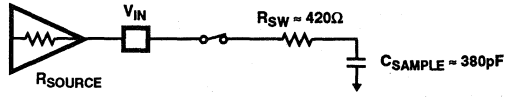
CONDITIONS: V_{DD} = V_{AA}+ = 5.0V, V_{REF}+ = 4.608V, V_{IN} = 4.608V, CLK = 750kHz, T_A = +25°C

FIGURE 18. TYPICAL ANALOG INPUT CURRENT

As long as these current spikes settle completely by end of the signal acquisition period, converter accuracy will be preserved. The analog input is tracked for 3 clock cycles. With an external clock of 750kHz the track period is 4µs.

A simplified analog input model is presented in Figure 19. During tracking, the A/D input (V_{IN}) typically appears as a 380pF capacitor being charged through a 420Ω internal switch resistance. The time constant is 160ns. To charge this capacitor from an external "zero Ω" source to 0.5 LSB (1/8192), the charging time must be at least 9 time constants or 1.4µs. The maximum source impedance (R_{SOURCE} Max) for a 4µs acquisition time settling to within 0.5LSB is 750Ω.

If the clock frequency was slower, or the converter was not restarted immediately (causing a longer sample time), a higher source impedance could be tolerated.



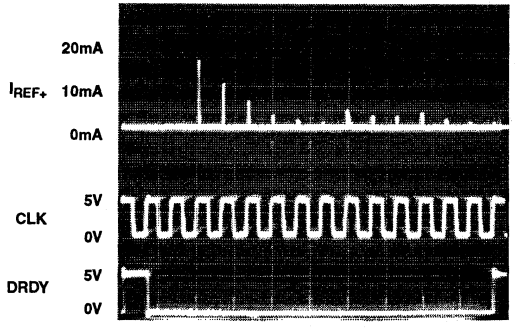
$$R_{SOURCE\ (MAX)} = \frac{-t_{ACQ}}{C_{SAMPLE} \ln [2^{-(N+1)}]} - R_{SW}$$

FIGURE 19. ANALOG INPUT MODEL IN TRACK MODE

Reference Input

The reference input $V_{REF}+$ should be driven from a low impedance source and be well decoupled.

As shown in Figure 20, current spikes are generated on the reference pin during each bit test of the successive approximation part of the conversion cycle as the charge-balancing capacitors are switched between $V_{REF}-$ and $V_{REF}+$ (clock periods 5 - 14). These current spikes must settle completely during each bit test of the conversion to not degrade the accuracy of the converter. Therefore $V_{REF}+$ and $V_{REF}-$ should be well bypassed. Reference input $V_{REF}-$ is normally connected directly to the analog ground plane. If $V_{REF}-$ is biased for nulling the converters offset it must be stable during the conversion cycle.



CONDITIONS: $V_{DD} = V_{AA}+ = 5.0V$, $V_{REF}+ = 4.608V$, $V_{IN} = 2.3V$, CLK = 750kHz, $T_A = +25°C$

FIGURE 20. TYPICAL REFERENCE INPUT CURRENT

The HI5812 is specified with a 4.608V reference, however, it will operate with a reference down to 3V having a slight degradation in performance. A typical graph of accuracy vs reference voltage is presented.

Full Scale and Offset Adjustment

In many applications the accuracy of the HI5812 would be sufficient without any adjustments. In applications where accuracy is of utmost importance full scale and offset errors may be adjusted to zero.

The $V_{REF}+$ and $V_{REF}-$ pins reference the two ends of the analog input range and may be used for offset and full scale adjustments. In a typical system the $V_{REF}-$ might be returned to a clean ground, and the offset adjustment done on an input amplifier. $V_{REF}+$ would then be adjusted to null out the full scale error. When this is not possible, the $V_{REF}-$ input can be adjusted to null the offset error, however, $V_{REF}-$ must be well decoupled.

Full scale and offset error can also be adjusted to zero in the signal conditioning amplifier driving the analog input (V_{IN}).

Control Signal

The HI5812 may be synchronized from an external source by using the $\overline{STRT}$ (Start Conversion) input to initiate conversion, or if $\overline{STRT}$ is tied low, may be allowed to free run. Each conversion cycle takes 15 clock periods.

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by T_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by T_{D1}DRDY) after the start of clock period 1, and returns low (specified by T_{D2}DRDY) after the start of clock period 2.

The 12 data bits are available in parallel on tri-state bus driver outputs. When low, the $\overline{OEM}$ input enables the most significant byte (D4 through D11) while the $\overline{OEL}$ input enables the four least significant bits (D0 - D3). T_{EN} and T_{DIS} specify the output enable and disable times.

If the output data is to be latched externally, either the trailing edge of data ready or the next falling edge of the clock after data ready goes high can be used.

When $\overline{STRT}$ input is used to initiate conversions, operation is slightly different depending on whether an internal or external clock is used.

Figure 3 illustrates operation with an internal clock. If the $\overline{STRT}$ signal is removed (at least $T_R\overline{STRT}$) before clock period 1, and is not reapplied during that period, the clock will shut off after entering period 2. The input will continue to track and the DRDY output will remain high during this time.

A low signal applied to $\overline{STRT}$ (at least $T_W\overline{STRT}$ wide) can now initiate a new conversion. The $\overline{STRT}$ signal (after a delay of ($T_D\overline{STRT}$)) causes the clock to restart.

Depending on how long the clock was shut off, the low portion of clock period 2 may be longer than during the remaining cycles.

The input will continue to track until the end of period 3, the same as when free running.

Figure 2 illustrates the same operation as above but with an external clock. If $\overline{STRT}$ is removed (at least $T_R\overline{STRT}$) before clock period 2, a low signal applied to $\overline{STRT}$ will drop the DRDY flag as before, and with the first positive-going clock edge that meets the ($T_{SU}\overline{STRT}$) setup time, the converter will continue with clock period 3.

Clock

The HI5812 can operate either from its internal clock or from one externally supplied. The CLK pin functions either as the clock output or input. All converter functions are synchronized with the rising edge of the clock signal.

Figure 21 shows the configuration of the internal clock. The clock output drive is low power: if used as an output, it should not have more than 1 CMOS gate load applied, and stray wiring capacitance should be kept to a minimum.

The internal clock will shut down if the A/D is not restarted after a conversion. The clock could also be shut down with an open collector driver applied to the CLK pin. This should only be done during the sample portion (the first three clock periods) of a conversion cycle, and might be useful for using the device as a digital sample and hold.

If an external clock is supplied to the CLK pin, it must have sufficient drive to overcome the internal clock source. The external clock can be shut off, but again, only during the sample portion of a conversion cycle. At other times, it must be above the minium frequency shown in the specifications. In the above two cases, a further restriction applies in that the clock should not be shut off during the third sample period for more than 1ms. This might cause an internal charge-pump voltage to decay.

If the internal or external clock was shut off during the conversion time (clock cycles 4 through 15) of the A/D, the output might be invalid due to balancing capacitor droop.

An external clock must also meet the minimum T_{LOW} and T_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

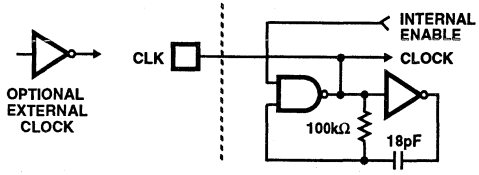


FIGURE 21. INTERNAL CLOCK CIRCUITRY

Power Supplies and Grounding

V_{DD} and V_{SS} are the digital supply pins: they power all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for V_{AA}+, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}. Input transients above V_{DD} or below V_{SS} will get steered to the digital supplies.

The V_{AA}+ and V_{AA}- terminals supply the charge-balancing comparator only. Because the comparator is autobalanced between conversions, it has good low-frequency supply rejection. It does not reject well at high frequencies however; V_{AA}- should be returned to a clean analog ground and V_{AA}+ should be RC decoupled from the digital supply as shown in Figure 22.

There is approximately 50Ω of substrate impedance between V_{DD} and V_{AA}+. This can be used, for example, as part of a low-pass RC filter to attenuate switching supply noise. A 10μF capacitor from V_{AA}+ to ground would attenuate 30kHz noise by approximately 40dB. Note that back-to-back diodes should be placed from V_{DD} to V_{AA}+ to handle supply to capacitor turn-on or turn-off current spikes.

Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the A/D. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is than transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See typical performance characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured RMS signal to RMS sum of noise at a specified input and sampling frequency. The noise is the RMS sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76) dB. For an ideal 12-bit converter the SNR is 74dB. Differential and integral linearity errors will degrade SNR.

$$SNR = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Total Noise Power}}$$

Signal-To-Noise + Distortion Ratio

SINAD is the measured RMS signal to RMS sum of noise plus harmonic power and is expressed by the following.

$$SINAD = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (2nd - 6th)}}$$

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data;

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of the second through sixth harmonic components to the fundamental RMS signal for a specified input and sampling frequency.

$$THD = 10 \log \frac{\text{Total Harmonic Power (2nd - 6th Harmonic)}}{\text{Sinewave Signal Power}}$$

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

$$SFDR = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Highest Spurious Signal Power}}$$

TABLE 2. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE† V_{REF+} = 4.608V V_{REF-} = 0.0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB											LSB
			D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale (FS)	4.6069	4095	1	1	1	1	1	1	1	1	1	1	1	1
FS - 1 LSB	4.6058	4094	1	1	1	1	1	1	1	1	1	1	1	0
3/4 FS	3.4560	3072	1	1	0	0	0	0	0	0	0	0	0	0
1/2 FS	2.3040	2048	1	0	0	0	0	0	0	0	0	0	0	0
1/4 FS	1.1520	1024	0	1	0	0	0	0	0	0	0	0	0	0
1 LSB	0.001125	1	0	0	0	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0	0	0	0

†The voltages listed above represent the ideal lower transition of each output code shown as a function of the reference voltage.

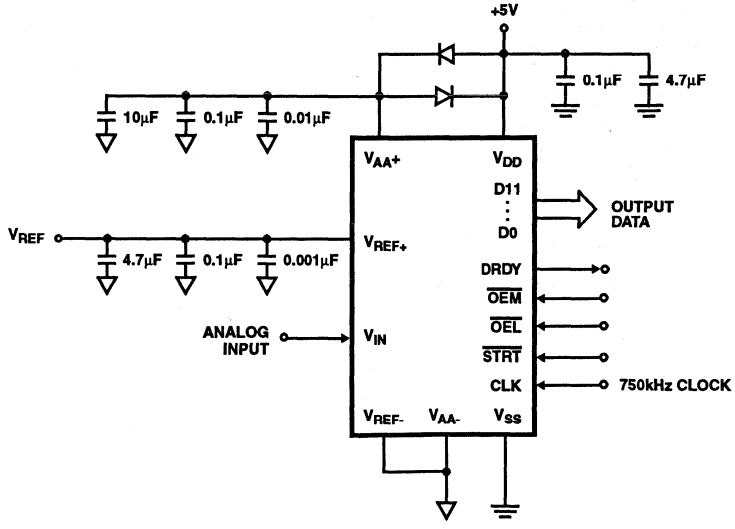


FIGURE 22. GROUND AND SUPPLY DECOUPLING

Die Characteristics

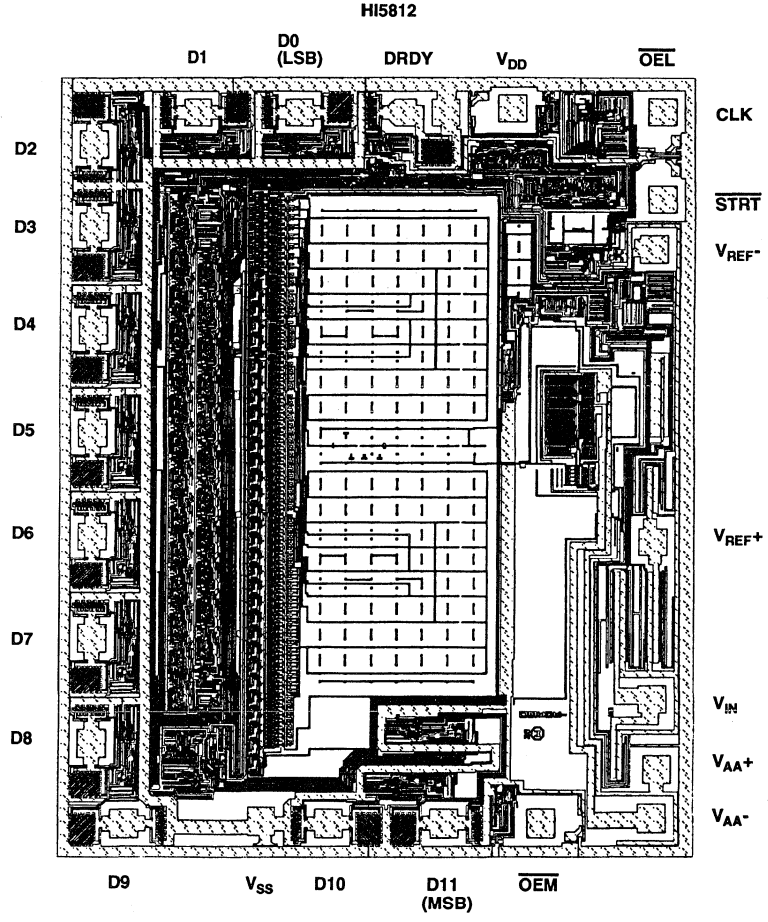
DIE DIMENSIONS:
3200µm x 3940µm

METALLIZATION:
Type: AlSi
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: PSG
Thickness: 13kÅ ± 2.5kÅ

WORST CASE CURRENT DENSITY:
1.84×10^5 A/cm^2

Metallization Mask Layout



HI5813

CMOS 3.3V, 25µs 12-Bit Sampling A/D Converter with Internal Track and Hold

December 1993

Features

- 25µs Conversion Time
- 40KSPS Throughput Rate
- Built-In Track and Hold
- Single +3.3V Supply Voltage
- 3.3mW Maximum Power Consumption (+25°C)

Applications

- Remote Low Power Data Acquisition Systems
- Battery Operated Systems
- Pen Based PC Handheld Scanners
- DSP Modems
- General Purpose DSP Front End
- µP Controlled Measurement Systems
- PCMCIA Type II Compliant
- PC Based Industrial Controls/DAQ Systems

Description

The HI5813 is a 3.3V, very low power, 12-bit successive approximation analog-to-digital converter. It can operate from a single 3V to 6V supply and typically draws a maximum of 1.0mA (at +25°C) when operating at 3.3V. The HI5813 features a built-in track and hold. The conversion time is as low as 25µs with a 3.3V supply.

The twelve data outputs feature full high speed CMOS tri-state bus driver capability, and are latched and held through a full conversion cycle. The output is user selectable: (i.e.) 12-bit , 8-bit (MSBs), and/or 4-bit (LSBs). A data ready flag and conversion start input complete the digital interface.

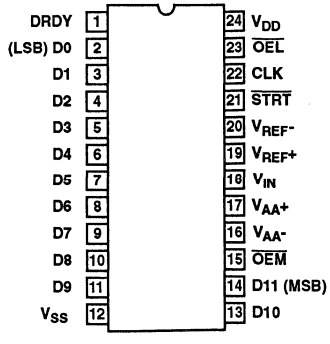
The HI5813 is rated over the full industrial temperature range and is offered in 24 lead narrow body Plastic DIP, narrow body Ceramic DIP, and Plastic SOIC packages.

Ordering Information

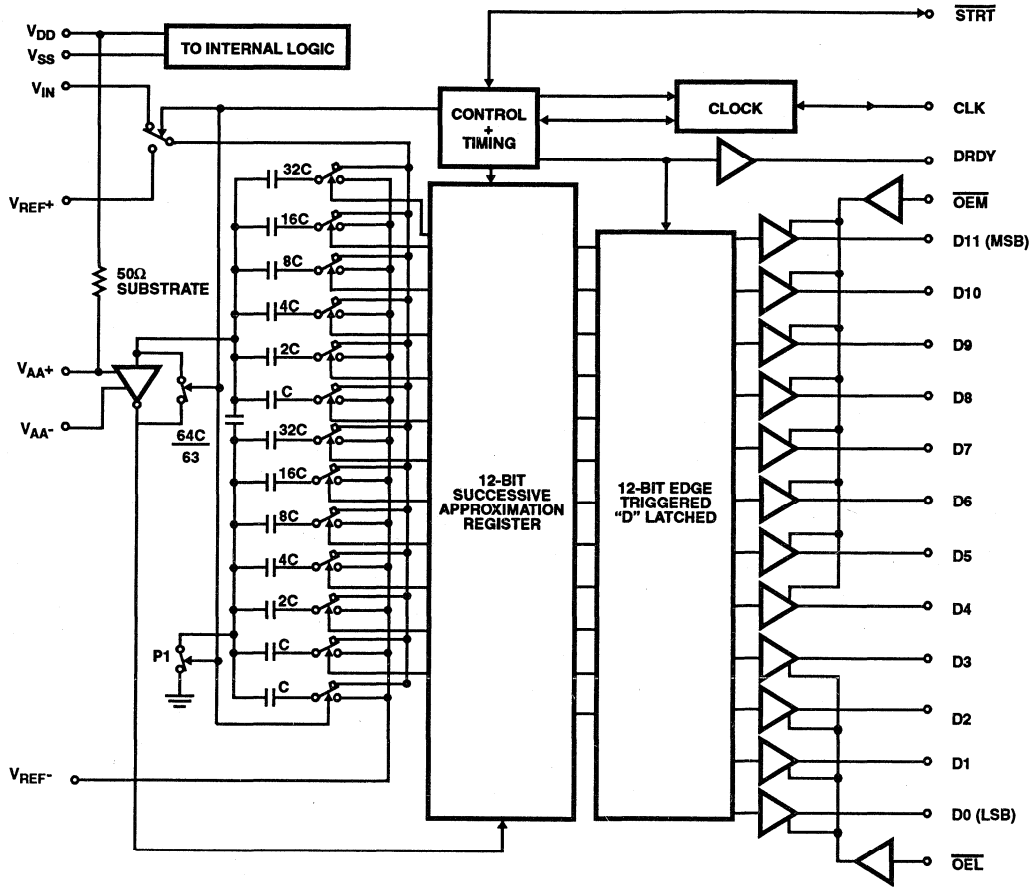
PART NUMBER	INL (LSB) (MAX OVER TEMP.)	TEMP. RANGE	PACKAGE
HI5813JIP	±4.0	-40°C to +85°C	24 Lead Plastic DIP
HI5813KIP	±2.5	-40°C to +85°C	24 Lead Plastic DIP
HI5813JIB	±4.0	-40°C to +85°C	24 Lead Plastic SOIC
HI5813KIB	±2.5	-40°C to +85°C	24 Lead Plastic SOIC
HI5813JIJ	±4.0	-40°C to +85°C	24 Lead Ceramic DIP
HI5813KIJ	±2.5	-40°C to +85°C	24 Lead Ceramic DIP

Pinout

HI5813 (PDIP, CDIP, SOIC)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage
- V_{DD} to V_{SS} ..... (V_{SS} -0.5V) < V_{DD} < +6.5V
- V_{AA}+ to V_{AA}- ..... (V_{SS} -0.5V) to (V_{SS} +6.5V)
- V_{AA}+ to V_{DD} ..... ±0.3V

Analog and Reference Inputs
- V_{IN}, V_{REF}+, V_{REF}- ..... (V_{SS} -0.3V) < V_{INA} < (V_{DD} +0.3V)

Digital I/O Pins ..... (V_{SS} -0.3V) < VI/O < (V_{DD} +0.3V)

Operating Temperature Range
- Plastic DIP, Plastic SOIC, and Ceramic DIP ..... -40°C to +85°C

Junction Temperature
- Plastic Dip and Plastic SOIC ..... +150°C
- Ceramic DIP ..... +175°C

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}
Plastic DIP	80°C/W
Plastic SOIC	75°C/W
Package Power Dissipation at +85°C (Note 1)	
Plastic DIP	0.810W
Plastic SOIC	0.870W
Power Dissipation Derating Factor above +85°C	
Plastic DIP	12mW/°C
Plastic SOIC	13mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = V_{AA}+ = V_{REF}+ = 3.3V, V_{SS} = V_{AA}- = V_{REF}- = GND, CLK = 600kHz (J suffix), CLK = 500kHz (K suffix), Unless Otherwise Specified.

PARAMETER		TEST CONDITIONS	+25°C MIN	+25°C TYP	+25°C MAX	-40°C TO +85°C MIN	-40°C TO +85°C MAX	UNITS
ACCURACY								
Resolution			12	-	-	12	-	Bits
Integral Linearity Error, INL (End Point)	J		-	-	±4.0	-	±4.0	LSB
	K		-	-	±2.5	-	±2.5	LSB
Differential Linearity Error, DNL	J		-	-	±4.0	-	±4.0	LSB
	K		-	-	±2.0	-	±2.0	LSB
Gain Error, FSE (Adjustable to Zero)	J		-	-	±2.0	-	±2.0	LSB
	K		-	-	±2.0	-	±2.0	LSB
Offset Error, V_{OS} (Adjustable to Zero)	J		-	-	±3.0	-	±3.0	LSB
	K		-	-	±2.5	-	±2.5	LSB
DYNAMIC CHARACTERISTICS								
Signal to Noise Ratio, SINAD $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	J	f_S = 600kHz, f_{IN} = 1kHz	-	61.5	-	-	-	dB
	K	f_S = 500kHz, f_{IN} = 1kHz	-	63.9	-	-	-	dB
Signal to Noise Ratio, SNR $\frac{\text{RMS Signal}}{\text{RMS Noise}}$	J	f_S = 600kHz, f_{IN} = 1kHz	-	63.2	-	-	-	dB
	K	f_S = 500kHz, f_{IN} = 1kHz	-	65.1	-	-	-	dB
Total Harmonic Distortion, THD	J	f_S = 750kHz, f_{IN} = 1kHz	-	-68.4	-	-	-	dBc
	K	f_S = 750kHz, f_{IN} = 1kHz	-	-70.8	-	-	-	dBc
Spurious Free Dynamic Range, SFDR	J	f_S =600kHz, f_{IN} = 1kHz	-	69.0	-	-	-	dB
	K	f_S = 500kHz, f_{IN} = 1kHz	-	71.8	-	-	-	dB

Electrical Specifications $V_{DD} = V_{AA}+ = V_{REF}+ = 3.3V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = 600kHz (J suffix), CLK = 500kHz (K suffix), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	+25°C			-40°C TO +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
ANALOG INPUT							
Input Current, Dynamic	At $V_{IN} = V_{REF}+$, 0V	-	±50	±100	-	±100	µA
Input Current, Static	Conversion Stopped	-	±0.4	±10	-	±10	µA
Input Bandwidth -3dB		-	1		-	-	MHz
Reference Input Current		-	160	-	-	-	µA
Input Series Resistance, R_S	In Series with Input C_{SAMPLE}	-	420	-	-	-	Ω
Input Capacitance, C_{SAMPLE}	During Sample State	-	380	-	-	-	pF
Input Capacitance, C_{HOLD}	During Hold State	-	20	-	-	-	pF
DIGITAL INPUTS $\overline{OEL}$, $\overline{OEM}$, $\overline{STRT}$							
High-Level Input Voltage, V_{IH}		2.4	-	-	2.4	-	V
Low-Level Input Voltage, V_{IL}		-	-	0.8	-	0.8	V
Input Leakage Current, I_{IL}	Except CLK, V_{IN} = 0V, 5V	-	-	±10		±10	µA
Input Capacitance, C_{IN}		-	10		-	-	pF
DIGITAL OUTPUTS							
High-Level Output Voltage, V_{OH}	I_{SOURCE} = -400µA	2.6	-	-	2.6	-	V
Low-Level Output Voltage, V_{OL}	I_{SINK} = 1.6mA	-	-	0.4	-	0.4	V
Tri-State Leakage, I_{OZ}	Except DRDY, V_{OUT} = 0V, 3.3V	-	-	±10	-	±10	µA
Output Capacitance, C_{OUT}	Except DRDY	-	20	-	-	-	pF
TIMING							
Conversion Time ($t_{CONV} + t_{ACQ}$) (Includes Acquisition Time) J		25	-	-	25	-	µs
K		30	-	-	30	-	µs
Clock Frequency	(Note 2)	0.05	-	0.75	0.05	0.75	MHz
Clock Pulse Width, t_{LOW}, t_{HIGH}	(Note 2)	100	-	-	100	-	ns
Aperture Delay, t_DAPR	(Note 2)	-	35	50	-	70	ns
Clock to Data Ready Delay, t_{D1}DRDY	(Note 2)	-	180	210	-	240	ns
Clock to Data Ready Delay, t_{D2}DRDY	(Note 2)	-	180	220	-	250	ns
Start Removal Time, $t_R\overline{STRT}$	(Note 2)	75	30	-	75	-	ns
Start Setup Time, $t_{SU}\overline{STRT}$	(Note 2)	85	60	-	30	-	ns

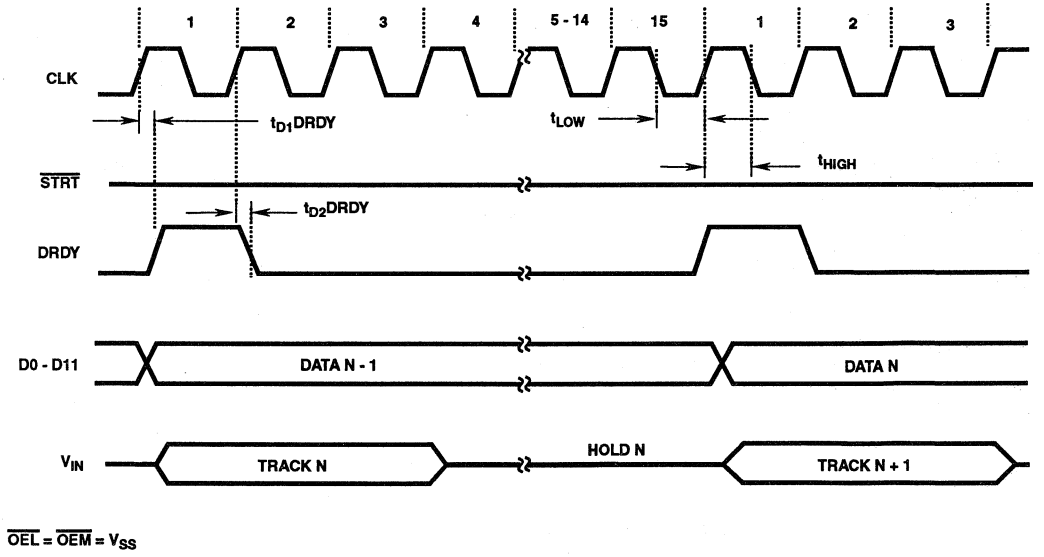
Electrical Specifications $V_{DD} = V_{AA}+ = V_{REF}+ = 3.3V$, $V_{SS} = V_{AA}- = V_{REF}- = GND$, CLK = 600kHz (J suffix), CLK = 500kHz (K suffix), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	+25°C			-40°C TO +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
Start Pulse Width, $t_W\overline{STRT}$	(Note 2)	-	15	25	-	25	ns
Start to Data Ready Delay, t_{D3} DRDY	(Note 2)	-	110	130	-	160	ns
Output Enable Delay, t_{EN}	(Note 2)	-	65	75	-	80	ns
Output Disabled Delay, t_{DIS}	(Note 2)	-	95	110	-	130	ns
POWER SUPPLY CHARACTERISTICS							
Supply Current, $I_{DD} + I_{AA}$		-	0.5	1	-	2.5	mA

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Parameter guaranteed by design or characterization, not production tested.

Timing Diagrams



$\overline{OEL} = \overline{OEM} = V_{SS}$

FIGURE 1. CONTINUOUS CONVERSION MODE

Timing Diagrams (Continued)

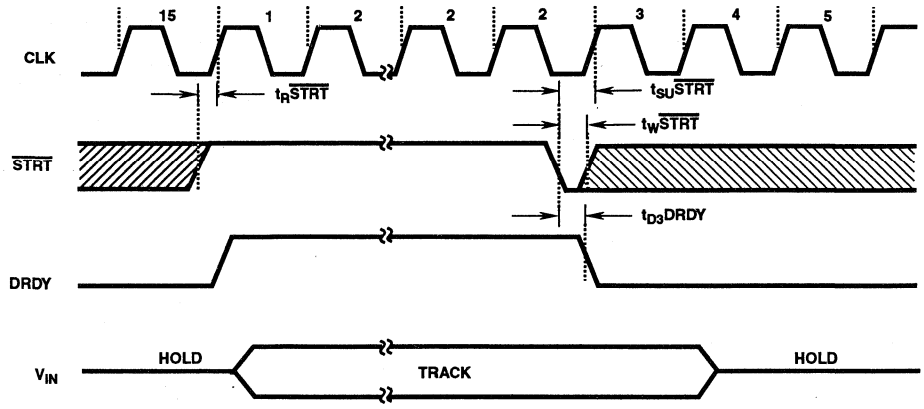


FIGURE 2. SINGLE SHOT MODE

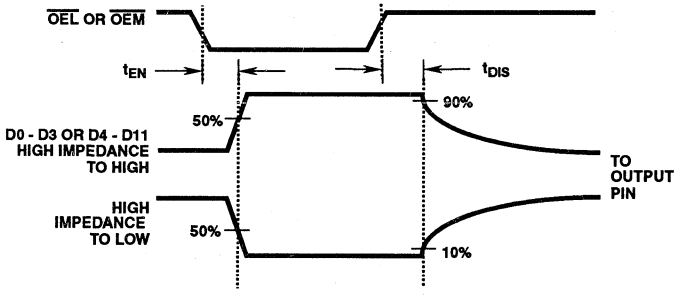


FIGURE 3A.

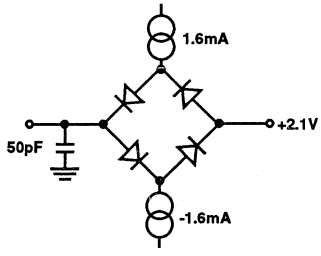


FIGURE 3B.

FIGURE 3. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

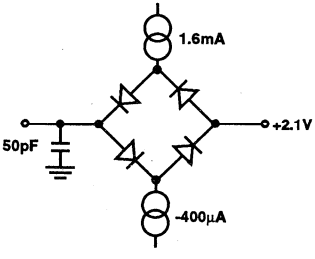


FIGURE 4. GENERAL TIMING LOAD CIRCUIT

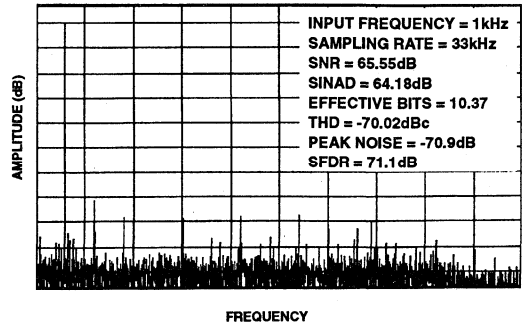


FIGURE 5. FFT SPECTRUM

Typical Performance Curves

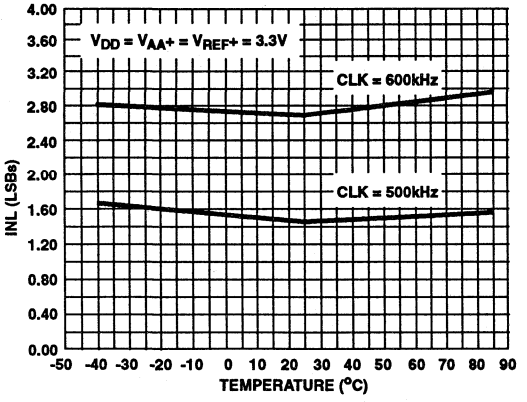


FIGURE 6. INL vs TEMPERATURE

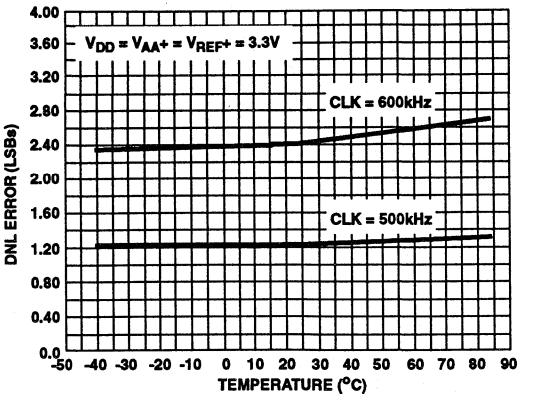


FIGURE 7. DNL vs TEMPERATURE

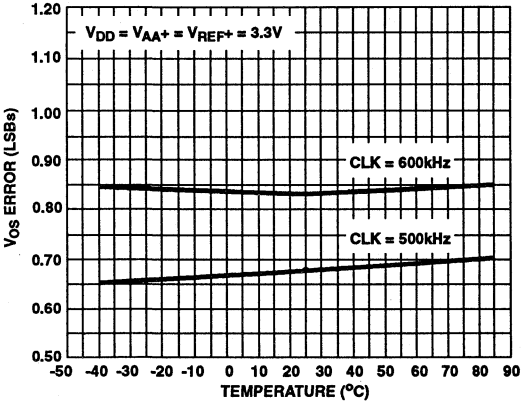


FIGURE 8. OFFSET ERROR vs TEMPERATURE

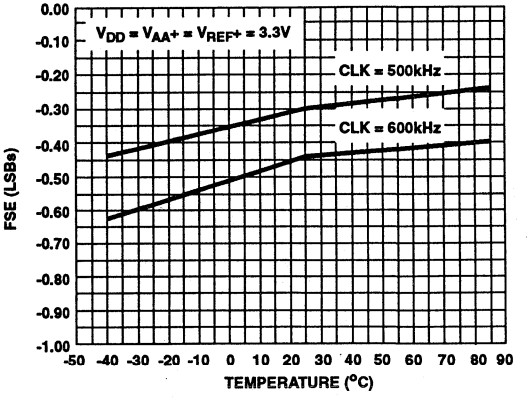


FIGURE 9. FULL SCALE ERROR vs TEMPERATURE

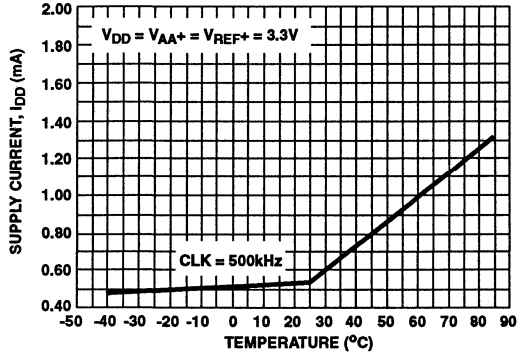


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

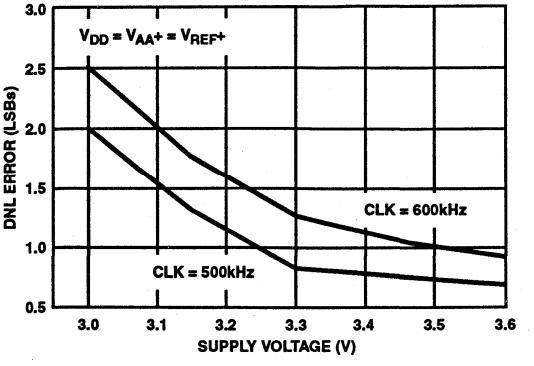


FIGURE 11. DNL vs SUPPLY VOLTAGE

TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	DRDY	Output flag signifying new data is available. Goes high at end of clock period 15. Goes low when new conversion is started.
2	D0	Bit-0 (Least significant bit, LSB)
3	D1	Bit-1
4	D2	Bit-2
5	D3	Bit-3
6	D4	Bit-4
7	D5	Bit-5
8	D6	Bit-6
9	D7	Bit-7
10	D8	Bit-8
11	D9	Bit-9
12	V_{SS}	Digital ground, (0V).
13	D10	Bit-10
14	D11	Bit-11 (Most significant bit, MSB)
15	$\overline{OEM}$	Tri-state enable for D4-D11. Active low input.
16	V_{AA}-	Analog ground, (0V).
17	V_{AA}+	Analog positive supply. (+3.3V) (See text)
18	V_{IN}	Analog input.
19	V_{REF}+	Reference voltage positive input, sets 4095 code end of input range.
20	V_{REF}-	Reference voltage negative input, sets 0 code end of input range.
21	$\overline{STRT}$	Start conversion input active low, recognized after end of clock period 15.
22	CLK	CLK input. Conversion functions are synchronized to positive going edge. (See text)
23	$\overline{OEL}$	Tri-state enable for D0 - D3. Active low input.
24	V_{DD}	Digital positive supply (+3.3V).

Theory of Operation

HI5813 is a CMOS 12-Bit Analog-to-Digital Converter that uses capacitor charge balancing to successively approximate the analog input. A binary weighted capacitor network forms the A/D heart of the device. See the block diagram for the HI5813.

The capacitor network has a common node which is connected to a comparator. The second terminal of each capacitor is individually switchable to the input, V_{REF}+ or V_{REF}-.

During the first three clock periods of a conversion cycle, the switchable end of every capacitor is connected to the input and the comparator is being auto balanced at the capacitor common node.

During the fourth period, all capacitors are disconnected from the input; the one representing the MSB (D11) is connected to the V_{REF}+ terminal; and the remaining capacitors to V_{REF}-. The capacitor common node, after the charges balance out, will indicate whether the input was above $^1/_2$ of (V_{REF}+ - V_{REF}-). At the end of the fourth period, the comparator output is stored and the MSB capacitor is either left connected to V_{REF}+ (if the comparator was high) or returned to V_{REF}-. This allows the next comparison to be at either $^3/_4$ or $^1/_4$ of (V_{REF}+ - V_{REF}-).

At the end of periods 5 through 14, capacitors representing D10 through D1 are tested, the result stored, and each capacitor either left at V_{REF}+ or at V_{REF}-.

At the end of the 15th period, when the LSB (D0) capacitor is tested, (D0) and all the previous results are shifted to the output registers and drivers. The capacitors are reconnected to the input, the comparator returns to the balance state, and the data ready output goes active. The conversion cycle is now complete.

Analog Input

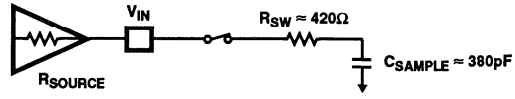
The analog input pin is a predominately capacitive load that changes between the track and hold periods of the conversion cycle. During hold, clock period 4 through 15, the input loading is leakage and stray capacitance, typically less than 5µA and 20pF.

At the start of input tracking, clock period 1, some charge is dumped back to the input pin. The input source must have low enough impedance to dissipate the current spike by the end of the tracking period. The amount of charge is dependent on supply and input voltages. The average current is also proportional to clock frequency.

As long as these current spikes settle completely by end of the signal acquisition period, converter accuracy will be preserved. The analog input is tracked for 3 clock cycles. With a clock of 500kHz the track period is 6µs.

A simplified analog input model is presented in Figure 12. During tracking, the A/D input (V_{IN}) typically appears as a 380pF capacitor being charged through a 420Ω internal switch resistance. The time constant is 160ns. To charge this capacitor from an external "zero Ω" source to 0.5 LSB (1/8192), the charging time must be at least 9 time constants or 1.4µs. The maximum source impedance (R_{SOURCE} Max) for a 6µs acquisition time settling to within 0.5 LSB is 1.3kΩ.

If the clock frequency was slower, or the converter was not restarted immediately (causing a longer sample time), a higher source impedance could be tolerated.



$$R_{SOURCE\ (MAX)} = \frac{-t_{ACQ}}{C_{SAMPLE} \ln [2^{-(N+1)}]} - R_{SW}$$

FIGURE 12. ANALOG INPUT MODEL IN TRACK MODE

Reference Input

The reference input $V_{REF}+$ should be driven from a low impedance source and be well decoupled.

Current spikes are generated on the reference pin during each bit test of the successive approximation part of the conversion cycle as the charge balancing capacitors are switched between $V_{REF}-$ and $V_{REF}+$ (clock periods 5 - 14). These current spikes must settle completely during each bit test of the conversion to not degrade the accuracy of the converter. Therefore $V_{REF}+$ and $V_{REF}-$ should be well bypassed. Reference input $V_{REF}-$ is normally connected directly to the analog ground plane. If $V_{REF}-$ is biased for nulling the converters offset it must be stable during the conversion cycle.

Full Scale and Offset Adjustment

In many applications the accuracy of the HI5813 would be sufficient without any adjustments. In applications where accuracy is of utmost importance full scale and offset errors may be adjusted to zero.

The $V_{REF}+$ and $V_{REF}-$ pins reference the two ends of the analog input range and may be used for offset and full scale adjustments. In a typical system the $V_{REF}-$ might be returned to a clean ground, and the offset adjustment done on an input amplifier. $V_{REF}+$ would then be adjusted to null out the full scale error. When this is not possible, the $V_{REF}-$ input can be adjusted to null the offset error, however, $V_{REF}-$ must be well decoupled.

Full scale and offset error can also be adjusted to zero in the signal conditioning amplifier driving the analog input (V_{IN}).

Control Signal

The HI5813 may be synchronized from an external source by using the $\overline{STRT}$ (Start Conversion) input to initiate conversion, or if $\overline{STRT}$ is tied low, may be allowed to free run. Each conversion cycle takes 15 clock periods.

The input is tracked from clock period 1 through period 3, then disconnected as the successive approximation takes place. After the start of the next period 1 (specified by T_D data), the output is updated.

The DRDY (Data Ready) status output goes high (specified by T_{D1}DRDY) after the start of clock period 1, and returns low (specified by T_{D2}DRDY) after the start of clock period 2.

The 12 data bits are available in parallel on tri-state bus driver outputs. When low, the $\overline{OEM}$ input enables the most significant byte (D4 through D11) while the $\overline{OEL}$ input enables the four least significant bits (D0 - D3). T_{EN} and T_{DIS} specify the output enable and disable times.

If the output data is to be latched externally, either the trailing edge of data ready or the next falling edge of the clock after data ready goes high can be used.

Figure 2 shows operation of the HI5813 when the $\overline{STRT}$ pin is used to initate a conversion. If $\overline{STRT}$ is taken high at least $T_R\overline{STRT}$ before clock period 1 and is not reapplied during that period, the converter will stay in the track mode and the DRDY output will remain high. A low signal applied to $\overline{STRT}$ will bring the DRDY flag low and the conversion will continue with clock period 3 on the first positive going clock edge that meets the $T_{SU}\overline{STRT}$ setup time.

Clock

The clock used to drive the HI5813 can range in frequency from 50kHz up to 750kHz. All converter functions are synchronized with the rising edge of the clock signal. The clock can be shut off only during the sample (track) portion of the conversion cycle. At other times it must be above the minimum frequency shown in the specifications. In the above two cases, a further restriction applies in that the clock should not be shut off during the third sample period for more than 1ms. This might cause an internal charge pump voltage to decay.

If the clock is shut off during the conversion time (clock cycles 4 through 15) of the A/D, the output might be invalid due to balancing capacitor droop.

The clock must also meet the minimum T_{LOW} and T_{HIGH} times shown in the specifications. A violation may cause an internal miscount and invalidate the results.

Power Supplies and Grounding

V_{DD} and V_{SS} are the digital supply pins: they power all internal logic and the output drivers. Because the output drivers can cause fast current spikes in the V_{DD} and V_{SS} lines, V_{SS} should have a low impedance path to digital ground and V_{DD} should be well bypassed.

Except for $V_{AA}+$, which is a substrate connection to V_{DD}, all pins have protection diodes connected to V_{DD} and V_{SS}. Input transients above V_{DD} or below V_{SS} will get steered to the digital supplies.

The $V_{AA}+$ and $V_{AA}-$ terminals supply the charge balancing comparator only. Because the comparator is autobalanced between conversions, it has good low frequency supply rejection. It does not reject well at high frequencies however; $V_{AA}-$ should be returned to a clean analog ground and $V_{AA}+$ should be RC decoupled from the digital supply as shown in Figure 10.

There is approximately 50Ω of substrate impedance between V_{DD} and $V_{AA}+$. This can be used, for example, as part of a low pass RC filter to attenuate switching supply noise. A 10µF capacitor from $V_{AA}+$ to ground would attenuate 30kHz noise by approximately 40dB. Note that back to back diodes should be placed from V_{DD} to $V_{AA}+$ to handle supply to capacitor turn-on or turn-off current spikes.

Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the A/D. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is than transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See typical performance characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured RMS signal to RMS sum of noise at a specified input and sampling frequency. The noise is the RMS sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76)dB. For an ideal 12-bit converter the SNR is 74dB. Differential and integral linearity errors will degrade SNR.

$$SNR = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Total Noise Power}}$$

Signal-To-Noise + Distortion Ratio

SINAD is the measured RMS signal to RMS sum of noise plus harmonic power and is expressed by the following.

$$SINAD = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (2nd - 6th)}}$$

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data;

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of the second through sixth harmonic components to the fundamental RMS signal for a specified input and sampling frequency.

$$THD = 10 \log \frac{\text{Total Harmonic Power (2nd - 6th Harmonic)}}{\text{Sinewave Signal Power}}$$

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the rms amplitude of the next largest spur or spectral component. If the harmonics are buried in the noise floor it is the largest peak.

$$SFDR = 10 \log \frac{\text{Sinewave Signal Power}}{\text{Highest Spurious Signal Power}}$$

TABLE 2. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE† $V_{REF}+ = 3.3V$ $V_{REF}- = 0.0V$ (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB											LSB
			D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full Scale (FS)	3.2992	4095	1	1	1	1	1	1	1	1	1	1	1	1
FS - 1 LSB	3.2984	4094	1	1	1	1	1	1	1	1	1	1	1	0
$^3/_4$ FS	2.4750	3072	1	1	0	0	0	0	0	0	0	0	0	0
$^1/_2$ FS	1.6500	2048	1	0	0	0	0	0	0	0	0	0	0	0
$^1/_4$ FS	0.8250	1024	0	1	0	0	0	0	0	0	0	0	0	0
1 LSB	0.00080566	1	0	0	0	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0	0	0	0

†The voltages listed above represent the ideal lower transition of each output code shown as a function of the reference voltage.

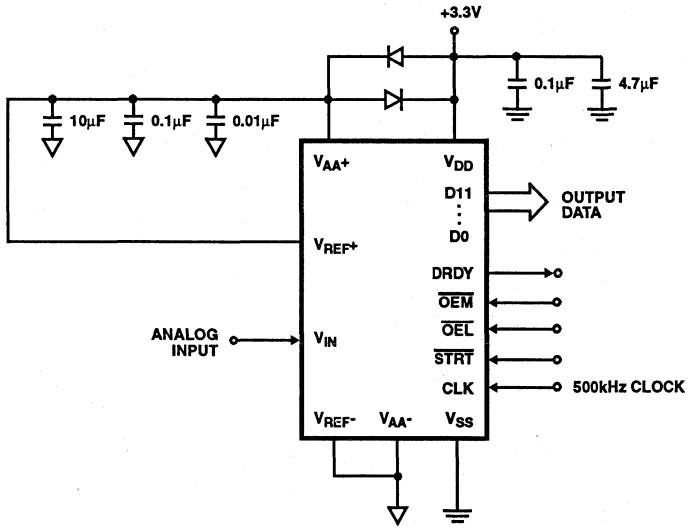


FIGURE 13. GROUND AND SUPPLY DECOUPLING

Die Characteristics

DIE DIMENSIONS:
3200µm x 3940µm

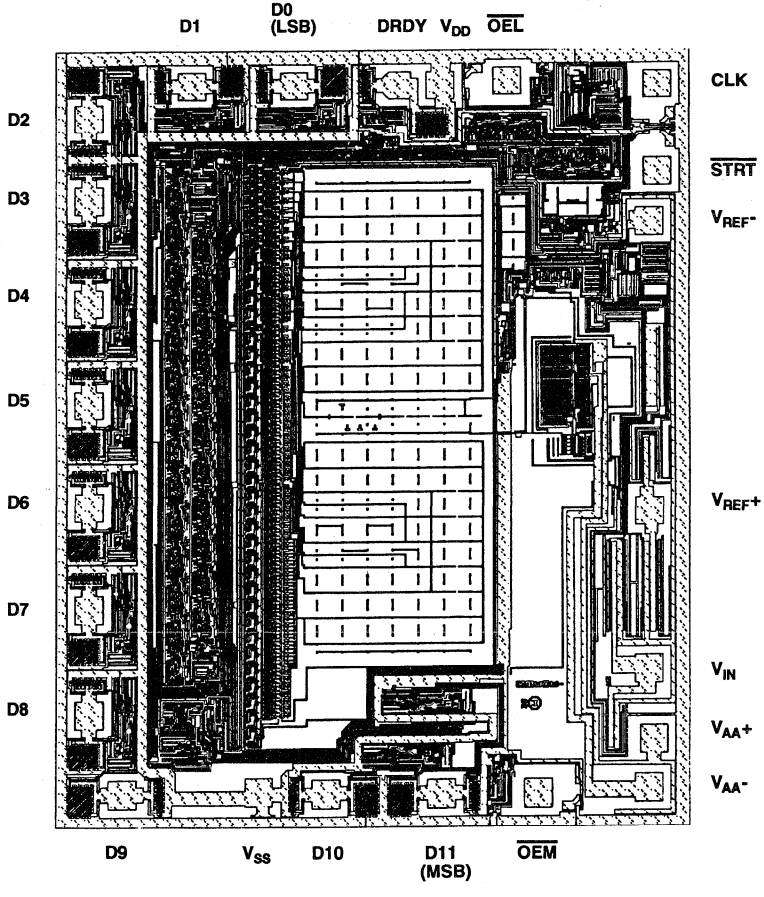
METALLIZATION:
Type: AlSi
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: PSG
Thickness: 13kÅ ± 2.5kÅ

WORST CASE CURRENT DENSITY:
1.84×10^5 A/cm^2

Metallization Mask Layout

HI5813



DATA ACQUISITION 6

A/D CONVERTERS - FLASH

NOTE: Bold Type Designates a New Product from Harris.

4-BIT FLASH

DEVICE	SUFFIX CODE	OUTPUTS	CONVERSION	CONVERSION TIME (ns)	TECHNOLOGY	RANGE MIN (V)	INL (LSB)	DNL (LSB)	FEATURES
CA3304A	D	Parallel, Binary, 4-Bit Latch, Tri-State	Flash	40	CMOS-S.O.S.	2.0	±0.125	±0.125	Low Power - 25mW Typ at 25msps Video
CA3304A	E						±0.125	±0.125	
CA3304	D						±0.25	±0.25	
CA3304	E						±0.25	±0.25	

6-BIT FLASH

DEVICE	SUFFIX CODE	MIL SPEC	OUTPUTS	CONVERSION	CONVERSION TIME (ns)	TECHNOLOGY	RANGE MIN (V)	INL (LSB)	DNL (LSB)	FEATURES
CA3306A	D		Parallel, Binary, 6-Bit Latch, Tri-State	Flash	67	CMOS-S.O.S.	5.0	±0.25	±0.25	Low Power - 70mW Typ at 15msps, 1kΩ Ladder Resistance,
CA3306A	E				67			±0.25	±0.25	
CD3306	D				67			±0.5	±0.5	
CA3306	E				67			±0.5	±0.5	Replaces Micropower MP7682
CA3306	M				67			±0.5	±0.5	
CA3306	J3				100			±0.5	±0.5	
CA3306C	D				100			±0.5	±0.5	
CA3306C	E				100			±0.5	±0.5	
CA3306C	M				100			±0.5	±0.5	
CA3306C	J3				100			±0.5	±0.5	
HI3-5701K	-5	HI1-5701T/883			33	CMOS-JI	4.0	±1.25	±0.6	Low cost
HI9P-5701K	-5	HI1-5701T/883			33			±1.25	±0.6	
HI3-5701B	-9	HI1-5701T/883			33			±1.25	±0.6	
HI9P-5701B	-9	HI1-5701T/883			33			±1.25	±0.6	

8-BIT FLASH

DEVICE	SUFFIX CODE	MIL SPEC	OUTPUTS	CONVERSION	CONVERSION TIME (ns)	BAND WIDTH (MHz)	TECHNOLOGY	RANGE MIN (V)	INL (LSB)	DNL (LSB)	FEATURES
CA3318C	D		Parallel, Binary, 3-Bit Latch, Tri-State	Flash	67	2.5	CMOS-S.O.S.	6.4	±1.5	±1.0 - 0.8	Lowest Power 8-Bit FlasH
CA3318C	E				67	2.5	CMOS-S.O.S.	6.4	±1.5	±1.0 - 0.8	
CA3318C	M				67	2.5	CMOS-S.O.S.	6.4	±1.5	±1.0 - 0.8	
HI3-5700	-9				50	9.0	CMOS-JI	5.0	±2.0	±1.75 - 1.0	Flash, Improved MP7684
HI3-5700J	-5	HI1-5700S/883			50	18	CMOS-JI	4	±2.0	±0.9	Low cost
HI9P-5700J	-5	HI1-5700S/883			50	18	CMOS-JI	4	±2.0	±0.9	
HI3-5700A	-9	HI1-5700S/883			50	18	CMOS-JI	4	±2.0	±0.9	
HI9P-5700A	-9	HI1-5700S/883			50	18	CMOS-JI	4	±2.0	±0.9	
HI1386JCP			Parallel, Binary, 8-Bit Latch		13	150	Bipolar	2	±0.5	±0.5	High Performance Low-Power 580mW typ at 75msps
HI1386AIL					13	150	Bipolar	2	±0.5	±0.5	
HI1396JCJ					8	200	Bipolar	2	±0.5	±0.5	High Performance Low-Power 870mW typ at 125msps
HI1396AIL					8	200	Bipolar	2	±0.5	±0.5	
HI1396JCP					8	200	Bipolar	2	±0.5	±0.5	
HI1166AIL					4	250	Bipolar	2	±0.5	±0.5	High Performance Low-Power 1.4W typ at 250msps
HI1276AIL					2.5	300	Bipolar	2	±0.5	±0.5	High Performance Low-Power 2.2W typ at 500msps

HARRIS SEMICONDUCTOR

CA3304

CMOS Video Speed 4-Bit Flash A/D Converter

December 1993

Features

- CMOS/SOS Low Power with Video Speed (25mW Typ.)
- Parallel Conversion Technique
- Single Power Supply Voltage (3V to 7.5V)
- 25MHz Sampling Rate (40ns Conversion Time) at 5V Supply
- 4-Bit Latched Tri-State Output with Overflow and Data Change Outputs
- $^1/_8$ LSB Maximum Nonlinearity (A Version)
- Inherent Resistance to Latch-Up Due to SOS Process
- Bipolar Input Range with Optional Second Supply
- Wide Input Bandwidth (25MHz Typ.)

Applications

- TV Video Digitizing (Industrial/Security)
- High Speed A/D Conversion
- Ultrasound Signature Analysis
- Transient Signal Analysis
- High Energy Physics Research
- General-Purpose Hybrid ADCs
- Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- Robot Vision

Description

The Harris CA3304 is a CMOS parallel (FLASH) analog-to-digital converter designed for applications demanding both low-power consumption and high speed digitization. Digitizing at 25MHz, for example, requires only about 35mW.

The CA3304 operates over a wide, full-scale signal input voltage range of 0.5V up to the supply voltage. Power consumption is as low as 10mW, depending upon the clock frequency selected.

The intrinsic high conversion rate makes the CA3304 types ideally suited for digitizing high speed signals. The overflow bit makes possible the connection of two or more CA3304s in series to increase the resolution of the conversion system. A series connection of two CA3304s may be used to produce a 5-bit, 25MHz converter. Operation of two CA3304s in parallel doubles the conversion speed (i.e., increases the sampling rate from 25MHz to 50MHz). A data change pin indicates when the present output differs from the previous, thus allowing compaction of data storage.

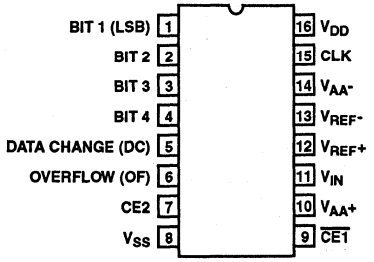
Sixteen paralleled auto-balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel-bit outputs in the CA3304. Fifteen comparators are required to quantize all input voltage levels in this 4-bit converter, and the additional comparator is required for the overflow bit.

Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	SAMPLING RATE	TEMPERATURE RANGE	PACKAGE
CA3304E	±0.25 LSB	25MHz (40ns)	-40°C to +85°C	16 Lead Plastic DIP
CA3304AE	±0.125 LSB	25MHz (40ns)	-40°C to +85°C	16 Lead Plastic DIP
CA3304M	±0.25 LSB	25MHz (40ns)	-40°C to +85°C	16 Lead Plastic SOIC (W)
CA3304AM	±0.125 LSB	25MHZ (40ns)	-40°C to +85°C	16 Lead Plastic SOIC (W)
CA3304D	±0.25 LSB	25MHz (40ns)	-55°C to +125°C	16 Lead Ceramic DIP
CA3304AD	±0.125 LSB	25MHz (40ns)	-55°C to +125°C	16 Lead Ceramic DIP

Pinout

CA3304 (CDIP, PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1790.1

Absolute Maximum Ratings

DC Supply Voltage Range (V_{DD} or V_{AA}+)
(Voltage Referenced to V_{SS} or V_{AA}- Terminal, Whichever is More Negative) ..... -0.5V to +8V
Input Voltage Range
CE1, CE2 Inputs ..... V_{SS} -0.5V to V_{DD} +0.5V
Clock, V_{REF}+, V_{REF}-, V_{IN} Inputs ..... V_{AA} -0.5V to V_{AA} +0.5V
DC Input Current, Any Input ..... ±20mA
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CA3304D	80°C/W	16°C/W
CA3304E	100°C/W	-
CA3304M	100°C/W	-

Maximum Power Dissipation 241mW
Junction Temperature
Ceramic Package ..... +175°C
Plastic Package ..... +150°C
Operating Temperature
CA3304D ..... -55°C to +125°C
CA3304E, CA3304M ..... -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended Operating Conditions

Recommended Supply Voltage Range (V_{DD} or V_{AA}+) ..... 3V to 7.5V
Recommended V_{AA}+ Voltage Range ..... V_{DD} -1V to V_{DD} +2.5V
Recommended V_{AA}- Voltage Range ..... V_{SS} -2.5V to V_{SS} +1V

Electrical Specifications

T_A = +25°C, V_{REF}+ = 2V, V_{DD} = V_{AA}+ = 5V, V_{AA}- = V_{REF}- = V_{SS} = GND, f_{CLK} = 25MHz Unless Otherwise Specified

PARAMETERS			TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE							
Resolution				4	-	-	Bits
Input Errors	Integral Linearity Error	CA3304A		-	±0.1	±0.125	LSB
		CA3304		-	±0.125	±0.25	LSB
	Differential Linearity Error	CA3304A		-	±0.1	±0.125	LSB
		CA3304		-	±0.125	±0.25	LSB
	Offset Error (Unadjusted)	CA3304A		-	-	±0.75	LSB
		CA3304		-	-	±1.0	LSB
	Gain Error (Unadjusted)	CA3304A		-	-	±0.75	LSB
		CA3304		-	-	±1.0	LSB
DYNAMIC CHARACTERISTICS (Input Signal Level 0.5dB Below Full Scale)							
Conversion Timing	Aperture Delay			-	3	-	ns
Signal to Noise Ratio (SNR) = RMS Signal / RMS Noise			F_S = 25MHz, f_{IN} = 100kHz	-	23.7	-	dB
			F_S = 25MHz, f_{IN} = 5MHz	-	23.6	-	dB
Signal to Noise Ratio (SINAD) = RMS Signal / RMS Noise + Distortion			F_S = 25MHz, f_{IN} = 100kHz	-	23.4	-	dB
			F_S = 25MHz, f_{IN} = 5MHz	-	22.8	-	dB
Total Harmonic Distortion, THD			F_S = 25MHz, f_{IN} = 100kHz	-	-34.5	-	dBc
			F_S = 25MHz, f_{IN} = 5MHz	-	-31.0	-	dBc
Effective Number of Bits (ENOB)			F_S = 25MHz, f_{IN} = 100kHz	-	3.67	-	Bits
			F_S = 25MHz, f_{IN} = 5MHz	-	3.57	-	Bits
ANALOG INPUTS							
Input Range	Full Scale Input Range		(Notes 1, 4)	0.5	-	V_{AA}	V
Input Loading	Input Capacitance			-	10	-	pF
	Input Current		V_{IN} = 2.0V (Note 2)	-	150	200	µA
Allowable Input Bandwidth			(Note 4)	-	25	f_{CLK}/2	MHz
-3dB Input Bandwidth				-	40	-	MHz

Electrical Specifications T_A = +25°C, V_{REF}+ = 2V, V_{DD} = V_{AA}+ = 5V, V_{AA}- = V_{REF}- = V_{SS} = GND, f_{CLK} = 25MHz Unless Otherwise Specified **(Continued)**

PARAMETERS			TEST CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE INPUTS							
Input Range	V_{REF}+ Range		(Note 4)	V_{AA}- +0.5	-	V_{AA}+	V
	V_{REF}- Range		(Note 4)	V_{AA}-	-	V_{AA}+ -0.5	V
Input Loading	Resistor Ladder Impedance		V_{IN} = 5V, CLK = Low	640	-	960	Ω
DIGITAL INPUTS							
Digital Input	Maximum V_{IN}, Low	CLOCK	(Notes 3, 4)	-	-	0.3 x V_{AA}	V
		$\overline{CE1}$, CE2	(Note 4)	-	-	0.3 x V_{DD}	V
	Minimum V_{IN}, High	CLOCK	(Notes 3, 4)	0.7 x V_{AA}	-	-	V
		$\overline{CE1}$, CE2	(Note 4)	0.7 x V_{DD}	-	-	V
	Input Leakage, Except CLK		V = 0V, 5V	-	-	±1	µA
	Input Leakage, CLK		(Note 3)	-	±100	±150	µA
DIGITAL OUTPUTS							
Digital Outputs	Output Low (Sink) Current		V_O = 0.4V	6	-	-	mA
	Output High (Source) Current		V_O = 4.6V	-3	-	-	mA
	Tri-State Leakage Current		V_O = 0V, 5V	-	±0.2	±5	µA
TIMING CHARACTERISTICS							
Conversion Timing	Maximum Conversion Speed		CLK = Square Wave	25	35	-	MSPS
	Auto-Balance Time (ϕ1)			20	-	-	ns
	Sample Time (ϕ2)			20	-	5000	ns
Output Timing	Data Valid Delay		(Note 4)	-	30	40	ns
	Data Hold Time		(Note 4)	15	25	-	ns
	Output Enable Time			-	15	-	ns
	Output Disable Time			-	10	-	ns
POWER SUPPLY CHARACTERISTICS							
Device Current, I_{AA}			Continuous Clock	-	5.5	-	mA
			Continuous ϕ2	-	0.4	-	mA
			Continuous ϕ1	-	2	-	mA
Device Current, I_{DD}			Continuous Clock	-	1.5	-	mA
	V_{AA}+ = 5V, V_{SS} = $\overline{CE1}$ = V_{AA}- = CLK = GND		Continuous ϕ2	-	5	10	mA
	V_{AA}+ = 7V		Continuous ϕ1	-	5	20	mA

NOTES:

1. Full scale input range, V_{REF}+ - V_{REF}-, may be in the range of 0.5V to V_{AA}+ -V_{AA}- volts. Linearity errors increase at lower full scale ranges, however.
2. Input current is due to energy transferred to the input at the start of the sample period. The average value is dependent on input and V_{DD} voltage.
3. The CLK input is a CMOS inverter with a 50kΩ feedback resistor. It operates from the V_{AA}+ and V_{AA}- supplies. It may be AC-coupled with a 1V peak-to-peak minimum source.
4. Parameter not tested, but guaranteed by design or characterization.

Pin Description

PIN NUMBER	NAME	DESCRIPTION	
1	Bit 1	Bit 1 (LSB)	Output Data Bits (High = True)
2	Bit 2	Bit 2	
3	Bit 3	Bit 3	
4	Bit 4	Bit 4 (MSB)	
5	DC	Data Change	
6	OF	Overflow	
7	CE2	Tri-state output enable input, active low. See the Chip Enable Truth Table.	
8	V_{SS}	Digital Ground	
9	$\overline{CE1}$	Tri-state output enable input, active high. See the Chip Enable Truth Table.	
10	$V_{AA}+$	Analog power supply, +5V	
11	V_{IN}	Analog signal input	
12	$V_{REF}+$	Reference Voltage Positive Input	
13	$V_{REF}-$	Reference Voltage Negative Input	
14	$V_{AA}-$	Analog Ground	
15	CLK	Clock Input	
16	V_{DD}	Digital Power Supply, +5V	

CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	BIT 1 - BIT 4	DC, OF
0	1	Valid	Valid
1	1	Tri-State	Valid
X	0	Tri-State	Tri-State

X = Don't Care

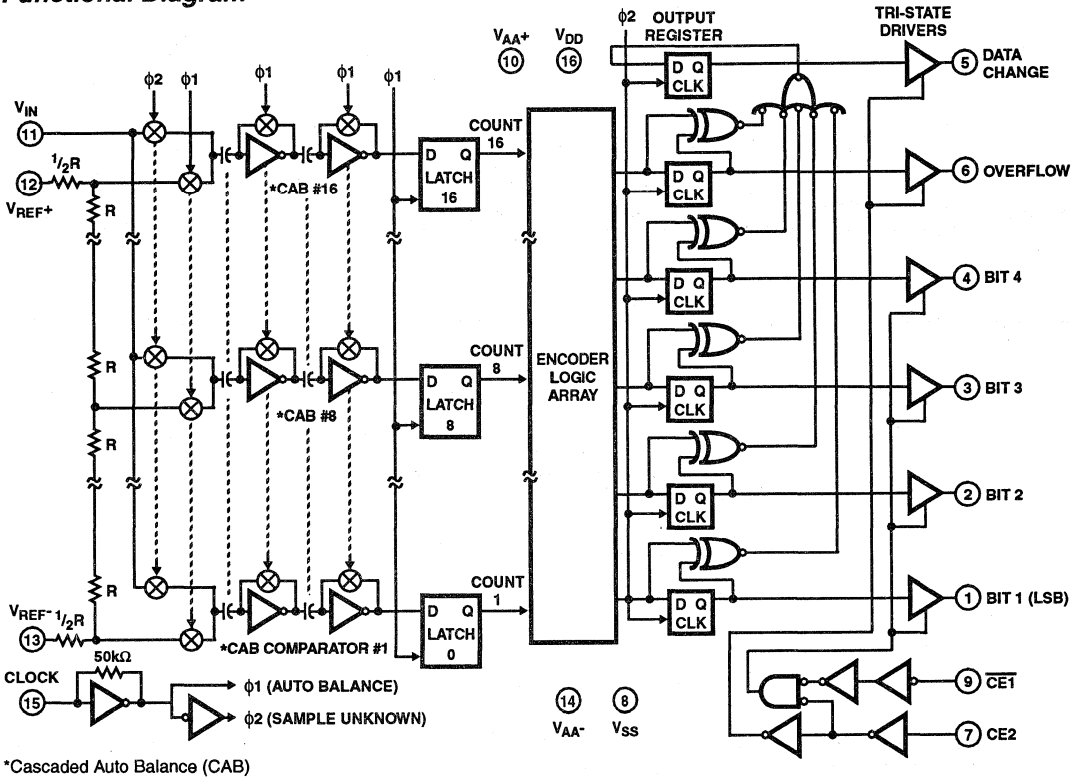
TABLE 1. OUTPUT CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE (V)					OUTPUT CODE					DECIMAL COUNT
	$V_{REF}+$ = 1V $V_{REF}-$ = -1V	1.6V 0V	2V 0V	3.2V 0V	4.8V 0V	OF	B4	B3	B2	B1	
Zero	-1.000	0	0	0	0	0	0	0	0	0	0
1 LSB	-0.875	0.1	0.125	0.2	0.3	0	0	0	0	1	1
2 LSB	-0.750	0.2	0.250	0.4	0.6	0	0	0	1	0	2
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
$^1/_2$ Full Scale -1 LSB	-0.125	0.7	0.875	1.4	2.1	0	0	1	1	1	7
$^1/_2$ Full Scale	0	0.8	1.000	1.6	2.4	0	1	0	0	0	8
$^1/_2$ Full Scale +1 LSB	0.125	0.9	1.125	1.8	2.7	0	1	0	0	1	9
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
Full Scale -1 LSB	0.750	1.4	1.750	2.8	4.2	0	1	1	1	0	14
Full Scale	0.875	1.5	1.875	3.0	4.5	0	1	1	1	1	15
Overflow	1.000	1.6	2.000	3.2	4.8	1	1	1	1	1	31
Step Size	0.125	0.1	0.125	0.2	0.3						

NOTES:

1. The voltages listed are the ideal centers of each output code shown as a function of its associated reference voltage See Ideal Transfer Curve Figure 6. The output code should exist for an input equal to the ideal center voltage $\pm^1/_2$ of the step size.

Functional Diagram



*Cascaded Auto Balance (CAB)

NOTE: $\overline{CE1}$ and CE2 inputs and data outputs have standard CMOS protection networks to V_{DD} and V_{SS}. Analog inputs and clock have standard CMOS protection networks to V_{AA}+ and V_{AA}-.

Timing Diagrams

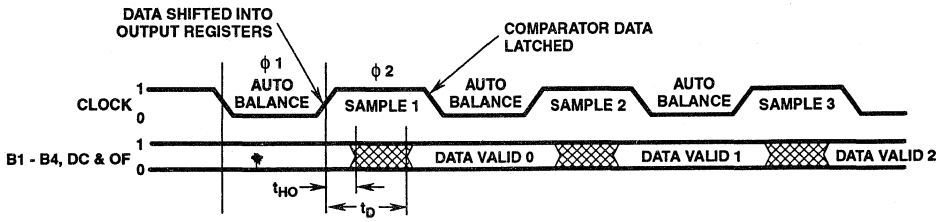


FIGURE 1. TIMING DIAGRAM

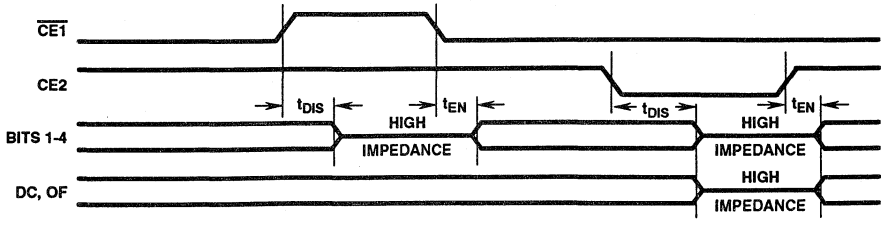


FIGURE 2. OUTPUT ENABLE/DISABLE TIMING

Timing Diagrams (Continued)

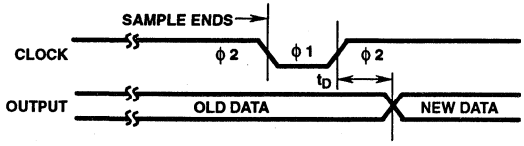


FIGURE 3A.

With ϕ2 as standby state (fastest method, but standby limited to 5μs maximum)

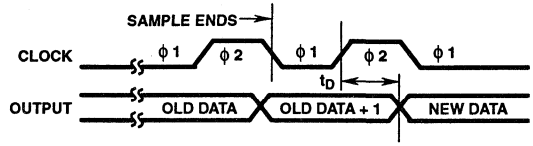


FIGURE 3B.

With ϕ1 as standby state (indefinite standby, double pulse needed)

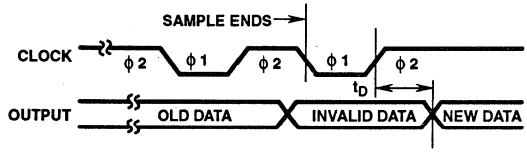


FIGURE 3C.

With ϕ2 as standby state (indefinite standby, lower power than 3B)

FIGURE 3. PULSE-MODE TIMING DIAGRAMS

Typical Performance Curves

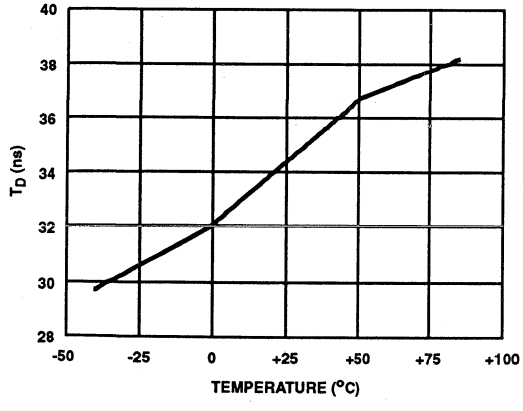


FIGURE 4. DATA DELAY vs TEMPERATURE

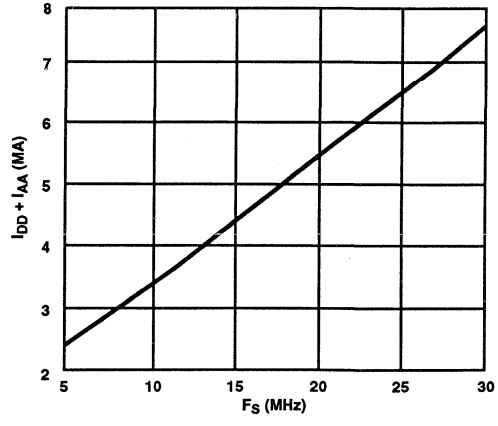


FIGURE 5. DEVICE CURRENT vs SAMPLE FREQUENCY

Typical Performance Curves (Continued)

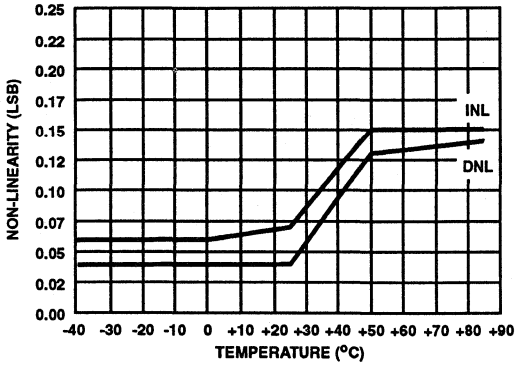


FIGURE 6. NON-LINEARITY vs TEMPERATURE

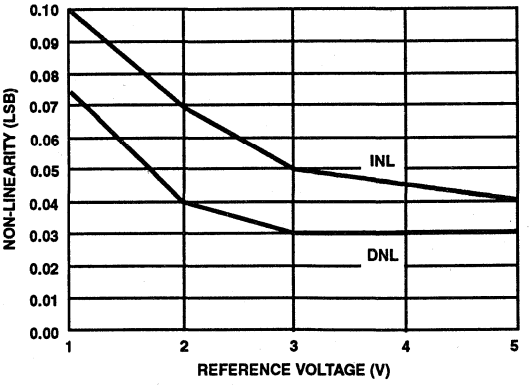


FIGURE 7. NON-LINEARITY vs REFERENCE VOLTAGE

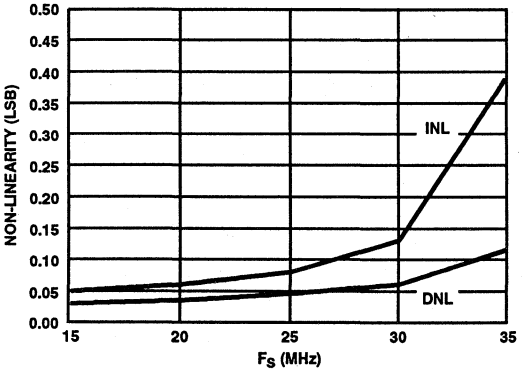


FIGURE 8. NON-LINEARITY vs SAMPLE FREQUENCY

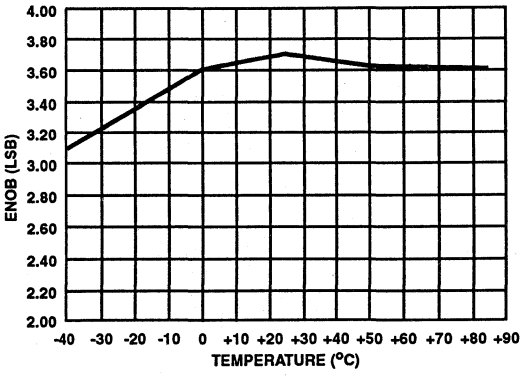


FIGURE 9. EFFECTIVE BITS vs TEMPERATURE

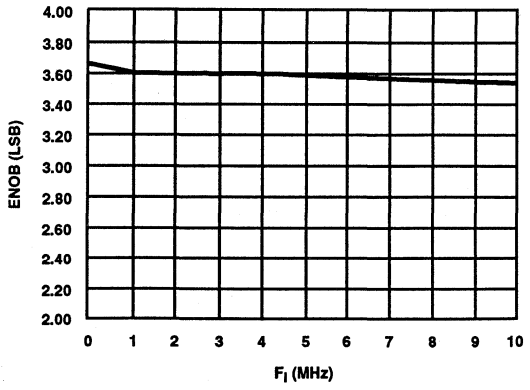


FIGURE 10. EFFECTIVE BITS vs INPUT FREQUENCY

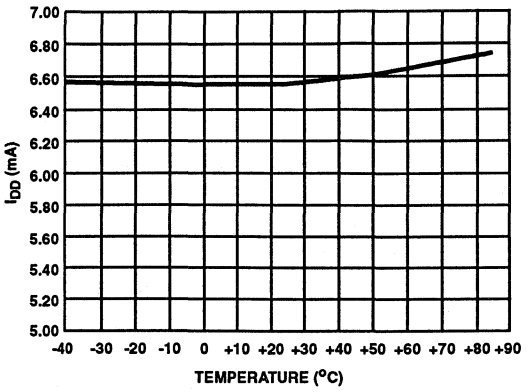


FIGURE 11. DEVICE CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

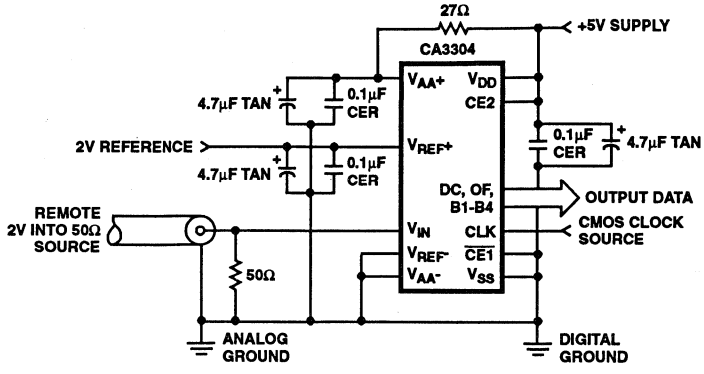


FIGURE 12A. TYPICAL CA3304 UNIPOLAR CIRCUIT CONFIGURATION

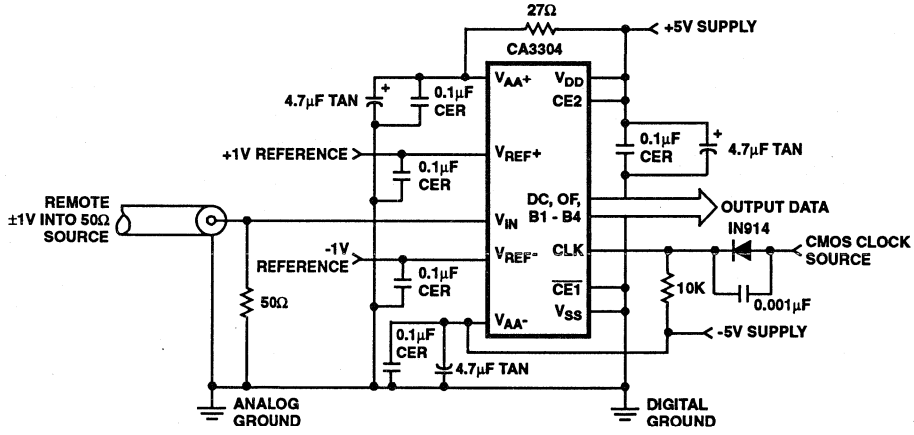


FIGURE 12B. TYPICAL CA3304 BIPOLAR CIRCUIT CONFIGURATION

FIGURE 12.

Description

Device Operation

A sequential parallel technique is used by the CA3304 converter to obtain its high speed operation. The sequence consists of the "Auto Balance" phase and the "Sample Unknown" phase (Refer to the circuit diagram). Each conversion takes one clock cycle.† The "Auto Balance" (ϕ1) occurs during the Low period of the clock cycle, and the "Sample Unknown" (ϕ2) occurs during the High period of the clock cycle.

† This device requires only a single-phase clock. The terminology of ϕ1 and ϕ2 refers to the High and Low periods of the same clock.

During the "Auto Balance" phase, a transmission-gate switch is used to connect each of 16 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{TAP}(N) = [(V_{REF}/16) \times N] - [V_{REF}/(2 \times 16)]$$
$$= V_{REF}[(2N - 1)/32]$$

Where: $V_{TAP}(N)$ = Reference ladder tap voltage at point N.

V_{REF} = Voltage across V_{REF}- to V_{REF}+

N = Tap number (1 through 16)

The other side of the capacitor is connected to a single-stage inverting amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately $(V_{DD} - V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and V_{IN} is switched to all 16 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators whose tap voltages were lower than V_{IN} will drive the comparator outputs to a "low" state. All comparators whose tap voltages were higher than V_{IN} will drive the comparator outputs to a "high" state. A second, capacitor-coupled, auto-zeroed amplifier further amplifies the outputs.

The status of all these comparator amplifiers are stored at the end of this phase (ϕ2), by a secondary latching amplifier stage. Once latched, the status of the 16 comparators is decoded by a 16 to 5 bit decode array and the results are clocked into a storage register at the rising edge of the next ϕ2.

If the input is greater than 31/32 x V_{REF}, the overflow output will go "high". (The bit outputs will remain high). If the output differs from that of the previous conversion, the data change output will go "high".

A tri-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B4 when it is in a high state. CE2 will independently disable B1 through B4 and the OF and DC buffers when it is in the low state.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3304 via the following steps. (Refer to timing diagram Figure 3). The rising edge of the clock input will start a "sample" phase. During this entire "High" state of the clock, the 16 comparators will track the input voltage and the 16 latches will track the comparator outputs. At the falling edge of the clock, all 16 comparator outputs are captured by the 16 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this "Low" state of the clock the output of the latches propagates through the decode array and a 6-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 6-bit code is shifted into the output registers and appears with time delay t_D as valid data at the output of the tri-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse Mode Operation

For sampling high speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of three ways. The fastest method is to keep the converter in the Sample Unknown phase, ϕ2, during the standby state. The device can now be pulsed through the Auto Balance phase with as little as 20ns. The analog value is captured on the leading edge of ϕ1 and is transferred into the output registers on the trailing edge of ϕ1. We are now back in the standby state, ϕ2, and another conversion can be started within 20ns, but not later than 5μs due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between ϕ2 and ϕ1, the lower the power consumption. (See Timing Diagram Figure 3A).

The second method uses the Auto Balance phase, ϕ1, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two ϕ2 pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second ϕ2 pulse is needed to transfer the date into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes place in 40ns, but the repetition rate may be as slow as desired. The disadvantage to this method is the slightly higher device dissipation due to the low ratio of ϕ2 to ϕ1. (See Timing Diagram Figure 3B).

For applications requiring both indefinite standby and lowest power, standby can be in the ϕ2 (Sample Unknown) state with two ϕ1 pulses to generate valid data (see Figure 3C). The conversion process now takes 60ns. [Note that the above numbers do not include the t_D (Output Delay) time.]

Increased Accuracy

In most case the accuracy of the CA3304 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, two adjustments can be made to obtain better accuracy; i.e., offset trim and gain trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a DC shift to V_{IN} or by the offset trim of the op amp. When this is not possible the V_{REF}- input can be adjusted to produce an offset trim.

The theoretical input voltage to produce the first transition is 1/2 LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = {}^1/_2 \text{ LSB} = {}^1/_2(V_{REF}/16)$$
$$= V_{REF}/32$$

Adjust offset by applying this input voltage and adjusting the V_{REF}- voltage or input amplifier offset until an output code alternating between 0 and 1 occurs.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op-amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 15 to overflow transition. That voltage is ${}^1/_2$ LSB less than V_{REF}+ and is calculated as follows:

$$V_{IN} \text{ (15 to 16 transition)} = V_{REF} - V_{REF}/32$$
$$= V_{REF}\ (31/32)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 15 to overflow transition. Now adjust V_{REF}+ until that transition occurs on the outputs.

Layout, Input And Supply Considerations

The CA3304 should be mounted on a ground-planed, printed-circuit board, with good high-frequency decoupling capacitors mounted as close as possible. If the supply is noisy, decouple V_{AA}+ with a resistor as shown in Figure 12A. The CA3304 outputs current spikes to its input at the start of the auto-balance and sample clock phases. A low impedance source, such as a locally-terminated 50Ω coax cable, should be used to drive the input terminal. A fast-settling buffer such as the HA-5033, HA-5242, or CA3450 should be used if the source is high impedance. The V_{REF} terminals also have current spikes, and should be well bypassed.

Care should be taken to keep digital signals away from the analog input, and to keep digital ground currents away from the analog ground. If possible, the analog ground should be connected to digital ground only at the CA3304.

Bipolar Operation

The CA3304, with separate analog (V_{AA}+, V_{AA}-) and digital (V_{DD}, V_{SS}) supply pins, allows true bipolar or negative input operation. The V_{AA}- pin may be returned to a negative supply (observing maximum voltage ratings to V_{AA}+ or V_{DD} and recommended rating to V_{SS}), thus allowing the V_{REF}- potential also to be negative. Figure 12B shows operation with an input range of -1V to +1V. Similarly, V_{AA}+ and V_{REF}+ could be maintained at a higher voltage than V_{DD}, for an input range above the digital supply.

Digital Input And Output Levels

The clock input is a CMOS inverter operating from and with logic input levels determined by the V_{AA} supplies. If V_{AA}+ or V_{AA}- are outside the range of the digital supplies, it may be necessary to level shift the clock input to meet the required 30% to 70% of V_{AA} input swing. Figure 12B shows an example for a negative V_{AA}-.

An alternate way of driving the clock is to capacitively couple the pin from a source of at least 1V peak-to-peak. An internal 50kΩ feedback resistor will keep the DC level at the intrinsic trip point. Extremely non-symmetrical clock waveforms should be avoided, however.

The remaining digital inputs and outputs are referenced to V_{DD} and V_{SS}. If TTL or other lower voltage sources are to drive the CA3304, either pull-up resistors or CD74HCT series "QMOS" buffers are recommended.

5-Bit Resolution

To obtain 5-bit resolution, two CA3304s can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, tri-state outputs, and chip-enable controls - all of which are available on the CA3304.

The first step for connecting a 5-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 13. Since the absolute-resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the fifth bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The tri-state outputs of the two devices (bits 1 through 4) are now connected in parallel to complete the circuitry.

Definitions

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the CA3304. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from fullscale for all these tests.

Signal-to-Noise (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR})/6.02$$

where: $V_{CORR} = 0.5dB$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

Operating and Handling Considerations

1. Handling

All inputs and outputs of CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in ICAN-6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause the power supply voltages to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} or $V_{AA}+$ nor less than V_{SS} or $V_{AA}-$ (depending upon which supply the protection network is referenced. See Maximum Ratings). Input currents must not exceed 20mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to any supply potential may damage CMOS devices by exceeding the maximum device dissipation.

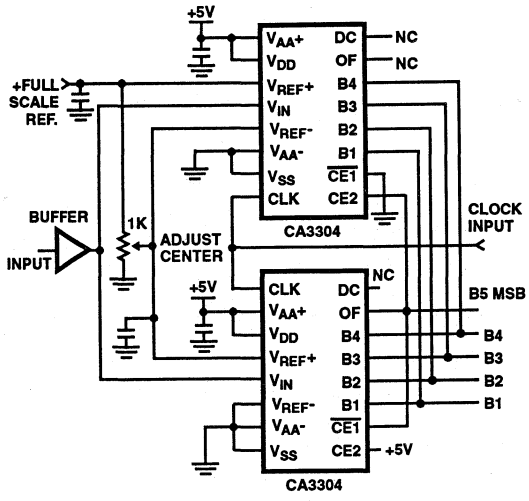


FIGURE 13. TYPICAL CA3304 5-BIT CONFIGURATION

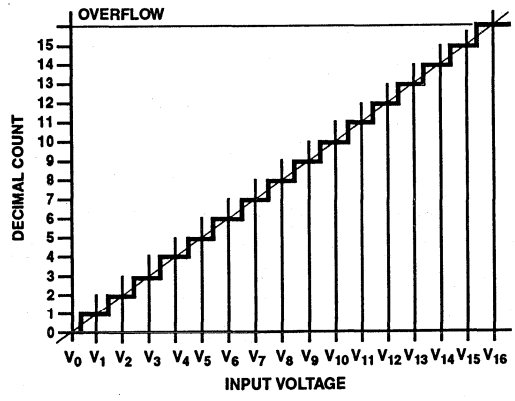


FIGURE 14. IDEAL TRANSFER CURVE

HARRIS SEMICONDUCTOR

CA3306

CMOS Video Speed 6-Bit Flash A/D Converter

December 1993

Features

- CMOS Low Power with Video Speed (70mW Typ.)
- Parallel Conversion Technique
- Signal Power Supply Voltage (3V to 7.5V)
- 15MHz Sampling Rate with Single 5V Supply
- 6-Bit Latched Tri-State Output with Overflow Bit
- Pin-for-Pin Retrofit for the CA3300

Applications

- TV Video Digitizing
- Ultrasound Signature Analysis
- Transient Signal Analysis
- High Energy Physics Research
- High Speed Oscilloscope Storage/Display
- General Purpose Hybrid ADCs
- Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- Robot Vision

Description

The CA3306 family are CMOS parallel (FLASH) analog-to-digital converters designed for applications demanding both low power consumption and high speed digitization. Digitizing at 15MHz, for example, requires only about 50mW.

The CA3306 family operates over a wide, full scale signal input voltage range of 1V up to the supply voltage. Power consumption is as low as 15mW, depending upon the clock frequency selected. The CA3306 types may be directly retrofitted into CA3300 sockets, offering improved linearity at a lower reference voltage and high operating speed with a 5V supply.

The intrinsic high conversion rate makes the CA3306 types ideally suited for digitizing high speed signals. The overflow bit makes possible the connection of two or more CA3306s in series to increase the resolution of the conversion system. A series connection of two CA3306s may be used to produce a 7-bit high speed converter. Operation of two CA3306s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15MHz to 30MHz).

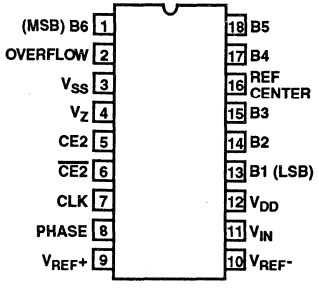
Sixty-four paralleled auto balanced comparators measure the input voltage with respect to a known reference to produce the parallel bit outputs in the CA3306. Sixty-three comparators are required to quantize all input voltage levels in this 6-bit converter, and the additional comparator is required for the overflow bit.

Ordering Information

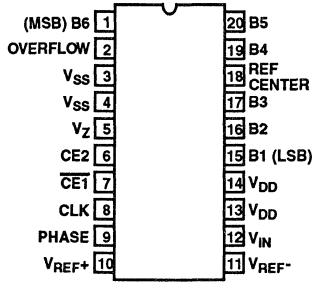
PART NUMBER	LINEARITY (INL, DNL)	SAMPLING RATE	TEMPERATURE RANGE	PACKAGE
CA3306E	±0.5 LSB	15MHz (67ns)	-40°C to +85°C	18 Lead Plastic DIP
CA3306AE	±0.25 LSB	15MHz (67ns)	-40°C to +85°C	18 Lead Plastic DIP
CA3306CE	±0.5 LSB	10MHz (100ns)	-40°C to +85°C	18 Lead Plastic DIP
CA3306M	±0.5 LSB	15MHz (67ns)	-40°C to +85°C	20 Lead Plastic SOIC
CA3306CM	±0.5 LSB	10MHz (100ns)	-40°C to +85°C	20 Lead Plastic SOIC
CA3306D	±0.5 LSB	15MHz (67ns)	-55°C to +125°C	18 Lead Ceramic DIP
CA3306AD	±0.25 LSB	15MHz (67ns)	-55°C to +125°C	18 Lead Ceramic DIP
CA3306CD	±0.5 LSB	10MHz (100ns)	-55°C to +125°C	18 Lead Ceramic DIP
CA3306J3	±0.5 LSB	15MHz (67ns)	-55°C to +125°C	20 Lead LCC
CA3306J3	±0.5 LSB	10MHz (100ns)	-55°C to +125°C	20 Lead LCC

Pinouts

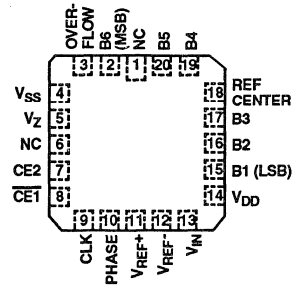
CA3306 (PDIP, CDIP)
TOP VIEW



CA3306 (SOIC)
TOP VIEW



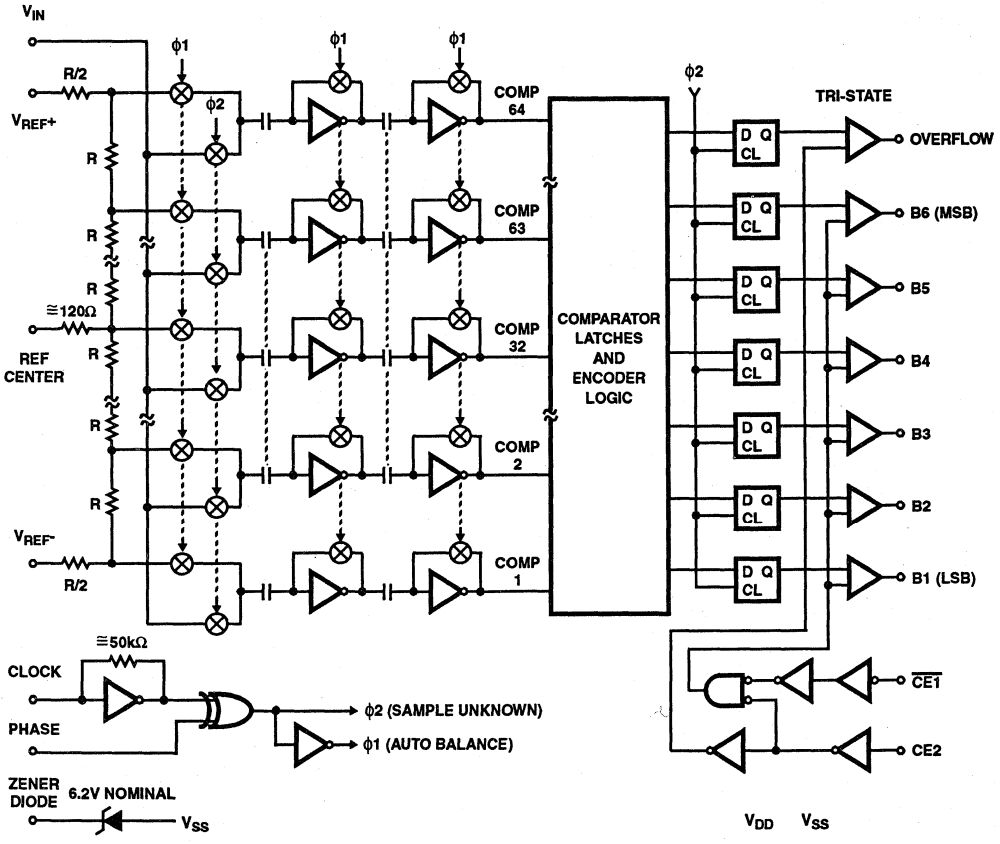
CA3306 (LCC)
TOP VIEW



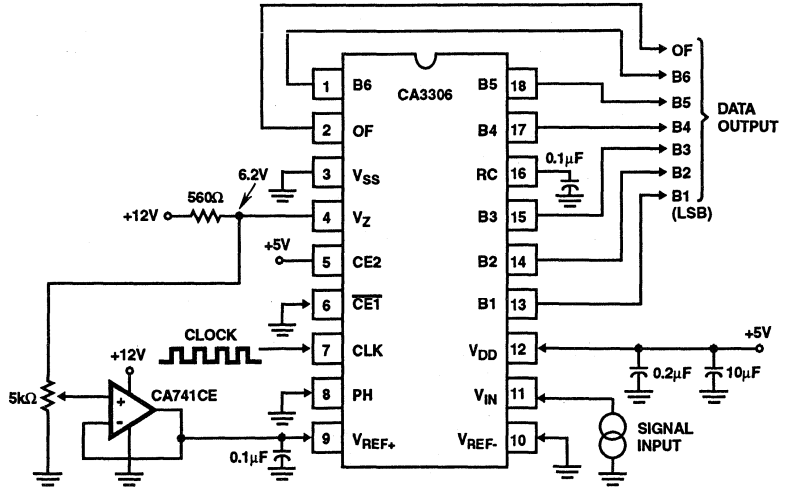
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3102

Functional Block Diagram



Typical Application Circuit



Absolute Maximum Ratings

DC Supply Voltage Range, V_{DD}
Voltage Referenced to V_{SS} Terminal . . . . . -0.5V to +8.5V
Input Voltage Range
All Inputs Except Zener . . . . . -0.5V to V_{DD} + 0.5V
DC Input Current
CLK, PH, $\overline{CE1}$, CE2, V_{IN} . . . . . ±20mA
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	70°C/W	12°C/W
Plastic DIP	95°C/W	-
Plastic SOIC	95°C/W	-
Ceramic LCC	65°C/W	12°C/W

Maximum Power Dissipation
E, M, or D Package 315mW
Operating Temperature Range (T_A)
Ceramic Package (D Suffix) . . . . . -55°C to +125°C
Plastic Package (E or M Suffix) . . . . . -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage Range . . . . . 3V to 8V

Max Junction Temperature
Ceramic Package . . . . . +175°C
Plastic Package . . . . . +150°C

Electrical Specifications

T_A = +25°C, V_{DD} = 5V, V_{REF}+ = 4.8V, V_{SS} = V_{REF}- = GND, Clock = 15MHz Square Wave for CA3306 or CA3306A, 10MHz for CA3306C

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE						
Resolution			6	-	-	Bits
Integral Linearity Error, INL	CA3306, CA3306C		-	±0.25	±0.5	LSB
	CA3306A		-	±0.2	±0.25	LSB
Differential Linearity Error, DNL	CA3306, CA3306C		-	±0.25	±0.5	LSB
	CA3306A		-	±0.2	±0.25	LSB
Offset Error (Unadjusted)	CA3306, CA3306C	(Note 1)	-	±0.5	±1	LSB
	CA3306A		-	±0.25	±0.5	LSB
Gain Error (Unadjusted)	CA3306, CA3306C	(Note 2)	-	±0.5	±1	LSB
	CA3306A		-	±0.25	±0.5	LSB
Gain Temperature Coefficient			-	+0.1	-	mV/°C
Offset Temperature Coefficient			-	-0.1	-	mV/°C
DYNAMIC CHARACTERISTICS (Input Signal Level 0.5dB Below Full Scale)						
Maximum Conversion Speed	CA3306C		10	13	-	MSPS
	CA3306, CA3306A		15	20	-	MSPS
Maximum Conversion Speed	CA3306C	(Note 4)	12	-	-	MSPS
	CA3306, CA3306A	$\phi1$, $\phi2 \geq$ Minimum	18	-	-	MSPS
Allowable Input Bandwidth		(Note 4)	DC	-	$f_{CLOCK/2}$	MHz
-3dB Input Bandwidth			-	30	-	MHz
Signal to Noise Ratio (SNR) $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$		F_S = 15MHz, f_{IN} = 100kHz	-	34.6	-	dB
		F_S = 15MHz, f_{IN} = 5MHz	-	33.4	-	dB
Signal to Noise Ratio (SINAD) $= \frac{\text{RMS Signal}}{\text{RMS Noise+Distortion}}$		F_S = 15MHz, f_{IN} = 100kHz	-	34.2	-	dB
		F_S = 15MHz, f_{IN} = 5MHz	-	29.0	-	dB
Total Harmonic Distortion, THD		F_S = 15MHz, f_{IN} = 100kHz	-	-46.0	-	dBc
		F_S = 15MHz, f_{IN} = 5MHz	-	-30.0	-	dBc
Effective Number of Bits (ENOB)		F_S = 15MHz, f_{IN} = 100kHz	-	5.5	-	Bits
		F_S = 15MHz, f_{IN} = 5MHz	-	4.5	-	Bits

Electrical Specifications T_A = +25°C, V_{DD} = 5V, V_{REF}+ = 4.8V, V_{SS} = V_{REF}- = GND, Clock = 15MHz Square Wave for CA3306 or CA3306A, 10MHz for CA3306C **(Continued)**

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Positive Full Scale Input Range		(Notes 3, 4)	1	4, 8	V_{DD} + 0.5	V
Negative Full Scale Input Range		(Notes 3, 4)	-0.5	0	V_{DD} - 1	V
Input Capacitance			-	15	-	pF
Input Current		V_{IN} = 4.92V, V_{DD} = 5V	-	-	±500	µA
INTERNAL VOLTAGE REFERENCE						
Zener Voltage		I_Z = 10mA	5.4	6.2	7.4	V
Zener Dynamic Impedance		I_Z = 10mA, 20mA	-	12	25	Ω
Zener Temperature Coefficient			-	-0.5	-	mV/°C
REFERENCE INPUTS						
Resistor Ladder Impedance			650	1100	1550	Ω
DIGITAL INPUTS						
Maximum V_{IN}, Logic 0		All Digital Inputs (Note 4)	-	-	0.3 x V_{DD}	V
Maximum V_{IN}, Logic 1		All Digital Inputs (Note 4)	0.7 x V_{DD}	-	-	V
Digital Input Current		Except CLK, V_{IN} = 0V, 5V	-	±1	±5	µA
Digital Input Current		CLK Only	-	±100	±200	µA
DIGITAL OUTPUTS						
Digital Output Tri-State Leakage		V_{OUT} = 0V, 5V	-	±1	±5	µA
Digital Output Source Current		V_{OUT} = 4.6V	-1.6	-	-	mA
Digital Output Sink Current		V_{OUT} = 0.4V	3.2	-	-	mA
TIMING CHARACTERISTICS						
Auto Balance Time (ϕ1)	CA3306C		50	-	∞	ns
	CA3306, CA3306A		33	-	∞	
Sample Time (ϕ2)	CA3306C	(Note 4)	33	-	5000	ns
	CA3306, CA3306A		22	-	5000	ns
Aperture Delay			-	8	-	ns
Aperture Jitter			-	100	-	ps_{P-P}
Output Data Valid Delay (T_D)	CA3306C		-	35	50	ns
	CA3306, CA3306A		-	30	40	ns
Output Data Hold Time (T_H)		(Note 4)	15	25	-	ns
Output Enable Time, (T_{EN})			-	20	-	ns
Output Disable Time (T_{DIS})			-	15	-	ns
POWER SUPPLY CHARACTERISTICS						
I_{DD} Current, Refer to Figure 4	CA3306C	Continuous Conversion (Note 4)	-	11	20	mA
	CA3306, CA3306A		-	14	25	mA
I_{DD} Current		Continuous ϕ1	-	7.5	15	mA

NOTES:

1. OFFSET ERROR is the difference between the input voltage that causes the 00 to 01 output code transition and (V_{REF}+ - V_{REF}-)/128.
2. GAIN ERROR is the difference the input voltage that causes the $3F_{16}$ to overflow output code transition and (V_{REF}+ - V_{REF}-) x 127/128.
3. The total input voltage range, set by V_{REF}+ and V_{REF}-, may be in the range of 1 to (V_{DD} + 1) V.
4. Parameter not tested, but guaranteed by design or characterization.

Timing Waveforms

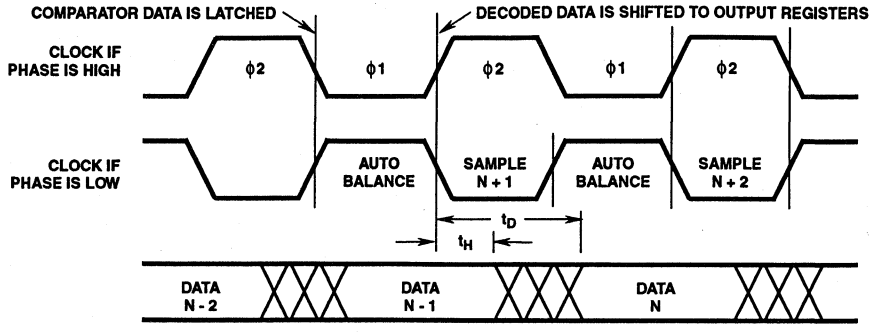


FIGURE 1. INPUT-TO-OUTPUT

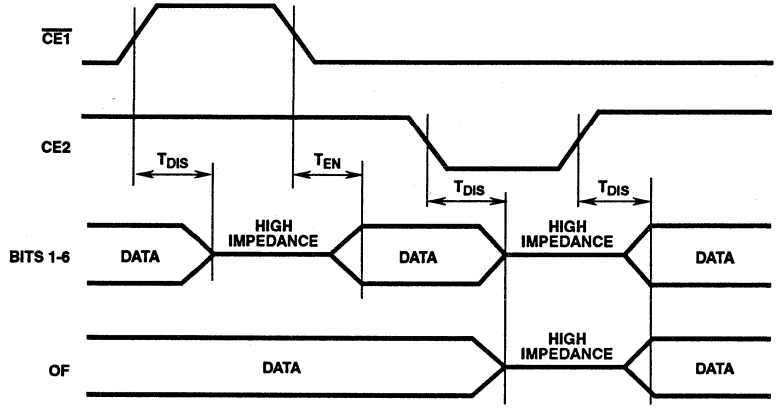


FIGURE 2. OUTPUT ENABLE

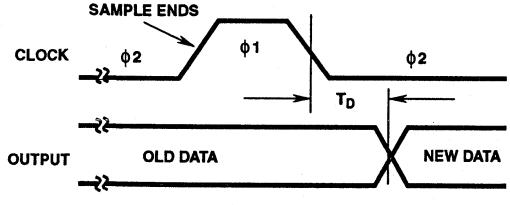


FIGURE 3A.

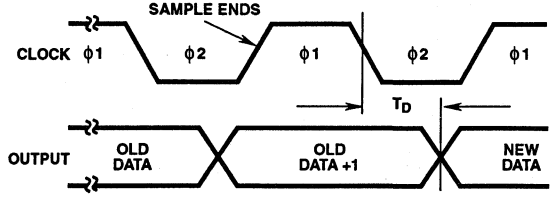


FIGURE 3B.

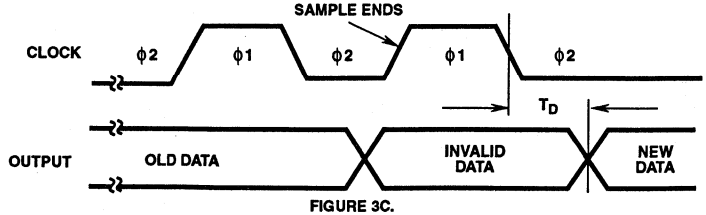


FIGURE 3C.

FIGURE 3. PULSE MODE

Typical Performance Curves

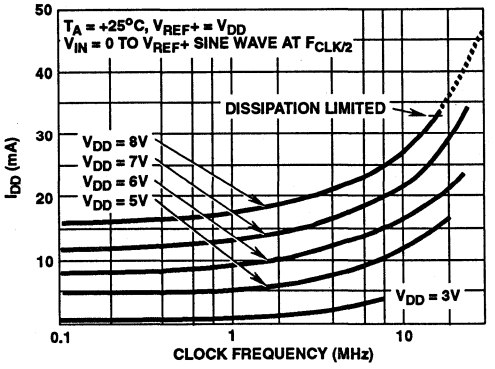


FIGURE 4. TYPICAL I_{DD} AS A FUNCTION OF V_{DD}

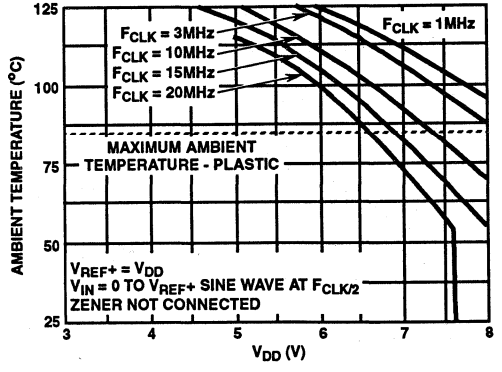


FIGURE 5. TYPICAL MAXIMUM AMBIENT TEMPERATURE AS A FUNCTION OF SUPPLY VOLTAGE

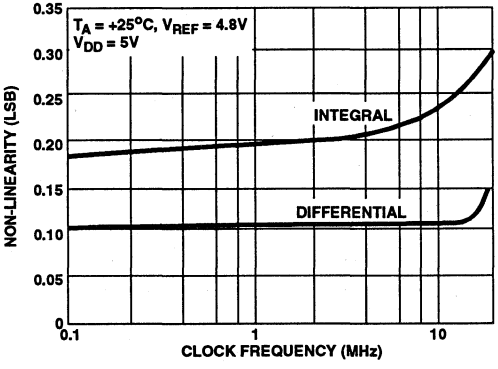


FIGURE 6. TYPICAL NON-LINEARITY AS A FUNCTION OF CLOCK SPEED

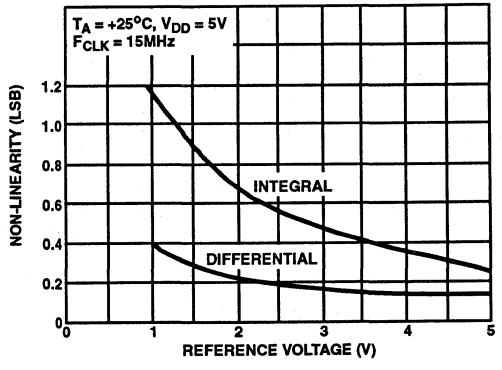


FIGURE 7. TYPICAL NON-LINEARITY AS A FUNCTION OF REFERENCE VOLTAGE

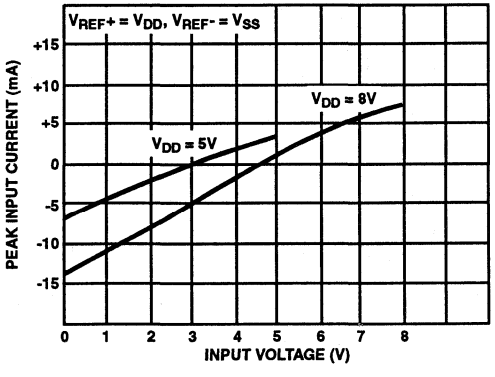


FIGURE 8. TYPICAL PEAK INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

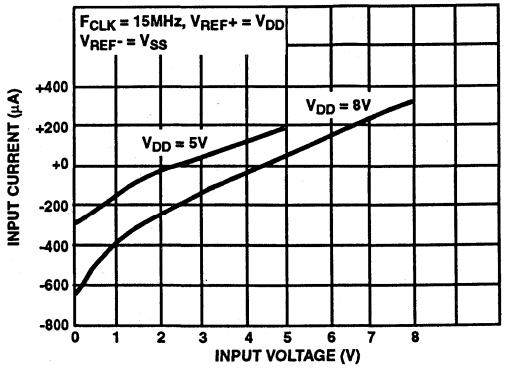


FIGURE 9. TYPICAL AVERAGE INPUT CURRENT AS A FUNCTION OF INPUT VOLTAGE

Typical Performance Curves (Continued)

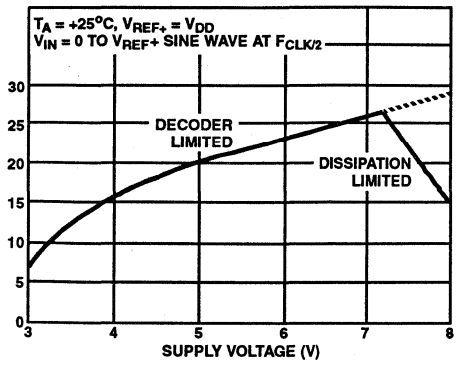


FIGURE 10. TYPICAL MAXIMUM CLOCK FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

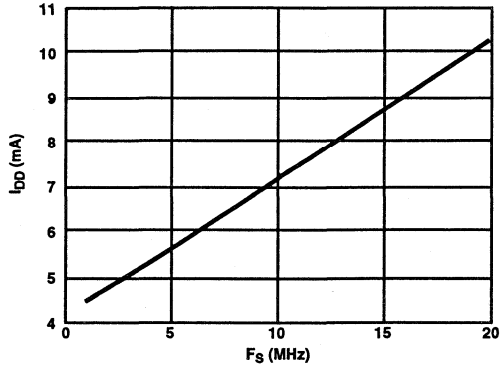


FIGURE 11. DEVICE CURRENT vs SAMPLE FREQUENCY

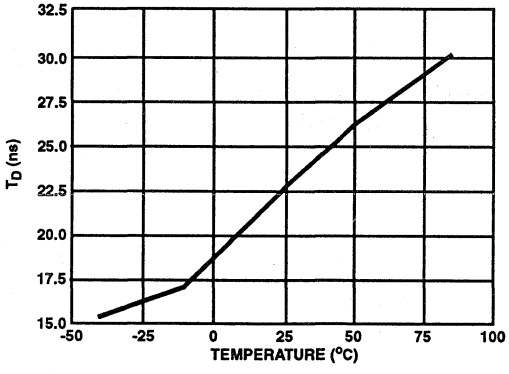


FIGURE 12. DATA DELAY vs TEMPERATURE

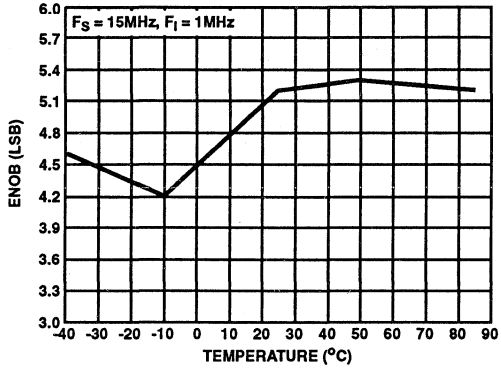


FIGURE 13. ENOB vs TEMPERATURE

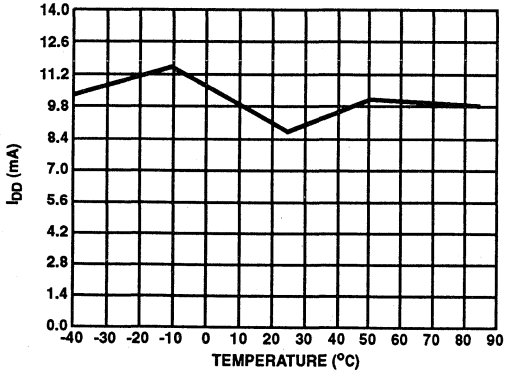


FIGURE 14. I_{DD} vs TEMPERATURE

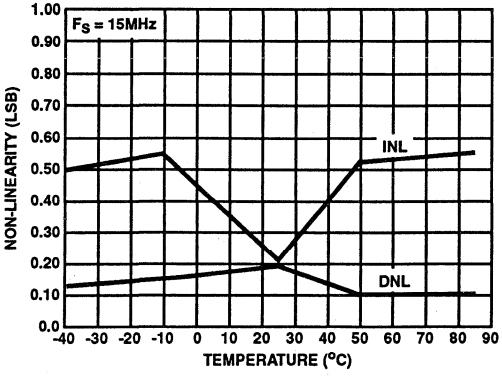


FIGURE 15. NON-LINEARITY vs TEMPERATURE

Typical Performance Curves (Continued)

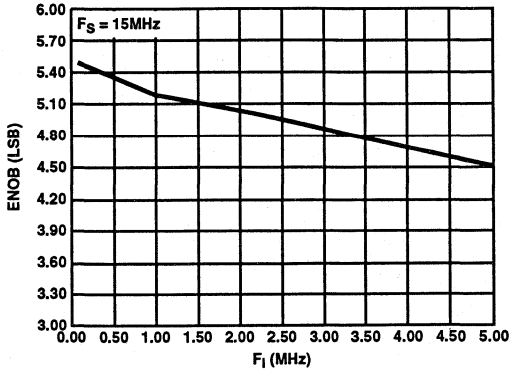


FIGURE 18. ENOB vs INPUT FREQUENCY

Pin Descriptions

PIN NUMBER		NAME	DESCRIPTION
DIP	SOIC		
1	1	B6	Bit 6, Output (MSB).
2	2	OF	Overflow, Output.
3	3, 4	V_{SS}	Digital Ground.
4	5	VZ	Zener Reference Output.
5	6	CE2	Tri-State Output Enable Input, Active Low. See Table 1.
6	7	$\overline{CE1}$	Tri-State Output Enable Input, Active High. See Table 1.
7	8	CLK	Clock Input.
8	9	Phase	Sample clock phase control input. When PHASE is low, "Sample Unknown" occurs when the clock is low and "Auto Balance" occurs when the clock is high (see text).
9	10	$V_{REF}+$	Reference Voltage Positive Input.
10	11	$V_{REF}-$	Reference Voltage Negative Input.
11	12	V_{IN}	Analog Signal Input.
12	13, 14	V_{DD}	Power Supply, +5V.
13	15	B1	Bit 1, Output (LSB).
14	16	B2	Bit 2, Output.
15	17	B3	Bit 3, Output.
16	18	REF(CTR)	Reference Ladder Midpoint.
17	19	B4	Bit 4, Output.
18	20	B5	Bit 5, Output.

TABLE 1. CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	B1 - B6	OF
0	1	Valid	Valid
1	1	Tri-State	Valid
X	0	Tri-State	Tri-State

X = Don't care

TABLE 2. OUTPUT CODE TABLE

CODE DESCRIPTION	(NOTE 1) INPUT VOLTAGE				BINARY OUTPUT CODE (LSB)							DECIMAL COUNT
	V_{REF} 6.40 (V)	V_{REF} 5.12 (V)	V_{REF} 4.80 (V)	V_{REF} 3.20 (V)	OF	B6	B5	B4	B3	B2	B1	
Zero	0.00	0.00	0.00	0.00	0	0	0	0	0	0	0	0
1 LSB	0.10	0.08	0.075	0.05	0	0	0	0	0	0	1	1
2 LSB	0.20	0.16	0.15	0.10	0	0	0	0	0	1	0	2
•			•					•				•
•			•					•				•
•			•					•				•
•			•					•				•
$^1/_2$ Full Scale - 1 LSB	3.10	2.48	2.325	1.55	0	0	1	1	1	1	1	31
$^1/_2$ Full Scale	3.20	2.56	2.40	1.60	0	1	0	0	0	0	0	32
$^1/_2$ Full Scale + 1 LSB	3.30	2.64	2.475	1.65	0	1	0	0	0	0	1	33
•			•					•				•
•			•					•				•
•			•					•				•
•			•					•				•
Full Scale - 1 LSB	6.20	4.96	4.65	3.10	0	1	1	1	1	1	0	62
Full Scale	6.30	5.04	4.725	3.15	0	1	1	1	1	1	1	63
Overflow	6.40	5.12	4.80	3.20	1	1	1	1	1	1	1	127

NOTE:

1. The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Device Operation

A sequential parallel technique is used by the CA3306 converter to obtain its high speed operation. The sequence consists of the "Auto Balance" phase $\phi 1$ and the "Sample Unknown" phase $\phi 2$. (Refer to the circuit diagram.) Each conversion takes one clock cycle.* With the phase control low, the "Auto Balance" ($\phi 1$) occurs during the High period of the clock cycle, and the "Sample Unknown" ($\phi 2$) occurs during the low period of the clock cycle.

During the "Auto Balance" phase, a transmission-gate switch is used to connect each of 64 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{TAP}(N) = [(V_{REF}/64) \times N] - [V_{REF}/(2 \times 64)]$$
$$= V_{REF}[(2N - 1)/126]$$

Where: $V_{TAP}(N)$ = reference ladder tap voltage at point N
V_{REF} = voltage across V_{REF}- to V_{REF}+
N = tap number (I through 64)

* This device requires only a single-phase clock The terminology of $\phi 1$ and $\phi 2$ refers to the High and Low periods of the same clock.

The other side of the capacitor is connected to a single-stage inverting amplifier whose output is shorted to its input by a switch. This biases the amplifier at its intrinsic trip point, which is approximately, $(V_{DD} - V_{SS})/2$. The capacitors now charge to their associated tap voltages, priming the circuit for the next phase.

In the "Sample Unknown" phase, all ladder tap switches are opened, the comparator amplifiers are no longer shorted, and V_{IN} is switched to all 64 capacitors. Since the other end of the capacitor is now looking into an effectively open circuit, any voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators whose tap voltages were lower than V_{IN} will drive the comparator outputs to a "low" state. All comparators whose tap voltages were higher than V_{IN} will drive the comparator outputs to a "high" state. A second, capacitor-coupled, auto-zeroed amplifier further amplifies the outputs.

The status of all these comparator amplifiers are stored at the end of this phase ($\phi 2$), by a secondary latching amplifier stage. Once latched, the status of the 64 comparators is decoded by a 64-bit 7-bit decode array and the results are clocked into a storage register at the rising edge of the next $\phi 2$.

A tri-state buffer is used at the output of the 7 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable 81 through 86 when it is in a high state. CE2 will independently disable B1 through B6 and the OF buffers when it is in the low state (Table 1).

To facilitate usage of this device a phase-control input is provided which can effectively complement the clock as it enters the chip. Also, an on-board zener is provided for use as a reference voltage.

Continuous Clock Operation

One complete conversion cycle can be traced through the CA3306 via the following steps. (Refer to timing diagram, Figure 1.) With the phase control in a "High" state, the rising edge of the clock input will start a "sample" phase. During this entire "High" state of the clock, the 64 comparators will track the input voltage and the 64 latches will track the comparator outputs. At the falling edge of the clock, after the specified aperture delay, all 64 comparator outputs are captured by the 64 latches. This ends the "sample" phase and starts the "auto balance" phase for the comparators. During this "Low" state of the clock the output of the latches propagates through the decode array and a 7-bit code appears at the D inputs of the output registers. On the next rising edge of the clock, this 7-bit code is shifted into the output registers and appears with time delay to as valid data at the output of the tri-state drivers. This also marks the start of a new "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse Mode Operation

For sampling high speed nonrecurrent or transient data, the converter may be operated in a pulse mode in one of three ways. The fastest method is to keep the converter in the Sample Unknown phase, $\phi 2$, during the standby state. The device can now be pulsed through the Auto Balance phase with a single pulse. The analog value is captured on the leading edge of $\phi 1$ and is transferred into the output registers on the trailing edge of $\phi 1$. We are now back in the standby state, $\phi 2$, and another conversion can be started, but not later than 5µs due to the eventual droop of the commutating capacitors. Another advantage of this method is that it has the potential of having the lowest power drain. The larger the time ratio between $\phi 2$ and $\phi 1$, the lower the power consumption. (See Timing Waveform, Figure 3.)

The second method uses the Auto Balance phase, $\phi 1$, as the standby state. In this state the converter can stay indefinitely waiting to start a conversion. A conversion is performed by strobing the clock input with two $\phi 2$ pulses. The first pulse starts a Sample Unknown phase and captures the analog value in the comparator latches on the trailing edge. A second $\phi 2$ pulse is needed to transfer the data into the output registers. This occurs on the leading edge of the second pulse. The conversion now takes slightly longer, but the repetition rate may be as slow as desired. The disadvantage to this method is the higher device dissipation due to the low ratio of $\phi 2$ to $\phi 1$. (See Timing Waveform, Figure 3B.)

For applications requiring both indefinite standby and lowest power, standby can be in the $\phi 2$ (Sample Unknown) state with two $\phi 1$ pulses to generate valid data (see Figure 3C). Valid data now appears two full clock cycles after starting the conversion process.

Analog Input Considerations

The CA3306 input terminal is characterized by a small capacitance (see Specifications) and a small voltage-dependent current (See Typical Performance Curves). The signal-source impedance should be kept low, however, when operating the CA3306 at high clock rates.

The CA3306 outputs a short (less than 10ns) current spike of up to several mA amplitude (See Typical Performance Curves) at the beginning of the sample phase. (To a lesser extent, a spike also appears at the beginning of auto balance.) The driving source must recover from the spike by the end of the same phase, or a loss of accuracy will result.

A locally terminated 50Ω or 75Ω source is generally sufficient to drive the CA3306. If gain is required, a high speed, fast settling operational amplifier, such as the HA-5033, HA-2542, or HA5020 is recommended.

Digital Input And Output Interfacing

The two chip-enable and the phase-control inputs are standard CMOS units. They should be driven from less than 0.3 x V_{DD} to at least 0.7 x V_{DD}. This can be done from 74HC series CMOS (QMOS), TTL with pull-up resistors, or, if V_{DD} is greater than the logic supply, open collector or open drain drivers plus pull-ups. (See Figure 20.)

The clock input is more critical to timing variations, such as $\phi 1$ becoming too short, for instance. Pull-up resistors should generally be avoided in favor of active drivers. The clock input may be capacitively coupled, as it has an internal 50kΩ feedback resistor on the first buffer stage, and will seek its own trip point. A clock source of at least $1V_{P-P}$ is adequate, but extremely non-symmetrical waveforms should be avoided.

The output drivers have full rail-to-rail capability. If driving CMOS systems with V_{DD} below the V_{DD} of the CA3306, a CD74HC4050 or CD74HC4049 should be used to step down the voltage. If driving LSTTL systems, no step-down should be necessary, as most LSTTLs will take input swings up to 10V to 15V.

Although the output drivers are capable of handling typical data bus loading, the capacitor charging currents will produce local ground disturbances. For this reason, an external bus driver is recommended.

Increased Accuracy

In most cases the accuracy of the CA3306 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, three adjustments can be made to obtain better accuracy; i.e., offset trim, gain trim, and midpoint trim.

Offset Trim

In general offset correction can be done in the preamp circuitry by introducing a DC shift to V_{IN} or by the offset trim of the operational amplifier. When this is not possible the V_{REF}- input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is 1/2 LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = {}^1/_2 \text{ LSB} = {}^1/_2(V_{REF}/64)$$
$$= V_{REF}/128$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50Ω pot connected between V_{REF}- and ground will accomplish the adjustment. Set V_{IN} to $^1/_2$ LSB and trim the pot until the 0 to 1 transition occurs.

If V_{IN} for the first transition is greater than the theoretical, then the 50Ω pot should be connected between V_{REF} and a negative voltage of about 2 LSBs. The trim procedure is as stated previously.

Gain Trim

In general the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the operational amplifier. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 63 to overflow transition. That voltage is $^1/_2$ LSB less than V_{REF}+ and is calculated as follows:

$$V_{IN} \text{ (63 to 64 transition)} = V_{REF} - V_{REF}/128$$
$$= V_{REF}(127/128)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overtlow transition. Now adjust V_{REF}+ until that transition occurs on the outputs.

Midpoint Trim

The reference center (RC) is available to the user as the midpoint of the resistor ladder. To trim the midpoint, the offset and gain trims should be done first. The theoretical transition from count 31 to 32 occurs at 31 $^1/_2$ LSBs. That voltage is as follows:

$$V_{IN} \text{ (31 to 32 transition)} = 31.5\ (V_{REF}/64)$$
$$= V_{REF}(63/128)$$

An adjustable voltage follower can be connected to the RC pin or a 2k pot can be connected between V_{REF}+ and V_{REF}- with the wiper connected to RC. Set V_{IN} to the 31 to 32 transition voltage, then adjust the voltage follower or the pot until the transition occurs on the output bits.

The Reference Center point can also be used to create unique transfer functions. The user must remember, however, that there is approximately 120Ω in series with the RC pin.

Applications

7-Bit Resolution

To obtain 7-bit resolution, two CA3306s can be wired together. Necessary ingredients include an open-ended ladder network, an overtlow indicator, tri-state outputs, and chip-enabler controls - all of which are available on the CA3306.

The first step for connecting a 7-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 17. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overflow output of the lower device now becomes the seventh bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overflow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The tri-state outputs of the two devices (bits 1 through 6) are now connected in parallel to complete the circuitry.

Doubled Sampling Speed

The phase control and both positive and negative true chip enables allow the parallel connection of two CA3306s to double the sampling speed. Figure 18 shows this configuration. One converter samples on the positive phase of the clock, and the second on the negative. The outputs are also alternately enabled. Care should be taken to provide a near square-wave clock it operating at close to the maximum clock speed for the devices.

8-Bit to 12-Bit Conversion Techniques

To obtain 8-bit to 12-bit resolution and accuracy, use a feed-forward conversion technique. Two A/D converters will be needed to convert up to 11 bits; three A/D converters to convert 12 bits. The high speed of the CA3306 allows 12-bit conversions in the 500ns to 900ns range.

The circuit diagram of a high-speed 12-bit A/D converter is shown in Figure 19. In the feed-forward conversion method two sequential conversions are made. Converter A first does a coarse conversion to 6 bits. The output is applied to a 6-bit D/A converter whose accuracy level is good to 12 bits. The D/A converter output is then subtracted from the input voltage, multiplied by 32, and then converted by a second flash A/D converter, which is connected in a 7-bit configuration. The answers from the first and second conversions are added together with bit 1 of the first conversion overlapping bit 7 of the second conversion.

When using this method, take care that:

- The linearity of the first converter is better than $^1/_2$ LSB.
- An offset bias of 1 LSB (1/64) Is subtracted from the first conversion since the second converter is unipolar.
- The D/A converter and its reference are accurate to the total number of bits desired for the final conversion (the A/D converter need only be accurate to 6 bits).

The first converter can be offset-biased by adding a 20Ω resistor at the bottom of the ladder and increasing the reference voltage by 1 LSB. If a 6.4V reference is used in the system, for example, then the first CA3306 will require a 6.5V reference.

Definitions

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the converter. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from fullscale for all these tests.

Signal-to-Noise (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR})/6.02$$

where: $V_{CORR} = 0.5dB$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

Operating and Handling Considerations

1. Handling

All inputs and outputs of Harris CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in AN6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause V_{DD} - V_{SS} to exceed the absolute maximum rating.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 20mA even when the power supply is off. The zener (pin 4) is the only terminal allowed to exceed V_{DD}.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{DD} or V_{SS}, whichever is appropriate.

Output Short Circuits

Shorting of outputs to V_{DD} or V_{SS} may damage CMOS devices by exceeding the maximum device dissipation.

Application Circuits

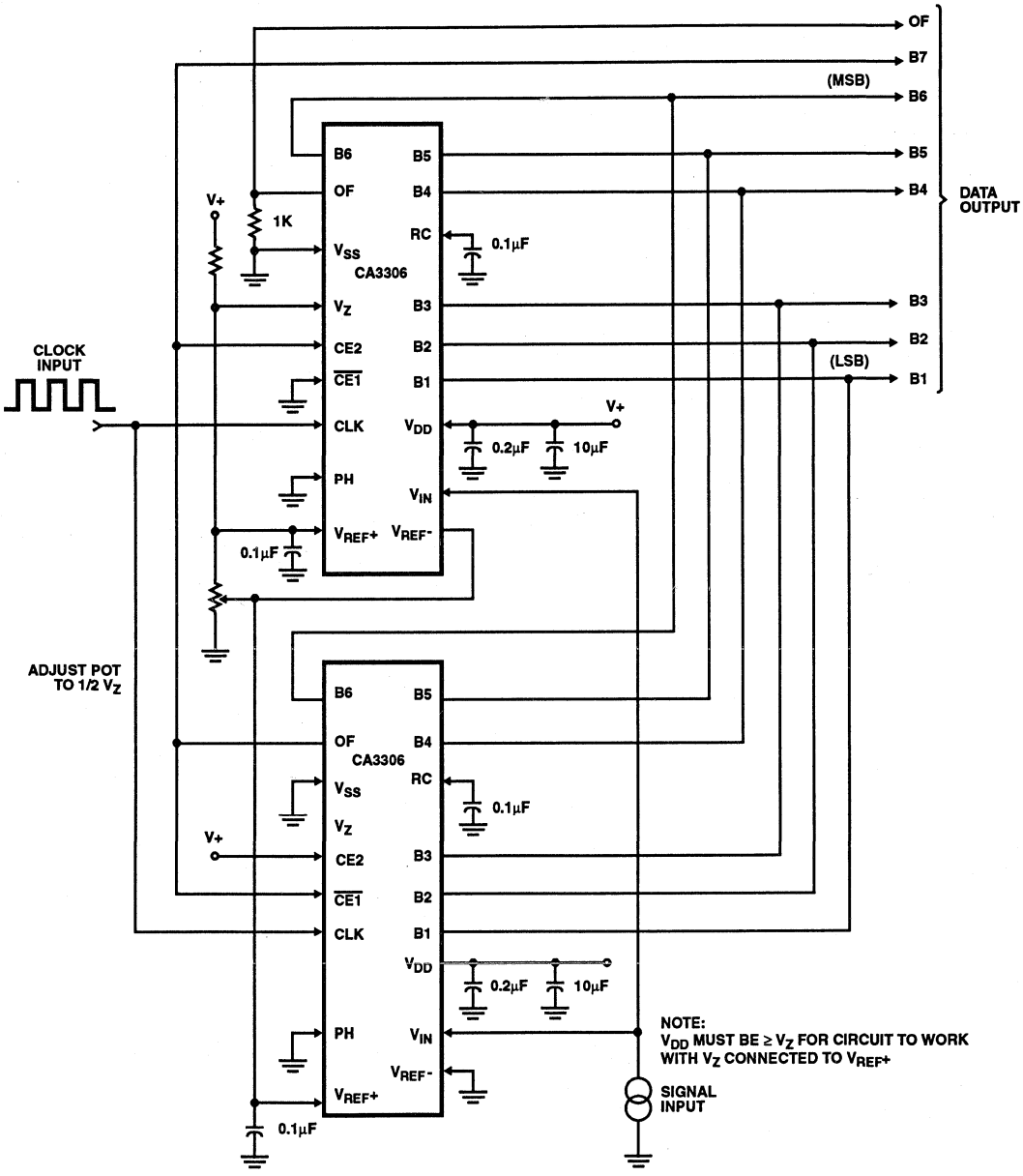


FIGURE 17. TYPICAL CA3306 7-BIT RESOLUTION CONFIGURATION

Application Circuits (Continued)

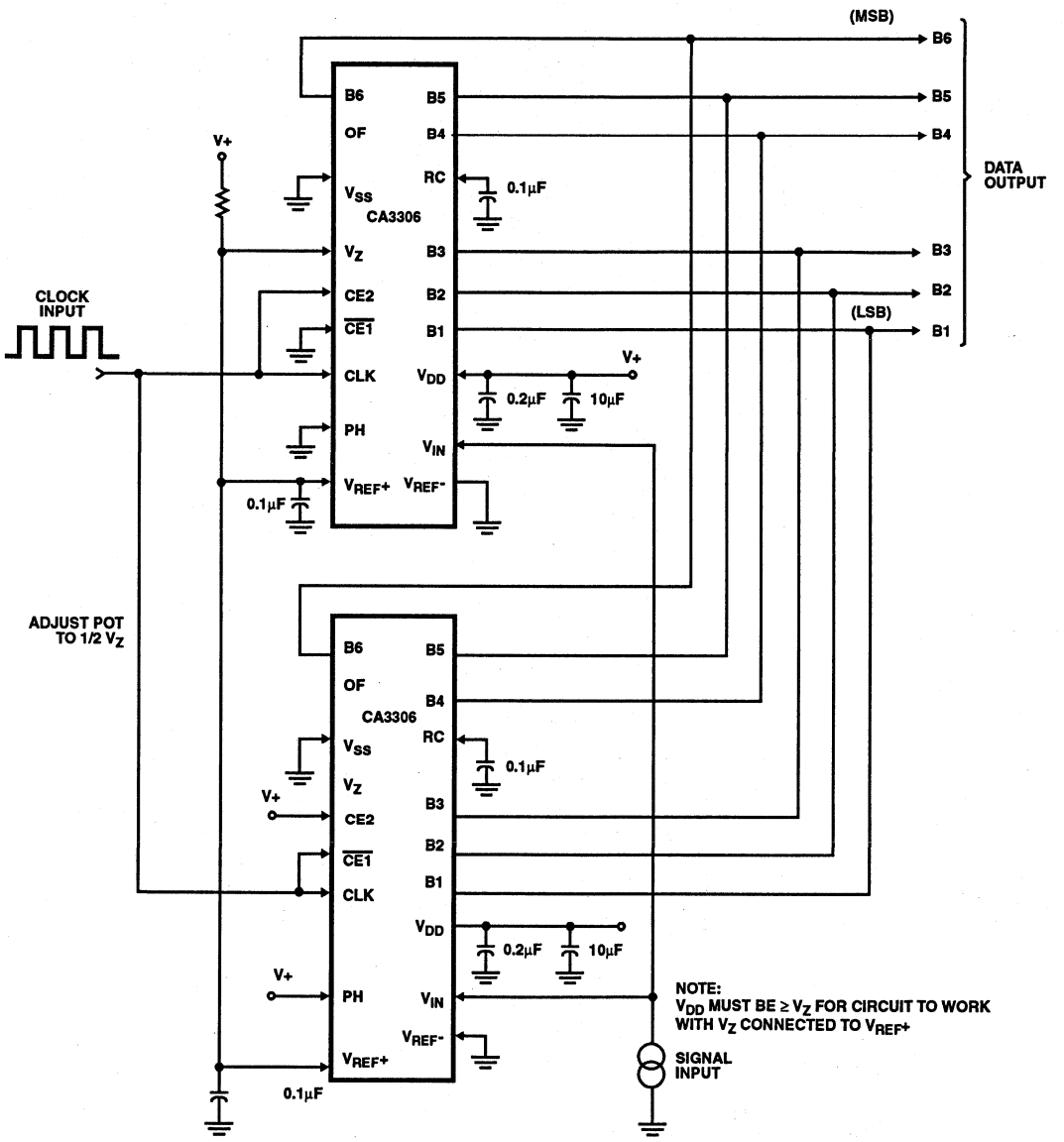


FIGURE 18. TYPICAL CA3306 6-BIT RESOLUTION CONFIGURATION WITH DOUBLE SAMPLING RATE CAPABILITY

Application Circuits (Continued)

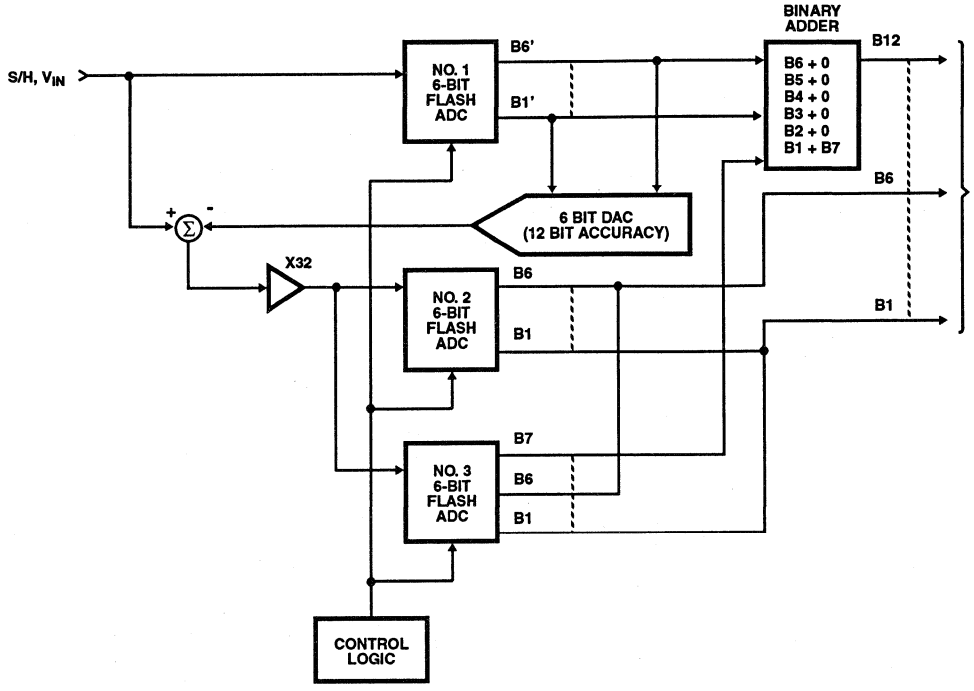


FIGURE 19. TYPICAL CA3306, 800ns, 12-BIT ADC SYSTEM

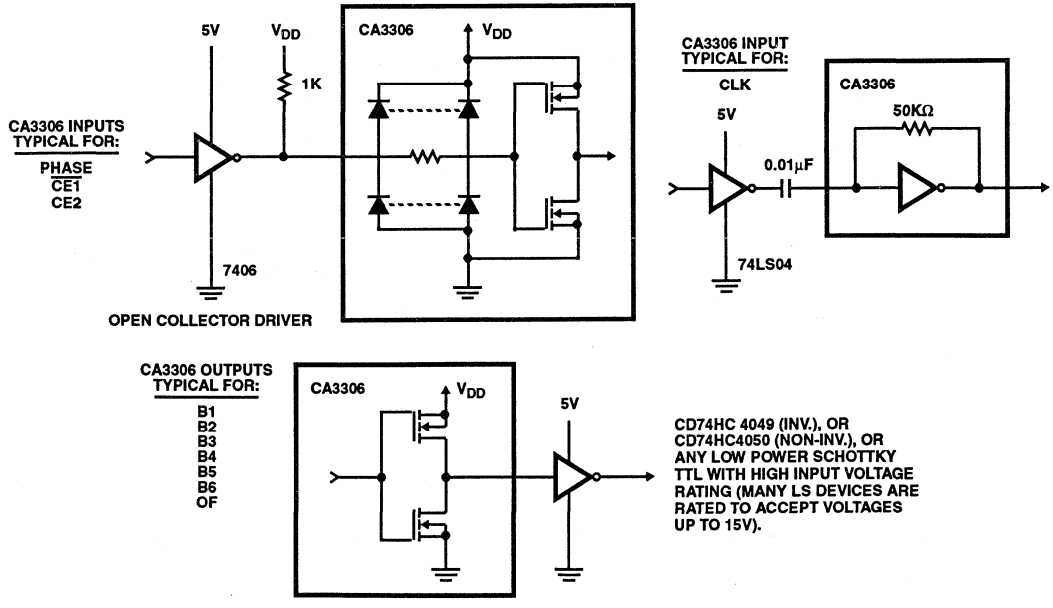


FIGURE 20. 5V LOGIC INTERFACE CIRCUIT FOR V_{DD} > 5.5V

HARRIS SEMICONDUCTOR

CA3318C

CMOS Video Speed 8-Bit Flash A/D Converter

December 1993

Features

- CMOS Low Power with SOS Speed (150mW Typ.)
- Parallel Conversion Technique
- 15MHz Sampling Rate (67ns Conversion Time)
- 8-Bit Latched Tri-State Output with Overflow Bit
- ±1 LSB Accuracy (Typ.)
- Single Supply Voltage (4V to 7.5V)
- 2 Units in Series Allow 9-Bit Output
- 2 Units in Parallel Allow 30MHz Sampling Rate

Applications

- TV Video Digitizing (Industrial/Security/Broadcast)
- High-Speed A/D Conversion
- Ultrasound Signature Analysis
- Transient Signal Analysis
- High Energy Physics Research
- High Speed Oscilloscope Storage/Display
- General Purpose Hybrid ADCs
- Optical Character Recognition
- Radar Pulse Analysis
- Motion Signature Analysis
- µP Data Acquisition Systems

Description

The CA3318C is a CMOS parallel (FLASH) analog-to-digital converter designed for applications demanding both low power consumption and high speed digitization.

The CA3318 operates over a wide full scale input voltage range of 4V up to 7.5V with maximum power consumption depending upon the clock frequency selected. When operated from a 5V supply at a clock frequency of 15MHz, the typical power consumption of the CA3318 is 150mW.

The intrinsic high conversion rate makes the CA3318 ideally suited for digitizing high speed signals. The overflow bit makes possible the connection of two or more CA3318s in series to increase the resolution of the conversion system. A series connection of two CA3318s may be used to produce a 9-bit high speed converter. Operation of two CA3318s in parallel doubles the conversion speed (i.e., increases the sampling rate from 15MHz to 30MHz).

256 paralleled auto balanced voltage comparators measure the input voltage with respect to a known reference to produce the parallel bit outputs in the CA3318.

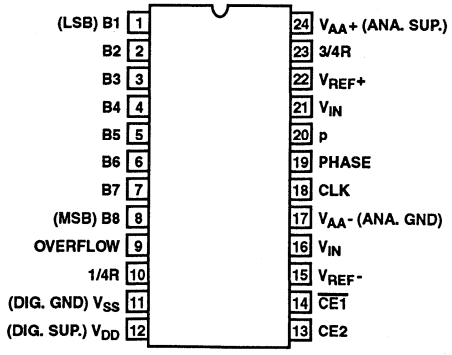
255 comparators are required to quantize all input voltage levels in this 8-bit converter, and the additional comparator is required for the overflow bit.

Ordering Information

PART NUMBER	LINEARITY (INL)	SAMPLING RATE	TEMPERATURE RANGE	PACKAGE
CA3318CE	±1.5 LSB	15MHz (67ns)	-40°C to +85°C	24 Lead Plastic DIP
CA3318CM	±1.5 LSB	15MHz (67ns)	-40°C to +85°C	24 Lead Plastic SOIC
CA3318CD	±1.5 LSB	15MHz (67ns)	-40°C to +85°C	24 Lead Ceramic DIP

Pinout

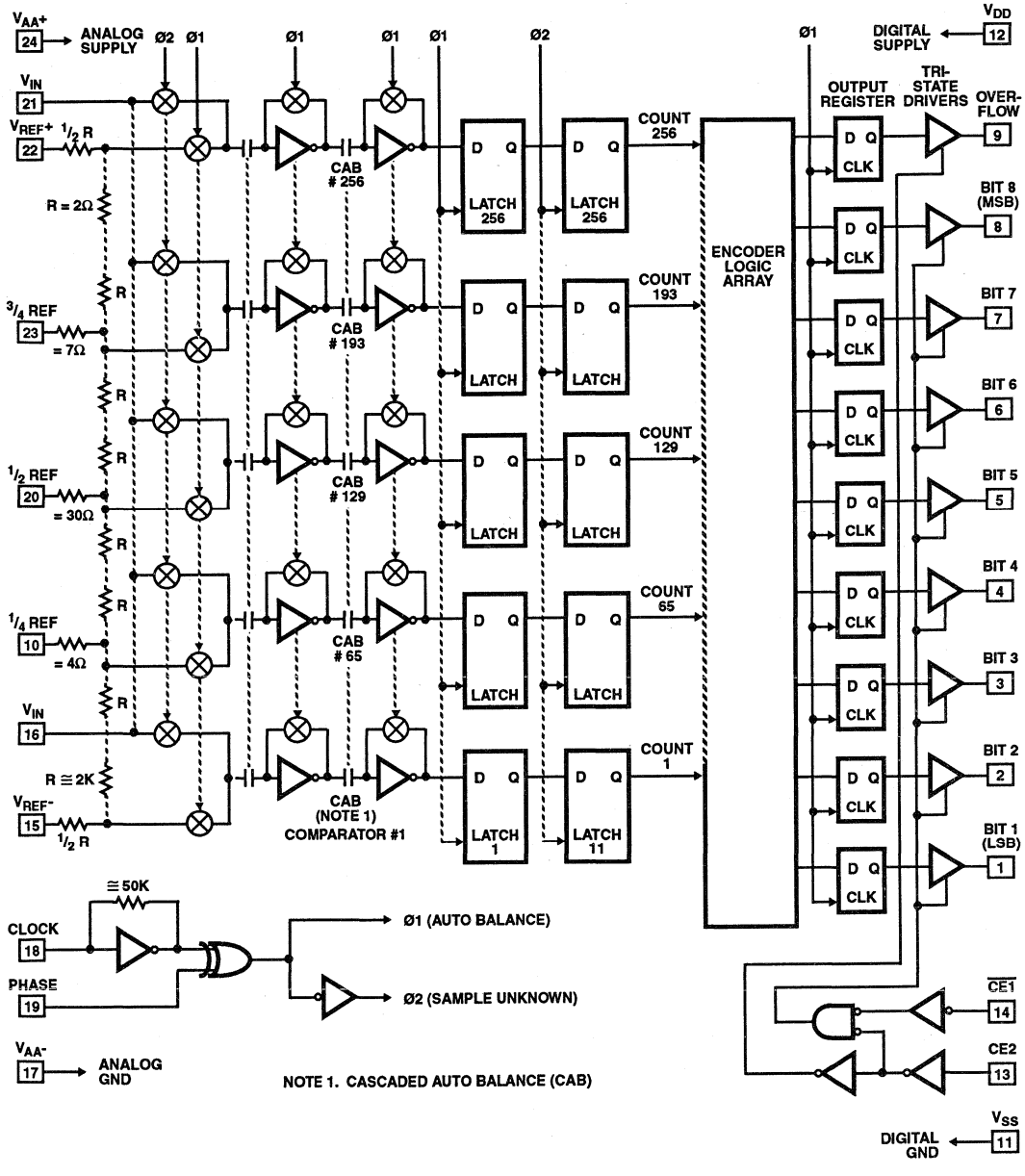
CA3318C (PDIP, CDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3103

Functional Block Diagram



NOTE 1. CASCADED AUTO BALANCE (CAB)

Absolute Maximum Ratings

DC Supply Voltage Range (V_{DD} or V_{AA}+) ..... -0.5V to +8V
(Referenced to V_{SS} or V_{AA}- Terminal, Whichever is More Negative)
Input Voltage Range
CE2 and $\overline{CE1}$ ..... V_{AA}- -0.5V to V_{DD} + 0.5V
Clock, Phase, V_{REF}-, $^1/_2$ Ref..... V_{AA}- -0.5V to V_{AA}+ + 0.5V
Clock, Phase, V_{REF}-, $^1/_4$ Ref..... V_{SS}- -0.5V to V_{DD} + 0.5V
V_{IN}, 3/4 REF, V_{REF}+ ..... V_{AA}- -0.5V to V_{AA}- + 7.5V
Output Voltage Range,..... V_{SS} - 0.5V to V_{DD} + 0.5V
Bits 1-8, Overflow (Outputs Off)
DC Input Current .....±20mA
Clock, Phase, $\overline{CE1}$, CE2, V_{IN}, Bits 1-8, Overflow
Operating Voltage Range (V_{DD} or V_{AA}+) .....4V Min to 7.5V Max
Recommended V_{AA}+ Operating Range ..... V_{DD} ± 1V
Recommended V_{AA}- Operating Range ..... V_{SS} ± 1V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s)..... +265°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	58°C/W	11°C/W
Plastic DIP Package	60°C/W	-
Plastic SOIC Package	75°C/W	-

Maximum Power Dissipation.....0.67W
Operating Temperature Range (T_A) .....-40°C to +85°C
Junction Temperature
Ceramic Package .....+175°C
Plastic Package.....+150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

At +25°C, V_{AA}+ = V_{DD} = 5V, V_{REF}+ = 6.4V, V_{REF}- = V_{AA}- = V_{SS}, CLK = 15MHz, All Reference Points Adjusted, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		8	-	-	Bits
Integral Linearity Error		-	-	± 1.5	LSB
Differential Linearity Error		-	-	+1, -0.8	LSB
Offset Error, Unadjusted	V_{IN} = V_{REF}- + 1/2 LSB	-0.5	4.5	6.4	LSB
Gain Error Unadjusted	V_{IN} = V_{REF}+ - 1/2 LSB	-1.5	0	1.5	LSB
DYNAMIC CHARACTERISTICS					
Maximum Input Bandwidth	(Note 1) CA3318C	2.5	5.0	-	MHz
Maximum Conversion Speed	CLK = Square Wave	15	17	-	MSPS
Signal to Noise Ratio (SNR) $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	F_S = 15MHz, f_{IN} = 100kHz	-	47	-	dB
	F_S = 15MHz, f_{IN} = 4MHz	-	43	-	dB
Signal to Noise Ratio (SINAD) $= \frac{\text{RMS Signal}}{\text{RMS Noise+Distortion}}$	F_S = 15MHz, f_{IN} = 100kHz	-	45	-	dB
	F_S = 15MHz, f_{IN} = 4MHz	-	35	-	dB
Total Harmonic Distortion, THD	F_S = 15MHz, f_{IN} = 100kHz	-	-46	-	dBc
	F_S = 15MHz, f_{IN} = 4MHz	-	-36	-	dBc
Effective Number of Bits (ENOB)	F_S = 15MHz, f_{IN} = 100kHz	-	7.2	-	Bits
	F_S = 15MHz, f_{IN} = 4MHz	-	5.5	-	Bits
Differential Gain Error	Unadjusted	-	2	-	%
Differential Phase Error	Unadjusted	-	1	-	%
ANALOG INPUTS					
Full Scale Range, V_{IN} and (V_{REF}+) - (V_{REF}-)	Notes 2, 4	4	-	7	V
Input Capacitance, V_{IN}		-	30	-	pF
Input Current, V_{IN}, (See Text)	V_{IN} = 5.0V, V_{REF}+ = 5.0V	-	-	3.5	mA
REFERENCE INPUTS					
Ladder Impedance		270	500	800	Ω

Electrical Specifications At +25°C, $V_{AA}+ = V_{DD} = 5V$, $V_{REF}+ = 6.4V$, $V_{REF}- = V_{AA}- = V_{SS}$, CLK = 15MHz, All Reference Points Adjusted, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS					
Low Level Input Voltage, V_{OL}					
$\overline{CE1}$, CE2	Note 4	-	-	$0.2V_{DD}$	V
Phase, CLK	Note 4	-	-	$0.2V_{AA}$	V
High Level Input Voltage, V_{IN}					
$\overline{CE1}$, CE2	Note 4	$0.7V_{DD}$	-	-	V
Phase, CLK	Note 4	$0.7V_{AA}$	-	-	V
Input Leakage Current, I_I (Except CLK Input	Note 3	-	±0.2	±5	µA
Input Capacitance, C_I		-	3	-	pF
DIGITAL OUTPUTS					
Output Low (Sink) Current	$V_O = 0.4V$	4	10	-	mA
Output High (Source) Current	$V_O = 4.5V$	-4	-6	-	mA
Tri-State Output Off-State Leakage Current, I_{OZ}		-	±0.2	±5	µA
Output Capacitance, C_O		-	4	-	pF
TIMING CHARACTERISTICS					
Auto Balance Time (φ1)		33	-	∞	ns
Sample Time (φ2)	Note 4	25	-	500	ns
Aperture Delay		-	15	-	ns
Aperture Jitter		-	100	-	ps
Data Valid Time, T_D	Note 4	-	50	65	ns
Data Hold Time, T_H	Note 4	25	40	-	ns
Output Enable Time, T_{EN}		-	18	-	ns
Output Disable Time, T_{DIS}		-	18	-	ns
POWER SUPPLY CHARACTERISTICS					
Device Current ($I_{DD} + I_A$) (Excludes I_{REF})	Continuous Conversion (Note 4)	-	30	60	mA
	Auto Balance (φ1)	-	30	60	mA

NOTES:

1. A full scale sine wave input of greater than $F_{CLOCK}/2$ or the specified input bandwidth (whichever is less) may cause an erroneous code. The -3dB bandwidth for frequency response purposes is greater than 30MHz.
2. V_{IN} (Full Scale) or $V_{REF}+$ should not exceed $V_{AA}+ + 1.5V$ for accuracy.
3. The clock input is a CMOS inverter with a 50kΩ feedback resistor and may be AC coupled with $1V_{P-P}$ minimum source.
4. Parameter not tested, but guaranteed by design or characterization.

Timing Waveforms

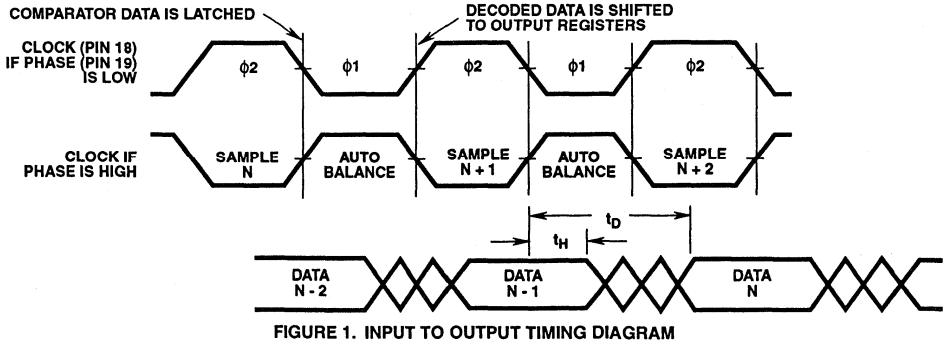


FIGURE 1. INPUT TO OUTPUT TIMING DIAGRAM

Timing Waveforms (Continued)

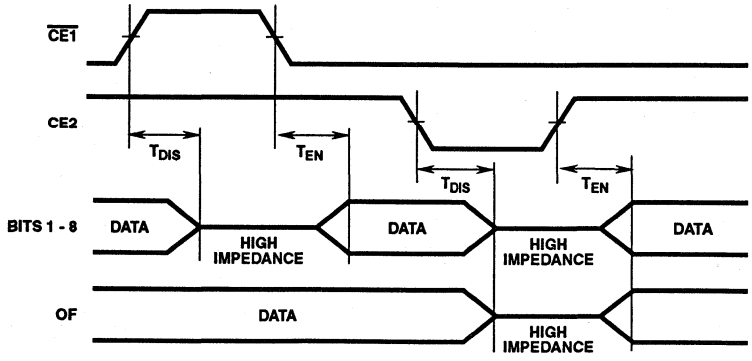


FIGURE 2. OUTPUT ENABLE TIMING DIAGRAM

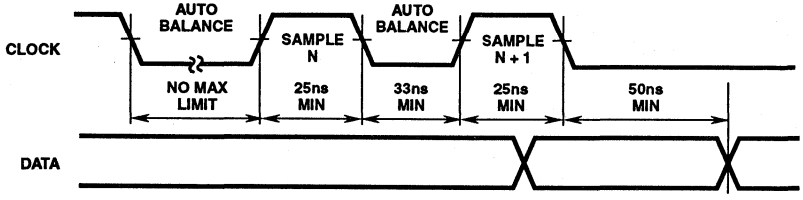


FIGURE 3A. STANDBY IN INDEFINITE AUTO BALANCE (SHOWN WITH PHASE = LOW)

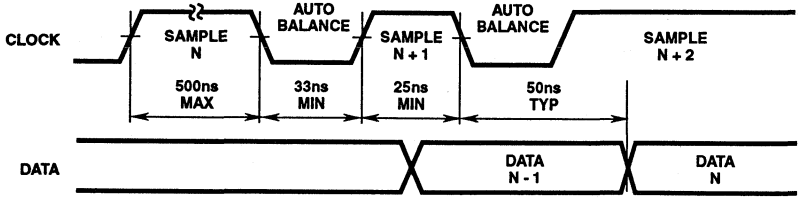


FIGURE 3B. STANDBY IN SAMPLE (SHOWN WITH PHASE = LOW)

FIGURE 3. PULSE MODE OPERATION

Typical Performance Curves

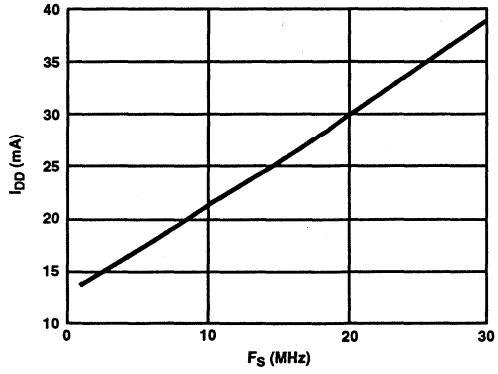


FIGURE 4. DEVICE CURRENT vs SAMPLE FREQUENCY

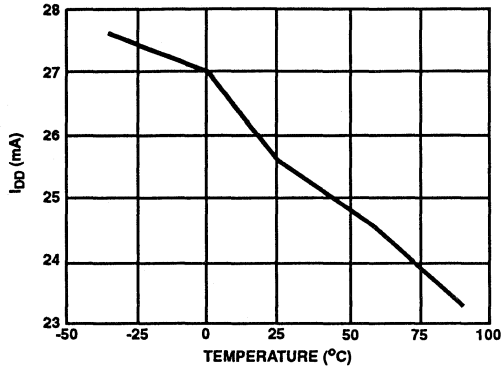


FIGURE 5. DEVICE CURRENT vs TEMPERATURE

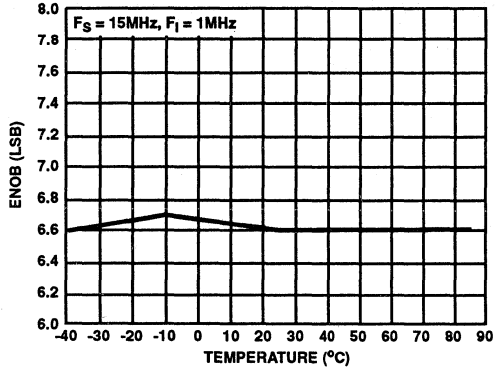


FIGURE 6. ENOB vs TEMPERATURE

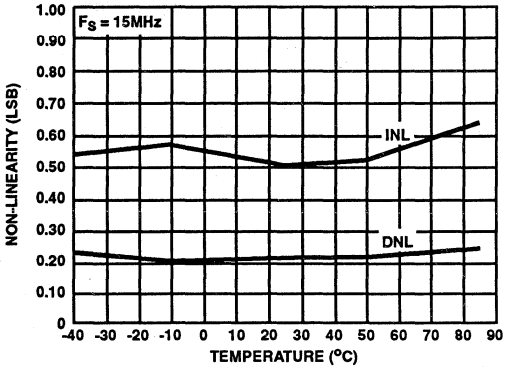


FIGURE 7. NON-LINEARITY vs TEMPERATURE

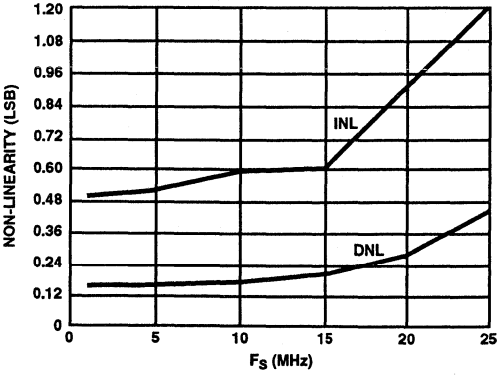


FIGURE 8. NON-LINEARITY vs SAMPLE FREQUENCY

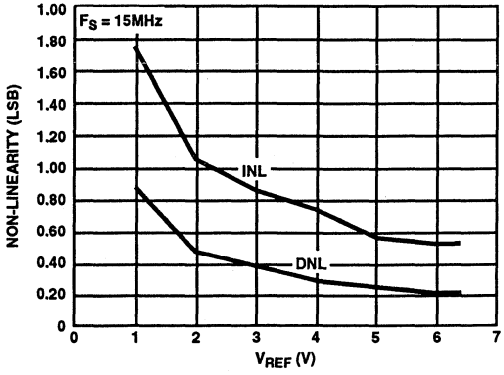


FIGURE 9. NON-LINEARITY vs REFERENCE VOLTAGE

Typical Performance Curves (Continued)

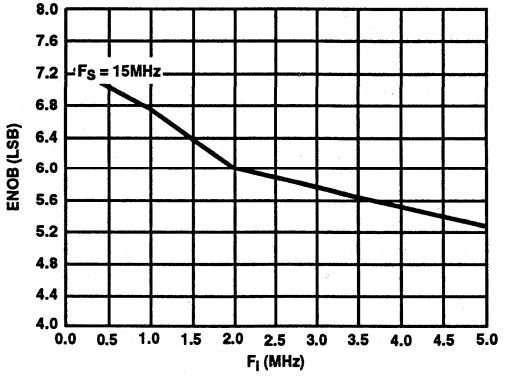


FIGURE 10. ENOB vs INPUT FREQUENCY

Pin Descriptions

PIN	NAME	DESCRIPTION	
1	B1	Bit 1 (LSB)	Output Data Bits (High = True)
2	B2	Bit 2	
3	B3	Bit 3	
4	B4	Bit 4	
5	B5	Bit 5	
6	B6	Bit 6	
7	B7	Bit 7	
8	B8	Bit 8 (MSB)	
9	OF	Overflow	
10	$^1/_4$ R	Reference Ladder $^1/_4$ Point	
11	V_{SS}	Digital Ground	
12	V_{DD}	Digital Power Supply, +5V	
13	CE2	Tri-State Output Enable Input, Active Low, See Truth Table.	
14	$\overline{CE1}$	Tri-State Output Enable Input Active High. See Truth Table.	
15	V_{REF}-	Reference Voltage Negative Input	
16	V_{IN}	Analog Signal Input	
17	V_{AA}-	Analog Ground	
18	CLK	Clock Input	
19	PHASE	Sample clock phase control input. When PHASE is low, "Sample Unknown" occurs when the clock is low and "Auto Balance" occurs when the clock is high (see text).	
20	$^1/_2$ R	Reference Ladder Midpoint	
21	V_{IN}	Analog Signal Input	
22	V_{REF}+	Reference Voltage Positive Input	
23	$^3/_4$ R	Reference Ladder $^3/_4$ Point	
24	V_{AA}+	Analog Power Supply, +5V	

CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	B1 - B8	OF
0	1	Valid	Valid
1	1	Tri-State	Valid
X	0	Tri-State	Tri-State

X = Don't Care

Theory of Operation

A sequential parallel technique is used by the CA3318 converter to obtain its high speed operation. The sequence consists of the "Auto-Balance" phase, ϕ1, and the "Sample Unknown" phase, ϕ2. (Refer to the circuit diagram.) Each conversion takes one clock cycle*. With the phase control (pin 19) high, the "Auto-Balance" (ϕ1) occurs during the high period of the clock cycle, and the "Sample Unknown" (ϕ2) occurs during the low period of the clock cycle.

* The device requires only a single phase clock The terminology of ϕ1 and ϕ2 refers to the high and low periods of the same clock.

During the "Auto-Balance" phase, a transmission switch is used to connect each of the first set of 256 commutating capacitors to their associated ladder reference tap. Those tap voltages will be as follows:

$$V_{TAP}(N) = [(N/256)\,V_{REF}] - (1/512)\,V_{REF}]$$
$$= [(2N - 1)/512]\,V_{REF}$$

Where:

V_{TAP} (n) = reference ladder tap voltage at point n.
V_{REF} = voltage across V_{REF}- to V_{REF}+
N = tap number (1 through 256)

The other side of these capacitors are connected to single-stage amplifiers whose outputs are shorted to their inputs by switches. This balances the amplifiers at their intrinsic trip points, which is approximately (V_{AA}+ - V_{AA}-)/2. The first set of capacitors now charges to their associated tap voltages.

At the same time a second set of commutating capacitors and amplifiers is also auto-balanced. The balancing of the second-stage amplifier at its intrinsic trip point removes any tracking differences between the first and second amplifier stages. The cascaded auto-balance (CAB) technique, used here, increases comparator sensitivity and temperature tracking.

In the "Sample Unknown" phase, all ladder tap switches and comparator shorting switches are opened. At the same time V_{IN} is switched to the first set of commutating capacitors. Since the other end of the capacitors are now looking into an effectively open circuit, any input voltage that differs from the previous tap voltage will appear as a voltage shift at the comparator amplifiers. All comparators that had tap voltages greater than V_{IN} will go to a "high" state at their outputs. All comparators that had tap voltages lower than V_{IN} will go to a "low" state.

The status of all these comparator amplifiers is AC coupled through the second-stage comparator and stored at the end of this phase ($\phi 2$) by a latching amplifier stage. The latch feeds a second latching stage, triggered at the end of $\phi 1$. This delay allows comparators extra settling time. The status of the comparators is decoded by a 256 to 9-bit decoder array, and the results are clocked into a storage register at the end of the next $\phi 2$.

A 3-stage buffer is used at the output of the 9 storage registers which are controlled by two chip-enable signals. $\overline{CE1}$ will independently disable B1 through B6 when it is in a high state. CE2 will independently disable B1 through B8 and the OF buffers when it is in the low state.

To facilitate usage of this device, a phase control input is provided which can effectively complement the clock as it enters the chip.

Continuous-Clock Operation

One complete conversion cycle can be traced through the CA3318 via the following steps. (Refer to timing diagram.) With the phase control in a "low" state, the rising edge of the clock input will start a "sample" phase. During this entire "high" state of the clock, the comparators will track the input voltage and the first-stage latches will track the comparator outputs. At the falling edge of the clock, all 256 comparator outputs are captured by the 256 latches. This ends the "sample" phase and starts the "auto-balance" phase for the comparators. During this "low" state of the clock, the output of the latches settles and is captured by a second row of latches when the clock returns high. The second-stage latch output propagates through the decode array, and a 9-bit code appears at the D inputs of the output registers. On the next falling edge of the clock, this 9-bit code is shifted into the output registers and appears with time delay t_D as valid data at the output of the tri-state drivers. This also marks the end of the next "sample" phase, thereby repeating the conversion process for this next cycle.

Pulse-Mode Operation

The CA3318 needs two of the same polarity clock edges to complete a conversion cycle: If, for instance, a negative going clock edge ends sample "N", then data "N" will appear after the next negative going edge. Because of this requirement, and because there is a maximum sample time of 500ns (due to capacitor droop), most pulse or intermittent sample applications will require double clock pulsing.

If an indefinite standby state is desired, standby should be in auto-balance, and the operation would be as in Figure 3A.

If the standby state is known to last less than 500ns and lowest average power is desired, then operation could be as in Figure 3B.

Increased Accuracy

In most cases the accuracy of the CA3318 should be sufficient without any adjustments. In applications where accuracy is of utmost importance, five adjustments can be made to obtain better accuracy, i.e., offset trim; gain trim; and $^1/_4$, $^1/_2$ and $^3/_4$ point trim.

Offset Trim

In general, offset correction can be done in the preamp circuitry by introducing a dc shift to V_{IN} or by the offset trim of the op amp. When this is not possible the V_{REF}- input can be adjusted to produce an offset trim. The theoretical input voltage to produce the first transition is $^1/_2$ LSB. The equation is as follows:

$$V_{IN} \text{ (0 to 1 transition)} = {}^1/_2 \text{ LSB} = {}^1/_2 (V_{REF}/256)$$
$$= V_{REF}/512$$

If V_{IN} for the first transition is less than the theoretical, then a single-turn 50Ω pot connected between V_{REF}- and ground will accomplish the adjustment. Set V_{IN} to 1/2 LSB and trim the pot until the 0-to-1 transition occurs.

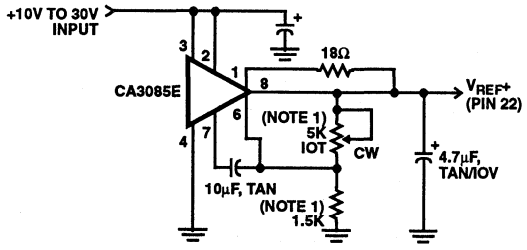
If V_{IN} for the first transition is greater than the theoretical, then the 50Ω pot should be connected between V_{REF}- and a negative voltage of about 2 LSB's. The trim procedure is as stated previously.

Gain Trim

In general, the gain trim can also be done in the preamp circuitry by introducing a gain adjustment for the op amp. When this is not possible, then a gain adjustment circuit should be made to adjust the reference voltage. To perform this trim, V_{IN} should be set to the 255 to overflow transition. That voltage is $^1/_3$ LSB less than V_{REF}+ and is calculated as follows:

$$V_{IN} \text{ (255 to 256 transition)} = V_{REF} - V_{REF}/512$$
$$= V_{REF}(511/512)$$

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 255 to overflow transition. Now adjust V_{REF}+ until that transition occurs on the outputs.

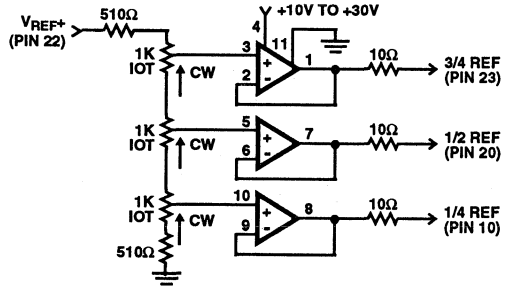


NOTE: Bypass $V_{REF}+$ to analog GND near A/D with 0.1µF ceramic cap. Parts noted should have low temperature drift.

FIGURE 11. TYPICAL VOLTAGE REFERENCE SOURCE FOR DRIVING $V_{REF}+$ INPUT

$^1/_4$ Point Trims

The $^1/_4$, $^1/_2$ and $^3/_4$ points on the reference ladder are brought out for linearity adjusting or if the user wishes to create a nonlinear transfer function. The $^1/_4$ points can be driven by the reference drivers shown (Figure 12) or by 2-K pots connected between $V_{REF}+$ and $V_{REF}-$. The $^1/_2$ (mid-) point should be set first by applying an input of 257/512 x (V_{REF}) and adjusting for an output changing from 128 to 129. Similarly the $^1/_4$ and $^3/_4$ points can be set with inputs of 129/512 and 385/512 x (V_{REF}) and adjusting for counts of 192 to 193 and 64 to 65. (Note that the points are actually $^1/_4$, $^1/_2$ and $^3/_4$ of full scale +1 LSB.)



NOTES:

1. All Op Amps = $^3/_4$ CA324E
2. Bypass all reference points to analog ground near A/D with 0.1µF ceramic caps.
3. Adjust V_{REF+} first, then $^1/_3$, $^3/_4$ and $^1/_4$ points.

FIGURE 12. TYPICAL 1/4 POINT DRIVERS FOR ADJUSTING LINEARITY (USE FOR MAXIMUM LINEARITY)

9-Bit Resolution

To obtain 9-bit resolution, two CA3318's can be wired together. Necessary ingredients include an open-ended ladder network, an overflow indicator, tri-state outputs, and chip-enable controls—all of which are available on the CA3318.

The first step for connecting a 9-bit circuit is to totem-pole the ladder networks, as illustrated in Figure 13. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The overtlow output of the lower device now becomes the ninth bit. When it goes high, all counts must come from the upper device. When it goes low, all counts must come from the lower device. This is done simply by connecting the lower overtlow signal to the $\overline{CE1}$ control of the lower A/D converter and the CE2 control of the upper A/D converter. The tri-state outputs of the two devices (bits 1 through 8) are now connected in parallel to complete the circuitry. The complete circuit for a 9-bit A/D converter is shown in Figure 14.

Grounding/Bypassing

The analog and digital supply grounds of a system should be kept separate and only connected at the A/D. This keeps digital ground noise out of the analog data to be converted. Reference drivers, input amps, reference taps, and the V_{AA} supply should be bypassed at the A/D to the analog side of the ground. See Figure 15 for a block diagram of this concept. All capacitors shown should be low impedance 0.1µF ceramics and should be mounted as close to the A/D as possible. If $V_{AA}+$ is derived from V_{DD}, a small (10Ω resistor or inductor and additional filtering (4.7µF tantalum) may be used to keep digital noise out of the analog system.

Input Loading

The CA3318 outputs a current pulse to the V_{IN} terminal at the start of every sample period. This is due to capacitor charging and switch feedthrough and varies with input voltage and sampling rate. The signal source must be capable of recovering from the pulse before the end of the sample period to guarantee a valid signal for the A/D to convert. Suitable high speed amplifiers include the HA-5033, HA-2542; and CA3450. Figure 16 is an example of an amplifier which recovers fast enough for sampling at 15MHz.

Output Loading

The CMOS digital output stage, although capable of driving large loads, will reflect these loads into the local ground. It is recommended that a local QMOS buffer such as CD74HC541 E be used to isolate capacitive loads.

Definitions

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the converter. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from fullscale for all these tests.

Signal-to-Noise (SNR)

SNR is the measured RMS signal to RMS noise at a specified input and sampling frequency. The noise is the RMS sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR})/6.02$$

where: $V_{CORR} = 0.5dB$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the RMS value of the measured input signal.

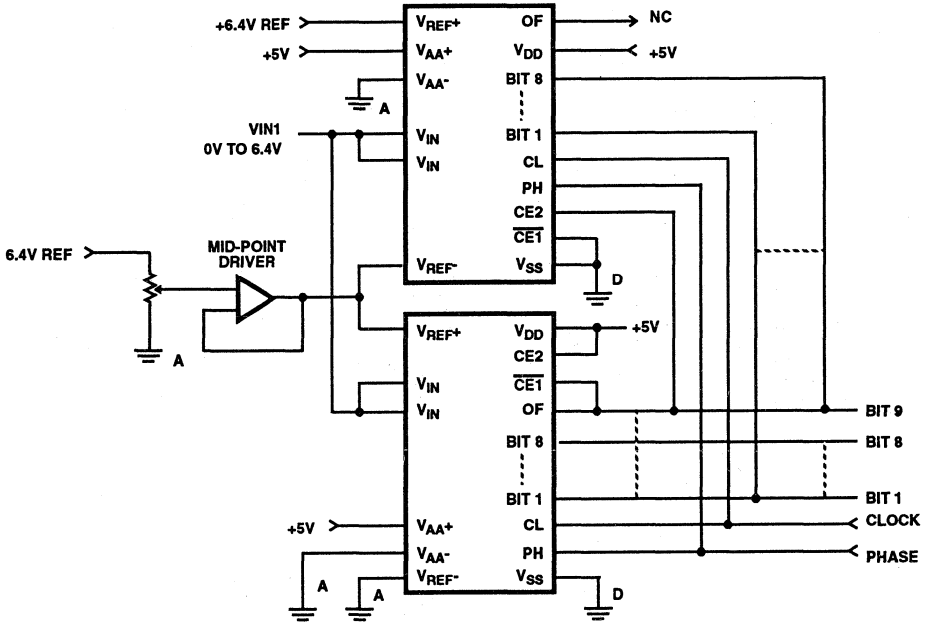


FIGURE 13. USING TWO CA3318s FOR 9-BIT RESOLUTION

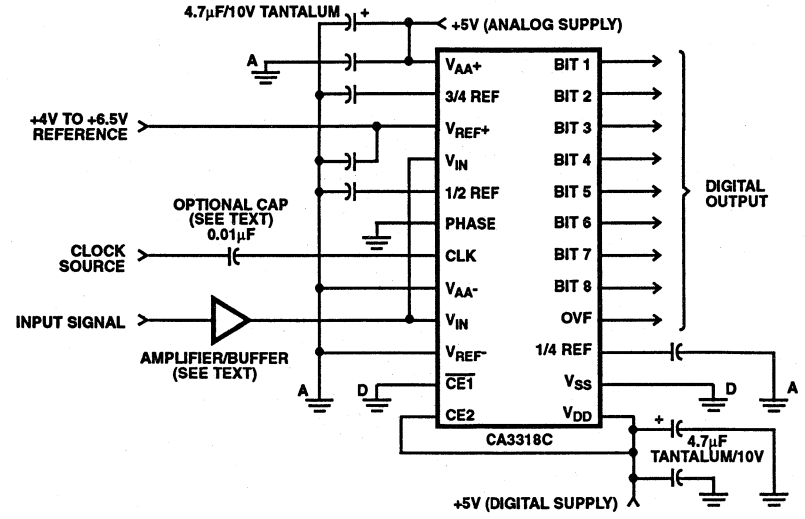


FIGURE 14. TYPICAL CIRCUIT CONFIGURATION FOR THE CA3318 WITH NO LINEARITY ADJUST

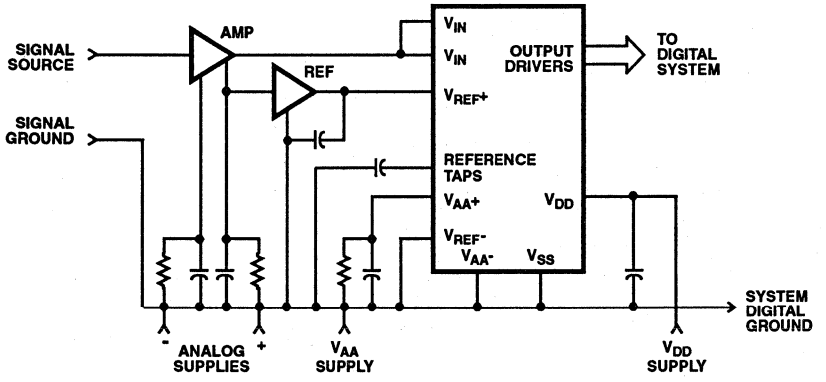
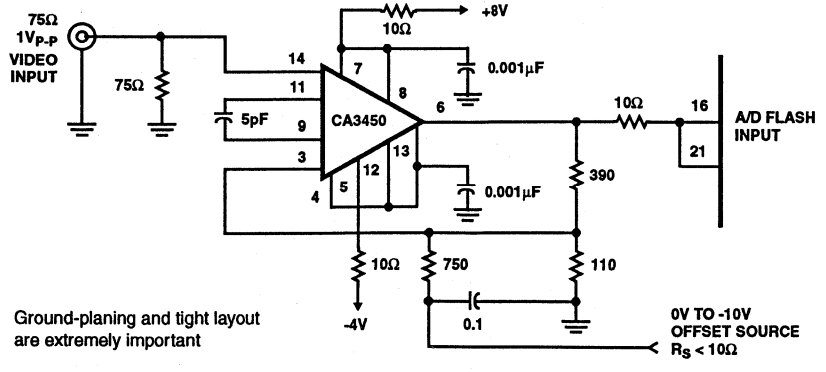


FIGURE 15. TYPICAL SYSTEM GROUNDING/BYPASSING



NOTE: Ground-planing and tight layout are extremely important

FIGURE 16. TYPICAL HIGH BANDWIDTH AMPLIFIER FOR DRIVING THE CA3318

TABLE 1. OUTPUT CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE (NOTE 1)		BINARY OUTPUT CODE									DECIMAL COUNT
	V_{REF} 6.40V (V)	V_{REF} 5.12V (V)	OF	MSB B8	B7	B6	B5	B4	B3	B2	LSB B1	
Zero	0.00	0.00	0	0	0	0	0	0	0	0	0	0
1 LSB	0.025	0.02	0	0	0	0	0	0	0	0	1	1
2 LSB	0.05	0.04	0	0	0	0	0	0	0	1	0	2
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
1/4 Full Scale	1.60	1.28	0	0	1	0	0	0	0	0	0	64
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
1/2 Full Scale - 1 LSB	3.175	2.54	0	0	1	1	1	1	1	1	1	127
1/2 Full Scale	3.20	2.56	0	1	0	0	0	0	0	0	0	128
1/2 Full Scale + 1 LSB	3.225	2.58	0	1	0	0	0	0	0	0	1	129
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
3/4 Full Scale	4.80	3.84	0	1	1	0	0	0	0	0	0	192
•	•	•					•					•
•	•	•					•					•
•	•	•					•					•
Full Scale - 1 LSB	6.35	5.08	0	1	1	1	1	1	1	1	0	254
Full Scale	6.375	5.10	0	1	1	1	1	1	1	1	1	255
Over Flow	6.40	5.12	1	1	1	1	1	1	1	1	1	511

NOTE: 1. The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Reducing Power

Most power is consumed while in the auto-balance state. When operating at lower than 15MHz clock speed, power can be reduced by stretching the sample ($\phi 2$) time. The constraints are a minimum balance time ($\phi 1$) of 33ns, and a maximum sample time of 500ns. Longer sample times cause droop in the auto-balance capacitors. Power can also be reduced in the reference string by switching the reference on only during auto-balance.

Clock Input

The Clock and Phase inputs feed buffers referenced to $V_{AA}+$ and $V_{AA}-$. Phase should be tied to one of these two potentials, while the clock (if DC coupled) should be driven at least from 0.2 to 0.7 x ($V_{AA}+$ - $V_{AA}-$). The clock may also be AC coupled with at least a 1 V_{P-P} swing. This allows TTL drive levels or 5V QMOS levels when $V_{AA}+$ is greater than 5V.

HI1166

December 1993

8-Bit, 250MSPS Flash A/D Converter

Features

- Differential Linearity Error ±0.5 LSB or Less
- Integral Linearity Error ±0.5 LSB or Less
- Built-In Integral Linearity Compensation Circuit
- Ultra High Speed Operation with Maximum Conversion Rate of 250MSPS (Min.)
- Low Input Capacitance 18pF (Typ.)
- Wide Analog Input Bandwidth 200MHz (Min. for Full-Scale Input)
- Single Power Supply -5.2V
- Low Power Consumption 1400mW (Typ.)
- Low Error Rate
- Capable of Driving 50Ω Loads
- Evaluation Board Available

Applications

- Spectrum Analyzers
- Video Digitizing
- Radar Systems
- Communication Systems
- Direct RF Down-Conversion
- Digital Oscilloscopes

Description

The HI1166 is an 8-bit ultra high speed flash Analog-to-Digital converter IC capable of digitizing analog signals at a maximum rate of 250MSPS. The digital I/O levels of the converter are compatible with ECL 100K/10KH/10K.

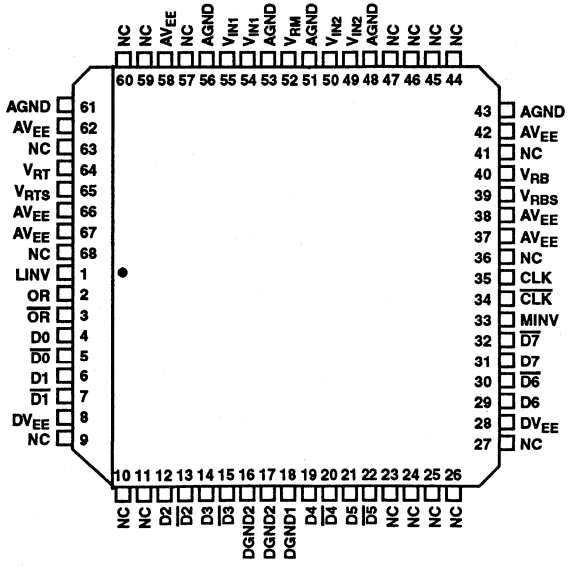
The HI1166 is available in the Industrial temperature range and is supplied in a 68 lead ceramic LCC package.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1166AIL	-20°C to +100°C	68 Lead LCC

Pinout

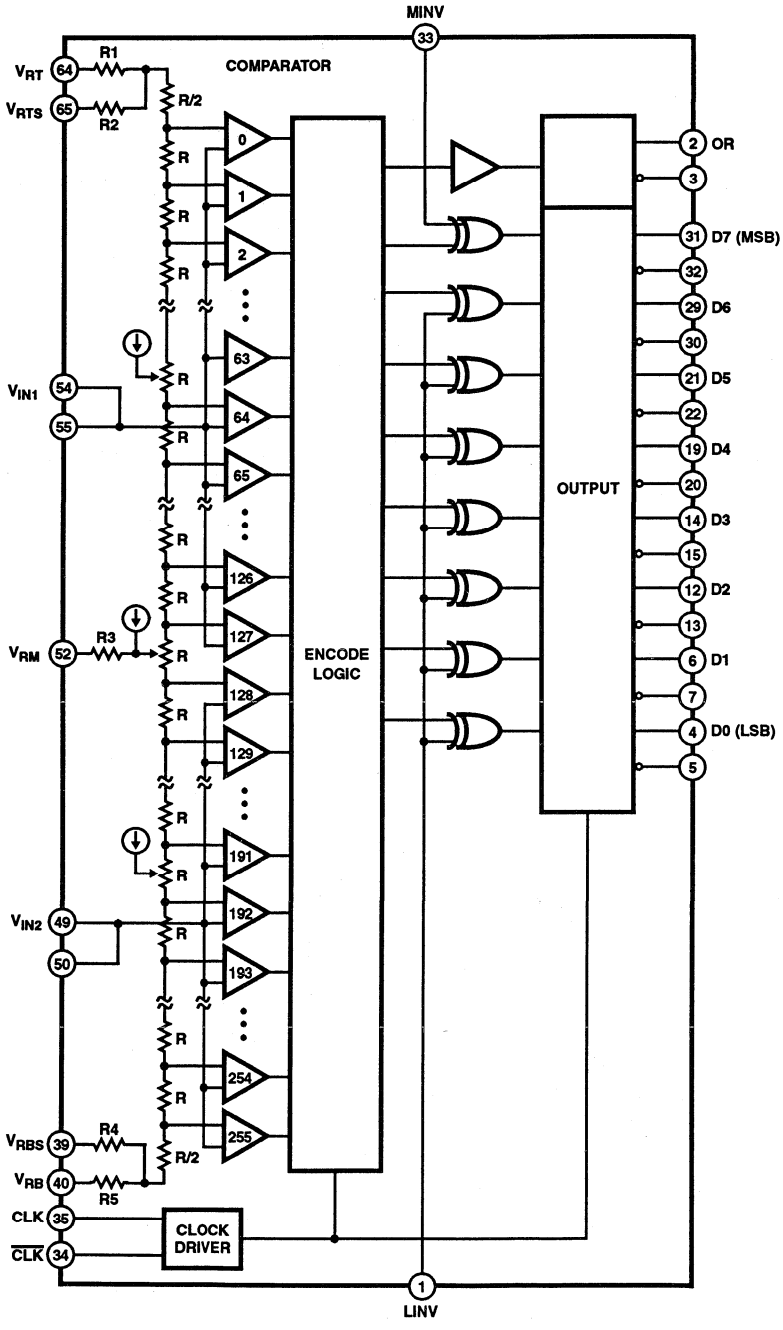
HI1166 (LCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3579.1

Functional Block Diagram



Absolute Maximum Ratings T_A = +25°C

Supply Voltage (AV_{EE}, DV_{EE}) ..... -7V to +0.5V
Analog Input Voltage (V_{IN}) ..... -2.7V to +0.5V
Reference Input Voltage
V_{RT}, V_{RB}, V_{RM} ..... -2.7V to +0.5V
$|V_{RT}-V_{RB}|$ 2.5V
Digital Input Voltage
MINV, $\overline{LINV}$, CLK, $\overline{CLK}$ ..... -4V to +0.5V
|CLK-$\overline{CLK}$| 2.7V
V_{RM} Pin Input Current (I_{VRM}) ..... -3mA to +3mA
Digital Output Current
(ID0 to ID7, IOR, $\overline{ID0}$ to $\overline{ID7}$, $\overline{IOR}$) ..... -30mA to 0mA
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
HI1166AIL	38°C/W	10°C/W

Maximum Power Dissipation 2.1W
Operating Temperature (Note 5)
T_A ..... -20°C to +100°C
T_C ..... -20°C to +125°C
Maximum Junction Temperature ..... +175°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions (Note 1)

Supply Voltage
AV_{EE}, DV_{EE} ..... -5.5V to -4.95V
AV_{EE}-DV_{EE} ..... -0.05V to 0.05V
AGND-DGND ..... -0.05V to 0.05V

Reference Input Voltage
V_{RT} ..... -0.1V to 0.1V
V_{RB} ..... -2.2V to -1.8V
Analog Input Voltage, V_{IN} ..... V_{RB} to V_{RT}

Electrical Specifications T_A = +25°C, AV_{EE} = DV_{EE} = -5.2V, V_{RT}, V_{RTS} = 0V, V_{RB}, V_{RBS} = -2V (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Resolution		-	8	-	Bits
Integral Linearity Error, (INL)	F_C = 250MSPS	-	±0.3	±0.5	LSB
Differential Linearity Error, (DNL)	F_C = 250MSPS	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Signal to Noise Ratio (SINAD) = RMS Signal / RMS Noise + Distortion	Input = 1kHz, Full Scale, F_C = 250MHz	-	46	-	dB
	Input = 60MHz, Full Scale, F_C = 250MHz	-	37	-	dB
Error Rate	Input = 50MHz, Full Scale, Error > 16 LSB, F_C = 250MHz	-	-	10^{-9}	TPS (Note 3)
	Input = 62.499MHz, Full Scale, Error > 16 LSB, F_C = 250MHz	-	10^{-8}	10^{-6}	TPS (Note 3)
Differential Gain Error, DG	NTSC 40IRE Mod. Ramp, F_C = 250MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Overrange Recovery Time		-	1.0	-	ns
Maximum Conversion Rate, F_C		250	-	-	MSPS
Aperture Jitter, T_{AJ}		-	9	-	ps
Sampling Delay, T_{DS}		0.4	1.4	2.4	ns
ANALOG INPUT					
Analog Input Capacitance, C_{IN}	V_{IN} = 1V + 0.07V_{RMS}	-	18	-	pF
Analog Input Resistance, R_{IN}		50	120	-	kΩ
Input Bias Current, I_{IN}	V_{IN} = -1V	20	-	450	µA
Full Scale Input Bandwidth	V_{IN} = 2V_{P-P}	200	250	-	MHz

Electrical Specifications T_A = +25°C, AV_{EE} = DV_{EE} = -5.2V, V_{RT}, V_{RTS} = 0V, V_{RB}, V_{RBS} = -2V (Note 1) **(Continued)**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE INPUTS						
Reference Resistance, R_{REF}			83	125	182	Ω
Residual Resistance	R1	Note 2	0.1	0.6	2.0	Ω
	R2		300	500	700	Ω
	R3		0.5	2.0	5.0	Ω
	R4		300	500	700	Ω
	R5		0.1	0.6	2.0	Ω
DIGITAL INPUTS						
Logic H Level, V_{IH}			-1.13	-	-	V
Logic L Level, V_{IL}			-	-	-1.5	V
Logic H Current, I_{IH}		Input Connected to GND	0	-	70	µA
Logic L Current, I_{IL}		Input Connected to -2V	-50	-	50	µA
Input Capacitance			-	4	-	pF
DIGITAL OUTPUTS						
Logic H Level, V_{OH}		R_L = 50Ω	-1.0	-	-	V
Logic L Level, V_{OL}		R_L = 50Ω	-	-	-1.6	V
TIMING CHARACTERISTICS						
H Pulse Width of Clock, T_{PW1}			1.8	-	-	ns
L Pulse Width of Clock, T_{PW0}			1.8	-	-	ns
Output Rise Time, T_R		R_L = 50Ω	-	0.6	1.5	ns
Output Fall Time, T_F		R_L = 50Ω	-	0.6	1.5	ns
Output Delay, T_{OD}		R_L = 50Ω	1.8	2.5	3.2	ns
POWER SUPPLY CHARACTERISTICS						
Supply Current, I_{EE}			-360	-270	-	mA
Power Consumption, P_D		Note 4	-	1.4	1.9	W

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. See Functional Block Diagram.
3. TPS: Times Per Sample.
4. $$P_D = I_{EEA} \bullet AV_{EE} + I_{EED} \bullet DV_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$$
5. T_A is specified in still air and without heatsink. To extend temperature range, appropriate heat management techniques must be employed (See Figure 2).

Timing Diagram

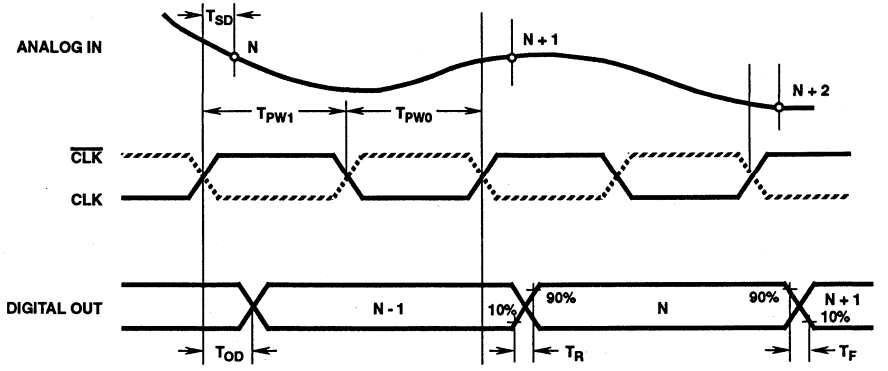


FIGURE 1.

Typical Performance Curves

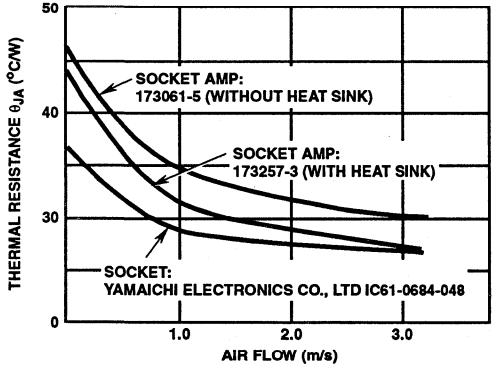


FIGURE 2. THERMAL RESISTANCE OF THE CONVERTER MOUNTED ON A BOARD

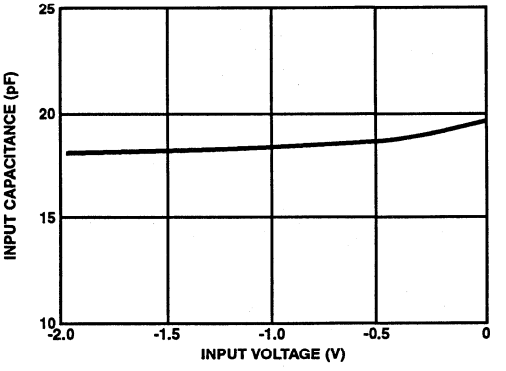


FIGURE 3. V_{IN} PIN CAPACITANCE vs VOLTAGE CHARACTERISTICS

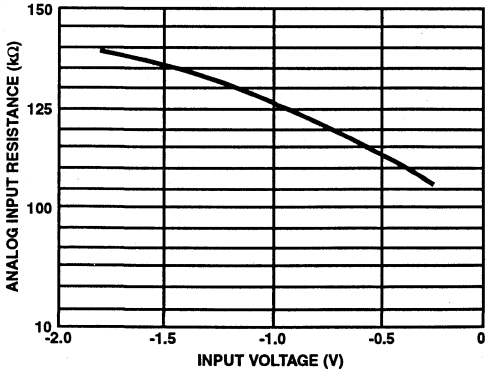


FIGURE 4. V_{IN} PIN INPUT RESISTANCE vs VOLTAGE CHARACTERISTICS

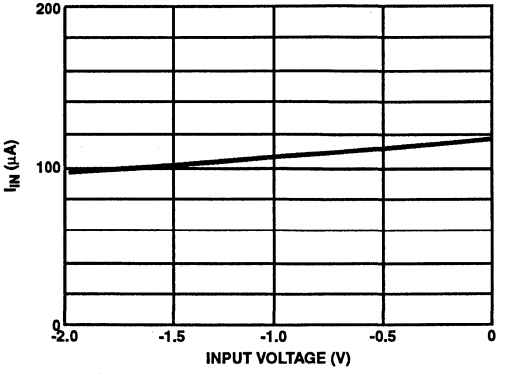


FIGURE 5. V_{IN} PIN INPUT CURRENT vs VOLTAGE CHARACTERISTICS

Typical Performance Curves (Continued)

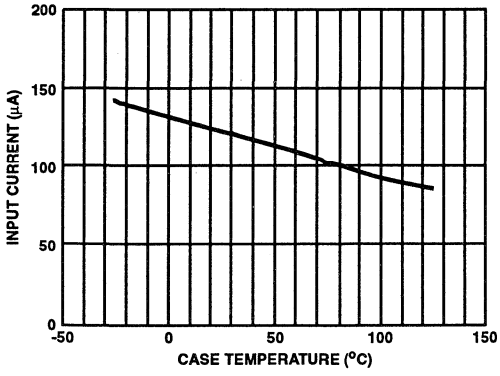


FIGURE 6. V_{IN} PIN INPUT CURRENT vs TEMPERATURE CHARACTERISTICS

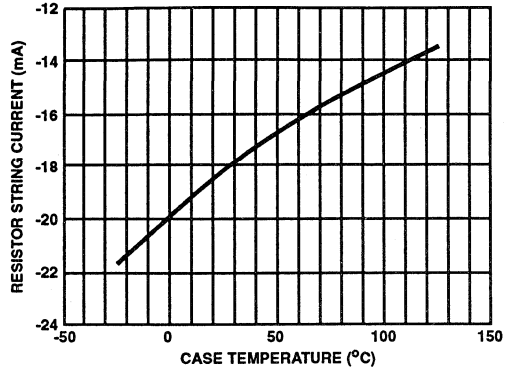


FIGURE 7. RESISTOR STRING CURRENT vs TEMPERATURE CHARACTERISTICS

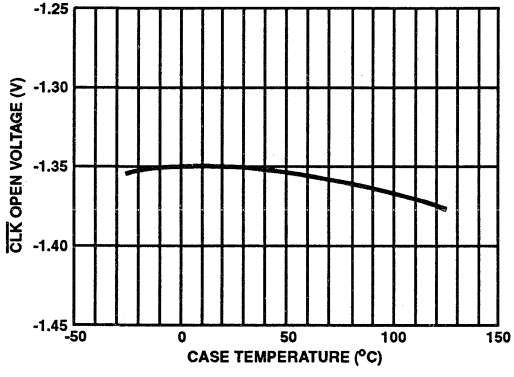


FIGURE 8. $\overline{CLK}$ OPEN VOLTAGE vs TEMPERATURE CHARACTERISTICS

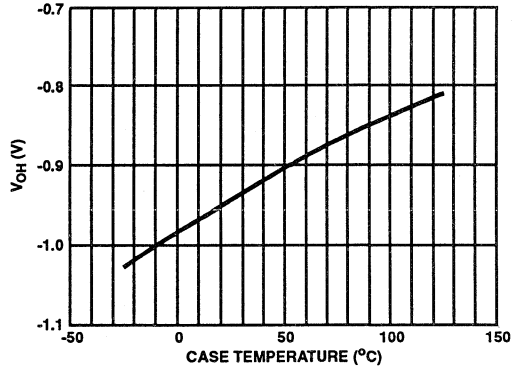


FIGURE 9. V_{OH} vs TEMPERATURE CHARACTERISTICS

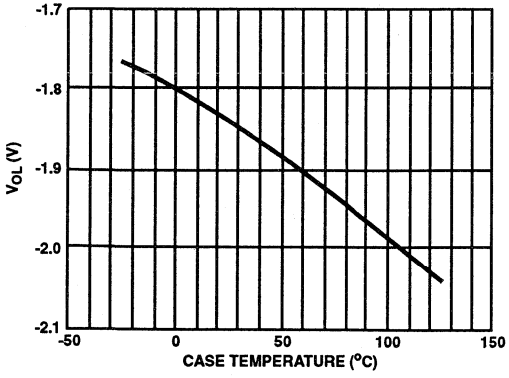


FIGURE 10. V_{OL} vs TEMPERATURE CHARACTERISTICS

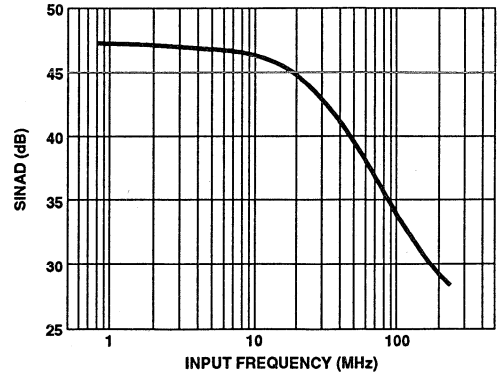


FIGURE 11. SINAD vs INPUT FREQUENCY RESPONSE CHARACTERISTICS

Typical Performance Curves (Continued)

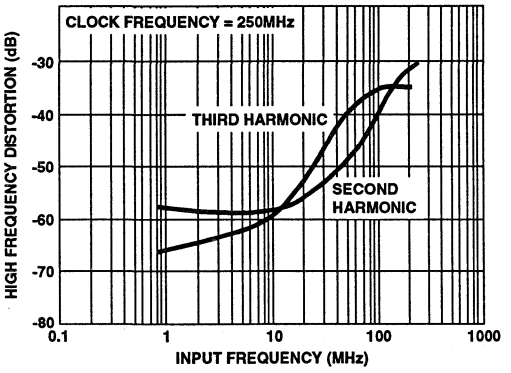


FIGURE 12. HARMONIC DISTORTION vs INPUT FREQUENCY RESPONSE CHARACTERISTICS

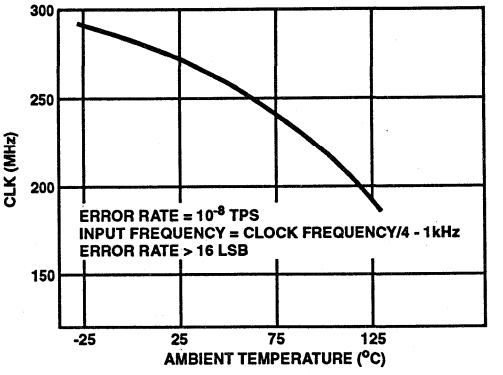


FIGURE 13. MAXIMUM CONVERSION RATE vs TEMPERATURE CHARACTERISTICS

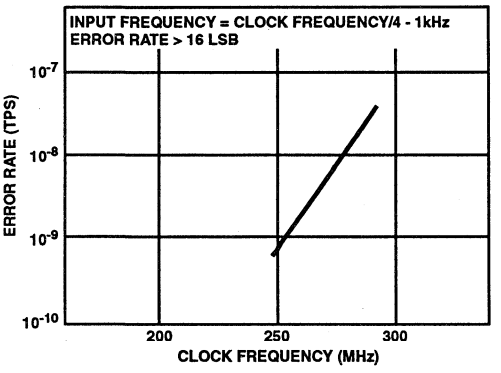


FIGURE 14. ERROR RATE vs CONVERSION RATE

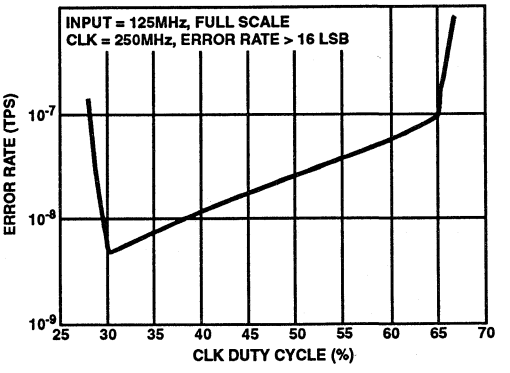


FIGURE 15. ERROR RATE vs CLOCK DUTY CYCLE

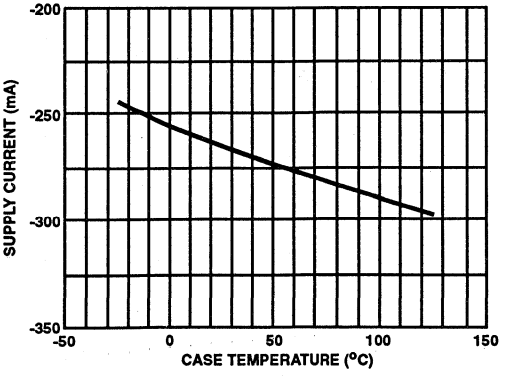
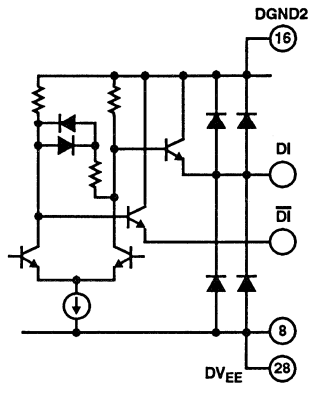
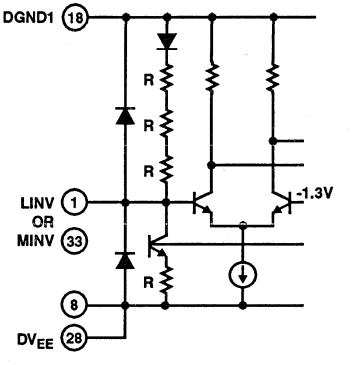
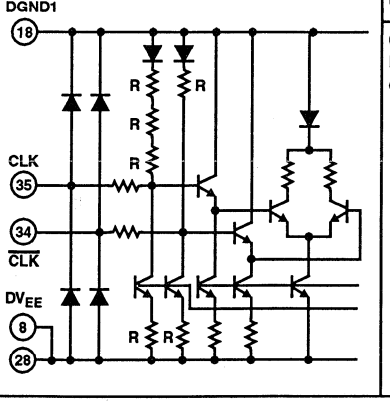
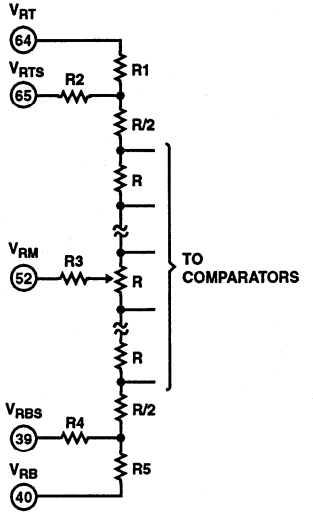
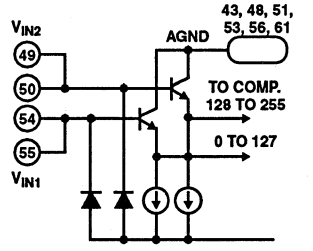
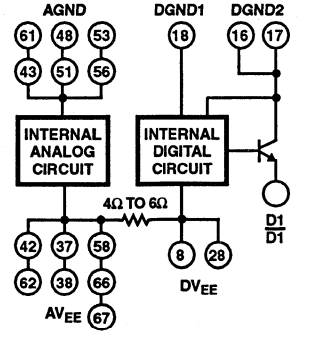


FIGURE 16. SUPPLY CURRENT vs TEMPERATURE CHARACTERISTICS

Pin Descriptions

PIN NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
4, 5	D0, $\overline{D0}$	O	ECL		LSB and complementary LSB output.
6, 7	D1, $\overline{D1}$				$\overline{D1}$ to $\overline{D6}$: Data output D1 to D6: Complementary Data output
12, 13	D2, $\overline{D2}$				
14, 15	D3, $\overline{D3}$				
19, 20	D4, $\overline{D4}$				
21, 22	D5, $\overline{D5}$				
29, 30	D6, $\overline{D6}$				
31, 32	D7, $\overline{D7}$				MSB complementary MSB data output.
2, 3	OR, $\overline{OR}$				Overrange and complementary overrange output.
1	LINV	I	ECL		Polarity selection for LSBs (refer to the A/D Output Code Table.) Pulled low when left open.
33	MINV	I	ECL		Polarity selection for MSB (refer to the A/D Output Code Table). Pulled low when left open.
35	CLK	I	ECL		CLK Input
34	$\overline{CLK}$				Complementary CLK input. Pulled down to -1.3V when left open.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
64	V_{RT}	I	0V		Analog reference voltage (top) (0V Typ.).
65	V_{RTS}	O	0V		Reference voltage sense (top).
52	V_{RM}	I	$V_{RB/2}$		Reference voltage mid point. Can be used for linearity compensation.
39	V_{RBS}	O	-2V		Reference voltage sense (bottom).
40	V_{RB}	I	-2V		Analog reference voltage (bottom).
49, 50	V_{IN2}	I	V_{RTS} to V_{RBS}		Analog input. All of the pins must be wired externally.
54, 55	V_{IN1}				
43, 48, 51, 53, 56, 61	AGND	-	0V		Analog ground.
37, 38, 42, 58, 62, 66, 67	AV_{EE}		-5.2V		Analog supply. Internally connected to DV_{EE} (resistance: 4Ω to 6Ω).
18	DGND1		0V		Digital ground.
16, 17	DGND2		0V		Digital ground for output drive.
8, 28	DV_{EE}		-5.2V		Digital supply. Internally connected to AV_{EE} (resistance: 4Ω to 6Ω).

A/D OUTPUT CODE TABLE

V_{IN} (Note 1)	STEP	MINV 1 LINV 1			0 1			1 0			0 0		
		OR	D7	D0	OR	D7	D0	OR	D7	D0	OR	D0	D7
0V		0	000•••••00		0	100•••••00		0	011•••••11		0	111•••••11	
	0	1	000•••••00		1	100•••••00		1	011•••••11		1	111•••••11	
	1	1	000•••••01		1	100•••••01		1	011•••••10		1	111•••••10	
			⋮			⋮			⋮			⋮	
-1V	127	1	011•••••11		1	111•••••11		1	000•••••00		1	100•••••00	
	128	1	100•••••00		1	000•••••00		1	111•••••11		1	011•••••11	
			⋮			⋮			⋮			⋮	
	254	1	111•••••10		1	011•••••10		1	100•••••01		1	000•••••01	
	255	1	111•••••11		1	011•••••11		1	100•••••00		1	000•••••00	
-2V		1	111•••••11		1	011•••••11		1	100•••••00		1	000•••••00	

NOTE:

1. $V_{RT} = V_{RTS} = 0V$, $V_{RM} = -1V$ or open, $V_{RB} = V_{RBS} = -2V$

Test Circuits

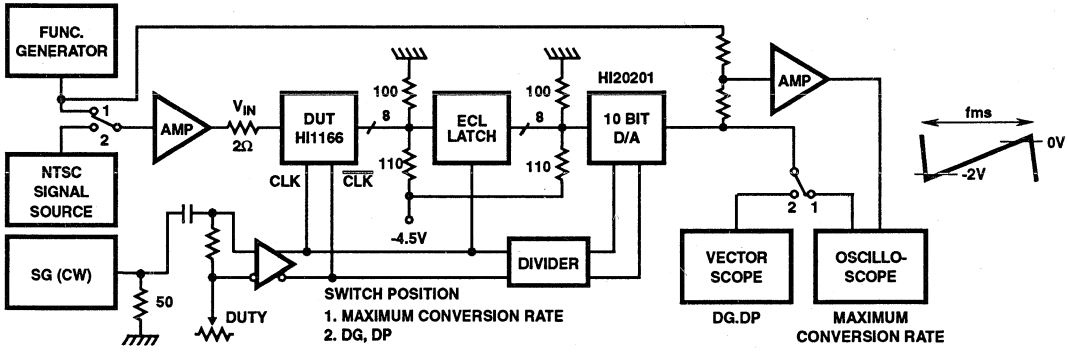


FIGURE 2. MAXIMUM CONVERSION RATE AND DIFFERENTIAL GAIN/PHASE ERROR TEST CIRCUIT

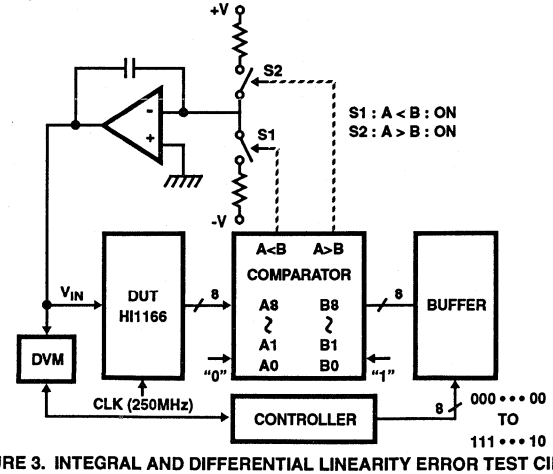


FIGURE 3. INTEGRAL AND DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits (Continued)

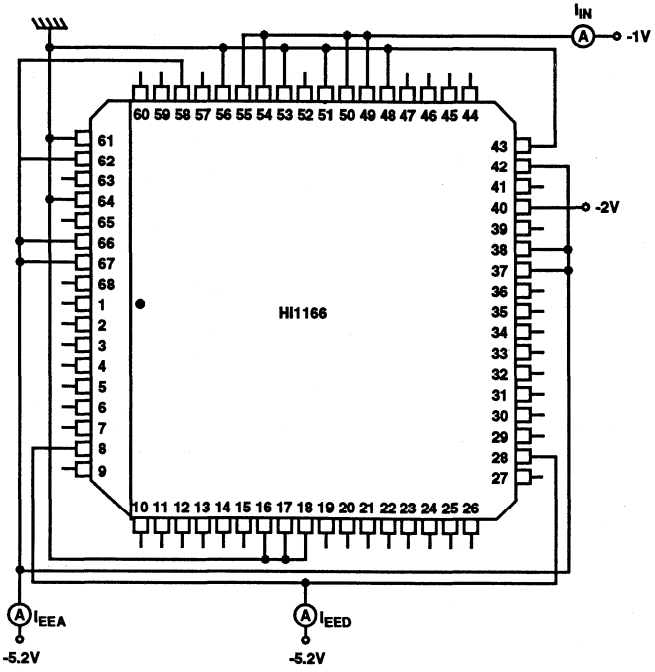


FIGURE 4. POWER SUPPLY AND ANALOG INPUT BIAS CURRENT TEST CIRCUIT

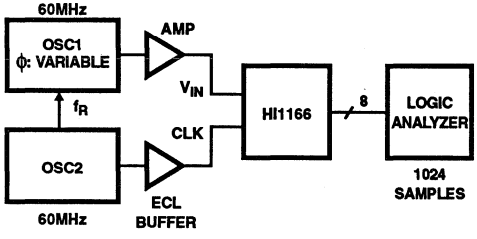


FIGURE 5A.

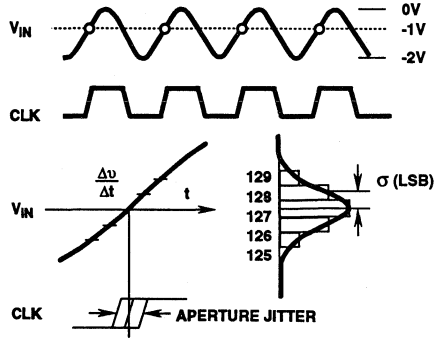


FIGURE 5B. APERTURE JITTER TEST METHOD

Aperture jitter is defined as follows:

$$T_{AJ} = \sigma / \frac{\Delta v}{\Delta t} = \sigma / (\frac{256}{2} \times 2\pi f)$$

Where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

FIGURE 5. SAMPLING DELAY AND APERTURE JITTER TEST CIRCUIT

HARRIS SEMICONDUCTOR

HI1276

December 1993

8-Bit, 500MSPS Flash A/D Converter

Features

- Differential Linearity Error ±0.5 LSB or Less
- Integral Linearity Error ±0.7 LSB or Less
- Built-In Integral Linearity Compensation Circuit
- Ultra High Speed Operation with Maximum Conversion Rate of 500MSPS (Min.)
- Low Input Capacitance 20pF (Typ.)
- Wide Analog Input Bandwidth 300MHz (Min. for Full-Scale Input)
- Single Power Supply -5.2V
- Low Power Consumption 2.8W (Typ.)
- Low Error Rate
- Capable of Driving 50Ω Loads
- Evaluation Board Available

Applications

- Radar Systems
- Communication Systems
- Digital Oscilloscopes
- Direct RF Down-Conversion

Description

The HI1276 is a 8-bit ultra high speed flash Analog-to-Digital converter IC capable of digitizing analog signals at a maximum rate of 500MSPS. The digital I/O levels of this A/D converter are compatible with ECL 100K/10KH/10K.

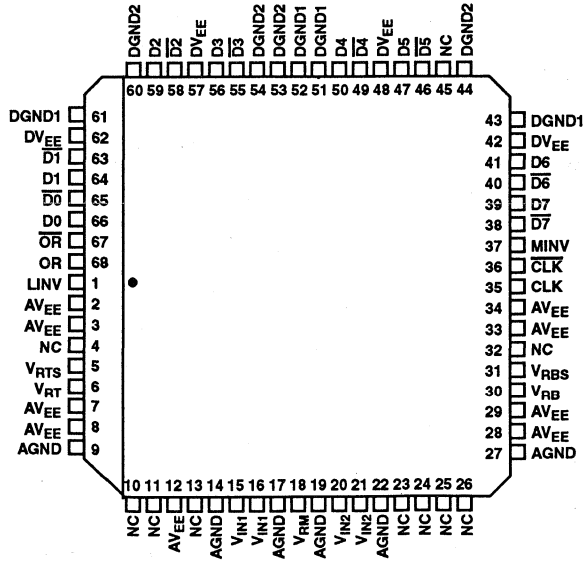
The HI1276 is available in the Industrial temperature range and is supplied in a 68 lead ceramic LCC package.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1276AIL	-20°C to +100°C	68 Lead Ceramic LCC

Pinout

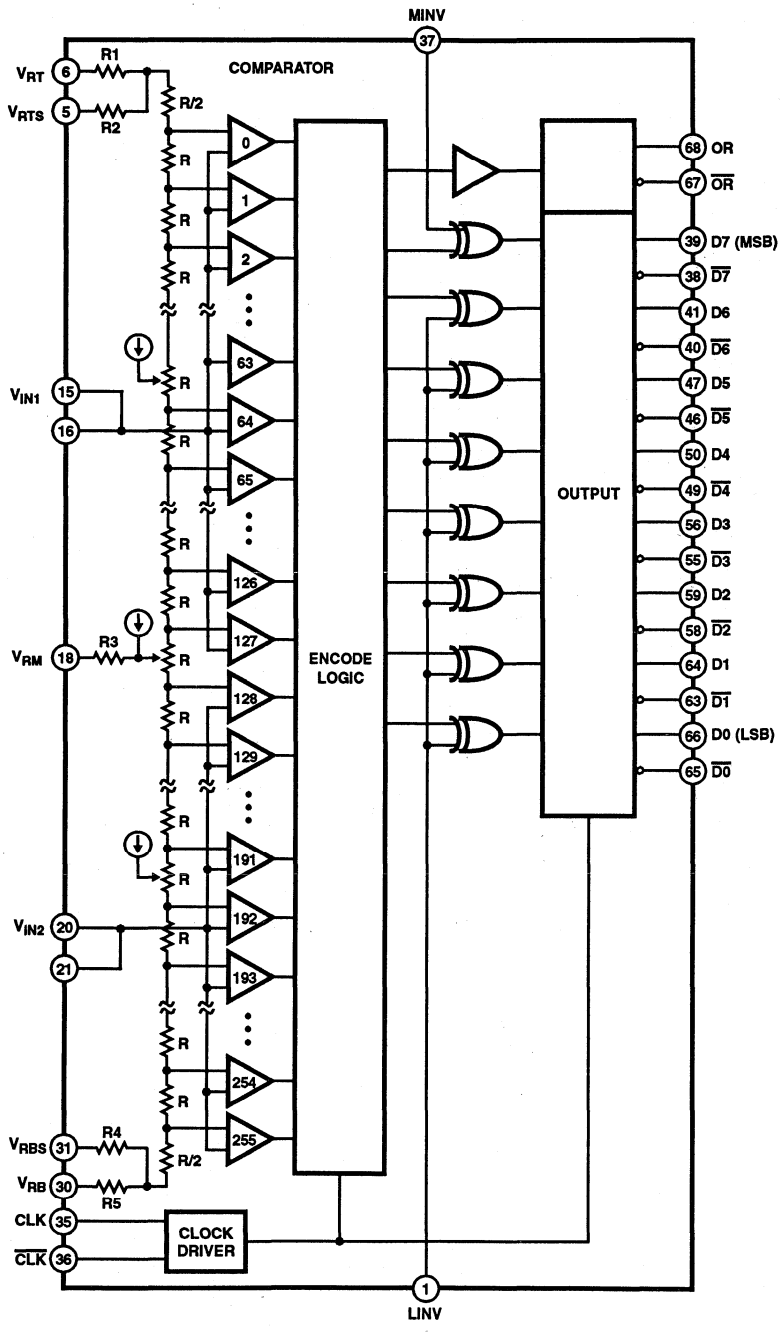
HI1276 (LCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3578.1

Functional Block Diagram



Absolute Maximum Ratings $T_A = +25°C$

Supply Voltage (AV_{EE}, DV_{EE}) ..... -7V to +0.5V
Analog Input Voltage (V_{IN}) ..... -2.7 to +0.5V
Reference Input Voltage
V_{RT}, V_{RB}, V_{RM} ..... AV_{EE} to +0.5V
$|V_{RT}-V_{RB}|$ 2.5V
Digital Input Voltage
MINV, $\overline{LINV}$ ..... -4V to +0.5V
CLK, $\overline{CLK}$, ... DV_{EE} to +0.5V
$|CLK-\overline{CLK}|$ 2.7V
V_{RM} Pin Input Current (I_{VRM}) ..... -3mA to +3mA
Digital Output Current
(ID0 to ID7, IOR, $\overline{ID0}$ to $\overline{ID7}$, $\overline{IOR}$) ..... -30mA to 0mA
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
HI1276AIL	18°C/W	4°C/W

Maximum Power Dissipation 3.8W
Operating Temperature (Note 5)
T_A ..... -20°C to +100°C
T_C ..... -20°C to +125°C
Maximum Junction Temperature ..... +175°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions (Note 1)

Supply Voltage
AV_{EE}, DV_{EE} ..... -5.5V to -4.95V
AV_{EE}-DV_{EE} ..... -0.05V to 0.05V
AGND-DGND ..... -0.05V to 0.05V

Reference Input Voltage
V_{RT} ..... -0.1V to 0.1V
V_{RB} ..... -2.2V to -1.8V
Analog Input Voltage, V_{IN} ..... V_{RB} to V_{RT}

Electrical Specifications $T_A = +25°C$, $AV_{EE} = DV_{EE} = -5.2V$, V_{RT}, $V_{RTS} = 0V$, V_{RB}, $V_{RBS} = -2V$ (Note 1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE						
Resolution			-	8	-	Bits
Integral Linearity Error, (INL)		F_C = 500MHz	-	±0.3	±0.7	LSB
Differential Linearity Error, (DNL)		F_C = 500MHz	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS						
Signal to Noise Ratio (SINAD) = RMS Signal / RMS Noise + Distortion		Input = 1kHz, Full Scale, F_C = 500MHz	-	46	-	dB
		Input = 100MHz, Full Scale, F_C = 500MHz	-	37	-	dB
Error Rate		Input = 100MHz, Full Scale, Error > 16 LSB, F_C = 400MHz	-	10^{-11}	10^{-9}	TPS (Note 3)
		Input = 125MHz, Full Scale, Error > 16 LSB, F_C = 500MHz	-	10^{-8}	10^{-6}	TPS (Note 3)
Differential Gain Error, DG		NTSC 40IRE Mod. Ramp, F_C = 500MSPS	-	1.0	-	%
Differential Phase Error, DP			-	0.5	-	Degree
Overrange Recovery Time			-	1.0	-	ns
Maximum Conversion Rate, F_C			500	-	-	MSPS
Aperture Jitter, T_{AJ}		Input = 150MHz	-	11	-	ps
Sampling Delay, T_{DS}		Input = 150MHz	0.2	0.8	1.5	ns
ANALOG INPUT						
Analog Input Capacitance, C_{IN}		V_{IN} = 1V + 0.07V_{RMS}	-	20	-	pF
Analog Input Resistance, R_{IN}			30	70	-	kΩ
Input Bias Current, I_{IN}		V_{IN} = -1V	-	-	620	µA
Full Scale Input Bandwidth		V_{IN} = 2V_{P-P}	300	-	-	MHz
REFERENCE INPUTS						
Reference Resistance, R_{REF}			70	110	160	Ω
Residual Resistance	R1	Note 2	0.1	0.5	2.0	Ω
	$\overline{R2}$		0.5	5.2	10	Ω
	R3		0.5	1.6	5.0	Ω
	$\overline{R4}$		0.5	8.7	20	Ω
	$\overline{R5}$		0.1	0.5	2.0	Ω

Electrical Specifications T_A = +25°C, AV_{EE} = DV_{EE} = -5.2V, V_{RT}, V_{RTS} = 0V, V_{RB}, V_{RBS} = -2V (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS					
Logic H Level, V_{IH}		-1.10	-	-	V
Logic L Level, V_{IL}		-	-	-1.55	V
Logic H Current, I_{IH}	Input Connected to -0.8V	-	-	70	µA
Logic L Current, I_{IL}	Input Connected to -1.6V	-50	-	60	µA
Input Capacitance		-	6	-	pF
DIGITAL OUTPUTS					
Logic H Level, V_{OH}	R_L = 50Ω	-1.03	-	-	V
Logic L Level, V_{OL}	R_L = 50Ω	-	-	-1.58	V
TIMING CHARACTERISTICS					
Clock Duty Cycle		45	50	55	%
Output Rise Time, T_R	R_L = 50Ω, 20% to 80%	0.5	0.7	1.0	ns
Output Fall Time, T_F	R_L = 50Ω, 80% to 20%	0.5	0.7	1.0	ns
Output Delay, T_{OD}		1.5	1.9	2.3	ns
POWER SUPPLY CHARACTERISTICS					
Supply Current, I_{EE}		-680	-520	-	mA
Power Consumption, P_D	Note 4	-	2.8	3.6	W

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. See Functional Block Diagram.
3. TPS: Times Per Sample.
4. $P_D = I_{EEA} \bullet AV_{EE} + I_{EED} \bullet DV_{EE} + \frac{(V_{RT}-V_{RB})^2}{R_{REF}}$
5. T_A is specified in still air and without heatsink. To extend temperature range, appropriate heat management techniques must be employed (See Figure 2).

Timing Diagram

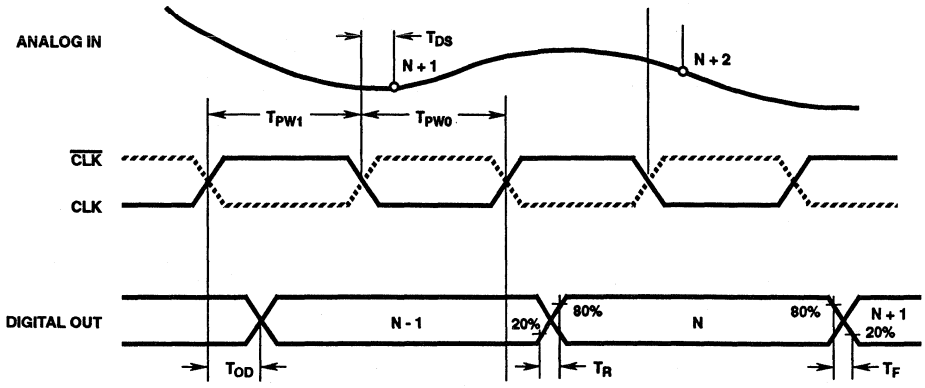


FIGURE 1.

Typical Performance Curves

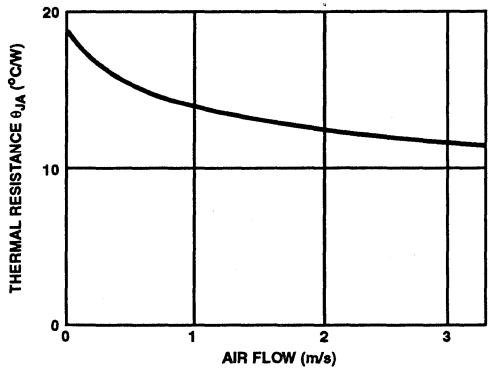


FIGURE 2. THERMAL RESISTANCE MOUNTED ON-BOARD

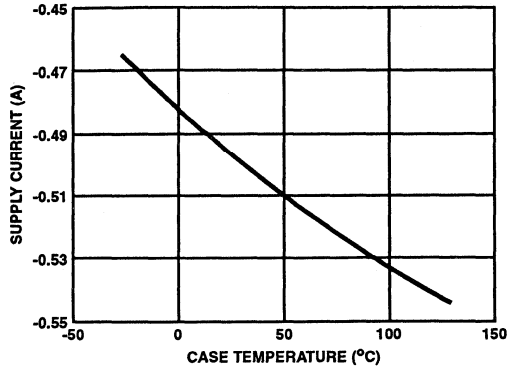


FIGURE 3. SUPPLY CURRENT vs TEMPERATURE CHARACTERISTICS

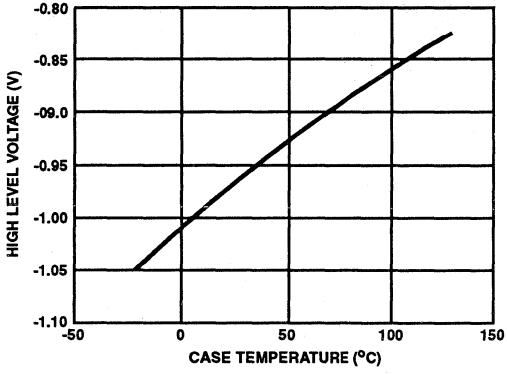


FIGURE 4. DO PIN HIGH LEVEL VOLTAGE vs TEMPERATURE CHARACTERISTICS

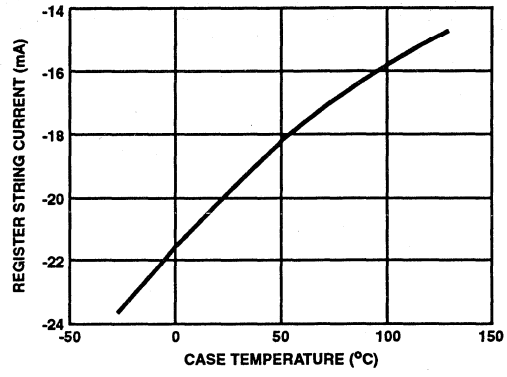


FIGURE 5. REGISTER STRING CURRENT vs TEMPERATURE CHARACTERISTICS

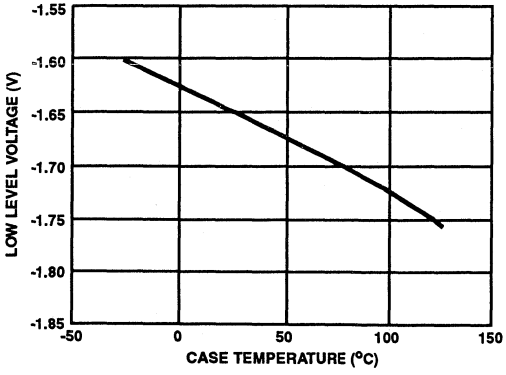


FIGURE 6. DO PIN LEVEL VOLTAGE vs TEMPERATURE CHARACTERISTICS

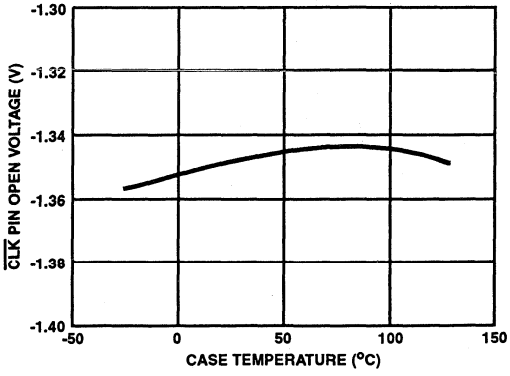


FIGURE 7. $\overline{CLK}$ PIN OPEN VOLTAGE vs TEMPERATURE CHARACTERISTICS

Typical Performance Curves (Continued)

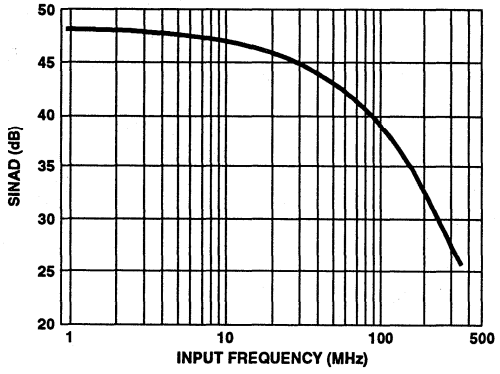


FIGURE 8. SINAD vs INPUT FREQUENCY CHARACTERISTICS

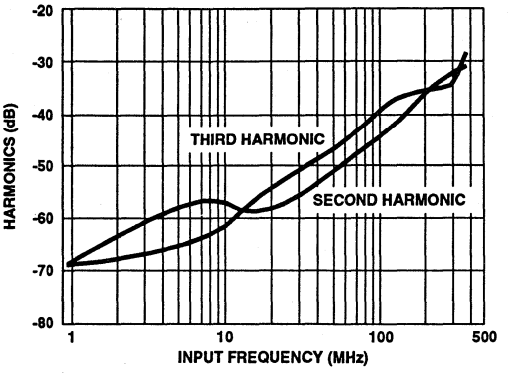


FIGURE 9. HARMONIC DISTORTION vs INPUT FREQUENCY CHARACTERISTICS

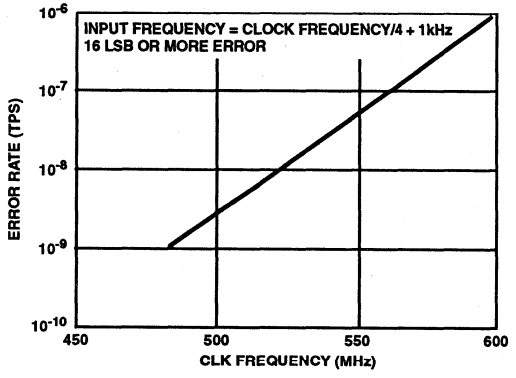


FIGURE 10. ERROR RATE vs CONVERSION FREQUENCY CHARACTERISTICS

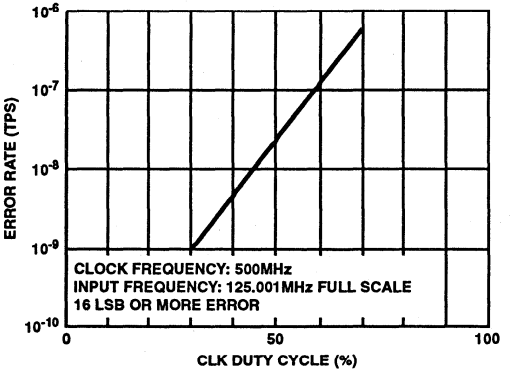


FIGURE 11. ERROR RATE vs CLOCK DUTY CYCLE CHARACTERISTICS

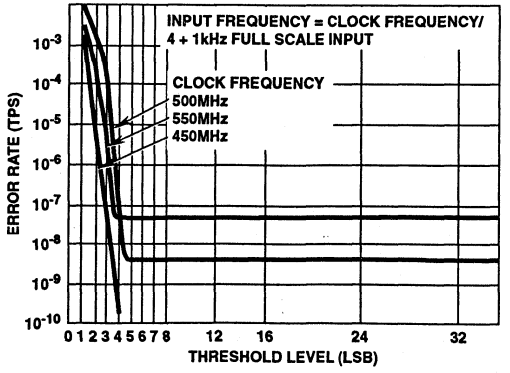
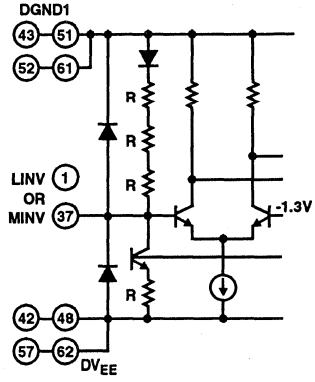
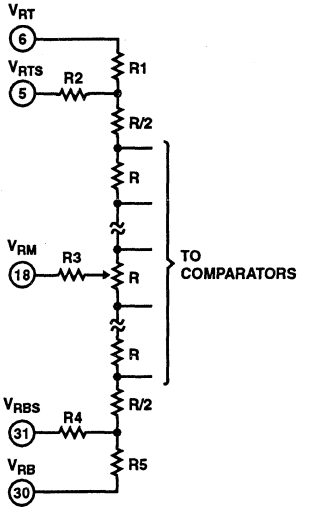
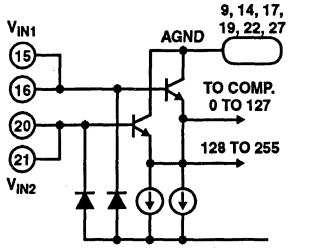
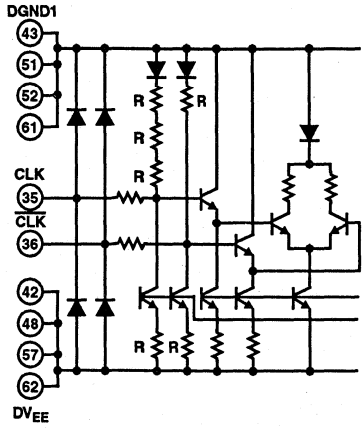
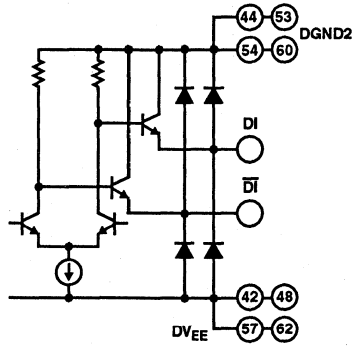
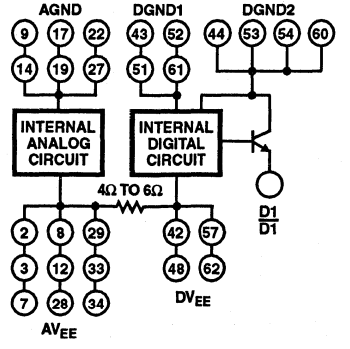


FIGURE 12. ERROR RATE vs THRESHOLD LEVEL CHARACTERISTICS

Pin Descriptions

PIN NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
1	LINV	I	ECL		Polarity selection for LSBs (refer to the A/D Output Code Table.) Pulled low when left open.
37	MINV				Polarity selection for MSB (refer to the A/D Output Code Table). Pulled low when left open.
6	V_{RT}	I	0V		Analog reference voltage (top) (0V typ.).
5	V_{RTS}	O	0V		Reference voltage sense (top).
18	V_{RM}	I	$V_{RB/2}$		Reference voltage mid point. Can be used for linearity compensation.
31	V_{RBS}	O	-2V		Reference voltage sense (bottom).
30	V_{RB}	I	-2V		Analog reference voltage (bottom).
15, 16	V_{IN1}	I	V_{RTS} to V_{RBS}		Analog input. All of the pins must be wired externally.
20, 21	V_{IN2}				

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
35	CLK	I	ECL		CLK Input
36	$\overline{CLK}$				Complementary CLK input. Pulled down to -1.3V when left open.
38, 39	$\overline{D7}$, D7	O	ECL		MSB and complementary MSB data output.
40, 41	$\overline{D6}$, D6				D1 to D6: Data output $\overline{D1}$ to $\overline{D6}$: Complementary data output
46, 47	$\overline{D5}$, D5				
49, 50	$\overline{D4}$, D4				
55, 56	$\overline{D3}$, D3				
58, 59	$\overline{D2}$, D2				
63, 64	$\overline{D1}$, D1				
65, 66	$\overline{D0}$, D0				LSB data complementary output LSB data output.
67, 68	$\overline{OR}$, OR				Overrange and complementary overrange output.
2, 3, 7, 8, 12, 28, 29, 33, 34	AV_{EE}	-	-5.2V		Analog supply. Internally connected to DV_{EE} (resistance: 4Ω to 6Ω).
9, 14, 17, 19, 22, 27	AGND		0V		Analog ground.
42, 48, 57, 62	DV_{EE}		-5.2V		Digital supply. Internally connected to AV_{EE} (resistance: 4Ω to 6Ω).
43, 51, 52, 61	DGND1		0V		Digital ground.
44, 53, 54, 60	DGND2 (Note 1)		0V		Digital ground for output drive.
4, 10, 11, 13, 23, 24, 25, 26, 32	NC				No connect pins. It is recommended to wire these pins to AGND.
45	NC				No connect pin. It is recommended to wire these pins to DGND.

A/D OUTPUT CODE TABLE

V_{IN} (NOTE 1)	STEP	MINV 1, LINV 1			0, 1			1, 0			0, 0		
		OR	D7	D0	OR	D7	D0	OR	D7	D0	OR	D0	D7
0V		0	000•••••00		0	100•••••00		0	011•••••11		0	111•••••11	
	0	1	000•••••00		1	100•••••00		1	011•••••11		1	111•••••11	
	1	1	000•••••01		1	100•••••01		1	011•••••10		1	111•••••10	
			•			•			•			•	
			•			•			•			•	
			•			•			•			•	
-1V	127	1	011•••••11		1	111•••••11		1	000•••••00		1	100•••••00	
	128	1	100•••••00		1	000•••••00		1	111•••••11		1	011•••••11	
			•			•			•			•	
			•			•			•			•	
			•			•			•			•	
	254	1	111•••••10		1	011•••••10		1	100•••••01		1	000•••••01	
	255	1	111•••••11		1	011•••••11		1	100•••••00		1	000•••••00	
-2V		1	111•••••11		1	011•••••11		1	100•••••00		1	000•••••00	

NOTE:

1. $V_{RT} = V_{RTS} = 0V$, $V_{RM} = -1V$ or open, $V_{RB} = V_{RBS} = -2V$

Test Circuits

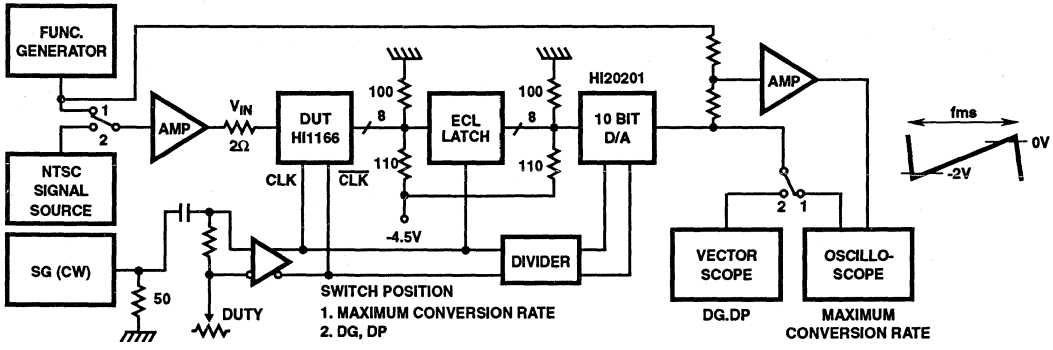


FIGURE 2. MAXIMUM CONVERSION RATE AND DIFFERENTIAL GAIN/PHASE ERROR TEST CIRCUIT

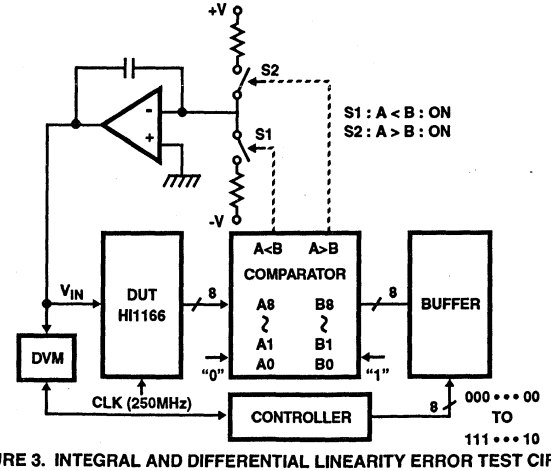


FIGURE 3. INTEGRAL AND DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits (Continued)

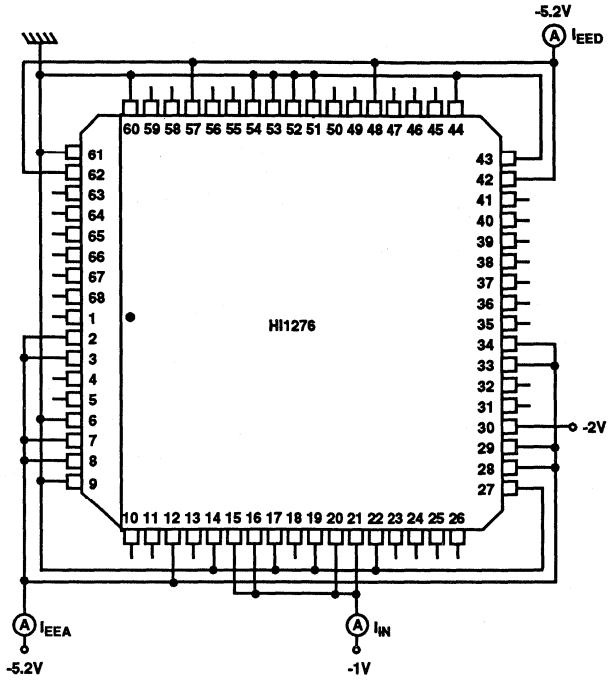


FIGURE 4. POWER SUPPLY AND ANALOG INPUT BIAS CURRENT TEST CIRCUIT

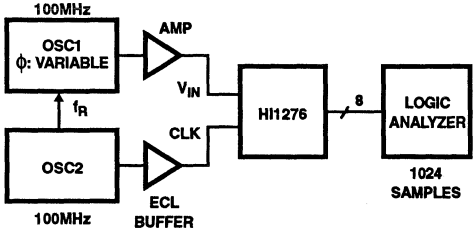
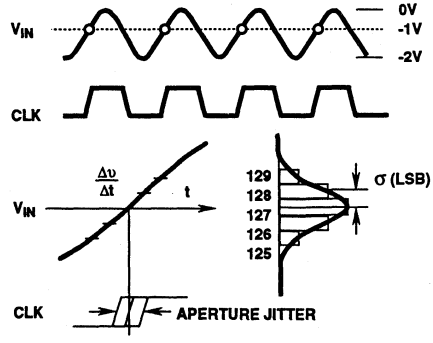


FIGURE 5A.



Aperture jitter is defined as follows:

$$T_{AJ} = \sigma / \frac{\Delta v}{\Delta t} = \sigma / (\frac{256}{2} \times 2\pi f)$$

FIGURE 5B. APERTURE JITTER TEST METHOD

Where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

FIGURE 5. SAMPLING DELAY AND APERTURE JITTER TEST CIRCUIT

HARRIS SEMICONDUCTOR

HI1386

December 1993

8-Bit, 75MSPS Flash A/D Converter

Features

- Differential Linearity Error ±0.5 LSB or Less
- Integral Linearity Error ±0.5 LSB or Less
- Built-In Integral Linearity Compensation Circuit
- High-Speed Operation with Maximum Conversion Rate of 75MSPS (Min.)
- Low Input Capacitance 17pF (Typ.)
- Wide Analog Input Bandwidth 150MHz (Min. for Full Scale Input)
- Single Power Supply -5.2V
- Low Power Consumption 580mW (Typ.)
- Low Error Rate
- Operable at 50% Clock Duty Cycle
- Capable of Driving 50Ω Loads
- Evaluation Board Available

Applications

- Video Digitizing
- HDTV (High Definition TV)
- Radar Systems
- Communication Systems
- Direct RF Down-Conversion
- Digital Oscilloscopes

Description

The HI1386 is a 8-bit high-speed flash analog-to-digital converter IC capable of digitizing analog signals at a maximum rate of 75MSPS. The digital I/O levels of this A/D converter are compatible with ECL 100K/10KH/10K.

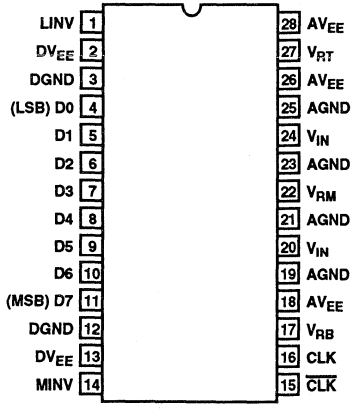
The HI1386 is available in the commercial and industrial temperature range and is supplied in 28 lead plastic DIP and 44 lead ceramic LCC packages.

Ordering Information

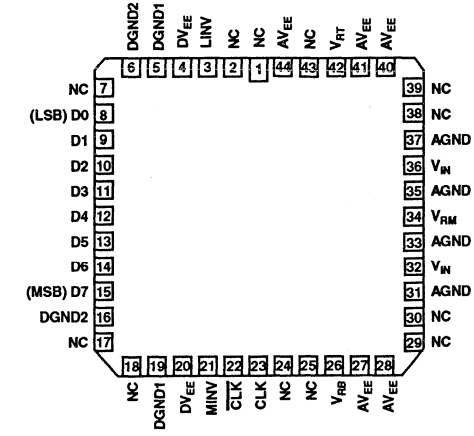
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1386JCP	-25°C to +75°C	28 Lead Plastic DIP
HI1386AIL	-25°C to +100°C	44 Lead LCC

Pinouts

HI1386 (PDIP)
TOP VIEW



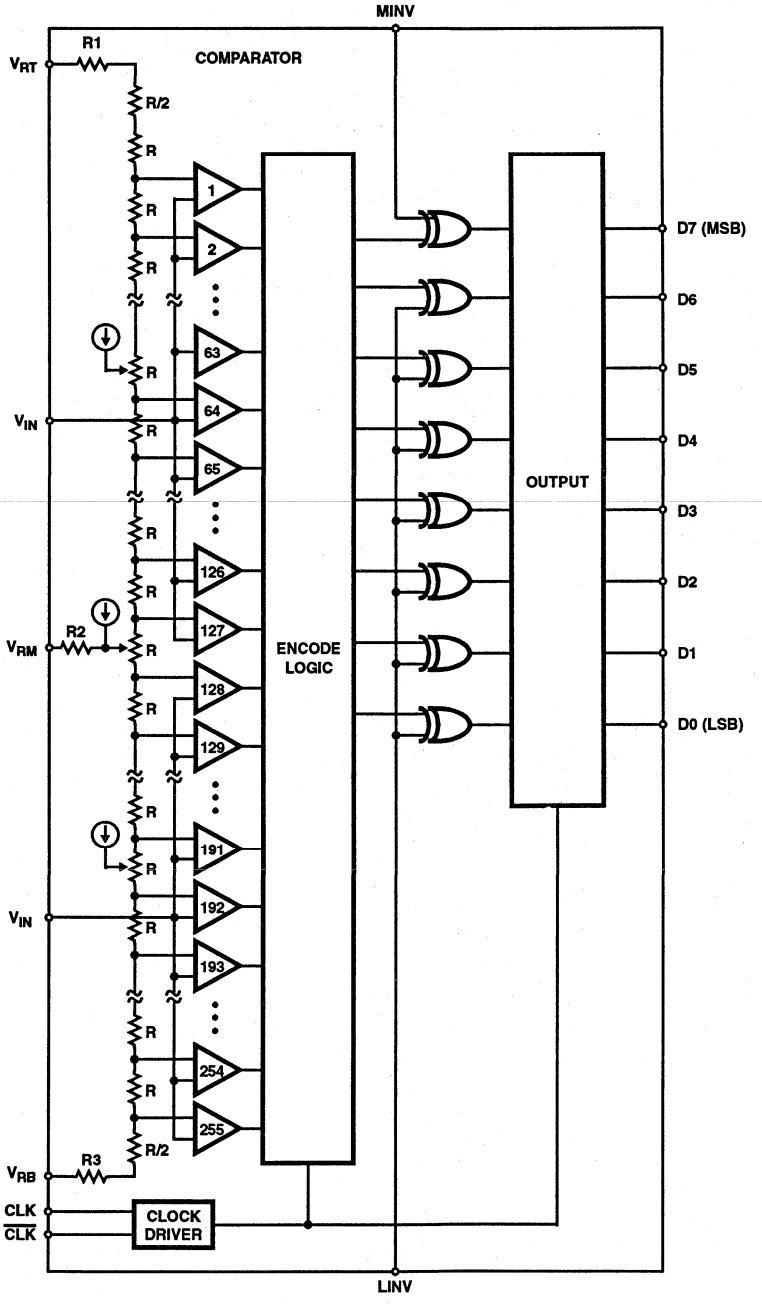
HI1386 (LCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3583.1**

Functional Block Diagram



Absolute Maximum Ratings T_A = +25°C

Supply Voltage (AV_{EE}, DV_{EE}) ..... -7V to +0.5V
Analog Input Voltage (V_{IN}) ..... -2.7V to +0.5V
Reference Input Voltage
V_{RT}, V_{RB}, V_{RM} ..... -2.7V to +0.5V
$|V_{RT} - V_{RB}|$ 2.5V
Digital Input Voltage
CLK, $\overline{CLK}$, MINV, LINV ..... -4V to +0.5V
$|CLK - \overline{CLK}|$ 2.7V
V_{RM} Pin Input Current (I_{VRM}) ..... -3mA to +3mA
Digital Output Current (ID0 to ID7) ..... -30mA to 0mA
Storage Temperature Range (T_{STG}) ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
HI1386JCP	58°C/W	-
HI1386AIL	45°C/W	11°C/W

Maximum Power Dissipation 1.17W
Maximum Junction Temperature
HI1386AIL ..... +175°C
HI1386JCP ..... +150°C
Operating Temperature (Note 4)
HI1386JCP (T_A) ..... -20°C to +75°C
HI1386AIL (T_C) ..... -20°C to +100°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Supply Voltage
AV_{EE}, DV_{EE} ..... -5.5V to -4.95V
AV_{EE}-DV_{EE} ..... -0.05V to 0.05V
AGND-DGND ..... -0.05V to 0.05V
Reference Input Voltage
V_{RT} ..... -0.1V to 0.1V
V_{RB} ..... -2.2V to -1.8V
Analog Input Voltage, V_{IN} ..... V_{RB} to V_{RT}
Pulse Width of Clock
T_{PW1} ..... 6.6ns Min.
T_{PW0} ..... 6.6ns Min.

Electrical Specifications T_A = +25°C, AV_{EE} = DV_{EE} = -5.2V, V_{RT} = 0V, V_{RB} = -2V (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Resolution		8	8	8	Bits
Integral Linearity Error, (INL)	F_C = 75MHz	-	±0.3	±0.5	LSB
Differential Linearity Error, (DNL)	F_C = 75MHz	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Signal to Noise Ratio (SINAD) = RMS Signal / RMS Noise + Distortion	Input = 1MHz, Full Scale, F_C = 75MHz	-	49	-	dB
	Input = 18.75MHz, Full Scale, F_C = 75MHz	-	41	-	dB
Error Rate	Input = 18.749MHz, Full Scale, Error > 16 LSB, F_C = 75MHz	-	-	10^{-9}	TPS (Note 2)
Differential Gain Error, DG	NTSC 40IRE Mod. Ramp, F_C = 75MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Maximum Conversion Rate, F_C	Error Rate of 10^{-9} TPS (Note 2)	75	-	-	MSPS
Aperture Jitter, T_{AJ}		-	10	-	ps
Sampling Delay, T_{DS}		-	3.0	-	ns
ANALOG INPUT					
Input Bandwidth	V_{IN} = $2V_{P-P}$, Input frequency at -3dB	150	-	-	MHz
Analog Input Capacitance, C_{IN}	V_{IN} = 1V + $0.07V_{RMS}$	-	17	-	pF
Analog Input Resistance, R_{IN}		-	390	-	kΩ
Input Bias Current, I_{IN}	V_{IN} = -1V	-	-	200	µA
REFERENCE INPUTS					
Reference Resistance, R_{REF}		75	110	155	Ω
Offset Voltage					
E_{OT} V_{RT}		8	18	32	mV
E_{OB} V_{RB}		0	10	24	mV

Electrical Specifications T_A = +25°C, AV_{EE} = DV_{EE} = -5.2V, V_{RT} = 0V, V_{RB} = -2V (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS					
Logic H Level, V_{IH}		-1.13	-	-	V
Logic L Level, V_{IL}		-	-	-1.50	V
Logic H Current, I_{IH}	-0.8V is Applied to Input	0	-	50	µA
Logic L Current, I_{IL}	-1.6V is Applied to Input	-50	-	50	µA
Input Capacitance		-	7	-	pF
DIGITAL OUTPUTS					
Logic H Level, V_{OH}	R_L = 620Ω to DV_{EE}	-1.03	-	-	V
Logic L Level, V_{OL}	R_L = 620Ω to DV_{EE}	-	-	-1.62	V
TIMING CHARACTERISTICS					
H Pulse Width of Clock, T_{PW1}		6.6	-	-	ns
L Pulse Width of Clock, T_{PW0}		6.6	-	-	ns
Output Rise Time, T_R	R_L = 620Ω to DV_{EE}, 20% to 80%	-	0.9	-	ns
Output Fall Time, T_F	R_L = 620Ω to DV_{EE}, 20% to 80%	-	2.1	-	ns
Output Delay, T_{OD}		4.0	6.5	9.0	ns
POWER SUPPLY CHARACTERISTICS					
Supply Current, I_{EE}		-150	-104	-	mA
Power Consumption, P_D	Note 3	-	580	-	mW

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. TPS: Times Per Sample.
3. $P_D = I_{EE} \bullet V_{EE} + \frac{(V_{RT}-V_{RB})^2}{R_{REF}}$
4. T_A specified in still air and without heat sink. To extend temperature range, appropriate heat management techniques must be employed.

Timing Diagram

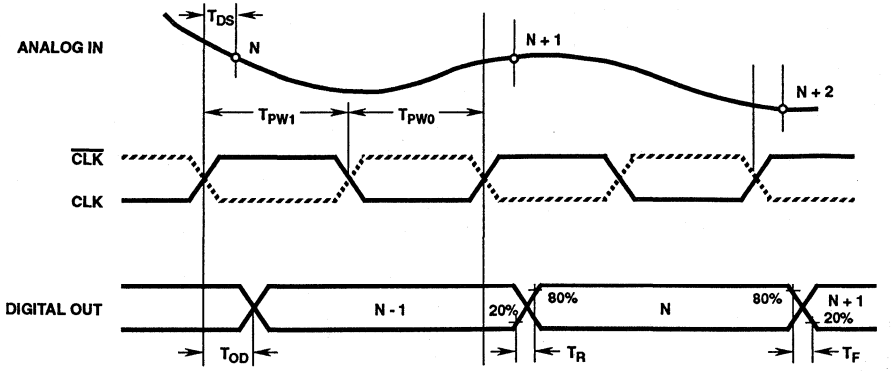
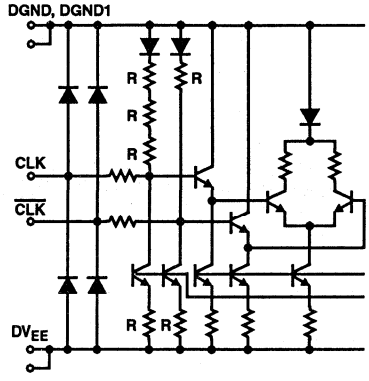
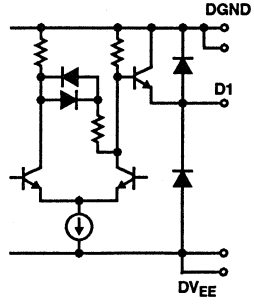
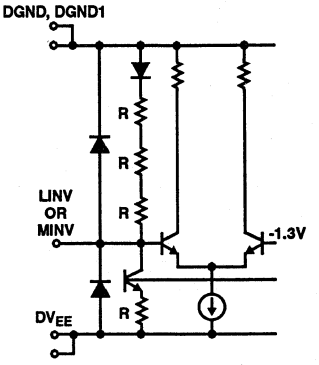
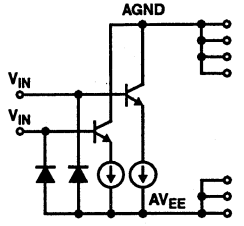
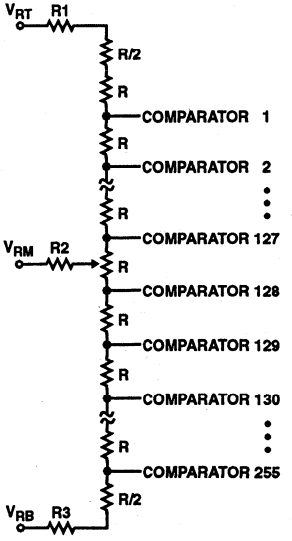


FIGURE 1.

Pin Descriptions and I/O Pin Equivalent Circuit

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
19, 21, 23, 25	31, 33, 35, 37	AGND	-	0V		Analog GND. Used as GND for input buffers and latches of comparators. Isolated from DGND, DGND1, and DGND2.
18, 26, 28	27, 28, 40, 41, 44	AV_{EE}	-	-5.2V		Analog V_{EE} -5.2V (Typ.). Internally connected to DV_{EE} (Resistance: 4Ω to 6Ω). Bypass with 0.1µF to AGND.
16	23	CLK	I	ECL		CLK Input
15	22	$\overline{CLK}$				Input complementary to CLK. When open pulled down to -1.3V. Device is operable without $\overline{CLK}$ input, but use of complementary inputs of CLK and $\overline{CLK}$ is recommended to obtain stable high speed operation.
3, 12	-	DGND	-	0V		Digital GND (used for internal circuits and output transistors).
-	5, 19	DGND1	-	0V		Digital GND (used for internal circuits and output transistors).
-	6, 16	DGND2	-	0V		Digital GND (used for output buffers).
2, 13	4, 20	DV_{EE}	-	-5.2V		Digital V_{EE}. Internally connected to AV_{EE} (resistance: 4Ω to 6Ω). Bypass with 0.1µF to DGND
4	8	D0	O	ECL		LSB of data outputs. External pull-down resistor is required.
5	9	D1				Data outputs. External pull-down resistors are required.
6	10	D2				
7	11	D3				
8	12	D4				
9	13	D5				
10	14	D6				
11	15	D7				MSB of data outputs. External pull-down resistor is required.

Pin Descriptions and I/O Pin Equivalent Circuit (Continued)

PIN NUMBER DIP	PIN NUMBER LCC	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
1	3	LINV	I	ECL		Input pin for D0 (LSB) to D6 output polarity inversion (see A/D Output Code Table). Pulled low when left open.
14	21	MINV	I	ECL		Input pin for D7 (MSB) output polarity inversion (see A/D Output Code Table). Pulled low when left open.
20, 24	32, 36	V_{IN}	I	V_{RT} to V_{RB}		Analog input pins. These two pins must be connected externally, since they are not internally connected. See Application Note for precautions.
17	26	V_{RB}	I	-2V		Reference voltage (bottom). Typically -2V. Bypass with a 0.1µF and 10µF to AGND.
22	34	V_{RM}	I	$V_{RB}/2$		Reference voltage mid point. Can be used as a pin for integral linearity compensation.
27	42	V_{RT}	I	0V		Reference voltage (top) typically 0V.

A/D OUTPUT CODE TABLE

V_{IN} (Note 1)	STEP	MINV 1 LINV 1 D7	MINV 1 LINV 1 D0	0 1 D7	0 1 D0	1 0 D7	1 0 D0	0 0 D7	0 0 D0
0V		000•••••00		100•••••00		011•••••11		111•••••11	
	0	000•••••00		100•••••00		011•••••11		111•••••11	
	1	000•••••01		100•••••01		011•••••10		111•••••10	
		⋮		⋮		⋮		⋮	
-1V	127	011•••••11		111•••••11		000•••••00		100•••••00	
	128	100•••••00		000•••••00		111•••••11		011•••••11	
		⋮		⋮		⋮		⋮	
	254	111•••••10		011•••••10		100•••••01		000•••••01	
	255	111•••••11		011•••••11		100•••••00		000•••••00	
-2V		111•••••11		011•••••11		100•••••00		000•••••00	

NOTE:

1. V_{RT} = 0V, V_{RB} = -2V

Test Circuits

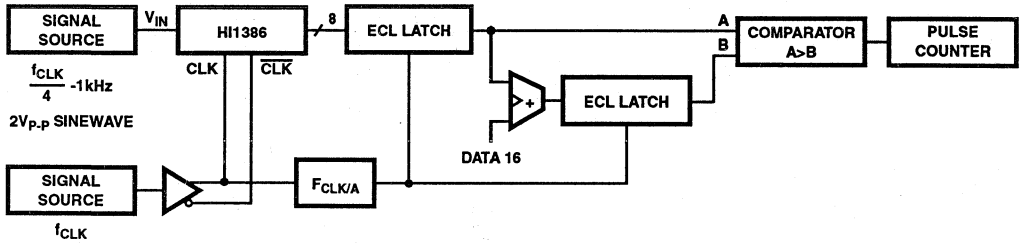


FIGURE 2. MAXIMUM CONVERSION RATE TEST CIRCUIT

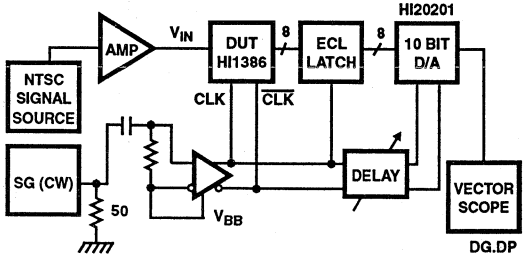


FIGURE 3. DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

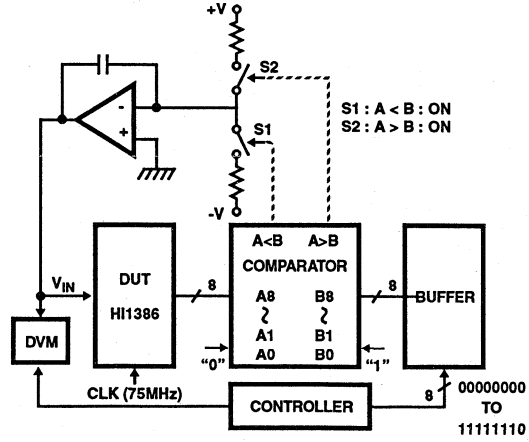


FIGURE 4. INTEGRAL AND DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits (Continued)

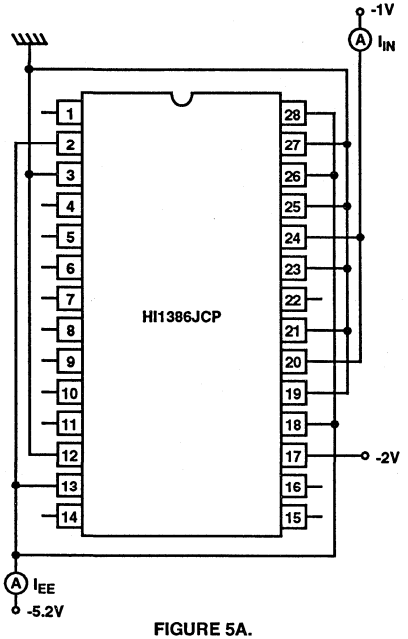


FIGURE 5A.

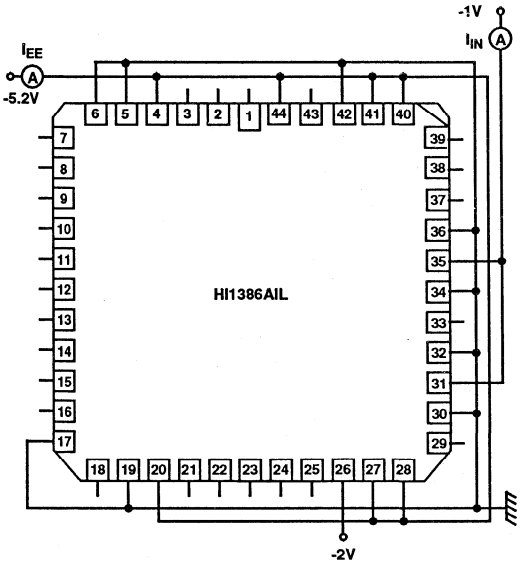


FIGURE 5B.

FIGURE 5. ANALOG INPUT BIAS AND POWER SUPPLY CURRENT TEST CIRCUITS

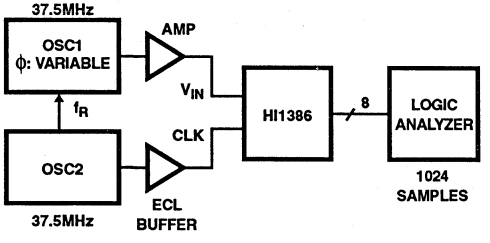
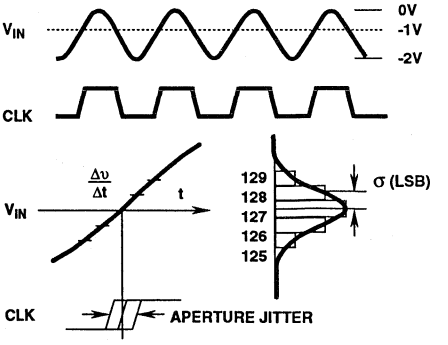


FIGURE 6A.



Aperture jitter is defined as follows:

$$T_{AJ} = \sigma / \frac{\Delta v}{\Delta t} = \sigma / \left(\frac{256}{2} \times 2\pi f\right)$$

FIGURE 6B. APERTURE JITTER TEST METHOD

Where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

FIGURE 6. SAMPLING DELAY AND APERTURE JITTER TEST CIRCUIT

HARRIS SEMICONDUCTOR

HI1396

December 1993

8-Bit, 125MSPS Flash A/D Converter

Features

- Differential Linearity Error ±0.5 LSB (Typ.) or Less
- Integral Linearity Error ±0.5 LSB (Typ.) or Less
- Built-In Integral Linearity Compensation Circuit
- Ultra High Speed Operation with Maximum Conversion Rate of 125MSPS (Min.)
- Low Input Capacitance 18pF (Typ.)
- Wide Analog Input Bandwidth 200MHz (Min. for Full-Scale Input)
- Single Power Supply -5.2V
- Low Power Consumption 870mW (Typ.)
- Low Error Rate
- Operable at 50% Clock Duty Cycle
- Capable of Driving 50Ω Loads
- Evaluation Board Available

Applications

- Video Digitizing
- HDTV (High Definition TV)
- Direct RF Down-Conversion
- Communication Systems
- Radar Systems
- Digital Oscilloscopes

Description

The HI1396 is an 8-bit ultra high speed flash analog-to-digital converter IC capable of digitizing analog signals at the maximum rate of 125MSPS. The digital I/O levels of the converter are compatible with ECL 100K/10KH/10K.

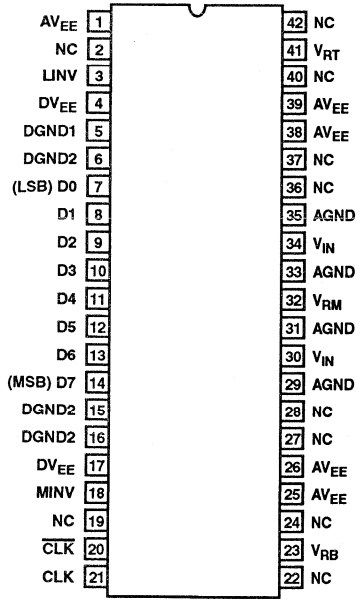
The HI1396 is available in the Commercial and Industrial temperature ranges and is supplied in a 68 lead ceramic LCC, 42 lead ceramic DIP and plastic DIP packages.

Ordering Information

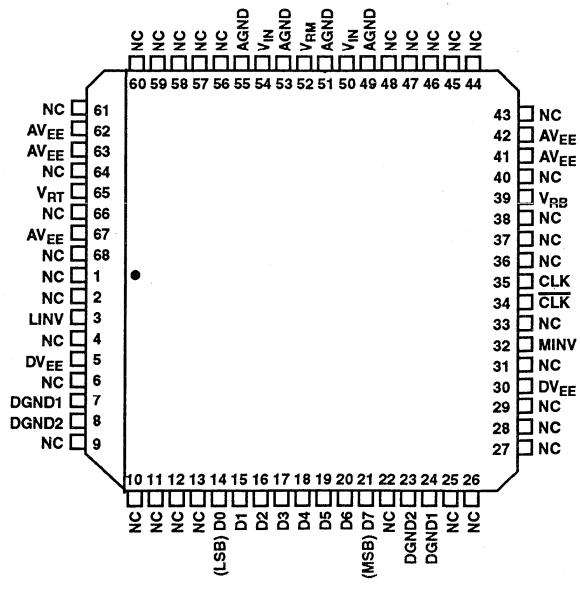
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1396JCJ	-20°C to +75°C	42 Lead Ceramic DIP
HI1396AIL	-20°C to +100°C	68 Lead Ceramic LCC
HI1396JCP	-20°C to +75°C	42 Lead Plastic DIP

Pinouts

HI1396 (CDIP, PDIP)
TOP VIEW



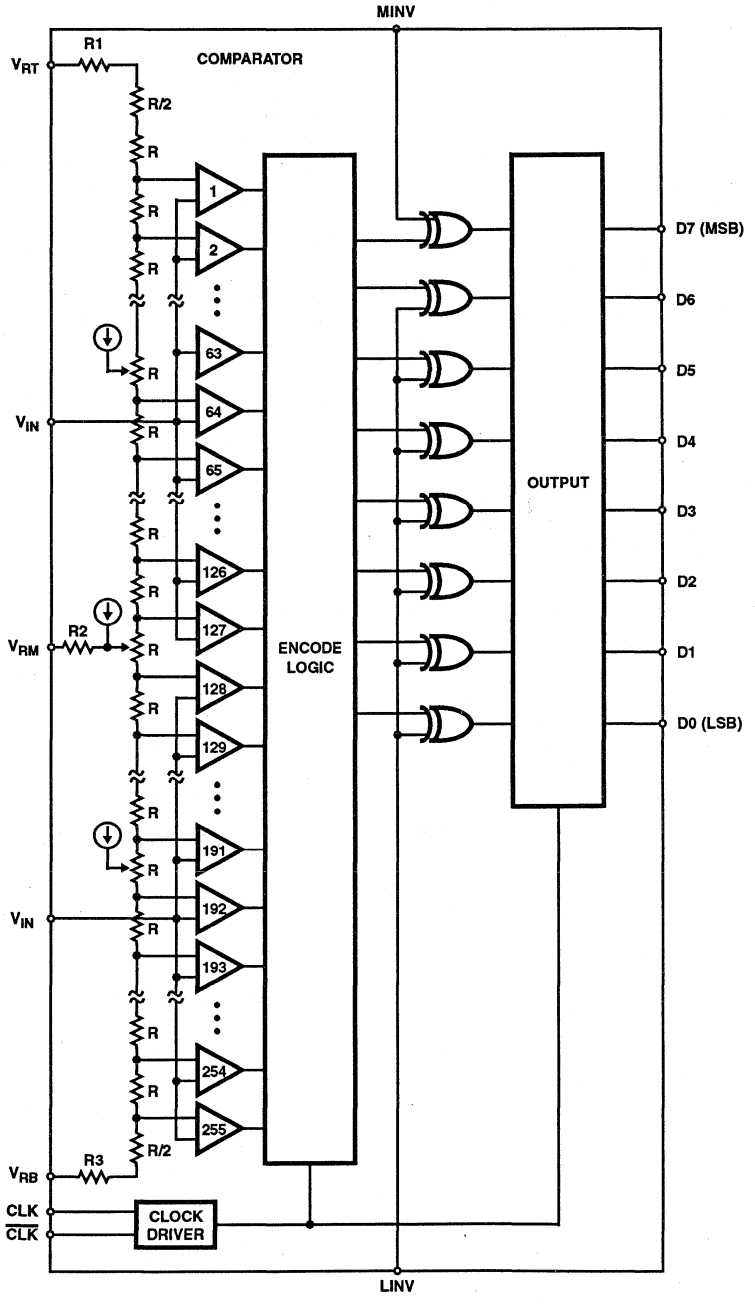
HI1396 (LCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3576.1

Functional Block Diagram



Absolute Maximum Ratings $T_A = +25°C$

Supply Voltage (AV_{EE}, DV_{EE}) . . . . . -7V
Analog Input Voltage (V_{IN}) . . . . . -2.7V to +0.5V
Reference Input Voltage
  V_{RT}, V_{RB}, V_{RM} . . . . . -2.7V to +0.5V
  $|V_{RT}-V_{RB}|$ 2.5V
Digital Input Voltage
  CLK, $\overline{CLK}$, MINV, LINV . . . . . -4V to +0.5V
  $|CLK-\overline{CLK}|$ 2.7V
V_{RM} Pin Input Current (I_{VRM}) . . . . . -3mA to +3mA
Digital Output Current (ID0 to ID7) . . . . . -30mA to 0mA
Storage Temperature Range (T_{STG}) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
HI1396JCP	52°C/W	-
HI1396JCJ	36°C/W	12°C/W
HI1396AIL	38°C/W	10°C/W

Maximum Power Dissipation
  Ceramic Package 1.61W
  Plastic Package 1.44W
Operating Temperature (Note 4)
  HI1396JCP, T_A . . . . . -20°C to +75°C
  HI1396JCJ, T_A . . . . . -20°C to +75°C
  HI1396AIL, T_C . . . . . -20°C to +100°C
Maximum Junction Temperature
  HI1396JCP . . . . . +150°C
  HI1396JCJ, HI1396AIL . . . . . +175°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions (Note 1)

Supply Voltage
  AV_{EE}, DV_{EE} . . . . . -5.5V to -4.95V
  AV_{EE}-DV_{EE} . . . . . -0.05V to 0.05V
  AGND-DGND . . . . . -0.05V to 0.05V
Reference Input Voltage
  V_{RT} . . . . . -0.1V to 0.1V
  V_{RB} . . . . . -2.2V to -1.8V
Analog Input Voltage, V_{IN} . . . . . V_{RB} to V_{RT}
Pulse Width of Clock
  TPW1 . . . . . 4.0ns Min.
  TPW0 . . . . . 4.0ns Min.

Electrical Specifications $T_A = +25°C$, $AV_{EE} = DV_{EE} = -5.2V$, $V_{RT} = 0V$, $V_{RB} = -2V$ (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Resolution		8	-	-	Bits
Integral Linearity Error, (INL)					
HI1396JCJ, HI1396AIL	F_C = 125MHz	-	-	±0.5	LSB
HI1396JCP		-	-	±0.8	LSB
Differential Linearity Error, (DNL)					
HI1396JCJ, HI1396AIL	F_C = 125MHz	-	-	±0.5	LSB
HI1396JCP		-	-	±0.7	LSB
ANALOG INPUT					
Input Bandwidth	$V_{IN} = 2V_{P-P}$	200	-	-	MHz
Analog Input Capacitance, C_{IN}	$V_{IN} = 1V + 0.07V_{RMS}$	-	18	-	pF
Analog Input Resistance, R_{IN}		50	190	-	kΩ
Input Bias Current, I_{IN}	V_{IN} = -1V	20	130	400	µA
REFERENCE INPUTS					
Reference Resistance, R_{REF}		75	110	155	Ω
Offset Voltage					
E_{OT} V_{RT}		8	19	32	mV
E_{OB} V_{RB}		0	9	24	mV

Electrical Specifications T_A = +25°C, AV_{EE} = DV_{EE} = -5.2V, V_{RT} = 0V, V_{RB} = -2V (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUTS					
Logic H Level, V_{IH}		-1.13	-	-	V
Logic L Level, V_{IL}		-	-	-1.50	V
Logic H Current, I_{IH}	Input Connected to -0.8V	0	-	50	µA
Logic L Current, I_{IL}	Input Connected to -1.6V	0	-	50	µA
Input Capacitance		-	7	-	pF
DIGITAL OUTPUTS					
Logic H Level, V_{OH}	R_L = 50Ω to -2V	-1.10	-	-	V
Logic L Level, V_{OL}	R_L = 50Ω to -2V	-	-	-1.62	V
TIMING CHARACTERISTICS					
Output Rise Time, T_R	R_L = 50Ω to -2V, 20% to 80%	0.5	0.9	1.2	ns
Output Fall Time, T_F	R_L = 50Ω to -2V, 20% to 80%	0.5	1.0	1.3	ns
Output Delay, T_{OD}		3.0	3.6	4.2	ns
H Pulse Width of Clock, T_{PW1}		4.0	-	-	ns
L Pulse Width of Clock, T_{PW0}		4.0	-	-	ns
DYNAMIC CHARACTERISTICS					
Maximum Conversion Rate, F_C	Error Rate 10^{-9} TPS (Note 2)	125	-	-	MSPS
Aperture Jitter, T_{AJ}		-	10	-	ps
Sampling Delay, T_{DS}		-	1.5	-	ns
Signal to Noise Ratio (SINAD) = $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	Input = 1MHz, Full Scale, F_C = 125MHz	-	46	-	dB
	Input = 31.5MHz, Full Scale, F_C = 125MHz	-	40	-	dB
Error Rate	Input = 31.249MHz, Full Scale, Error > 16 LSB, F_C = 125MHz	-	-	10^{-9}	TPS (Note 2)
Differential Gain Error, DG	NTSC 40IRE Mod. Ramp, F_C = 125MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
POWER SUPPLY CHARACTERISTICS					
Supply Current, I_{EE}		-230	-160	-	mA
Power Consumption	Note 3	-	870	-	mW

NOTES:

1. Electrical Specifications guaranteed within stated operating conditions.
2. TPS: Times Per Sample.
3. $P_D = I_{EE} \bullet V_{EE} + \frac{(V_{RT} - V_{RB})^2}{R_{REF}}$
4. T_A specified in still air and without heat sink. To extend temperature range, appropriate heat management techniques must be employed.

Timing Diagram

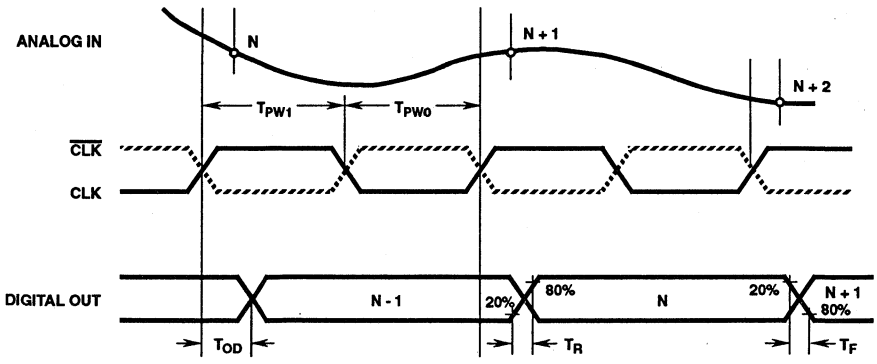
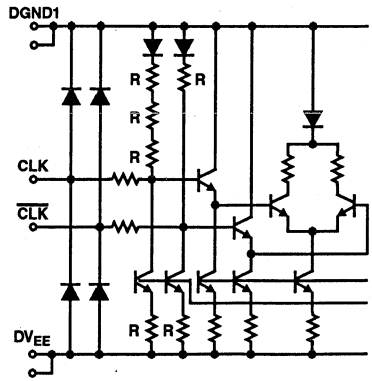
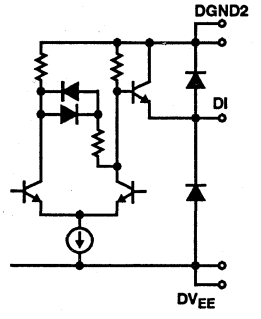
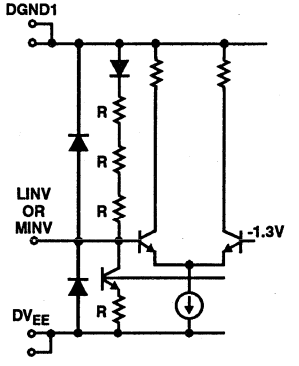
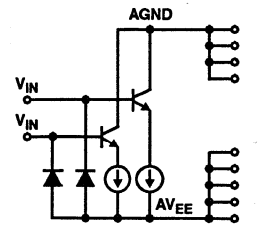


FIGURE 1.

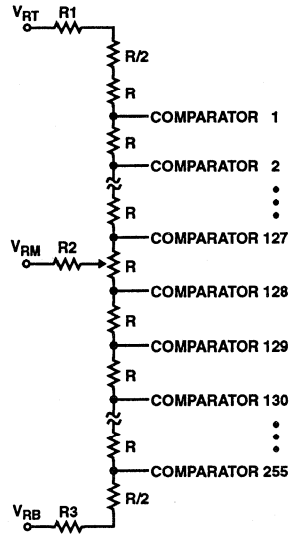
Pin Descriptions and I/O Pin Equivalent Circuit

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
29, 31, 33, 35	49, 51, 53, 55	AGND	-	0V		Analog GND. Used as GND for input buffers and latches of comparators. Isolated from DGND1, DGND2.
1, 25, 26, 38, 39	41, 42, 62, 63, 67	AV_{EE}	-	-5.2V		Analog V_{EE} -5.2V (Typ.). Internally connected to DV_{EE} (Resistance: 4Ω to 6Ω). Bypass with 0.1µF to AGND.
21	35	CLK	I	ECL		CLK Input
20	34	$\overline{CLK}$				Input complementary to CLK. When left open pulled down to -1.3V. Device is operable without $\overline{CLK}$ input, but use of complementary inputs of CLK and $\overline{CLK}$ is recommended to obtain stable high speed operation.

Pin Descriptions and I/O Pin Equivalent Circuit (Continued)

PIN NUMBER		SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
DIP	LCC					
5, 16	7, 24	DGND1	-	0V		Digital GND for internal circuits.
6, 15	8, 23	DGND2	-	0V		Digital GND for output transistors.
4, 17	5, 30	DV_{EE}	-	-5.2V		Digital V_{EE}. Internally connected to AV_{EE} (resistance: 4Ω to 6Ω). Bypass with 0.1µF to DGND
7	14	D0	O	ECL		LSB of data outputs. External pull-down resistor is required.
8	15	D1				Data outputs. External pull-down resistors are required.
9	16	D2				
10	17	D3				
11	18	D4				
12	19	D5				
13	20	D6				
14	21	D7				MSB of data outputs. External pull-down resistor is required.
3	3	LINV	I	ECL		Input pin for D0 (LSB) to D6 output polarity inversion (see A/D Output Code Table). Pulled low when left open.
18	32	MINV	I	ECL		Input pin for D7 (MSB) output polarity inversion (see A/D Output Code Table). Pulled low when left open.
30, 34	50, 54	V_{IN}	I	V_{RT} to V_{RB}		Analog input pins. These two pins must be connected externally, since they are not internally connected.

Pin Descriptions and I/O Pin Equivalent Circuit (Continued)

PIN NUMBER DIP	PIN NUMBER LCC	SYMBOL	I/O	STANDARD VOLTAGE LEVEL	EQUIVALENT CIRCUIT	DESCRIPTION
23	39	V_{RB}	I	-2V		Reference voltage (bottom). Typically -2V. Bypass with a 0.1µF and 10µF to AGND.
32	52	V_{RM}	I	$V_{RB}/2$		Reference voltage mid point. Can be used as a pin for integral linearity compensation. Reference voltage (top) typically 0V. When a voltage different from AGND is applied to this pin, bypass with a 0.1µF and 10µF to AGND.
41	65	V_{RT}	I	0V		
2, 19, 22, 24, 27, 28, 36, 37, 40, 42	1, 2, 4, 6, 9-13, 25-29, 31, 33, 36-38, 40, 43-48, 56-61, 64, 66, 68	NC	-	-		Unused pins. No internal connections have been made to these pins. Connecting them to AGND or DGND on PC board is recommended.

A/D OUTPUT CODE TABLE

V_{IN} (Note 1)	STEP	MINV 1, LINV 1 D7	MINV 1, LINV 1 D0	0, 1 D7	0, 1 D0	1, 0 D7	1, 0 D0	0, 0 D7	0, 0 D0
0V		000 • • • • •	00	100 • • • • •	00	011 • • • • •	11	111 • • • • •	11
	0	000 • • • • •	00	100 • • • • •	00	011 • • • • •	11	111 • • • • •	11
	1	000 • • • • •	01	100 • • • • •	01	011 • • • • •	10	111 • • • • •	10
		•		•		•		•	
		•		•		•		•	
		•		•		•		•	
-1V	127	011 • • • • •	11	111 • • • • •	11	000 • • • • •	00	100 • • • • •	00
	128	100 • • • • •	00	000 • • • • •	00	111 • • • • •	11	011 • • • • •	11
		•		•		•		•	
		•		•		•		•	
		•		•		•		•	
	254	111 • • • • •	10	011 • • • • •	10	100 • • • • •	01	000 • • • • •	01
	255	111 • • • • •	11	011 • • • • •	11	100 • • • • •	00	000 • • • • •	00
-2V		111 • • • • •	11	011 • • • • •	11	100 • • • • •	00	000 • • • • •	00

NOTE:
1. V_{RT} = 0V, V_{RB} = -2V.

Test Circuits

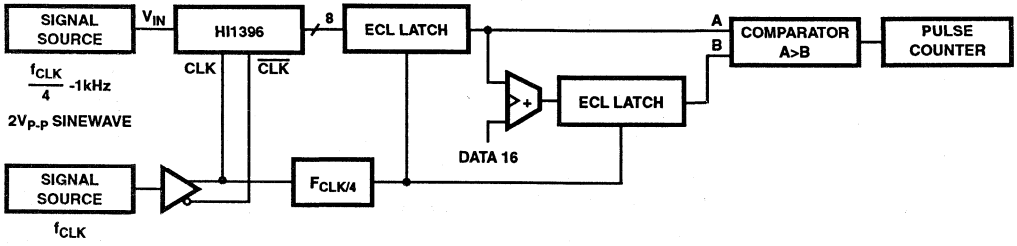


FIGURE 2. MAXIMUM CONVERSION RATE TEST CIRCUIT

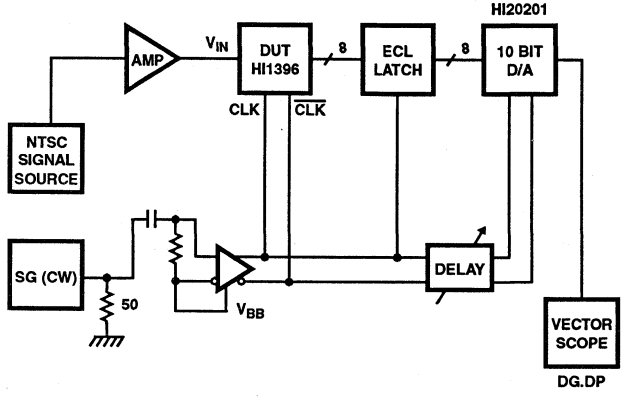


FIGURE 3. DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

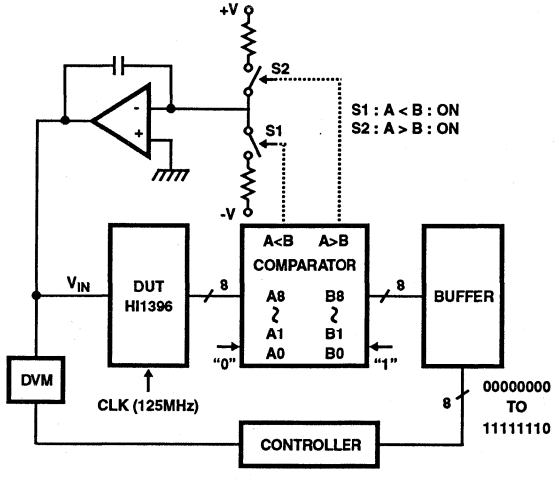


FIGURE 4. INTEGRAL AND DIFFERENTIAL LINEARITY ERROR TEST CIRCUIT

Test Circuits (Continued)

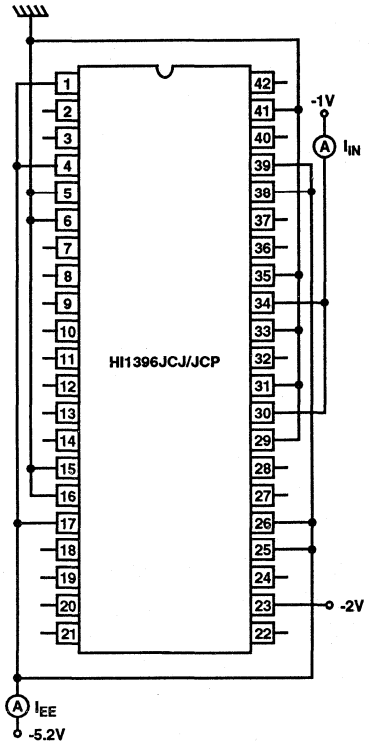


FIGURE 5A.

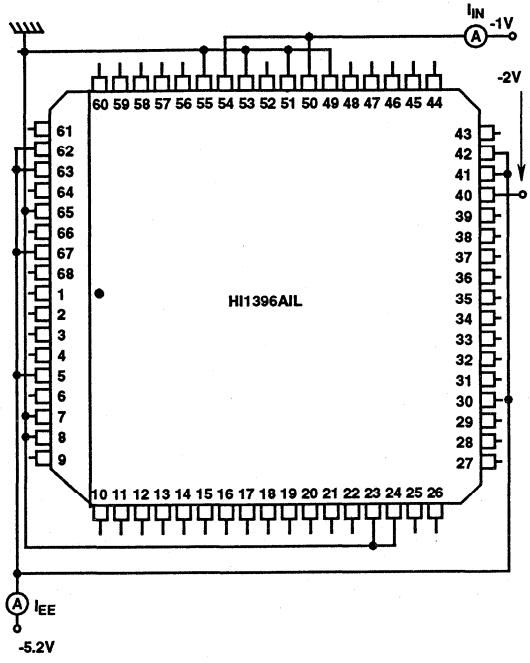


FIGURE 5B.

FIGURE 5. ANALOG INPUT BIAS AND POWER SUPPLY CURRENT TEST CIRCUITS

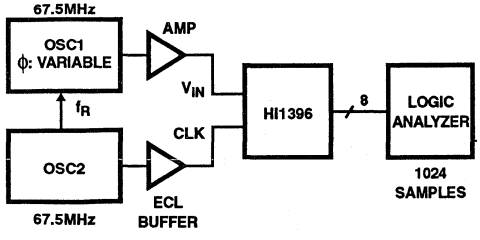
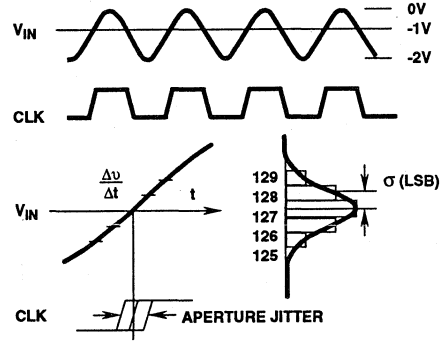


FIGURE 6A.



Aperture jitter is defined as follows:

$$T_{AJ} = \sigma / \frac{\Delta v}{\Delta t} = \sigma / (\frac{256}{2} \times 2\pi f)$$

FIGURE 6B. APERTURE JITTER TEST METHOD

Where σ (unit: LSB) is the deviation of the output codes when the input frequency is exactly the same as the clock and is sampled at the largest slew rate point.

FIGURE 6. SAMPLING DELAY AND APERTURE JITTER TEST CIRCUIT

HARRIS SEMICONDUCTOR

HI-5700

December 1993

8-Bit, 20MSPS Flash A/D Converter

Features

- 20MSPS with No Missing Codes
- 18MHz Full Power Input Bandwidth
- No Missing Codes Over Temperature
- Sample and Hold Not Required
- Single +5V Supply Voltage
- CMOS/TTL
- Overflow Bit
- Improved Replacement for MP7684
- Evaluation Board Available
- /883 Version Available

Applications

- Video Digitizing
- Radar Systems
- Medical Imaging
- Communication Systems
- High Speed Data Acquisition Systems

Description

The HI-5700 is a monolithic, 8 bit, CMOS Flash Analog-to-Digital Converter. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 20MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5700 delivers ±0.5 LSB differential nonlinearity while consuming only 725mW (typical) at 20MSPS. Microprocessor compatible data output latches are provided which present valid data to the output bus 1.5 clock cycles after the convert command is received. An overflow bit is provided to allow the series connection of two converters to achieve 9 bit resolution.

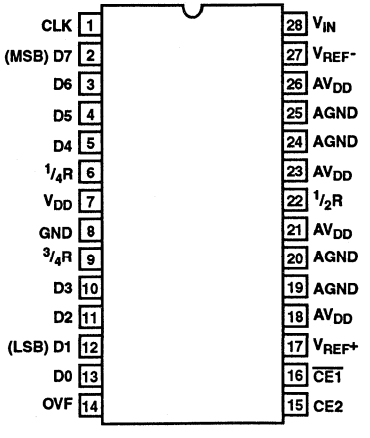
The HI-5700 is available in Commercial and Industrial temperature ranges and is supplied in 28 lead Plastic DIP and SOIC packages.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-5700J-5	0°C to +70°C	28 Lead Plastic DIP
HI9P5700J-5	0°C to +70°C	28 Lead SOIC
HI3-5700A-9	-40°C to +85°C	28 Lead Plastic DIP
HI9P5700A-9	-40°C to +85°C	28 Lead SOIC

Pinout

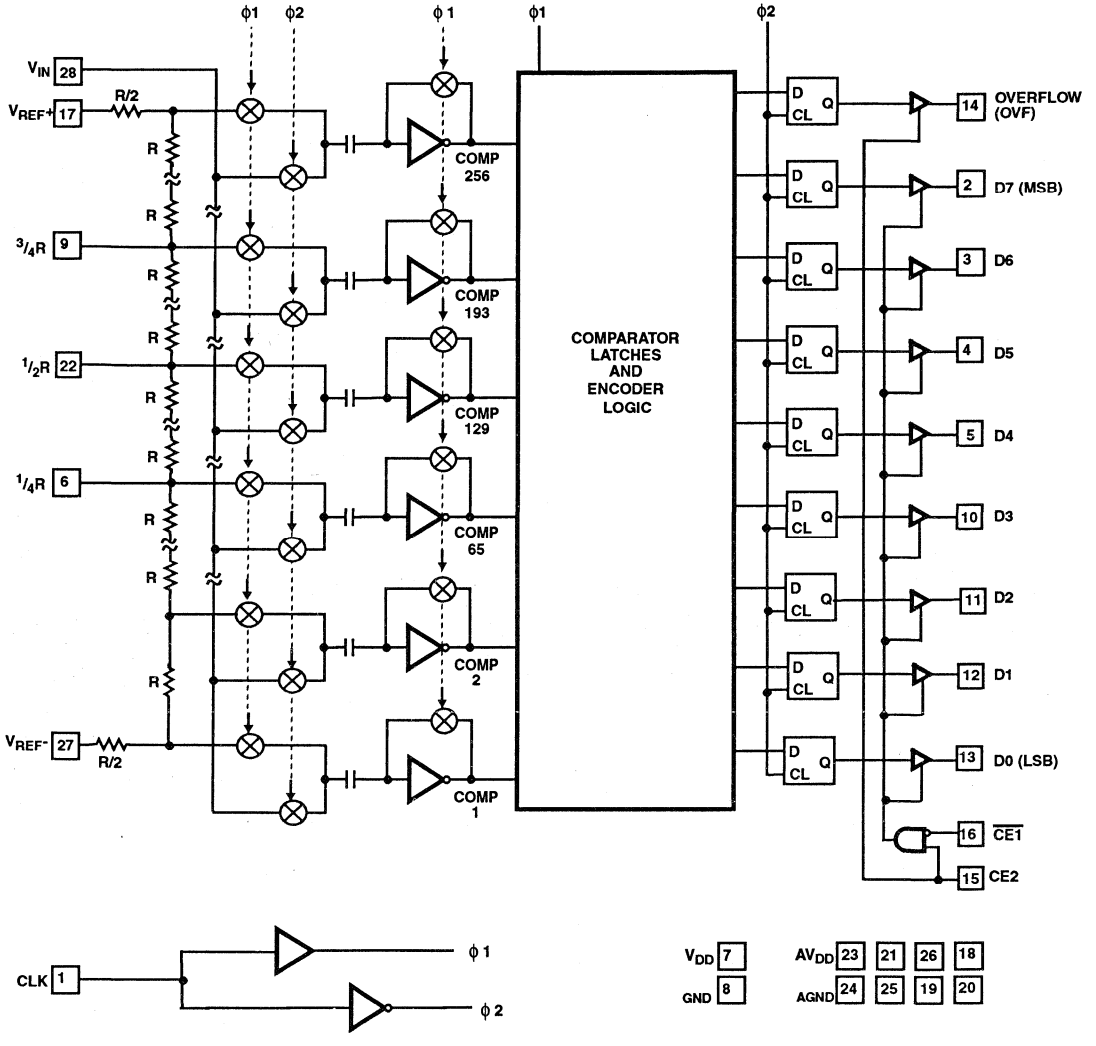
HI-5700
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3174.3

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{DD} to GND ..... (GND - 0.5) < V_{DD} < +7.0V
Analog and Reference Input Pins.... (V_{SS} - 0.5) < V_{INA} < (V_{DD} +0.5V)
Digital I/O Pins ..... (GND - 0.5) < $V_{I/O}$ < (V_{DD} +0.5V)
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... 300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
HI3-5700J-5, HI3-5700A-9	55°C/W	-
HI9P5700J-5, HI9P5700A-9	75°C/W	-

Maximum Power Dissipation +70°C 1.05W
Operating Temperature Range
HI3-5700J-5, HI9P5700J-5 ..... 0°C to +70°C
HI3-5700A-9, HI9P5700A-9 ..... -40°C to +85°C
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Electrical Specifications

$AV_{DD} = V_{DD} = +5.0V$; $V_{REF+} = +4.0V$; $V_{REF-} = GND = AGND = 0V$; F_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified.

PARAMETER	TEST CONDITION	+25°C			(NOTE 2) 0°C to +70°C -40°C to +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
SYSTEM PERFORMANCE							
Resolution		8			8		Bits
Integral Linearity Error (INL) (Best Fit Method)	F_S = 15MHz, f_{IN} = DC F_S = 20MHz, f_{IN} = DC		±0.9 ±1.0	±2.0 ±2.25		±2.25 ±3.25	LSB LSB
Differential Linearity Error (DNL) (Guaranteed No Missing Codes)	F_S = 15MHz, f_{IN} = DC F_S = 20MHz, f_{IN} = DC		±0.4 ±0.5	±0.9 ±0.9		±1.0 ±1.0	LSB LSB
Offset Error (VOS)	F_S = 15MHz, f_{IN} = DC F_S = 20MHz, f_{IN} = DC		±5.0 ±5.0	±8.0 ±8.0		±9.5 ±9.5	LSB LSB
Full Scale Error (FSE)	F_S = 15MHz, f_{IN} = DC F_S = 20MHz, f_{IN} = DC		±0.5 ±0.6	±4.5 ±4.5		±8.0 ±8.0	LSB LSB
DYNAMIC CHARACTERISTICS							
Maximum Conversion Rate	No Missing Codes	20	25		20		MSPS
Minimum Conversion Rate	No Missing Codes (Note 2)			0.125		0.125	MSPS
Full Power Input Bandwidth	F_S = 20MHz		18				MHz
Signal to Noise Ratio (SNR) = RMS Signal / RMS Noise	F_S = 15MHz, f_{IN} = 100kHz F_S = 15MHz, f_{IN} = 3.58MHz F_S = 15MHz, f_{IN} = 4.43MHz F_S = 20MHz, f_{IN} = 100kHz F_S = 20MHz, f_{IN} = 3.58MHz F_S = 20MHz, f_{IN} = 4.43MHz		46.5 44.0 43.4 45.9 42.0 41.6				dB dB dB dB dB dB
Signal to Noise Ratio (SINAD) = RMS Signal / RMS Noise + Distortion	F_S = 15MHz, f_{IN} = 100kHz F_S = 15MHz, f_{IN} = 3.58MHz F_S = 15MHz, f_{IN} = 4.43MHz F_S = 20MHz, f_{IN} = 100kHz F_S = 20MHz, f_{IN} = 3.58MHz F_S = 20MHz, f_{IN} = 4.43MHz		43.4 34.3 32.3 42.3 35.2 32.8				dB dB dB dB dB dB
Total Harmonic Distortion	F_S = 15MHz, f_{IN} = 100kHz F_S = 15MHz, f_{IN} = 3.58MHz F_S = 15MHz, f_{IN} = 4.43MHz F_S = 20MHz, f_{IN} = 100kHz F_S = 20MHz, f_{IN} = 3.58MHz F_S = 20MHz, f_{IN} = 4.43MHz		-46.9 -34.8 -32.8 -46.6 -36.6 -33.5				dBc dBc dBc dBc dBc dBc
Differential Gain	F_S = 14MHz, f_{IN} = 3.58MHz		3.5				%
Differential Phase Error	F_S = 14MHz, f_{IN} = 3.58MHz		0.9				Degree

Electrical Specifications $AV_{DD} = V_{DD} = +5.0V$; $V_{REF+} = +4.0V$; $V_{REF-} = GND = AGND = 0V$; F_S = Specified Clock Frequency at 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITION	+25°C MIN	+25°C TYP	+25°C MAX	(NOTE 2) 0°C to +70°C -40°C to +85°C MIN	(NOTE 2) 0°C to +70°C -40°C to +85°C MAX	UNITS
ANALOG INPUTS							
Analog Input Resistance, R_{IN}	$V_{IN} = 4V$	4	10				MΩ
Analog Input Capacitance, C_{IN}	$V_{IN} = 0V$		60				pF
Analog Input Bias Current, IB	$V_{IN} = 0V, 4V$		±0.01	±1.0		±1.0	µA
REFERENCE INPUTS							
Total Reference Resistance, R_L		250	330		235		Ω
Reference Resistance Tempco, T_C			+0.31				Ω/°C
DIGITAL INPUTS							
Input Logic High Voltage, V_{IH}		2.0			2.0		V
Input Logic Low Voltage, V_{IL}				0.8		0.8	V
Input Logic High Current, I_{IH}	$V_{IN} = 5V$			1.0		1.0	µA
Input Logic Low Current, I_{IL}	$V_{IN} = 0V$			1.0		1.0	µA
Input Capacitance, C_{IN}			7				pF
DIGITAL OUTPUTS							
Output Logic Sink Current, I_{OL}	$V_O = 0.4V$	3.2			3.2		mA
Output Logic Source Current, I_{OH}	$V_O = 4.5V$	-3.2			-3.2		mA
Output Leakage, I_{OZ}	$CE2 = 0V, V_O = 0V, 5V$			±1.0		±1.0	µA
Output Capacitance, C_{OUT}	$CE2 = 0V$		5.0				pF
TIMING CHARACTERISTICS							
Aperture Delay, t_{AP}			6				ns
Aperture Jitter, t_{AJ}			30				ps
Data Output Enable Time, t_{EN}			18	25		30	ns
Data Output Disable Time, t_{DIS}			15	20		25	ns
Data Output Delay, t_{OD}			20	25		30	ns
Data Output Hold, t_H		10	20		5		ns
POWER SUPPLY REJECTION							
Offset Error PSRR, ΔVOS	$V_{DD} = 5V \pm 10\%$		±0.1	±2.75		±5.0	LSB
Gain Error PSRR, ΔFSE	$V_{DD} = 5V \pm 10\%$		±0.1	±2.75		±5.0	LSB
POWER SUPPLY CURRENT							
Supply Current, I_{DD}	$F_S = 20MHz$		145	180		190	mA

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Parameter guaranteed by design or characterization and not production tested.

Timing Waveforms

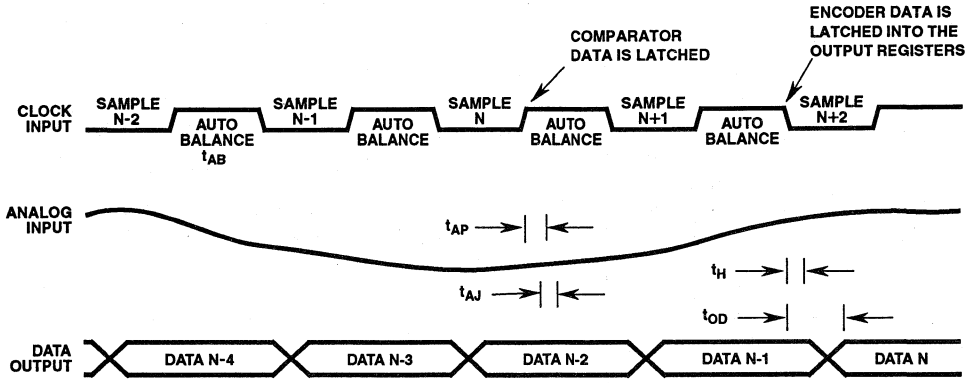


FIGURE 1. INPUT-TO-OUTPUT TIMING

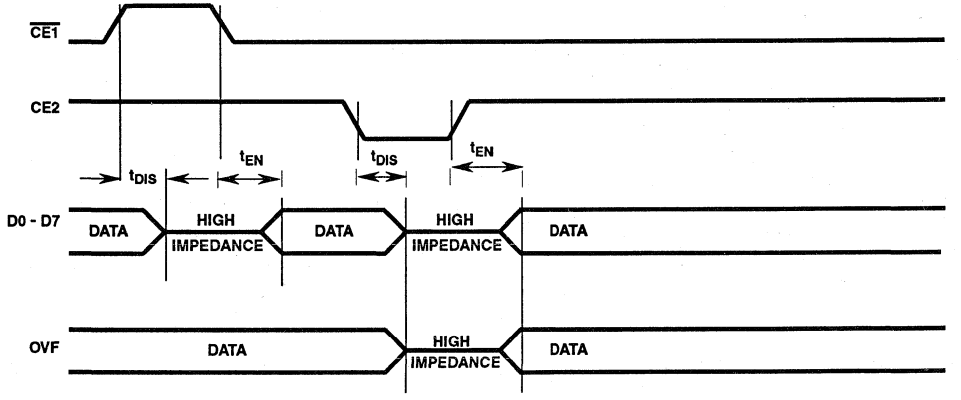


FIGURE 2. OUTPUT ENABLE TIMING

Typical Performance Curves

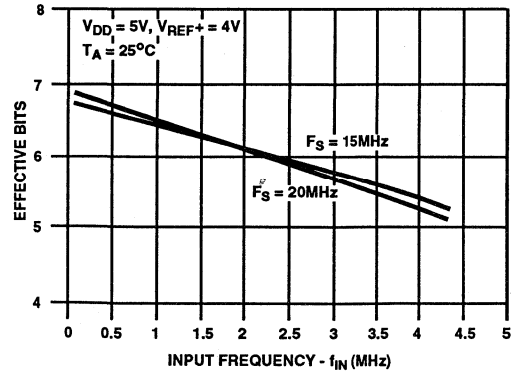


FIGURE 3. EFFECTIVE NUMBER OF BITS vs f_{IN}

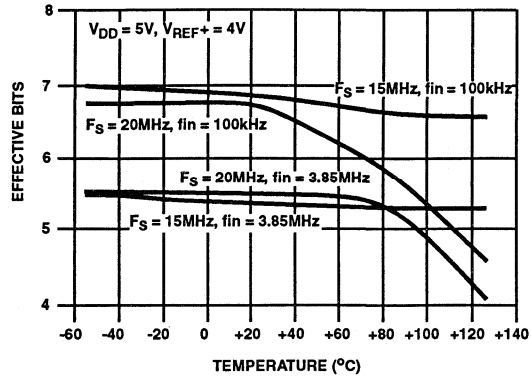


FIGURE 4. EFFECTIVE NUMBER OF BITS vs TEMPERATURE

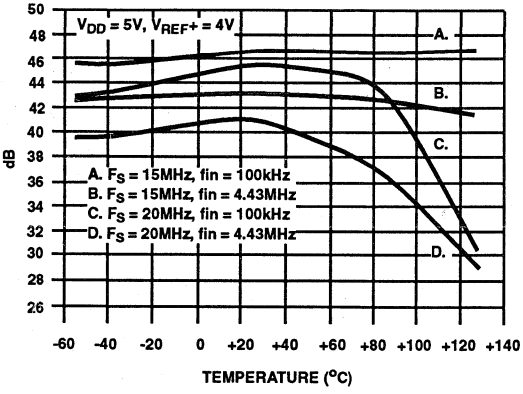


FIGURE 5. SNR vs TEMPERATURE

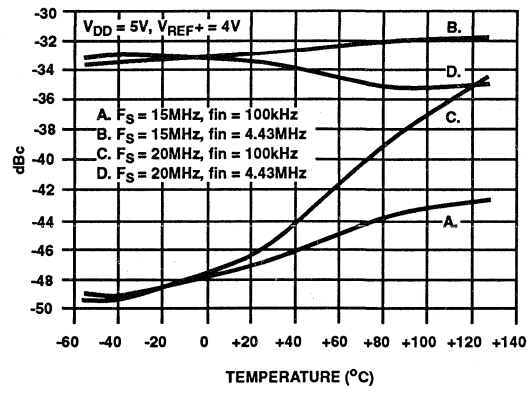


FIGURE 6. TOTAL HARMONIC DISTORTION vs TEMPERATURE

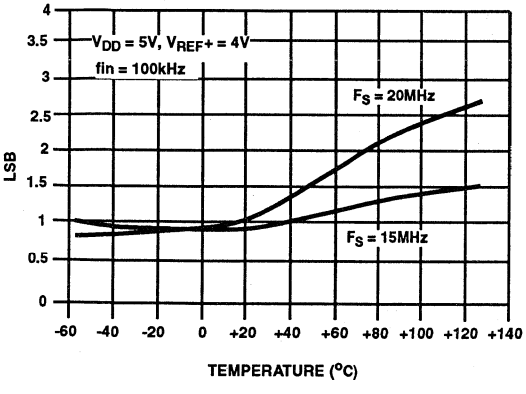


FIGURE 7. INL vs TEMPERATURE

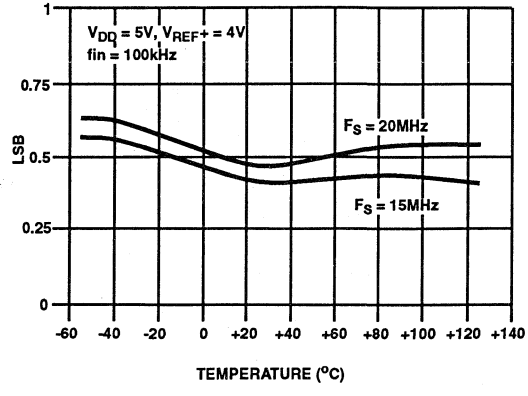


FIGURE 8. DNL vs TEMPERATURE

Typical Performance Curves (Continued)

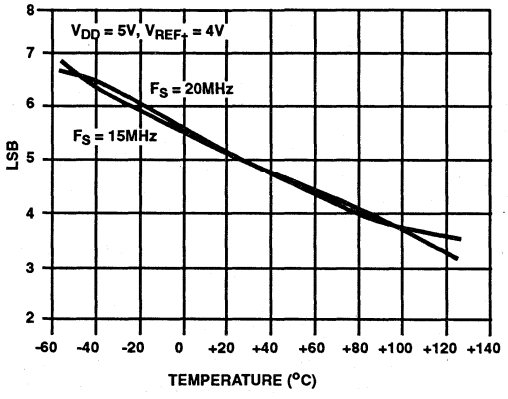


FIGURE 9. OFFSET VOLTAGE vs. TEMPERATURE

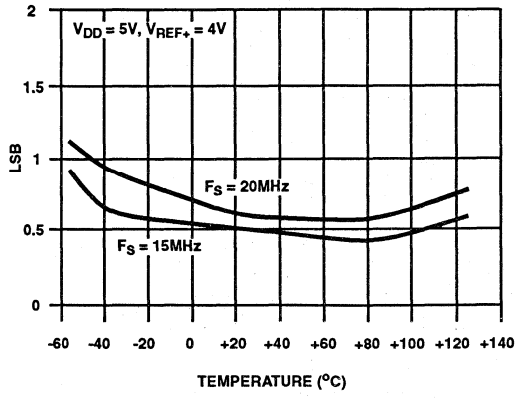


FIGURE 10. FULL SCALE ERROR vs TEMPERATURE

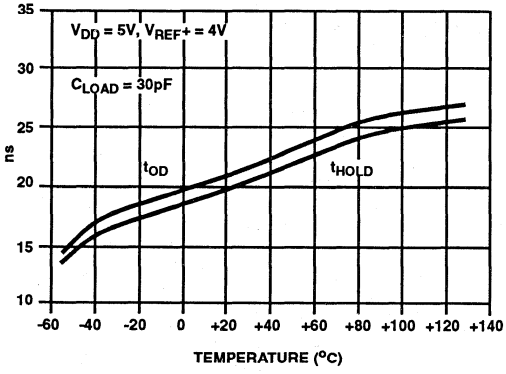


FIGURE 11. OUTPUT DELAY vs TEMPERATURE

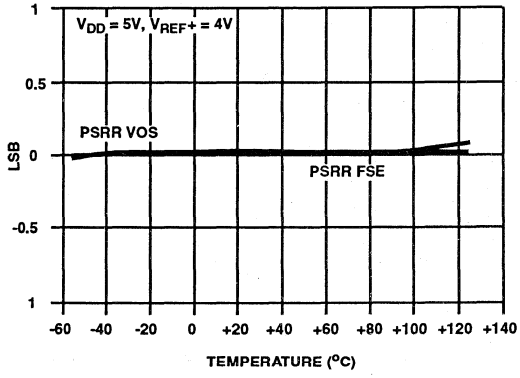


FIGURE 12. POWER SUPPLY REJECTION vs TEMPERATURE

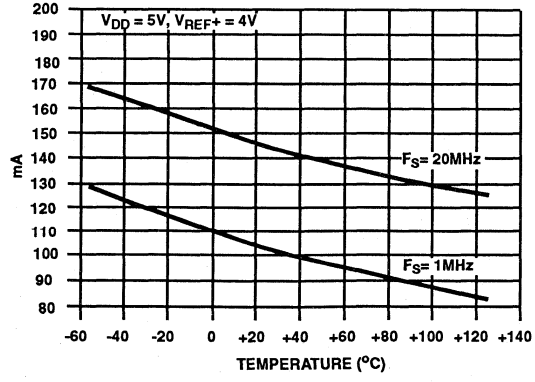


FIGURE 13. SUPPLY CURRENT vs TEMPERATURE

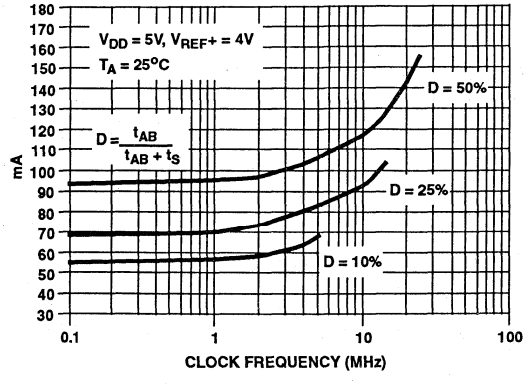


FIGURE 14. SUPPLY CURRENT vs CLOCK & DUTY CYCLE

TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	CLK	Clock Input
2	D7	Bit 7, Output (MSB)
3	D6	Bit 6, Output
4	D5	Bit 5, Output
5	D4	Bit 4, Output
6	$^1/_4$R	$^1/_4$th Point of Reference Ladder
7	V_{DD}	Digital Power Supply
8	GND	Digital Ground
9	$^3/_4$R	$^3/_4$th Point of Reference Ladder
10	D3	Bit 3, Output
11	D2	Bit 2, Output
12	D1	Bit 1, Output
13	D0	Bit 0, Output (LSB)
14	OVF	Overflow, Output
15	CE2	Tri-State Output Enable Input, Active High. (See Table 2)
16	$\overline{CE1}$	Tri-State Output Enable Input, Active Low. (See Table 2)
17	V_{REF}+	Reference Voltage Positive Input
18	AV_{DD}	Analog Power Supply, +5V
19	AGND	Analog Ground
20	AGND	Analog Ground
21	AV_{DD}	Analog Power Supply, +5V
22	$^1/_2$R	$^1/_2$ Point of Reference Ladder
23	AV_{DD}	Analog Power Supply, +5V
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AV_{DD}	Analog Power Supply, +5V
27	V_{REF}-	Reference Voltage Negative Input
28	V_{IN}	Analog Input

TABLE 2. CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	D0 - D7	OVF
0	1	Valid	Valid
1	1	Tri-State	Valid
X	0	Tri-State	Tri-State

X's = Don't Care.

Theory of Operation

The HI-5700 is an 8 bit analog-to-digital converter based on a parallel CMOS "flash" architecture. This flash technique is an extremely fast method of A/D conversion because all bit decisions are made simultaneously. In all, 256 comparators are used in the HI-5700: (2^8-1) comparators to encode the output word, plus an additional comparator to detect an overflow condition.

The CMOS HI-5700 works by alternately switching between a "Sample" mode and an "Auto Balance" mode. Splitting up the comparison process in this CMOS technique offers a number of significant advantages. The offset voltage of each CMOS comparator is dynamically canceled with each conversion cycle such that offset voltage drift is virtually eliminated during operation. The block diagram and timing diagram illustrate how the HI-5700 CMOS flash converter operates.

The input clock which controls the operation of the HI-5700 is first split into a non-inverting ϕ1 clock and an inverting ϕ2 clock. These two clocks, in turn, synchronize all internal timing of analog switches and control logic within the converter.

In the "Auto Balance" mode (ϕ1), all ϕ1 switches close and ϕ2 switches open. The output of each comparator is momentarily tied to its own input, self-biasing the comparator midway between GND and V_{DD} and presenting a low impedance to a small input capacitor. Each capacitor, in turn, is connected to a reference voltage tap from the resistor ladder. The Auto Balance mode quickly precharges all 256 input capacitors between the self-bias voltage and each respective tap voltage.

In the "Sample" mode (ϕ2), all ϕ1 switches open and ϕ2 switches close. This places each comparator in a sensitive high gain amplifier configuration. In this open loop state, the input impedance is very high and any small voltage shift at the input will drive the output either high or low. The ϕ2 state also switches each input capacitor from its reference tap to the input signal. This instantly transfers any voltage difference between the reference tap and input voltage to the comparator input. All 256 comparators are thus driven simultaneously to a defined logic state. For example, if the input voltage is at mid-scale, capacitors precharged near zero during ϕ1 will push comparator inputs higher than the self bias voltage at ϕ2; capacitors precharged near the reference voltage push the respective comparator inputs lower than the bias point. In general, all capacitors precharged by taps above the input voltage force a "low" voltage at comparator inputs; those precharged below the input voltage force "high" inputs at the comparators.

During the next ϕ1 Auto-Balancing state, comparator output data is latched into the encoder logic block and the first stage of encoding takes place. The following ϕ2 state completes the encoding process. The 8 data bits (plus overflow bit) are latched into the output flip-flops at the next falling clock edge. The Overflow bit is set if the input voltage exceeds V_{REF}+ - 0.5 LSB. The output bus may be either enabled or disabled according to the state of $\overline{CE1}$ and CE2 (See Table 2). When disabled, output bits assume a high impedance state.

As shown in the timing diagram, the digital output word becomes valid after the second ϕ1 state. There is thus a one and a half cycle pipeline delay between input sample and digital output. "Data Output Delay" time indicates the slight time delay for data to become valid at the end of the ϕ1 state.

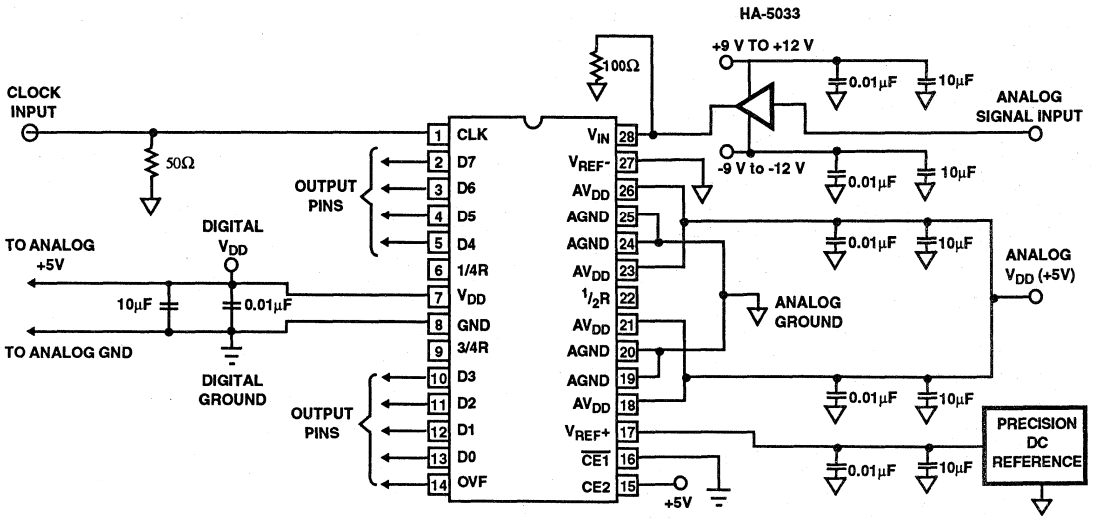


FIGURE 15. TEST CIRCUIT

Applications Information

Voltage Reference

The reference voltage is applied across the resistor ladder between $V_{REF}+$ and $V_{REF}-$. In most applications, $V_{REF}-$ is simply tied to analog ground such that the reference source drives $V_{REF}+$. The reference must be capable of supplying enough current to drive the minimum ladder resistance of 235Ω over temperature.

The HI-5700 is specified for a reference voltage of 4.0V, but will operate with voltages as high as the V_{DD} supply. In the case of 4.0V reference operation, the converter encodes the analog input into a binary output in LSB increments of $(V_{REF}+ - V_{REF}-)/256$, or 15.6mV. Reducing the reference voltage reduces the LSB size proportionately and thus increases linearity errors. The minimum practical reference voltage is about 2.5V. Because the reference voltage terminals are subjected to internal transient currents during conversion, it is important to drive the reference pins from a low impedance source and to decouple thoroughly. Again, ceramic and tantalum (0.01µF and 10µF) capacitors near the package pin are recommended. It is not necessary to decouple the $^1/_4$R, $^1/_2$R, and $^3/_4$R tap point pins for most applications.

It is possible to elevate $V_{REF}-$ from ground if necessary. In this case, the $V_{REF}-$ pin must be driven from a low impedance reference capable of sinking the current through the resistor ladder. Careful decoupling is again recommended.

Digital Control and Interface

The HI-5700 provides a standard high speed interface to external CMOS and TTL logic families. Two chip enable inputs control the tri-state outputs of output bits D0 through D7 and the Overflow (OVF) bit. As indicated in the Truth Table, all output bits are high impedance when CE2 is low, and output bits D0 through D7 are independently controlled by $\overline{CE1}$.

Although the Digital Outputs are capable of handling typical data bus loading, the bus capacitance charge/discharge currents will produce supply and local group disturbances. Therefore, an external bus driver is recommended.

Clock

The clock should be properly terminated to digital ground near the clock input pin. Clock frequency defines the conversion frequency and controls the converter as described in the "Theory of Operation" section. The Auto Balance ϕ1 half cycle of the clock may be reduced to approximately 20ns; the Sample ϕ2 half cycle may be varied from a minimum of 25ns to a maximum of 5µs.

Signal Source

A current pulse is present at the analog input (V_{IN}) at the beginning of every sample and auto balance period. The transient current is due to comparator charging and switch feedthrough in the capacitor array. It varies with the amplitude of the analog input and the converter's sampling rate.

The signal source must absorb these transients prior to the end of the sample period to ensure a valid signal for conversion. Suitable broad band amplifiers or buffers which exhibit low output impedance and high output drive include the HFA-0005, HA-5004, HA-5002, and HA-5003.

The signal source may drive above or below the power supply rails, but should not exceed 0.5V beyond the rails or damage may occur. Input voltages of -0.5V to +0.5 LSB are converted to all zeroes; input voltages of V_{REF}+ -0.5 LSB to V_{DD} +0.5V are converted to all ones with the Overflow bit set.

Full Scale Offset Error Adjustment

In applications where accuracy is of utmost importance, three adjustments can be made; i.e., offset, gain, and reference tap point trims. In general, offset and gain correction can be done in the preamp circuitry.

Offset Adjustment

Offset correction can be done in the preamp driving the converter by introducing a DC component to the input signal. An alternate method is to adjust V_{REF}- to produce the desired offset. It is adjusted such that the 0 to 1 code transition occurs at 0.5 LSB.

Gain Adjustment

In general, full scale error correction can be done in the preamp circuitry by adjusting the gain of the op amp. An alternate method is to adjust the V_{REF}+ voltage. The reference voltage is the ideal location.

Quarter Point Adjustment

The reference tap points are brought out for linearity adjustment or creating a nonlinear transfer function if desired. It is not necessary to decouple the $^1/_4$R, $^1/_2$R, and $^3/_4$R tap points in most applications.

Power Supplies

The HI-5700 operates nominally from 5V supplies but will work from 3V to 6V. Power to the device is split such that analog and digital circuits within the HI-5700 are powered separately. The analog supply should be well regulated and "clean" from significant noise, especially high frequency noise. The digital supply should match the analog supply within about 0.5V and should be referenced externally to the analog supply at a single point. Analog and digital grounds should not be separated by more that 0.5V. It is recommended that power supply decoupling capacitors be placed as close to the supply pins as possible. A combination of 0.01µF ceramic and 10µF tantalum capacitors is recommended for this purpose as shown in the test circuit.

Reducing Power Consumption

Power dissipation in the HI-5700 is related to clock frequency and clock duty cycle. For a fixed 50% clock duty cycle, power may be reduced by lowering the clock frequency. For a given conversion frequency, power may be reduced by decreasing the Auto-Balance (ϕ1) portion of the clock duty cycle. This relationship is illustrated in the performance curves.

TABLE 3. CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE* V_{REF}+ = 4.0V V_{REF}- = 0.0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB								LSB
			OVF	D7	D6	D5	D4	D3	D2	D1	D0
Overflow (OVF)	4.000	511	1	1	1	1	1	1	1	1	1
Full Scale (FS)	3.9766	255	0	1	1	1	1	1	1	1	1
FS - 1 LSB	3.961	254	0	1	1	1	1	1	1	1	0
3/4 FS	2.992	192	0	1	1	0	0	0	0	0	0
1/2 FS	1.992	128	0	1	0	0	0	0	0	0	0
1/4 FS	0.992	64	0	0	1	0	0	0	0	0	0
1 LSB	0.0078	1	0	0	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0	0	0

* The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage.

Glossary of Terms

Aperture Delay: Aperture delay is the time delay between the external sample command (the rising edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter: This is the RMS variation in the aperture delay due to variation of internal $\phi 1$ and $\phi 2$ clock path delays and variation between the individual comparator switching times.

Differential Linearity Error (DNL): The differential linearity error is the difference in LSBs between the spacing of the measured midpoint of adjacent codes and the spacing of ideal midpoints of adjacent codes. The ideal spacing of each midpoint is 1.0 LSB. The range of values possible is from -1.0 LSB (which implies a missing code) to greater than +1.0 LSB.

Full Power Input Bandwidth: Full power bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Full Scale Error (FSE): Full Scale Error is the difference between the actual input voltage of the 254 to 255 code transition and the ideal value of $V_{REF}+ - 1.5$ LSB. This error is expressed in LSBs.

Integral Linearity Error (INL): The integral linearity error is the difference in LSBs between the measured code centers and the ideal code centers. The ideal code centers are calculated using a best fit line through the converter's transfer function.

LSB: Least Significant Bit = $(V_{REF}+ - V_{REF}-)/256$. All HI-5700 specifications are given for a 15.6mV LSB size $V_{REF}+ = 4.0V$, $V_{REF}- = 0.0V$.

Offset Error (VOS): Offset error is the difference between the actual input voltage of the 0 to 1 code transition and the ideal value of $V_{REF}- + 0.5$ LSB, V_{OS} Error is expressed in LSBs.

Power Supply Rejection Ratio (PSRR): PSRR is expressed in LSBs and is the maximum shift in code transition points due to a power supply voltage shift. This is measured at the 0 to 1 code transition point and the 254 to 255 code transition point with a power supply voltage shift from the nominal value of 5.0V.

Signal to Noise Ratio (SNR): SNR is the ratio in dB of the RMS signal to RMS noise at specified input and sampling frequencies.

Signal to Noise and Distortion Ratio (SINAD): SINAD is the ratio in dB of the RMS signal to the RMS sum of the noise and harmonic distortion at specified input and sampling frequencies.

Total Harmonic Distortion (THD): THD is the ratio in dBc of the RMS sum of the first five harmonic components to the RMS signal for a specified input and sampling frequency.

Die Characteristics

DIE DIMENSIONS:
154.3 x 173.2 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

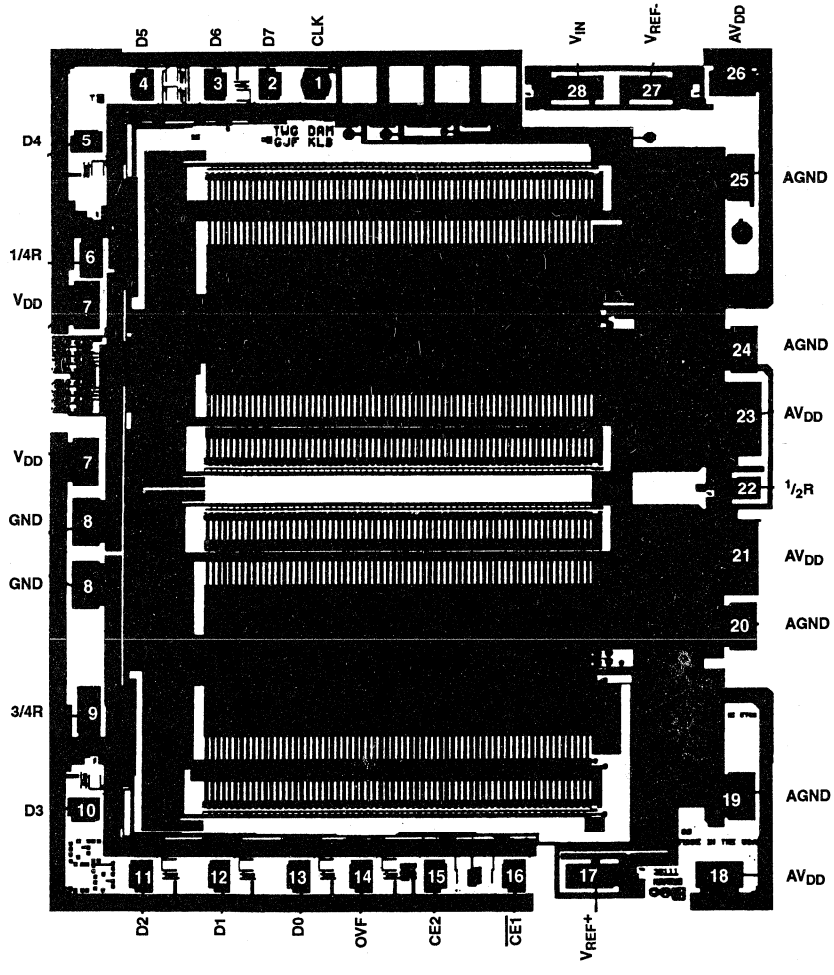
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

TRANSISTOR COUNT: 8000

SUBSTRATE POTENTIAL (Powered Up): V+

Metallization Mask Layout

HI-5700



HARRIS SEMICONDUCTOR

HI-5701

December 1993

6-Bit, 30MSPS Flash A/D Converter

Features

- 30 MSPS with No Missing Codes
- 20MHz Full Power Input Bandwidth
- No Missing Codes Over Temperature
- Sample and Hold Not Required
- Single +5V Supply Voltage
- 300mW (Max) Power Dissipation
- CMOS/TTL Compatible
- Overflow Bit
- Evaluation Board Available
- /883 Version Available

Applications

- Video Digitizing
- Radar Systems
- Communication Systems
- High Speed Data Acquisition Systems

Description

The HI-5701 is a monolithic, 6 bit, CMOS flash Analog-to-Digital Converter. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 30MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5701 delivers ±0.7LSB differential nonlinearity while consuming only 250mW (typical) at 30MSPS. Microprocessor compatible data output latches are provided which present valid data to the output bus 1.5 clock cycles after the convert command is received. An overflow bit is provided to allow the series connection of two converters to achieve 7 bit resolution.

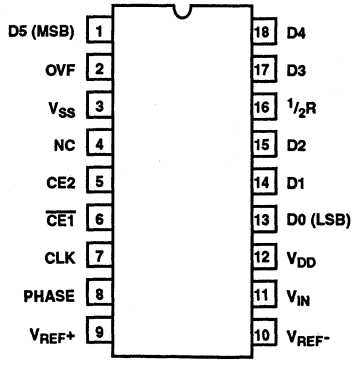
The HI-5701 is available in Commercial and Industrial temperature ranges and is supplied in 18 lead Plastic DIP and SOIC packages.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-5701K-5	0°C to +70°C	18 Lead Plastic DIP
HI9P5701K-5	0°C to +70°C	18 Lead SOIC (W)
HI3-5701B-9	-40°C to +85°C	18 Lead Plastic DIP
HI9P5701B-9	-40°C to +85°C	18 Lead SOIC (W)

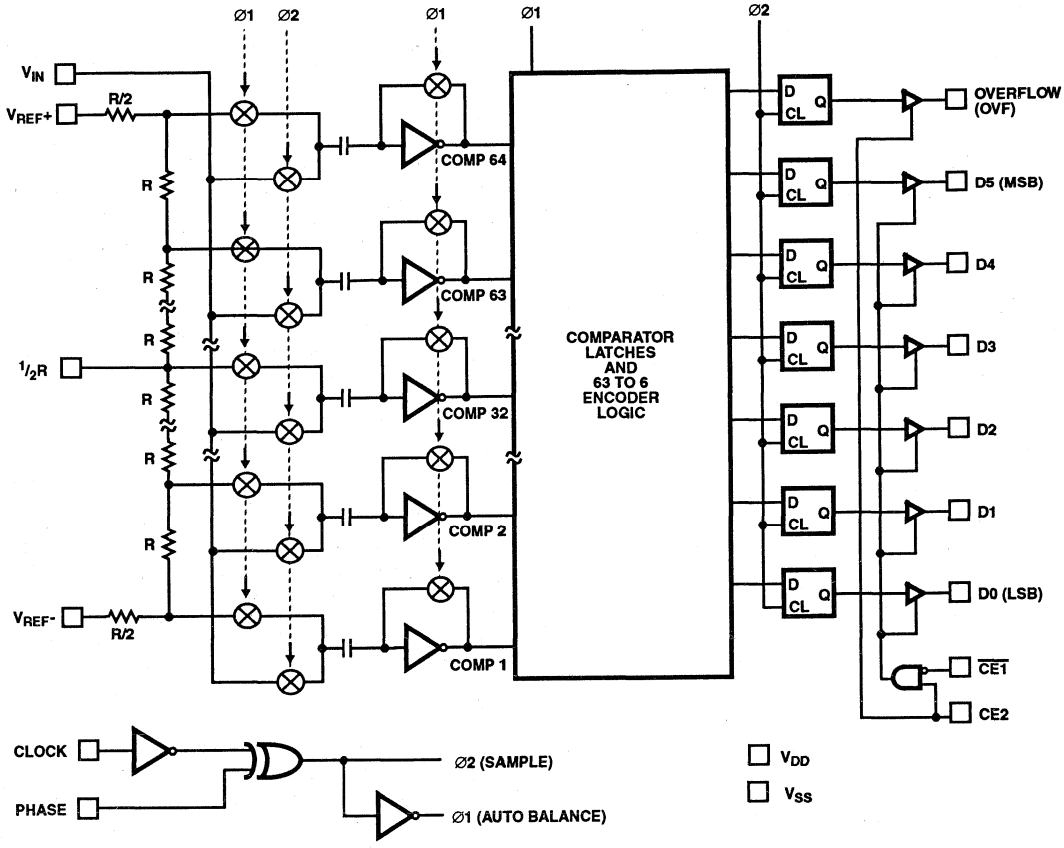
Pinout

HI-5701
(PDIP, SOIC)
TOP VIEW



File Number 2937.5

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage, V_{DD} to V_{SS} ..... $(V_{SS} - 0.5) < V_{DD} < +7.0V$
Analog and Reference Input Pins..... $(V_{SS} - 0.5) < V_{INA} < (V_{DD} +0.5V)$
Digital I/O Pins ..... $(V_{SS} - 0.5) < V_{I/O} < (V_{DD} +0.5V)$
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s)..... +300°C

Thermal Information

Thermal Resistance θ_{JA}
HI3-5701 ..... 95°C/W
HI9P5701..... 95°C/W
Maximum Power Dissipation at +70°C 635mW
Operating Temperature Range
HI3-5701-5 ..... 0°C to +70°C
HI9P5701-9 ..... -40°C to +85°C
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied.

Electrical Specifications: V_{DD} = +5.0V; $V_{REF}+$ = +4.0V; V_{REF-} = V_{SS} = GND; F_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	+25°C			(NOTE 2) 0°C to +70°C -40°C to +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
SYSTEM PERFORMANCE							
Resolution		6	-	-	6	-	Bits
Integral Linearity Error (INL) (Best Fit Line)	F_S = 20MHz	-	±0.5	±1.25	-	±2.0	LSB
	F_S = 30MHz	-	±1.5	-	-	-	LSB
Differential Linearity Error (DNL) (Guaranteed No Missing Codes)	F_S = 20MHz	-	±0.3	±0.6	-	±0.75	LSB
	F_S = 30MHz	-	±0.7	-	-		LSB
Offset Error (VOS) (Adjustable to Zero)	F_S = 20MHz (Note 2)	-	±0.5	±2.0	-	±2.5	LSB
	F_S = 30MHz	-	±0.5	-	-	-	LSB
Full Scale Error (FSE) (Adjustable to Zero)	F_S = 20MHz (Note 2)	-	±0.25	±2.0	-	±2.5	LSB
	F_S = 30MHz	-	±0.25	-	-	-	LSB
DYNAMIC CHARACTERISTICS							
Maximum Conversion Rate	No Missing Codes	30	40	-	30	-	MSPS
Minimum Conversion Rate	No Missing Codes (Note 2)	-	-	0.125	-	0.125	MSPS
Full Power Input Bandwidth	F_S = 30MHz	-	20	-	-	-	MHz
Signal to Noise Ratio (SNR) $= \frac{\text{RMS Signal}}{\text{RMS Noise}}$	F_S = 1MHz, f_{IN} = 100kHz	-	36	-	-	-	dB
	F_S = 30MHz, f_{IN} = 4MHz	-	31	-	-	-	dB
Signal to Noise Ratio (SINAD) $= \frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	F_S = 1MHz, f_{IN} = 100kHz	-	35	-	-	-	dB
	F_S = 30MHz, f_{IN} = 4MHz	-	30	-	-	-	dB
Total Harmonic Distortion	F_S = 1MHz, f_{IN} = 100kHz	-	-44	-	-	-	dBc
	F_S = 30MHz, f_{IN} = 4MHz	-	-38	-	-	-	dBc
Differential Gain	F_S = 14.32MHz, f_{IN} = 3.58MHz	-	2	-	-	-	%
Differential Phase	F_S = 14.32MHz, f_{IN} = 3.58MHz	-	2	-	-	-	Degree

Electrical Specifications: V_{DD} = +5.0V; V_{REF}+ = +4.0V; V_{REF-} = V_{SS} = GND; F_S = Specified Clock Frequency at 50% Duty Cycle; C_L = 30pF; Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	+25°C			(NOTE 2) 0°C to +70°C -40°C to +85°C		UNITS
		MIN	TYP	MAX	MIN	MAX	
ANALOG INPUTS							
Analog Input Resistance, R_{IN}	V_{IN} = 4V	-	30	-	-	-	MΩ
Analog Input Capacitance, C_{IN}	V_{IN} = 0V	-	20	-	-	-	pF
Analog Input Bias Current, IB	V_{IN} = 0V, 4V	-	0.01	±1.0	-	±1.0	µA
REFERENCE INPUTS							
Total Reference Resistance, R_L		250	370	-	235	-	Ω
Reference Resistance Tempco, T_C		-	+0.266	-	-	-	Ω/°C
DIGITAL INPUTS							
Input Logic High Voltage, V_{IH}		2.0	-	-	2.0	-	V
Input Logic Low Voltage, V_{IL}		-	-	-	-	-	V
Input Logic High Current, I_{IH}	V_{IN} = 5V	-	-	1.0	-	1.0	µA
Input Logic Low Current, I_{IL}	V_{IN} = 0V	-	-	1.0	-	1.0	µA
Input Capacitance, C_{IN}		-	7	-	-	-	pF
DIGITAL OUTPUTS							
Output Logic Sink Current, I_{OL}	V_O = 0.4V	3.2	-	-	3.2	-	mA
Output Logic Source Current, I_{OH}	V_O = 4.5V	-3.2	-	-	-3.2	-	mA
Output Leakage, I_{OFF}	CE2 = 0V	-	-	±1.0	-	±1.0	µA
Output Capacitance, C_{OUT}	CE2 = 0V	-	5.0	-	-	-	pF
TIMING CHARACTERISTICS							
Aperture Delay, t_{AP}		-	6	-	-	-	ns
Aperture Jitter, t_{AJ}		-	30	-	-	-	ps
Data Output Enable Time, t_{EN}	(Note 2)	-	12	20	-	20	ns
Data Output Disable Time, t_{DIS}	(Note 2)	-	11	20	-	20	ns
Data Output Delay, t_{OD}	(Note 2)	-	14	20	-	20	ns
Data Output Hold, t_H	(Note 2)	5	10	-	5	-	ns
POWER SUPPLY REJECTION							
Offset Error PSRR, ΔVOS	V_{DD} = 5V ± 10%	-	±0.1	±1.0	-	±1.5	LSB
Gain Error PSRR, ΔFSE	V_{DD} = 5V± 10%	-	±0.1	±1.0	-	±1.5	LSB
POWER SUPPLY CURRENT							
Supply Current, I_{DD}	F_S = 30MHz	-	50	60	-	75	mA

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Parameter guaranteed by design or characterization and not production tested.

Timing Waveforms

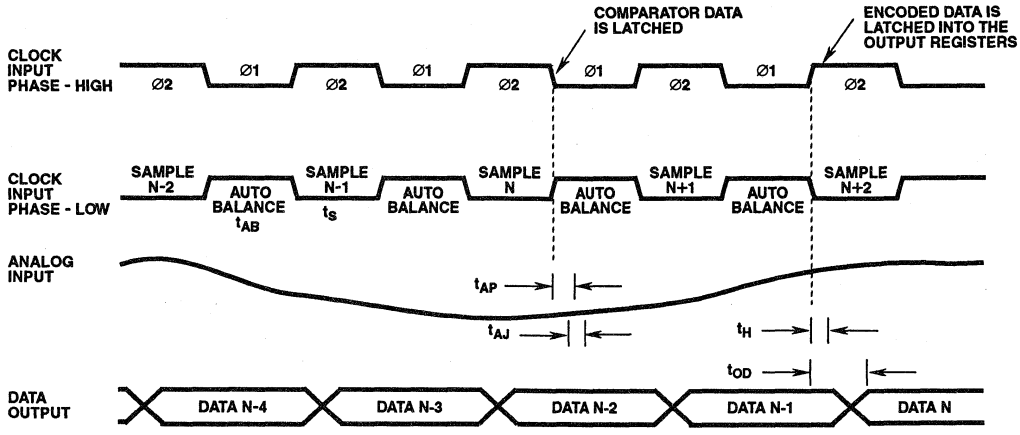


FIGURE 1. INPUT-TO-OUTPUT TIMING

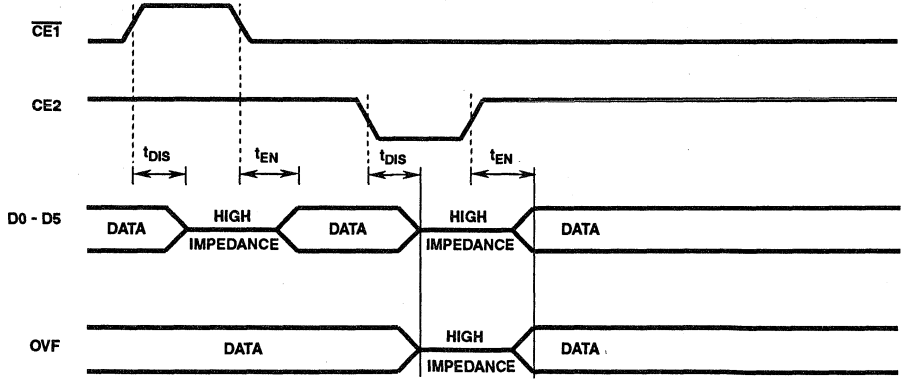


FIGURE 2. OUTPUT ENABLE TIMING

Typical Performance Curves

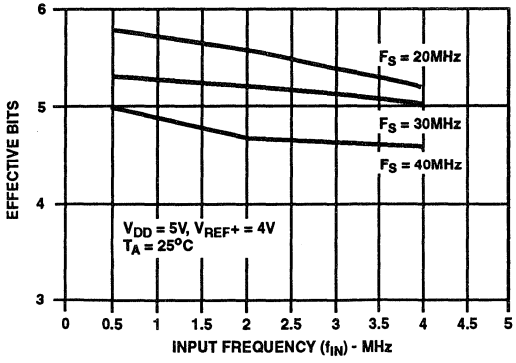


FIGURE 3. EFFECTIVE NUMBER OF BITS vs f_{IN}

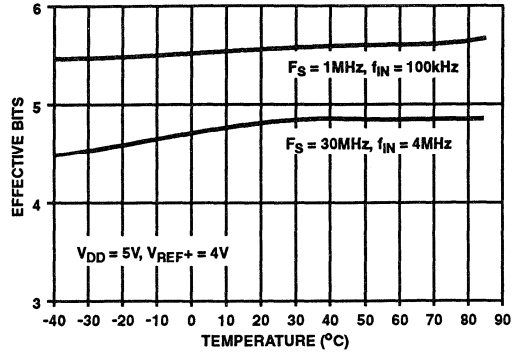


FIGURE 4. ENOB vs TEMPERATURE

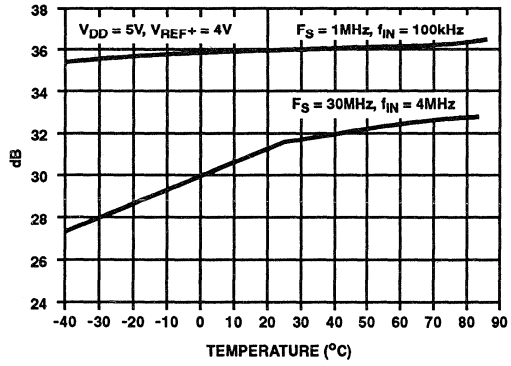


FIGURE 5. SNR vs TEMPERATURE

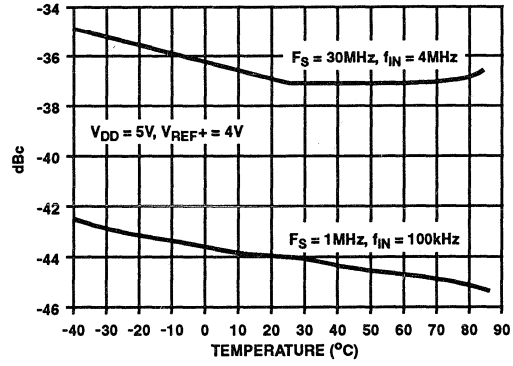


FIGURE 6. TOTAL HARMONIC DISTORTION vs TEMPERATURE

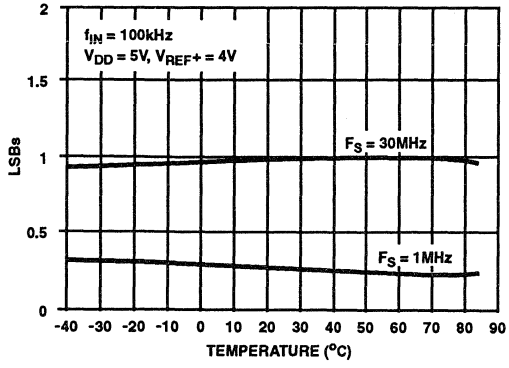


FIGURE 7. INL vs TEMPERATURE

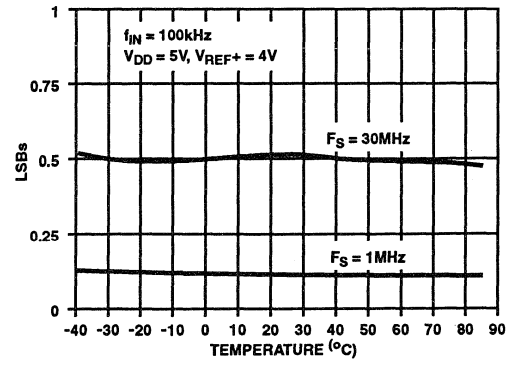


FIGURE 8. DNL vs TEMPERATURE

Typical Performance Curves (Continued)

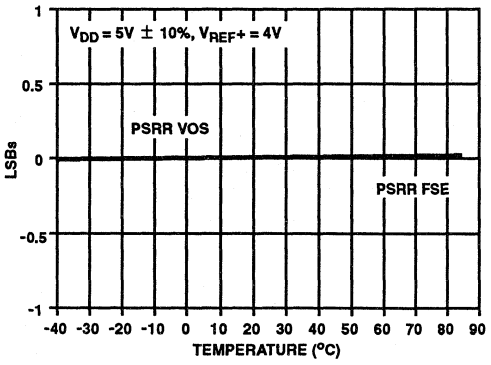


FIGURE 9. POWER SUPPLY REJECTION vs TEMPERATURE

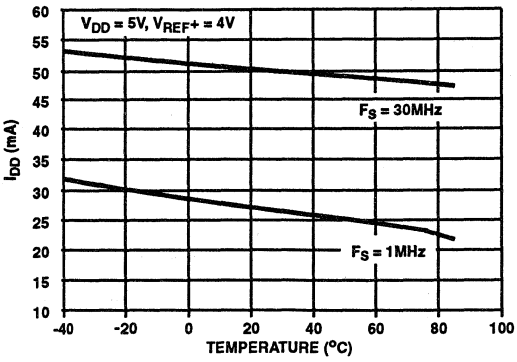


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

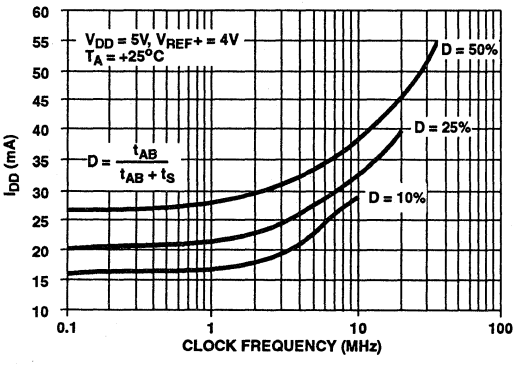


FIGURE 11. SUPPLY CURRENT vs CLOCK AND DUTY CYCLE

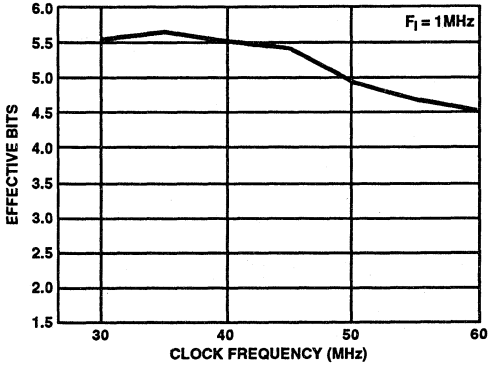


FIGURE 12. EFFECTIVE NUMBER OF BITS vs CLOCK FREQUENCY

TABLE 1. PIN DESCRIPTION

PIN #	NAME	DESCRIPTION
1	D5	Bit 6, Output (MSB)
2	OVF	Overflow, Output
3	V_{SS}	Digital Ground
4	NC	No Connection
5	CE2	Tri-State Output Enable Input, Active High (See Table 2).
6	$\overline{CE1}$	Tri-State Output Enable Input, Active Low (See Table 2).
7	CLK	Clock Input
8	PHASE	Sample Clock Phase Control Input. When Phase is Low, Sample Unknown (ϕ1) Occurs When the Clock is Low and Auto Balance (ϕ2) Occurs When the Clock is High (See Text).
9	V_{REF}+	Reference Voltage Positive Input
10	V_{REF}-	Reference Voltage Negative Input
11	V_{IN}	Analog Signal Input
12	V_{DD}	Power Supply, +5V
13	D0	Bit 1, Output (LSB)
14	D1	Bit 2, Output
15	D2	Bit 3, Output
16	$^1/_2$ R2	Reference Ladder Midpoint
17	D3	Bit 4, Output
18	D4	Bit 5, Output

TABLE 2. CHIP ENABLE TRUTH TABLE

$\overline{CE1}$	CE2	D0 - D5	OVF
0	1	Valid	Valid
1	1	Tri-State	Valid
X	0	Tri-State	Tri-State

X = Don't Care

Theory of Operation

The HI-5701 is a 6 bit analog-to-digital converter based on a parallel CMOS "flash" architecture. This flash technique is an extremely fast method of A/D conversion because all bit decisions are made simultaneously. In all, 64 comparators are used in the HI-5701; 63 comparators to encode the output word, plus an additional comparator to detect an overflow condition.

The CMOS HI-5701 works by alternately switching between a "Sample" mode and an "Auto Balance" mode. Splitting up the comparison process in this CMOS technique offers a number of significant advantages. The offset voltage of each CMOS comparator is dynamically canceled with each conversion cycle such that offset voltage drift is virtually eliminated during operation. The block diagram and timing diagram illustrate how the HI-5701 CMOS flash converter operates.

The input clock which controls the operation of the HI-5701 is first split into a non-inverting ϕ1 clock and an inverting ϕ2 clock. These two clocks, in turn, synchronize all internal timing of analog switches and control logic within the converter.

In the "Auto Balance" mode (ϕ1), all ϕ1 switches close and ϕ2 switches open. The output of each comparator is momentarily tied to its own input, self-biasing the comparator midway between V_{SS} and V_{DD} and presenting a low impedance to a small input capacitor. Each capacitor, in turn, is connected to a reference voltage tap from the resistor ladder. The Auto Balance mode quickly precharges all 64 input capacitors between the self-bias voltage and each respective tap voltage.

In the "Sample" mode (ϕ2), all ϕ1 switches open and ϕ2 switches close. This places each comparator in a sensitive high gain amplifier configuration. In this open loop state, the input impedance is very high and any small voltage shift at the input will drive the output either high or low. The ϕ2 state also switches each input capacitor from its reference tap to the input signal. This instantly transfers any voltage difference between the reference tap and input voltage to the comparator input. All 64 comparators are thus driven simultaneously to a defined logic state. For example, if the input voltage is at mid-scale, capacitors precharged near zero during ϕ1 will push comparator inputs higher than the self bias voltage at ϕ2; capacitors precharged near the reference voltage push the respective comparator inputs lower than the bias point. In general, all capacitors precharged by taps above the input voltage force a "low" voltage at comparator inputs; those precharged below the input voltage force "high" inputs at the comparators.

During the next ϕ1 state, comparator output data is latched into the encoder logic block and the first stage of encoding takes place. The following ϕ2 state completes the encoding process. The 6 data bits (plus overflow bit) are latched into the output flip-flops at the next falling clock edge. The Overflow bit is set if the input voltage exceeds V_{REF}+ - $^1/_2$LSB. The output bus may be either enabled or disabled according to the state of $\overline{CE1}$ and CE2 (See Table 2). When disabled, output bits assume a high impedance state.

As shown in the timing diagram, the digital output word becomes valid after the second ϕ1 state. There is thus a one and a half cycle pipeline delay between input sample and digital output. "Data Output Delay" time indicates the slight time delay for data to become valid at the end of the ϕ1 state. Refer to the Glossary of Terms for other definitions.

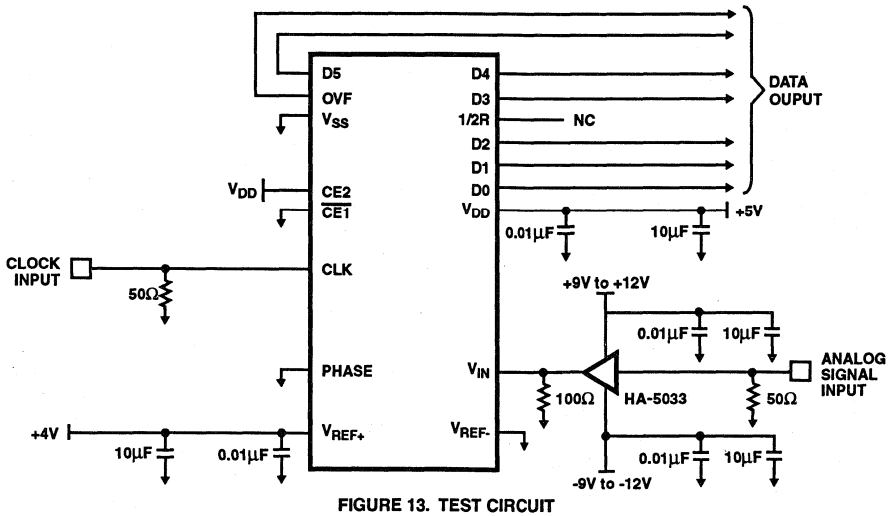


FIGURE 13. TEST CIRCUIT

Applications Information

Voltage Reference

The reference voltage is applied across the resistor ladder at the input of the converter, between $V_{REF}+$ and $V_{REF}-$. In most applications, $V_{REF}-$ is simply tied to analog ground such that the reference source drives $V_{REF}+$. The reference must be capable of supplying enough current to drive the minimum ladder resistance of 235Ω over temperature.

The HI-5701 is specified for a reference voltage of 4.0V, but will operate with voltages as high as the V_{DD} supply. In the case of 4.0V reference operation, the converter encodes the analog input into a binary output in LSB increments of $(V_{REF}+ - V_{REF}-)/64$, or 62.5mV. Reducing the reference voltage reduces the LSB size proportionately and thus increases linearity errors. The minimum practical reference voltage is about 2V. Because the reference voltage terminals are subjected to internal transient currents during conversion, it is important to drive the reference pins from a low impedance source and to decouple thoroughly. Again, ceramic and tantalum (0.01µF and 10µF) capacitors near the package pin are recommended. It is not necessary to decouple the $^1/_2$R tap point pin for most applications.

It is possible to elevate $V_{REF}-$ from ground if necessary. In this case, the $V_{REF}-$ pin must be driven from a low impedance reference capable of sinking the current through the resistor ladder. Careful decoupling is again recommended.

Digital Control and Interface

The HI-5701 provides a standard high speed interface to external CMOS and TTL logic families. Four digital inputs are provided to control the function of the converter. The clock and phase inputs control the sample and auto balance modes. The digital outputs change state on the clock phase which begins the sample mode. Two chip enable inputs control the tri-state outputs of output bits D0 through D5 and the Overflow OVF bit. As indicated in Table 2, all output bits are high impedance when CE2 is low, and output bits D0 through D5 are independently controlled by $\overline{CE1}$.

Although the Digital Outputs are capable of handling typical data bus loading, the bus capacitance charge/discharge currents will produce supply and local ground disturbances. Therefore, an external bus driver is recommended.

Clock

The clock should be properly terminated to digital ground near the clock input pin. Clock frequency defines the conversion frequency and controls the converter as described in the "Theory of Operation" section. The Auto Balance ϕ1 half cycle of the clock may be reduced to 16ns; the Sample ϕ2 half cycle may be varied from a minimum of 16ns to a maximum of 8µs.

TABLE 3. PHASE CONTROL

CLOCK	PHASE	INTERNAL GENERATION
0	0	Sample Unknown (ϕ2)
0	1	Auto Balance (ϕ1)
1	0	Auto Balance (ϕ1)
1	1	Sample Unknown (ϕ2)

Gain and Offset Adjustment

In applications where accuracy is of utmost importance, three adjustments can be made; i.e., offset, gain, and midpoint trim. In general, offset and gain correction can be done in the preamp circuitry.

Offset Adjustment

The preferred offset correction method is to introduce a DC component to V_{IN} of the converter. An alternate method is to adjust the $V_{REF}-$ input to produce the desired offset adjustment. The theoretical input voltage to produce the first transition is $^1/_2$LSB.

V_{IN} (0 to 1 transition) = $^1/_2$LSB = $^1/_2(V_{REF}/64) = V_{REF}/128$

Gain Adjustment

In general, full scale error correction can be done in the preamp circuitry by adjusting the gain of the op amp. An alternate method is to adjust the $V_{REF}+$ input voltage. This adjustment is performed by setting V_{IN} to the 63 to overflow transition. The theoretical input voltage to produce the transition is $^1/_2$ LSB less than $V_{REF}+$ and is calculated as follows:

V_{IN} (63 to 64 transition) = V_{REF} - (V_{REF}/128) = V_{REF}(127/128).

To perform the gain trim, first do the offset trim and then apply the required V_{IN} for the 63 to overflow transition. Now adjust $V_{REF}+$ until that transition occurs on the outputs.

Midpoint Trim

The reference center ($^1/_2$R) is available to the user as the midpoint of the resistor ladder. The $^1/_2$R point can be used to improve linearity or create unique transfer functions. The offset and gain trims should be done prior to adjusting the midpoint. The theoretical transition from count 31 to 32 occurs at 31.5 LSB's. That voltage is calculated as follows:

V_{IN} (31 to 32 transition) = 31.5(V_{REF}/64) = V_{REF}(63/128).

An adjustable voltage follower can be used to drive the $^1/_2$R pin. Set V_{IN} to the 31 to 32 transition voltage, then adjust the voltage follower until the transition occurs on the output bits.

Signal Source

A current pulse is present at the analog input (V_{IN}) at the beginning of every sample and auto balance period. The transient current is due to comparator charging and switch feed through in the capacitor array. It varies with the amplitude of the analog input and the sampling rate.

The signal source must be capable of recovering from the transient prior to the end of the sample period to ensure a valid signal for conversion. Suitable broad band amplifiers or buffers which exhibit low output impedance and high output drive include the HFA-0005, HA-5004, HA-5002, and HA-5033.

The signal source may drive above or below the power supply rails, but should not exceed 0.5V beyond the rails or damage may occur. Input voltages of -0.5V to +$^1/_2$ LSB are converted to all zeros; input voltages of $V_{REF}+$ - $^1/_2$ LSB to V_{DD} + 0.5 are converted to all ones with the Overflow bit set.

Power Supplies

The HI-5701 operates nominally from 5V supplies but will function from 3V to 6V. The analog supply should be well regulated and "clean" of significant noise, especially high frequency noise. It is recommended that power supply decoupling capacitors be placed as close to the supply pins as possible. A combination of 0.01µF ceramic and 10µF tantalum capacitors is recommended for this purpose as shown in the test circuit Figure 13.

Reducing Power Consumption

Power dissipation in the HI-5701 is related to clock frequency and clock duty cycle. For a fixed 50% clock duty cycle, power may be reduced by lowering the clock frequency. For a given conversion frequency, power may be reduced by shortening the Auto Balance ϕ1 portion of the clock duty cycle.

TABLE 4. OUTPUT CODE TABLE

CODE DESCRIPTION	INPUT VOLTAGE* $V_{REF}+$ = 4.0V $V_{REF}-$ = 0.0V (V)	DECIMAL COUNT	BINARY OUTPUT CODE MSB						LSB
			OVF	D5	D4	D3	D2	D1	D0
Overflow (OVF)	4.000	127	1	1	1	1	1	1	1
Full Scale (FS)	3.9063	63	0	1	1	1	1	1	1
FS - 1LSB	3.8438	62	0	1	1	1	1	1	0
	•					•			
	•					•			
						•			
3/4 FS	2.9688	48	0	1	1	0	0	0	0
	•					•			
	•					•			
	•					•			
1/2 FS	1.9688	32	0	1	0	0	0	0	0
	•					•			
	•					•			
	•					•			
1/4 FS	0.9688	16	0	0	1	0	0	0	0
	•					•			
	•					•			
	•					•			
1LSB	0.0313	1	0	0	0	0	0	0	1
Zero	0	0	0	0	0	0	0	0	0

* The voltages listed above represent the ideal transition of each output code shown as a function of the reference voltage.

Glossary of Terms

Aperture Delay: Aperture delay is the time delay between the external sample command (the rising edge of the clock) and the time at which the signal is actually sampled. This delay is due to internal clock path propagation delays.

Aperture Jitter: This is the RMS variation in the aperture delay due to variation of internal $\phi 1$ and $\phi 2$ clock path delays and variation between the individual comparator switching times.

Differential Linearity Error (DNL): The differential linearity error is the difference in LSBs between the spacing of the measured midpoint of adjacent codes and the spacing of ideal midpoints of adjacent codes. The ideal spacing of each midpoint is 1.0 LSB. The range of values possible is from -1.0 LSB (which implies a missing code) to greater than +1.0 LSB.

Full Power Input Bandwidth: Full power bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Full Scale Error (FSE): Full Scale Error is the difference between the actual input voltage of the 63 to 64 code transition and the ideal value of $V_{REF}+ - 1.5$ LSB. This error is expressed in LSBs.

Integral Linearity Error (INL): The integral linearity error is the difference in LSBs between the measured code centers and the ideal code centers. The ideal code centers are calculated using a best fit line through the converter's transfer function.

LSB: Least Significant Bit = $(V_{REF}+ - V_{REF}-)/64$. All HI-5701 specifications are given for a 62.5mV LSB size $V_{REF}+ = 4.0V$, $V_{REF}- = 0.0V$.

Offset Error (VOS): Offset error is the difference between the actual input voltage of the 0 to 1 code transition and the ideal value of $V_{REF}- + 0.5$ LSB. VOS error is expressed in LSBs.

Power Supply Rejection Ratio (PSRR): PSRR is expressed in LSBs and is the maximum shift in code transition points due to a power supply voltage shift. This is measured at the 0 to 1 code transition point and the 62 to 63 code transition point with a power supply voltage shift from the nominal value of 5.0V.

Signal to Noise Ratio (SNR): SNR is the ratio in dB of the RMS signal to RMS noise at specified input and sampling frequencies.

Signal to Noise and Distortion Ratio (SINAD): SINAD is the ratio in dB of the RMS signal to the RMS sum of the noise and harmonic distortion at specified input and sampling frequencies.

Total Harmonic Distortion (THD): THD is the ratio in dBc of the RMS sum of the first five harmonic components to the RMS signal for a specified input and sampling frequency.

Die Characteristics

DIE DIMENSIONS:
86.6 x 130.7 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

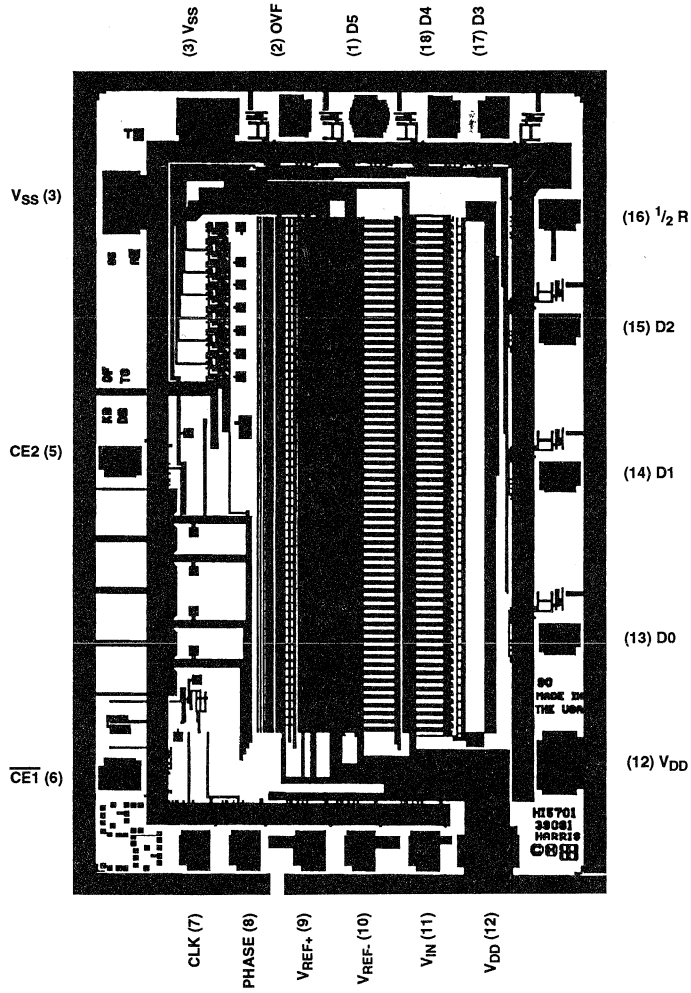
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

TRANSISTOR COUNT: 4000

SUBSTRATE POTENTIAL (Powered Up): V+

Metallization Mask Layout

HI-5701



DATA ACQUISITION 7

A/D CONVERTERS - SUBRANGING

NOTE: Bold Type Designates a New Product from Harris.

8-BIT SUBRANGING

DEVICE	SUFFIX CODE	MIL SPEC	OUTPUTS	CONVERSION TYPE	CONVERSION TIME (ns)	BANDWIDTH (MHz)	TECHNOLOGY	RANGE MIN (V)	INL (LSB)	DNL (LSB)	FEATURES
HI1175JCB			Parallel, Binary, 8-Bit Latch, Tri-State	Two-Step	50	18	CMOS	2	±1.3	±0.5	Low Power 60mW Typ at 20msps
HI1175JCP											
HI1176JCQ			Parallel, Binary, 8-Bit Latch, Tri-State	Two-Step	50	18	CMOS	2	±1.3	±0.5	Low Power 60mW Typ at 20msps DC Restore

10-BIT SUBRANGING

DEVICE	SUFFIX CODE	MIL SPEC	OUTPUTS	CONVERSION TYPE	CONVERSION TIME (µs)	TECHNOLOGY	RANGE MIN (V)	LINEARITY (LSB)	CLOCK TYP	FEATURES
HI3-7153J	-5	HI1-7153S/883	10-Bit + O/R 2's Complement	2 Step Flash	5 Max	CMOS-JI	±2.5	±1.0	600kHz	8 Input Mux, Internal Track and Hold, ±5VDC aPower 225mW, On Chip Buffers for Analog Input and Reference. 200kHz Throughput Rate
HI3-7153A	-9							±1.0		
HI3-7153S	-2							±1.0		

12-BIT SUBRANGING

DEVICE	SUFFIX CODE	MIL SPEC	OUTPUTS	CONVERSION TYPE	CONVERSION TIME (ns)	TECHNOLOGY	RANGE MIN (V)	INL (LSB)	REFERENCE VOLTAGE	FEATURES
HI5800AID			Parallel, Binary, Tri-State, 8-Bit Bus,12-Bit Bus and 16-Bit Bus	Two-Step	330ns	BiCMOS	5	±2.0	Internal 2.5V	HighPerformance Sampling A/D
HI5800BID								±1.0		
HI5800JCD								±2.0		
HI5800KCD								±1.0		
HI5800JCM								±2.0		
HI5800KCM								±1.0		

December 1993

8-Bit, 20MSPS Flash A/D Converter

Features

- Resolution: 8-Bit ±0.5 LSB (DNL)
- Maximum Sampling Frequency: 20MSPS
- Low Power Consumption: 60mW (at 20MSPS Typ.) (Reference Current Excluded)
- Built-In Sample and Hold Circuit
- Built-In Reference Voltage Self Bias Circuit
- Tri-State TTL Compatible Output
- Single +5V Power Supply
- Low Input Capacitance: 11pF (Typ.)
- Reference Impedance: 300Ω (Typ.)
- Evaluation Board Available
- Low Cost

Applications

- Video Digitizing
- Image Scanners
- Multimedia
- High Speed Data Acquisition Systems

Description

The HI1175 is an 8-bit CMOS analog-to -digital converter for video use. The adoption of a 2-step parallel system achieves low power consumption at a maximum conversion speed of 20MSPS minimum, 35MSPS typical.

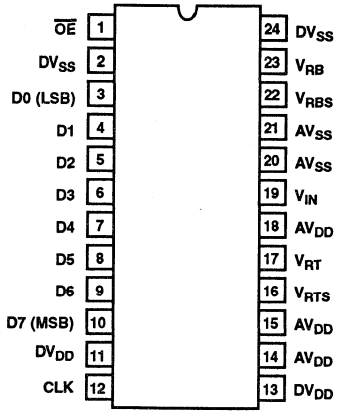
The HI1175 is available in the Commercial temperature range and is supplied in 24 lead plastic DIP (400 mil) and SOIC (200 mil) packages.

Ordering Information

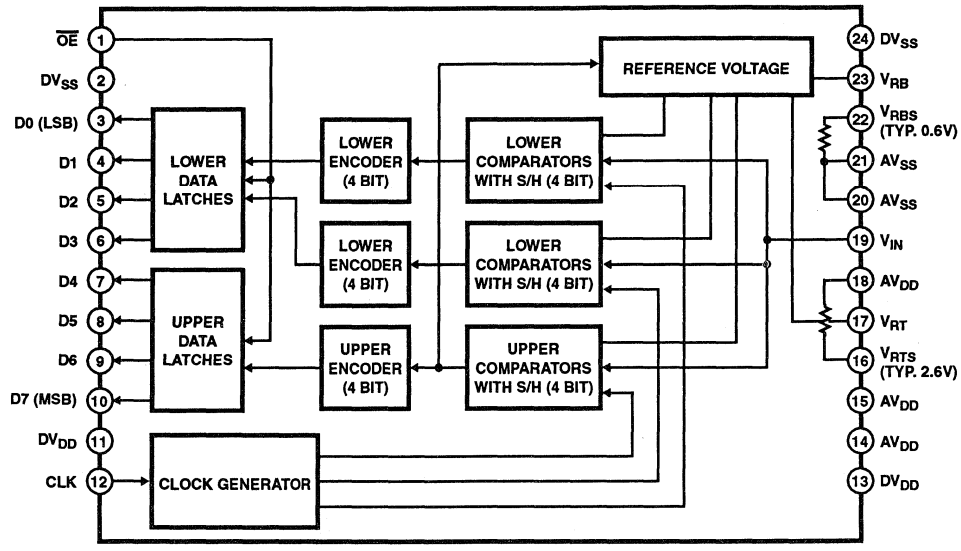
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1175JCP	-20°C to +75°C	24 Lead Plastic DIP (400 mil)
HI1175JCB	-20°C to +75°C	24 Lead SOIC (200 mil)

Pinout

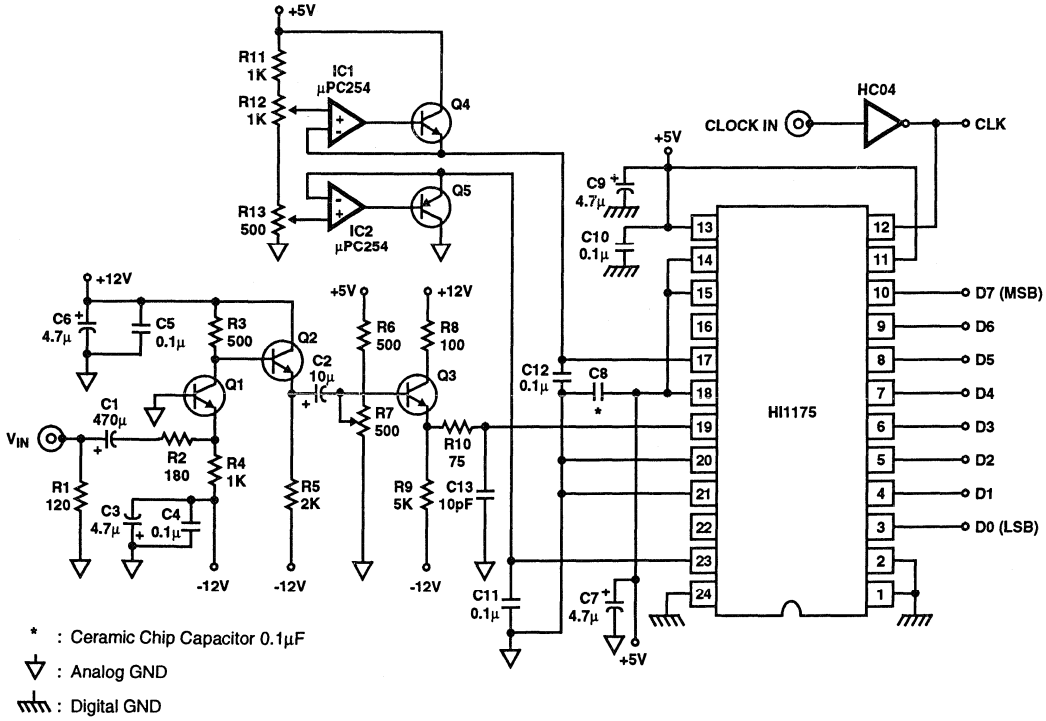
HI1175
(PDIP, SOIC)
TOP VIEW



Functional Block Diagram



Typical Application Schematic



NOTE: It is necessary that AV_{DD} and DV_{DD} pins be driven from the same supply. The gain of analog input signal can be changed by adjusting R3.

Absolute Maximum Ratings

Supply Voltage, V_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} ..... V_{DD} to V_{SS}
Analog Input Voltage, V_{IN} ..... V_{DD} to V_{SS}
Digital Input Voltage, CLK ..... V_{DD} to V_{SS}
Digital Output Voltage, V_{OH}, V_{OL} ..... V_{DD} to V_{SS}
Storage Temperature, T_{STG} ..... -55°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}
HI1175JCP (Plastic DIP)	78°C/W
HI1175JCB (SOIC)	98°C/W
Maximum Power Dissipation	108mW
Operating Temperature, T_A	-20°C to +75°C
Maximum Junction Temperature	+150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions (Note 1)

Supply Voltage
AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS} ..... +4.75V to +5.25V
|DGND-AGND| ..... 0mV to 100mV
Reference Input Voltage
V_{RB} ..... 0V and Above
V_{RT} ..... 2.8V and Below
Analog Input Voltage, V_{IN} ..... V_{RB} to V_{RT} ($1.8V_{P-P}$ to AV_{DD})
Clock Pulse Width
T_{PW1} ..... 25ns (Min.)
T_{PW0} ..... 25ns (Min.)

Electrical Specifications F_C = 20MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = +25°C (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Offset Voltage E_{OT}		-60	-35	-10	mV
E_{OB}		0	+15	+45	mV
Integral Non-Linearity, (INL)	F_C = 20MSPS, V_{IN} = 0.6V to 2.6V	-	±0.5	±1.3	LSB
Differential Non-Linearity, (DNL)	F_C = 20MSPS, V_{IN} = 0.6V to 2.6V	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Signal to Noise Ratio (SINAD) = $\frac{\text{RMS Signal}}{\text{RMS Noise + Distortion}}$	F_S = 20MHz, f_{IN} = 1MHz	-	46	-	dB
	F_S = 20MHz, f_{IN} = 3.58MHz	-	46	-	dB
Maximum Conversion Speed, F_C	V_{IN} = 0.6V to 2.6V, F_{IN} = 1kHz Ramp	20	30	-	MSPS
Differential Gain Error, DG	NTSC 40 IRE Mod Ramp, F_C = 14.3MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Aperture Jitter, t_{AJ}		-	30	-	ps
Sampling Delay, t_{DS}		-	4	-	ns
ANALOG INPUTS					
Analog Input Bandwidth (-1dB), BW		-	18	-	MHz
Analog Input Capacitance, C_{IN}	V_{IN} = 1.5V + $0.07V_{RMS}$	-	11	-	pF
REFERENCE INPUT					
Reference Pin Current, I_{REF}		4.5	6.6	8.7	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}		230	300	450	Ω

Electrical Specifications F_C = 20MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = +25°C (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REFERENCE						
Self Bias Mode 1						
V_{RB}	Short V_{RB} and V_{RBS}, Short V_{RT} and V_{RTS}		0.60	0.64	0.68	V
V_{RT} - V_{RB}			1.96	2.09	2.21	V
Self Bias Mode 2, V_{RT}	V_{RB} = AGND, Short V_{RT} and V_{RTS}		2.25	2.39	2.53	V
DIGITAL INPUTS						
Digital Input Voltage						
V_{IH}			4.0	-	-	V
V_{IL}			-	-	1.0	V
Digital Input Current						
I_{IH}	V_{DD} = Max.	V_{IH} = V_{DD}	-	-	5	µA
I_{IL}		V_{IL} = 0V	-	-	5	µA
DIGITAL OUTPUTS						
Digital Output Current						
I_{OH}	$\overline{OE}$ = V_{SS}, V_{DD} = Min.	V_{OH} = V_{DD} -0.5V	-1.1	-	-	mA
I_{OL}		V_{OL} = 0.4V	3.7	-	-	mA
Digital Output Current						
I_{OZH}	$\overline{OE}$ = V_{DD}, V_{DD} = Max.	V_{OH} = V_{DD}	-	-	16	µA
I_{OZL}		V_{OL} = 0V	-	-	16	µA
TIMING CHARACTERISTICS						
Output Data Delay, T_{DL}			-	18	30	ns
POWER SUPPLY CHARACTERISTIC						
Supply Current, I_{DD}	F_C = 20MSPS, NTSC Ramp Wave Input		-	12	17	mA

NOTE:

1. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams

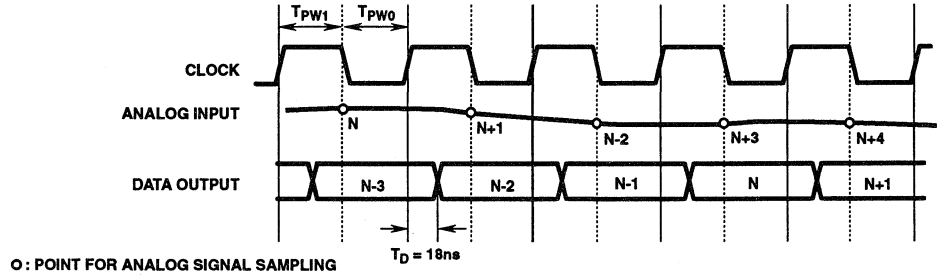


FIGURE 1.

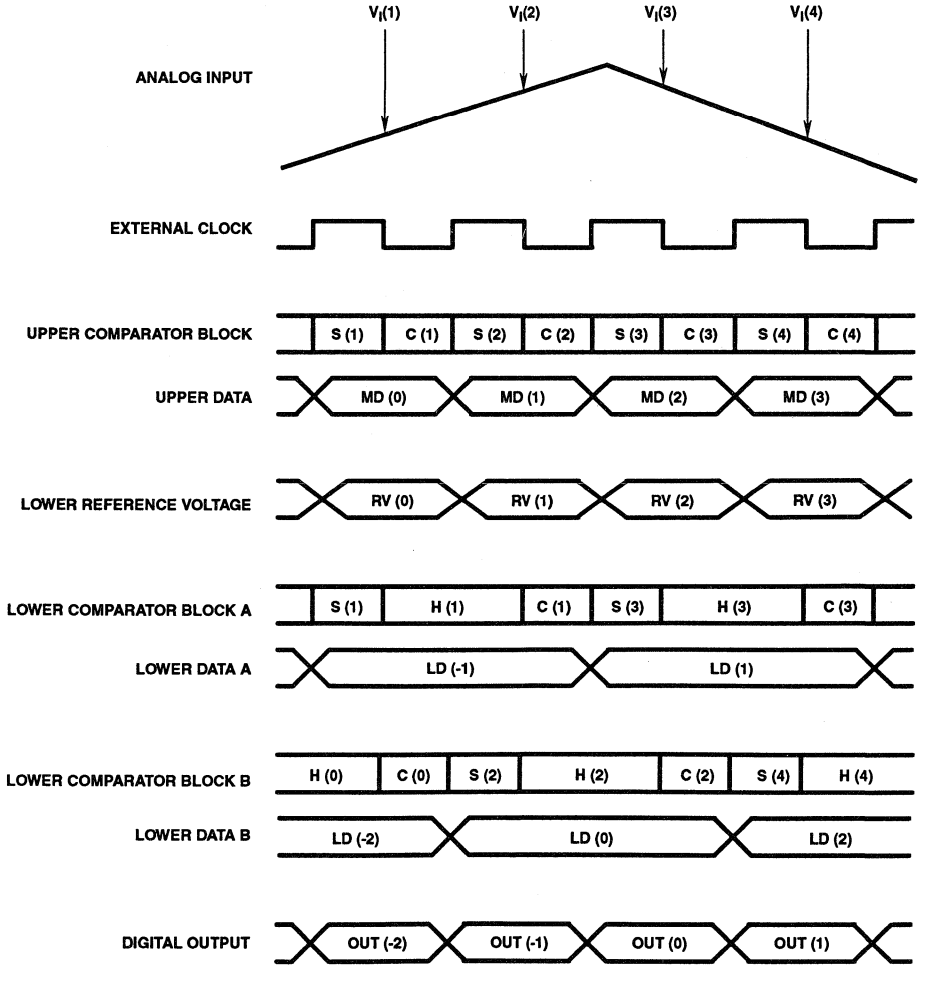


FIGURE 2.

Typical Performance Curves

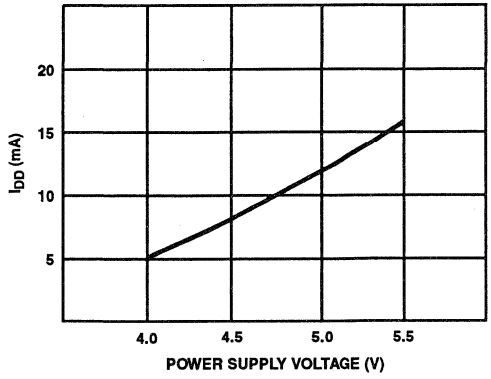


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

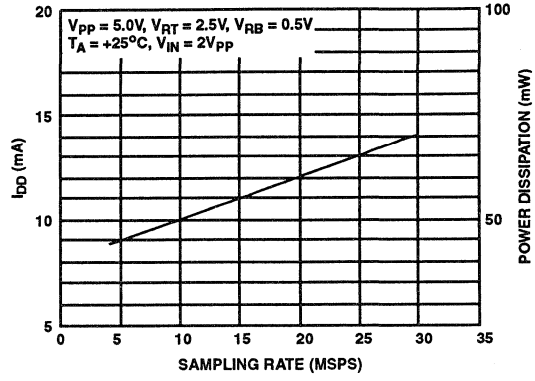


FIGURE 4. SUPPLY CURRENT AND POWER vs SAMPLING RATE

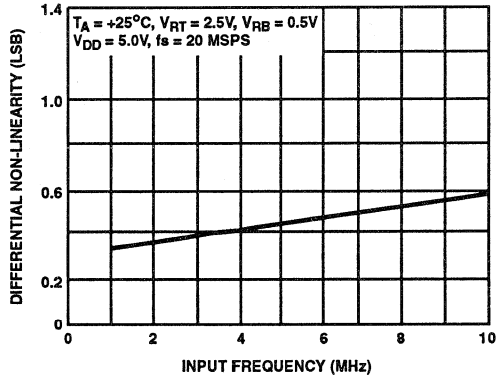
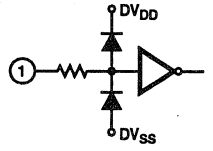
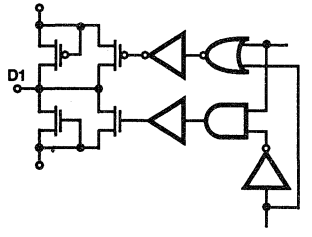
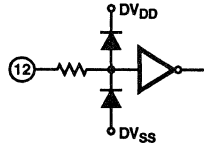
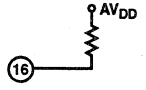
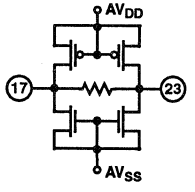
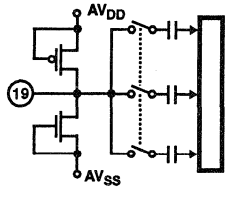
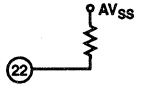


FIGURE 5. DIFFERENTIAL NON-LINEARITY vs INPUT FREQUENCY

Pin Descriptions and Equivalent Circuits

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1	$\overline{OE}$		When $\overline{OE}$ = Low, Data is valid. When $\overline{OE}$ = High, D0 to D7 pins high impedance.
2, 24	DV_{SS}		Digital GND.
3-10	D0 to D7		D0 (LSB) to D7 (MSB) output.
11, 13	DV_{DD}		Digital +5V.
12	CLK		Clock input.
16	V_{RTS}		Shorted with V_{RT} generates, +2.6V.
17	V_{RT}		Reference voltage (top).
23	V_{RB}		Reference voltage (bottom).
14, 15, 18	AV_{DD}		Analog +5V.
19	V_{IN}		Analog input.
20, 21	AV_{SS}		Analog GND.
22	V_{RBS}		Shorted with V_{RB} generates +0.6V.

A/D OUTPUT CODE TABLE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
V_{RT}	0	1	1	1	1	1	1	1	1
•	•					•			
•	•					•			
•	•					•			
•									
•	127	1	0	0	0	0	0	0	0
•	128	0	1	1	1	1	1	1	1
•									
•	•					•			
•	•					•			
	•					•			
V_{RB}	255	0	0	0	0	0	0	0	0

Detailed Description

The HI1175 is a 2-step A/D converter featuring a 4-bit upper comparator group and two lower comparator groups of 4 bits each. The reference voltage can be obtained from the onboard bias generator or be supplied externally. This IC uses an offset canceling type comparator that operates synchronously with an external clock. The operating modes of the part are input sampling (S), hold (H), and compare (C).

The operation of the part is illustrated in Figure 2. A reference voltage that is between V_{RT}-V_{RB} is constantly applied to the upper 4-bit comparator group. $V_I(1)$ is sampled with the falling edge of the first clock by the upper comparator block. The lower block A also samples $V_I(1)$ on the same edge. The upper comparator block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates a reference voltage RV(1) that corresponds to the upper results and applies it to the lower comparator block A. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as OUT(1) with the rising edge of the third clock. There is a 2.5 cycle clock delay from the analog input sampling point to the corresponding digital output data. Notice how the lower comparator blocks A and B alternate generating the lower data in order to increase the overall A/D sampling rate.

Power, Grounding, and Decoupling

To reduce noise effects, separate the analog and digital grounds.

In order to avoid latchup at power up, it is necessary that AV_{DD} and DV_{DD} be driven from the same supply.

Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1µF capacitor close to the pin.

Analog Input

The input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with an amplifier with sufficient bandwidth and drive capability. In order to prevent parasitic oscillation, it may be necessary to insert a resistor between the output of the amplifier and the A/D input.

Reference Input

The range of the A/D is set by the voltage between V_{RT} and V_{RB}. The internal bias generator will set V_{RTS} to 2.6V and V_{RBS} to 0.6V. These can be used as the part reference by shorting V_{RT} and V_{RTS} and V_{RB} to V_{RBS}. The analog input range of the A/D will now be from 0.6V to 2.6V and is referred to as Self Bias Mode 1. Self Bias Mode 2 is where V_{RB} is connected to AGND and V_{RT} is shorted to V_{RTS}. The analog input range will now be from 0V to 2.4V.

Test Circuits

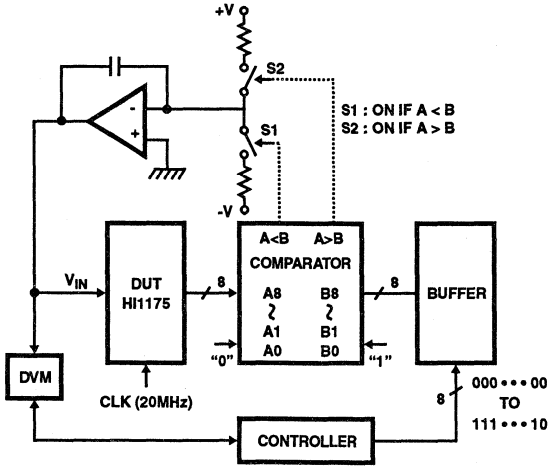


FIGURE 6. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

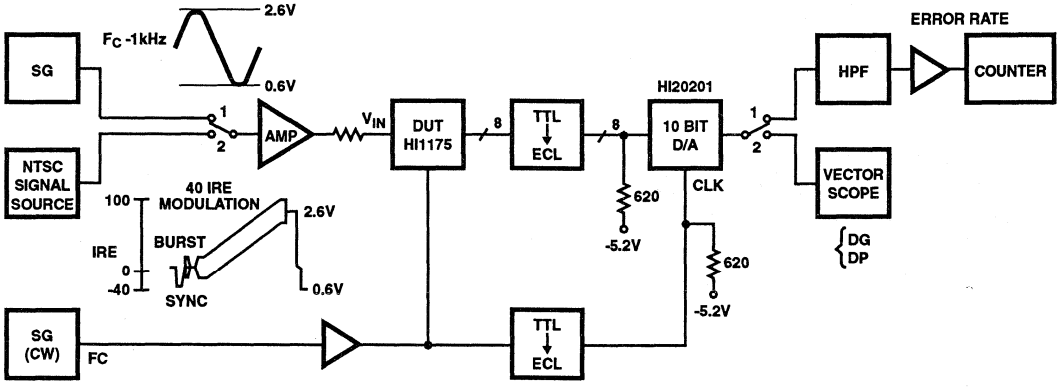


FIGURE 7. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

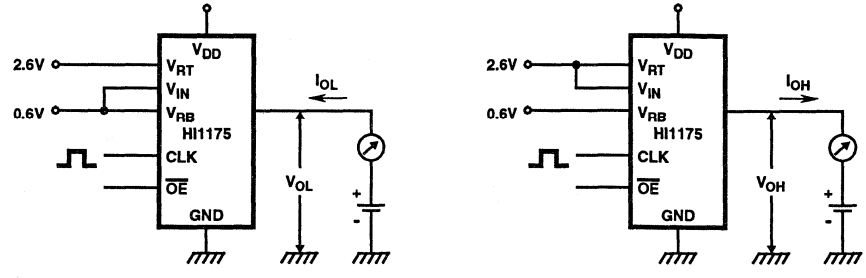


FIGURE 8. DIGITAL OUTPUT CURRENT TEST CIRCUIT

HARRIS SEMICONDUCTOR

HI1176

December 1993

8-Bit, 20MSPS Flash A/D Converter

Features

- Resolution 8-Bit ±0.5 LSB (DNL)
- Maximum Sampling Frequency 20MSPS
- Low Power Consumption 60mW (at 20MSPS Typ.) (Reference Current Excluded)
- Built-In Sync Clamp Function
- Built-In Monostable Multivibrator for Clamp Pulse Generation
- Built-In Sync Pulse Polarity Selection Function
- Clamp Pulse Direct Input Possible
- Built-In Clamp ON/OFF Function
- Built-In Reference Voltage Self Bias Circuit
- Input CMOS Compatible
- Tri-State TTL Compatible Output
- Single +5V Power Supply
- Low Input Capacitance 11pF (Typ.)
- Reference Impedance 300Ω (Typ.)
- Evaluation Board Available

Applications

- Video Digitizing
- Image Scanners
- Low Cost High Speed Data Acquisition Systems
- Multimedia

Description

The HI1176 is an 8-bit CMOS analog-to-digital converter for video use that features a sync clamp function. The adoption of a 2-step parallel method realizes low power consumption and a maximum conversion speed of 20MSPS.

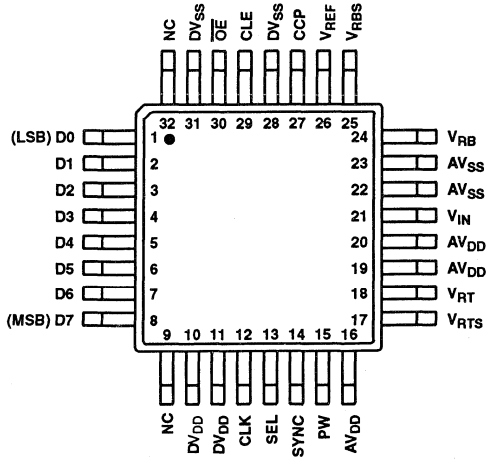
The HI1176 is available in the Commercial temperature range and is supplied in 32 lead Plastic Metric Quad Flatpack (MQFP) package.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1176JCQ	-20°C to +75°C	32 Lead Plastic Metric Quad Flatpack

Pinout

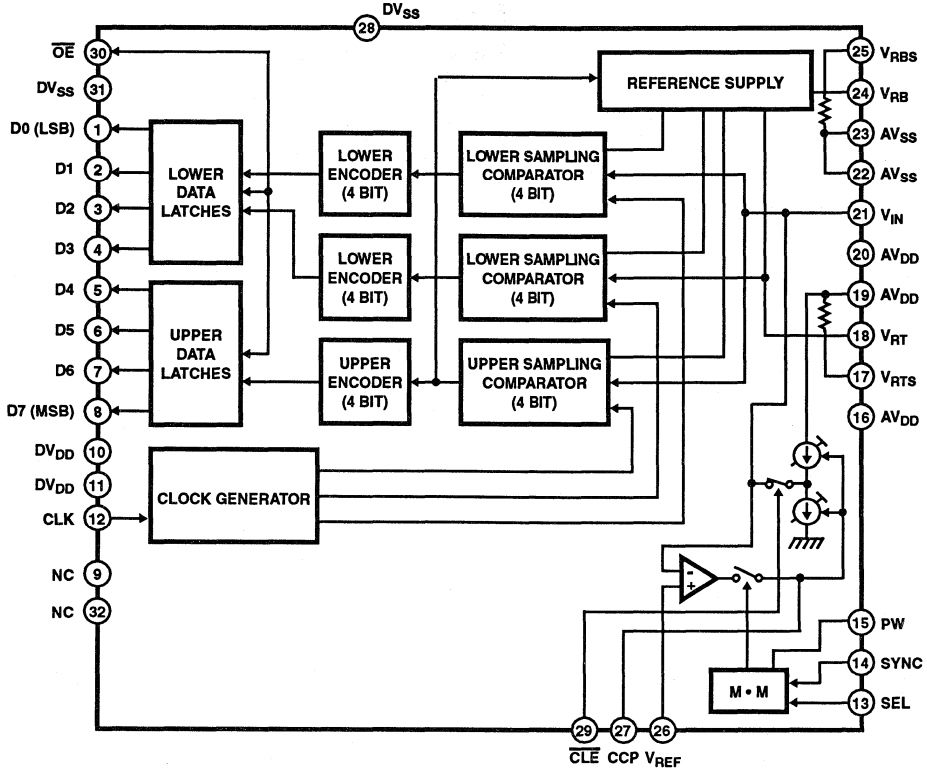
HI1176 (MQFP)
TOP VIEW



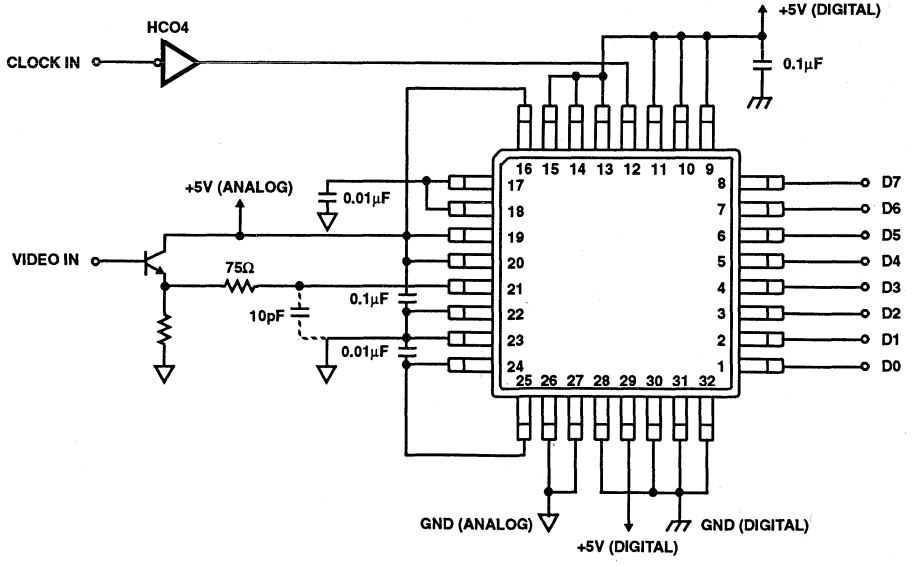
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3582.1

Functional Block Diagram



Typical Application Schematic



WHEN CLAMP IS NOT USED (SELF BIAS USED)

Absolute Maximum Ratings

Supply Voltage, V_{DD} 7V
Reference Voltage, V_{RT}, V_{RB} ..... V_{DD} to V_{SS}
Analog Input Voltage, V_{IN} ..... V_{DD} to V_{SS}
Digital Input Voltage, CLK ..... V_{DD} to V_{SS}
Digital Output Voltage, V_{OH}, V_{OL} ..... V_{DD} to V_{SS}
Storage Temperature, T_{STG} ..... -55°C to +150°C

Thermal Information

Thermal Resistance θ_{JA}
HI1176JCQ ..... 122°C/W
Maximum Power Dissipation 108mW
Operating Temperature, T_A ..... -20°C to +75°C
Maximum Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions (Note 1)

Supply Voltage
AV_{DD}, AV_{SS}, DV_{DD}, DV_{SS} ..... +4.75V to +5.25V
IDGND-AGNDI ..... 0mV to 100mV
Reference Input Voltage
V_{RB} ..... 0V and Above
V_{RT} ..... 2.8V and Below
Analog Input Voltage, V_{IN} ..... V_{RB} to V_{RT} ($1.8V_{P-P}$ to AV_{DD})
Clock Pulse Width
T_{PW1} ..... 25ns (Min.)
T_{PW0} ..... 25ns (Min.)

Electrical Specifications

F_C = 20MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = +25°C (Note 1)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYSTEM PERFORMANCE					
Offset Voltage E_{OT}		-60	-40	-20	mV
E_{OB}		+20	+40	+60	mV
Integral Non-Linearity, (INL)	F_C = 20MSPS, V_{IN} = 0.5V to 2.5V	-	±0.5	±1.3	LSB
Differential Non-Linearity, (DNL)	F_C = 20MSPS, V_{IN} = 0.5V to 2.5V	-	±0.3	±0.5	LSB
DYNAMIC CHARACTERISTICS					
Signal to Noise Ratio (SINAD) = RMS Signal / RMS Noise + Distortion	F_S = 20MHz, f_{IN} = 1MHz	-	46	-	dB
	F_S = 20MHz, f_{IN} = 3.58MHz	-	46	-	dB
Maximum Conversion Speed, F_C	V_{IN} = 0.5V to 2.5V, F_{IN} = 1kHz Ramp	20	35	-	MSPS
Differential Gain Error, DG	NTSC 40 IRE Mod Ramp, F_C = 14.3MSPS	-	1.0	-	%
Differential Phase Error, DP		-	0.5	-	Degree
Aperture Jitter, t_{AJ}		-	30	-	ps
Sampling Delay, t_{DS}		-	4	-	ns
ANALOG INPUTS					
Analog Input Bandwidth (-1dB), BW		-	18	-	MHz
Analog Input Capacitance, C_{IN}	V_{IN} = 1.5V + 0.07V_{RMS}	-	11	-	pF
REFERENCE INPUT					
Reference Pin Current, I_{REF}		4.5	6.6	8.7	mA
Reference Resistance (V_{RT} to V_{RB}), R_{REF}		230	300	450	Ω

Electrical Specifications F_C = 20MSPS, V_{DD} = +5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = +25°C (Note 1) **(Continued)**

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REFERENCES						
Self Bias						
V_{RB}	Short V_{RB} and V_{RBS}, Short V_{RT} and V_{RTS}		0.48	0.52	0.56	V
V_{RT} - V_{RB}			1.96	2.08	2.22	V
DIGITAL INPUTS						
Digital Input Voltage						
V_{IH}			4.0	-	-	V
V_{IL}			-	-	1.0	V
Digital Input Current						
I_{IH}	V_{DD} = Max.	V_{IH} = V_{DD}	-	-	5	µA
I_{IL}		V_{IL} = 0V	-	-	5	µA
DIGITAL OUTPUTS						
Digital Output Current						
I_{OH}	$\overline{OE}$ = V_{SS}, V_{DD} = Min.	V_{OH} = V_{DD} -0.5V	-1.1	-	-	mA
I_{OL}		V_{OL} = 0.4V	3.7	-	-	mA
Digital Output Current						
I_{OZH}	$\overline{OE}$ = V_{DD}, V_{DD} = Max.	V_{OH} = V_{DD}	-	-	16	µA
I_{OZL}		V_{OL} = 0V	-	-	16	µA
TIMING CHARACTERISTICS						
Output Data Delay, T_{DL}			-	18	30	ns
POWER SUPPLY CHARACTERISTIC						
Supply Current, I_{DD}	F_C = 20MSPS, NTSC Ramp Wave Input		-	12	18	mA
CLAMP CHARACTERISTICS						
Clamp Offset Voltage, E_{OC}	V_{IN} = DC, PWS = 3µsec	V_{REF} = 0.5V	0	+20	+40	mV
		V_{REF} = 2.5V	-50	-30	-10	mV
Clamp Pulse Width (Sync Pin Input), tcpw	C = 100pF, R = 130kΩ on Pin 15		1.75	2.75	3.75	µs
Clamp Pulse Delay, tcpd			-	25	-	ns

NOTE:

1. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagrams

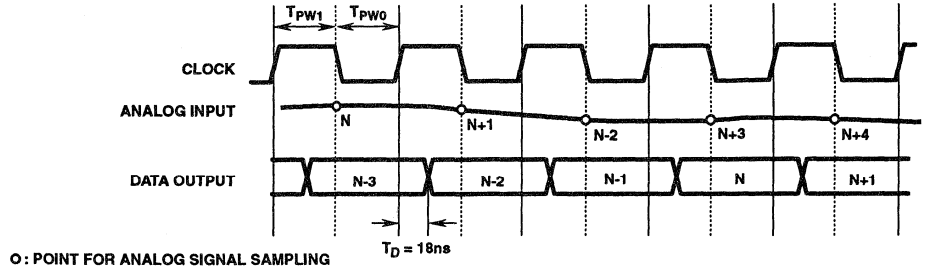


FIGURE 1.

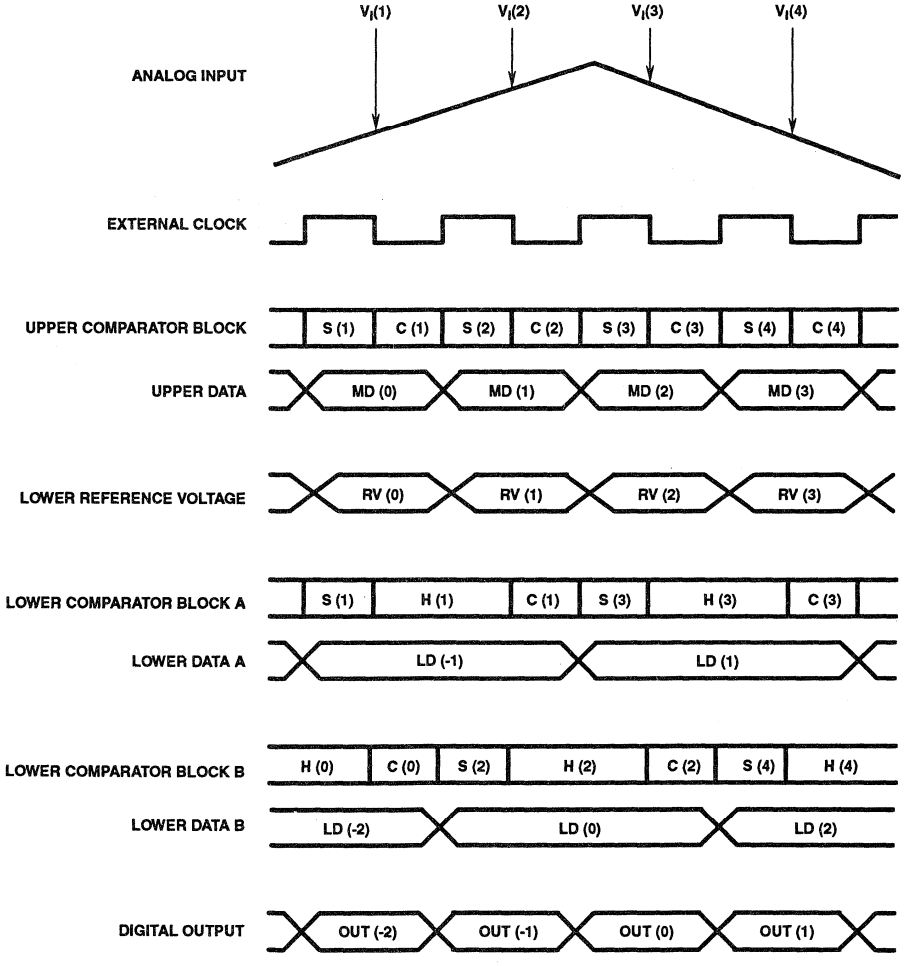


FIGURE 2.

Typical Performance Curves

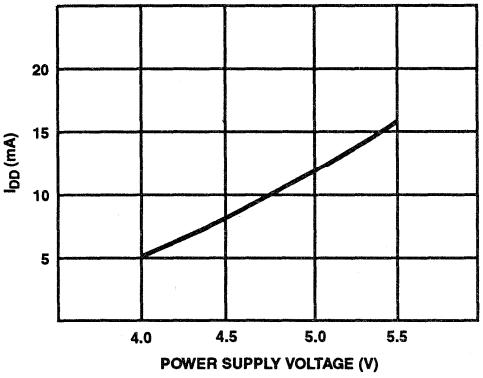


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

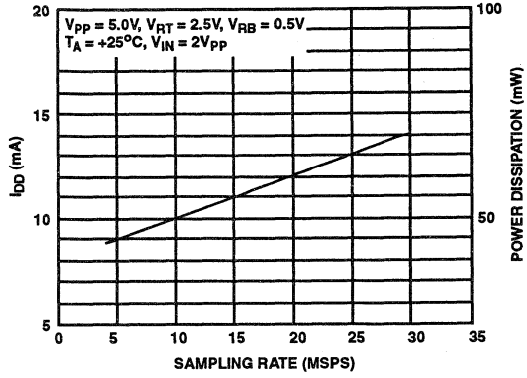


FIGURE 4. SUPPLY CURRENT AND POWER vs SAMPLING RATE

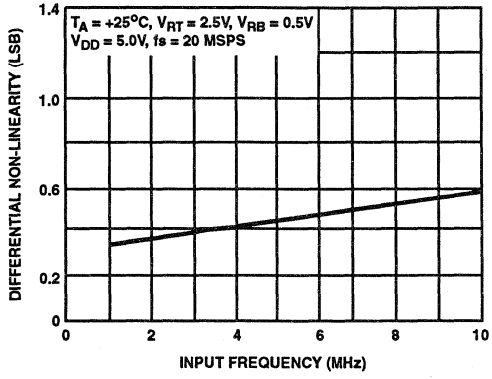
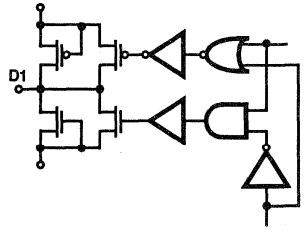
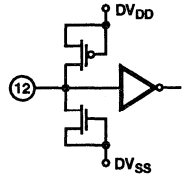
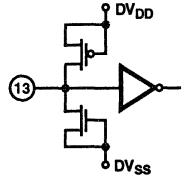
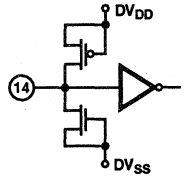
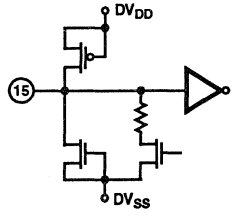
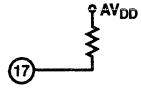
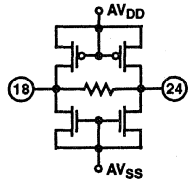


FIGURE 5. DIFFERENTIAL NON-LINEARITY vs INPUT FREQUENCY

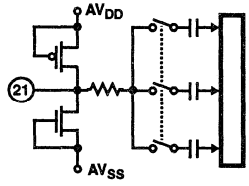
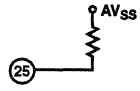
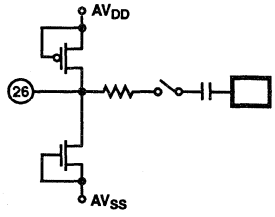
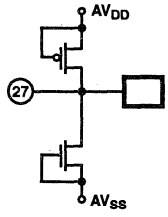
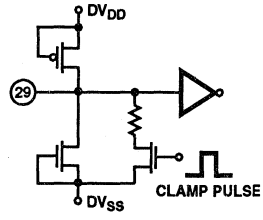
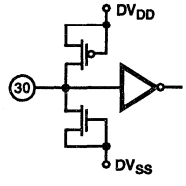
Pin Descriptions

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1-8	D0 to D7		D0 (LSB) to D7 (MSB) output.
10, 11	DV_{DD}		Digital +5V.

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
12	CLK		Clock input.
13	SEL		When SEL is low, the falling edge of Pin 14 (sync) triggers the monostable. When SEL is high, the rising edge of Pin 14 (sync) triggers the monostable.
14	SYNC		Trigger pulse input to the monostable multivibrator. Trigger polarity can be controlled by Pin 13 (SEL).
15	PW		When a clamp pulse is generated by the monostable, the pulse width is determined by the external R and C. When the clamp pulse is directly input, it is input to Pin 15 (PW).
16, 19, 20	AV_{DD}		Analog +5V.
17	V_{RTS}		When shorted with V_{RT}, generates approx. +2.6V.
18	V_{RT}		Reference voltage (top).
24	V_{RB}		Reference voltage (bottom).

Pin Descriptions (Continued)

PIN NUMBER	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
21	V_{IN}		Analog input.
22, 23	AV_{SS}		Analog ground.
25	V_{RBS}		When shorted with V_{RB}, generates approx. +0.5V.
26	V_{REF}		Clamp reference voltage input.
27	CCP		Integrates the voltage for clamp control.
28, 31	DV_{SS}		Digital GND.
29	$\overline{CLE}$		When $\overline{CLE}$ is low, clamp function is activated. When $\overline{CLE}$ is high, clamp function is OFF and only the usual A/D converter function is active. By connecting $\overline{CLE}$ pin to DV_{DD} via a several hundred Ω resistance, the clamp pulse can be tested.
30	$\overline{OE}$		When $\overline{OE}$ is low, data is valid. When $\overline{OE}$ is high, D0 to D7 pins are high impedance.

A/D OUTPUT CODE TABLE

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
V_{RT}	0	1	1	1	1	1	1	1	1
•	•					•			
•	•					•			
•	•					•			
•									
•	127	1	0	0	0	0	0	0	0
•	128	0	1	1	1	1	1	1	1
•									
•	•					•			
•	•					•			
	•					•			
V_{RB}	255	0	0	0	0	0	0	0	0

Detailed Description

The HI1176 is a 2-step A/D converter featuring a 4-bit upper comparator group and two lower comparator groups of 4 bits each. The reference voltage can obtained from the onboard bias generator or be supplied externally. This IC uses an offset canceling type comparator that operates synchronously with an external clock. The operating modes of the part are input sampling/autozero (S), hold (H), and compare (C).

The operation of the part is illustrated in Figure 2. A reference voltage that is between V_{RT}-V_{RB} is constantly applied to the upper 4-bit comparator group. $V_I(1)$ is sampled with the falling edge of the first clock by the upper comparator block. The lower block A also samples $V_I(1)$ on the same edge. The upper comparator block finalizes comparison data MD(1) with the rising edge of the first clock. Simultaneously the reference supply generates a reference voltage RV(1) that corresponds to the upper results and applies it to the lower comparator block A. The lower comparator block finalizes comparison data LD(1) with the rising edge of the second clock. MD(1) and LD(1) are combined and output as OUT(1) with the rising edge of the third clock. There is a 2.5 cycle clock delay from the analog input sampling point to the corresponding digital output data. Notice how the lower comparator blocks A and B alternate generating the lower data in order to increase the overall A/D sampling rate.

Power, Grounding, and Decoupling

To reduce noise effects, separate the analog and digital grounds.

Bypass both the digital and analog V_{DD} pins to their respective grounds with a ceramic 0.1µF capacitor close to the pin.

Analog Input

The input capacitance is small when compared with other flash type A/D converters. However, it is necessary to drive the input with an amplifier with sufficient bandwidth and drive capability. In order to prevent parasitic oscillation, it may be necessary to insert a resistor between the output of the amplifier and the A/D input.

Reference Input

The range of the A/D is set by the voltage between V_{RT} and V_{RB}. The internal bias generator will set V_{RTS} to 2.5V and V_{RBS} to 0.5V. These can be used as the part reference by shorting V_{RT} and V_{RTS} and V_{RB} to V_{RBS}. The analog input range of the A/D will now be from 0.5V to 2.5V. If a V_{RB} below +0.5V is used the linearity of the part will be degraded.

Bypass V_{RT} and V_{RB} to analog ground with a 0.1µF capacitor.

Clamp Operation

The HI1176 provides a clamp option that allows the user to clamp a portion of the analog input to a voltage set by the V_{REF} pin. The clamp function is enabled by bringing $\overline{CLE}$ low. An internal monostable multivibrator is provided that can be used to generate the clamp pulses. The monostable pulse width is determined by the external R and C connected to the PW pin. The trigger to the monostable is applied on the SYNC pin. The edge that triggers the monostable is determined by the SEL pin. When SEL is low the falling edge will trigger the monostable and when SEL is high the rising edge will trigger the monostable. Figure 6 shows the HI1176 configured for this mode of operation. The clamp pulse is latched by the ADC sampling clock. This is not necessary to the operation of the clamp function but if this is not done then a slight beat might be generated as vertical sag according to the relation between the sampling frequency and the clamp frequency.

The HI1176 can also be configured to operate with an external clamp pulse. In this case a negative going pulse is input to the PW pin. V_{IN} will now be clamped during the low period of the clamp pulse to the voltage on the V_{REF} pin. Figure 7 shows the HI1176 configured for this mode of operation.

Figure 1 illustrates the operation of HI1176 when the clamp function is not used.

Typical Application Circuits

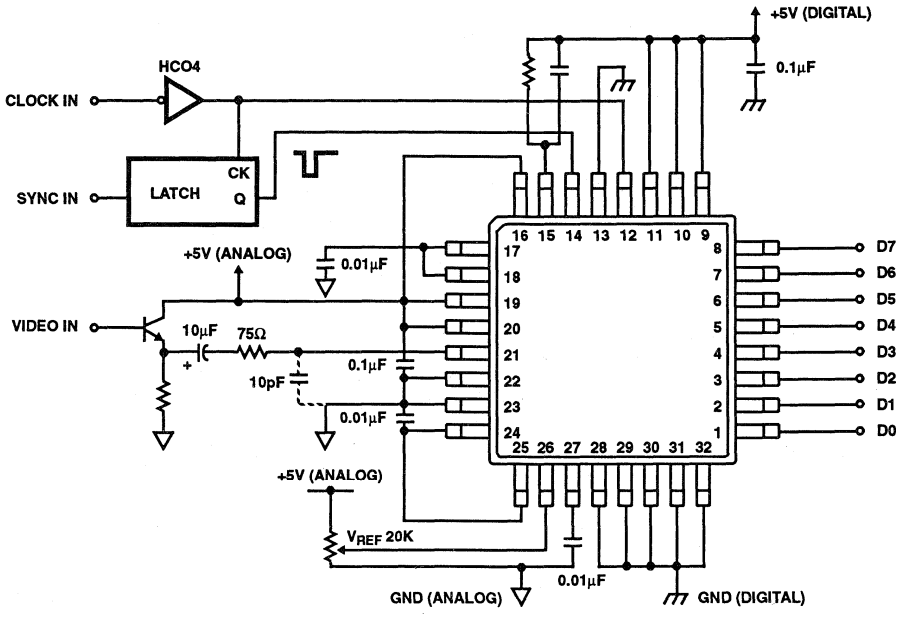


FIGURE 6. PEDESTAL CLAMP IS EXECUTED BY SYNC PULSE (SELF BIAS USED)

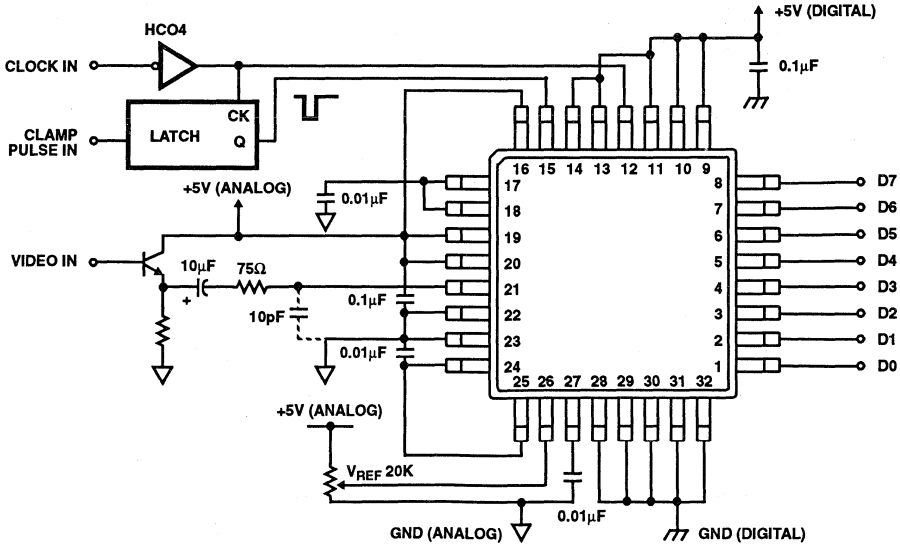


FIGURE 7. CLAMP PULSE IS DIRECTLY INPUT (SELF BIAS USED)

Test Circuits

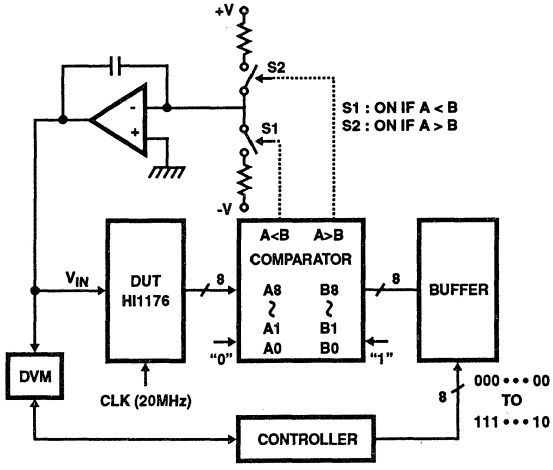


FIGURE 8. INTEGRAL AND DIFFERENTIAL NON-LINEARITY ERROR AND OFFSET VOLTAGE TEST CIRCUIT

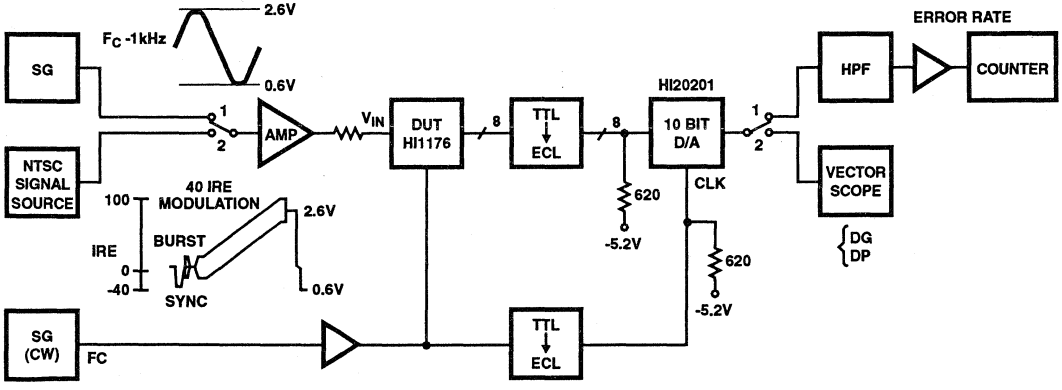


FIGURE 9. MAXIMUM OPERATIONAL SPEED AND DIFFERENTIAL GAIN AND PHASE ERROR TEST CIRCUIT

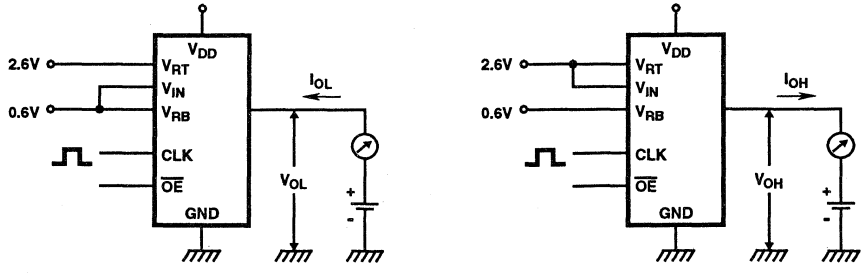


FIGURE 10. DIGITAL OUTPUT CURRENT TEST CIRCUIT

HARRIS SEMICONDUCTOR

HI5800

December 1993

12-Bit, 3MSPS Sampling A/D Converter

Features

- 3MSPS Throughput Rate
- 12-Bit, No Missing Codes over Temperature
- 1.0 LSB Integral Linearity Error
- Buffered Sample and Hold Amplifier
- Precision Voltage Reference
- ± 2.5V Input Signal Range
- 20MHz Input BW Allows Sampling Beyond Nyquist
- Zero Latency/No Pipeline Delay
- Evaluation Board Available

Applications

- High Speed Data Acquisition Systems
- Medical Imaging
- Radar Signal Analysis
- Document and Film Scanners
- Vibration/Waveform Spectrum Analysis
- Digital Servo Control

Description

The HI5800 is a monolithic, 12-bit, sampling Analog-to-Digital Converter fabricated in the HBC10 BiCMOS process. It is a complete subsystem containing a sample and hold amplifier, voltage reference, two-step subranging A/D, error correction, control logic, and timing generator. The HI5800 is designed for high speed applications where wide bandwidth, accuracy and low distortion are essential.

The HI5800 is available in Commercial and Industrial temperature ranges and is offered in a 40 lead Sidebraze and a 44 lead PLCC package.

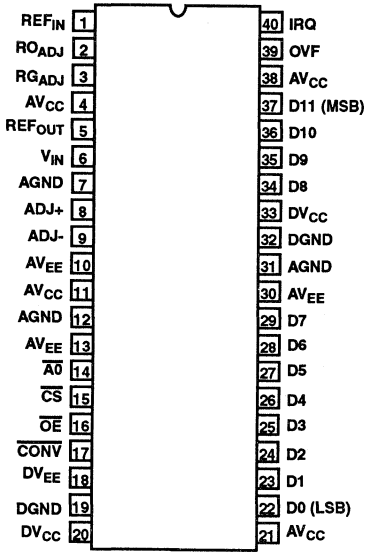
Ordering Information

PART NUMBER	LINEARITY	TEMP. RANGE	PACKAGE
HI5800AID HI5800BID	±2 LSB ±1 LSB	-40°C to +85°C	40 Lead Sidebraze
HI5800JCD HI5800KCD	±2 LSB ±1 LSB	0°C to +70°C	40 Lead Sidebraze
HI5800JCM* HI5800KCM*	±2 LSB ±1 LSB	0°C to +70°C	44 Lead PLCC

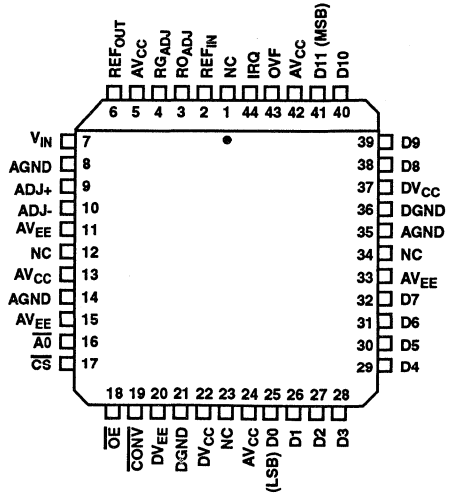
* Consult factory for availability

Pinouts

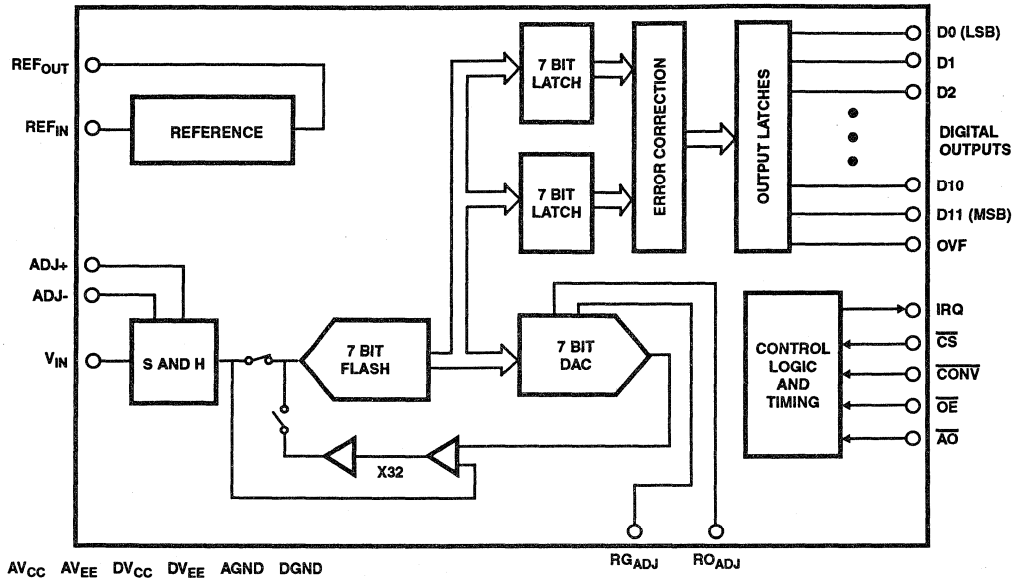
40 LEAD SIDEBRAZE
TOP VIEW



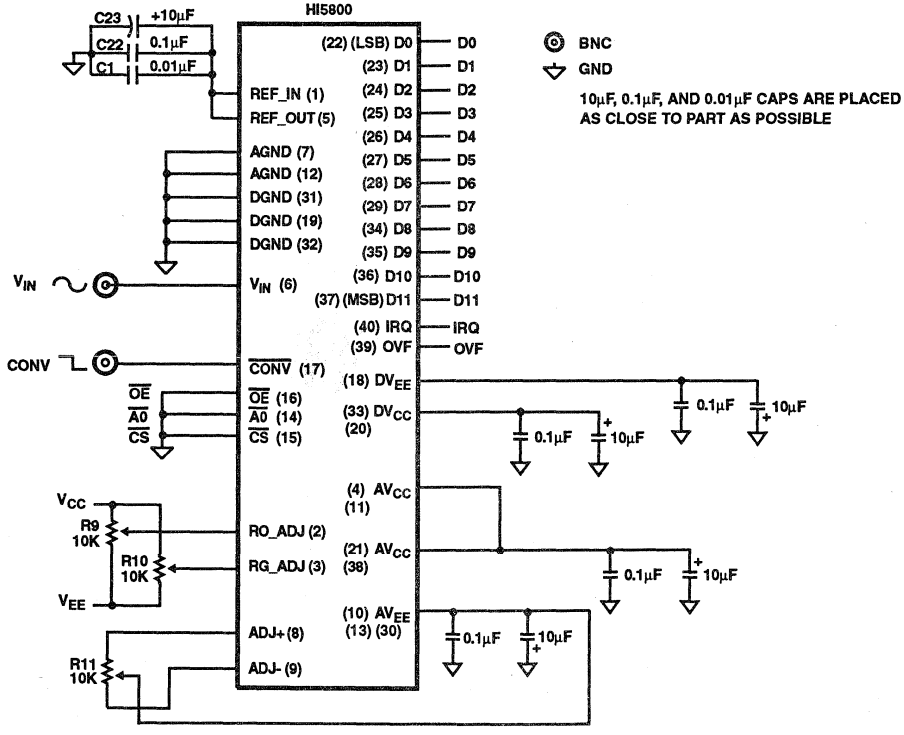
44 LEAD PLCC
TOP VIEW



Functional Block Diagram



Typical Application Schematic



Absolute Maximum Ratings

Supply Voltages
- AV_{CC} or DV_{CC} to GND ..... +5.5V
- AV_{EE} or DV_{EE} to GND ..... -5.5V
- DGND to AGND ..... ±0.3V

Analog Input Pins
- Reference Input REF_{IN} ..... +2.75V
- Signal Input V_{IN} ..... ±(REF_{IN} +0.2V)

RO_{ADJ}, RG_{ADJ}, ADJ+, ADJ- ..... V_{EE} to V_{CC}

Digital I/O Pins ..... GND to V_{CC}

Storage Temperature Range ..... -65°C to +150°C

Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
HI5800JCM/KCM	35°C/W	-
HI5800AID/BID/JCD/KCD	29°C/W	9°C/W

Maximum Power Dissipation +70°C 2.26W

Junction Temperature
- HI5800JCM/KCM/JCD/KCD ..... +150°C
- HI5800AID/BID ..... +175°C

Operating Temperature
- HI5800JCM/KCM/JCD/KCD ..... 0°C to +70°C
- HI5800AID/BID ..... -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used Unless Otherwise Specified

PARAMETER	TEST CONDITION	HI5800JCM/AID/JCD 0°C to +70°C -40°C to +85°C MIN	TYP	MAX	HI5800KCM/BID/KCD 0°C to +70°C -40°C to +85°C MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE								
Resolution		12	-	-	12	-	-	Bits
Integral Linearity Error, INL	F_S = 3MHz, f_{IN} = 45Hz Ramp	-	±0.7	±2	-	±0.7	±1	LSB
Differential Linearity Error, DNL (Guaranteed No Missing Codes)	F_S = 3MHz, f_{IN} = 45Hz Ramp	-	±0.5	±1	-	±0.4	±1	LSB
Offset Error, VOS (Adjustable to Zero)	(Note 7)	-	±2	±15	-	±2	±10	LSB
Full Scale Error, FSE (Adjustable to Zero)	(Note 7)	-	±2	±15	-	±2	±10	LSB
DYNAMIC CHARACTERISTICS (Input Signal Level 0.5dB below full scale)								
Throughput Rate	No Missing Codes	3.0	-	-	3.0	-	-	MSPS
Signal to Noise Ratio (SNR) = RMS Signal / RMS Noise	F_S = 3MHz, f_{IN} = 20kHz F_S = 3MHz, f_{IN} = 1MHz	66 65	69 67	-	68 67	71 69	-	dB dB
Signal to Noise Ratio (SINAD) = RMS Signal / RMS Noise + Distortion	F_S = 3MHz, f_{IN} = 20kHz F_S = 3MHz, f_{IN} = 1MHz	66 65	68 67	-	68 67	70 68	-	dB dB
Total Harmonic Distortion, THD	F_S = 3MHz, f_{IN} = 20kHz F_S = 3MHz, f_{IN} = 1MHz	-	-74 -70	-70 -68	-	-82 -75	-74 -70	dBc dBc
Spurious Free Dynamic Range, SFDR	F_S = 3MHz, f_{IN} = 20kHz F_S = 3MHz, f_{IN} = 1MHz	71 68	76 72	-	76 71	84 75	-	dBc dBc
Intermodulation Distortion, IMD	F_S = 3MHz, f1 = 49kHz, f_2 = 50kHz	-	-74	-66	-	-82	-70	dBc
Differential Gain	F_S = 1MHz	-	0.9	-	-	0.9	-	%
Differential Phase	F_S = 1MHz	-	0.05	-	-	0.05	-	Degrees
Aperture Delay, t_{AD}		-	12	20	-	12	20	ns
Aperture Jitter, t_{AJ}		-	10	20	-	10	20	ps

Electrical Specifications AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	HI5800JCM/AID/JCD 0°C to +70°C -40°C to +85°C			HI5800KCM/BID/KCD 0°C to +70°C -40°C to +85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT								
Input Voltage Range		-	±2.5	±2.7	-	±2.5	±2.7	V
Input Resistance		1	3	-	1	3	-	MΩ
Input Capacitance		-	5	-	-	5	-	pF
Input Current		-	1	±10	-	1	±10	µA
Input Bandwidth		-	20	-	-	20	-	MHz
INTERNAL VOLTAGE REFERENCE								
Reference Output Voltage, REFOUT (Loaded)		2.450	2.500	2.550	2.470	2.500	2.530	V
Reference Output Current	Note 5	2	-	-	2	-	-	mA
Reference Temperature Coefficient		-	20	-	-	20	-	ppm/°C
REFERENCE INPUT								
Reference Input Range		-	2.5	2.6	-	2.5	2.6	V
Reference Input Resistance		-	200	-	-	200	-	Ω
DIGITAL INPUTS								
Input Logic High Voltage, V_{IH}	Note 6	2.0	-	-	2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	-	-	0.8	V
Input Logic Current, I_{IL}	V_{IN} = 0V, 5V	-	1.0	±10	-	1	±10	µA
Digital Input Capacitance, C_{IN}	V_{IN} = 0V	-	5.0	-	-	5	-	pF
DIGITAL OUTPUTS								
Output Logic High Voltage, V_{OH}	I_{OUT} = -160µA	2.4	4.3	-	2.4	4.3	-	V
Output Logic Low Voltage, V_{OL}	I_{OUT} = 3.2mA	-	0.22	0.4	-	0.22	0.4	V
Output Logic High Current, I_{OH}		-0.160	6	-	-0.160	6	-	mA
Output Logic Low Current, I_{OL}		3.2	6	-	3.2	6	-	mA
Output Tri-state Leakage Current, I_{OZ}	V_{OUT} = 0V, 5V	-	±1	±10	-	±1	±10	µA
Digital Output Capacitance, C_{OUT}		-	10	-	-	10	-	pF
TIMING CHARACTERISTICS								
Minimum $\overline{CONV}$ Pulse, t1	(Notes 2, 3)	10	-	-	10	-	-	ns
$\overline{CS}$ to $\overline{CONV}$ Setup Time, t2	(Note 2)	10	-	-	10	-	-	ns
$\overline{CONV}$ to $\overline{CS}$ Setup Time, t3	(Note 2)	0	-	-	0	-	-	ns
Minimum $\overline{OE}$ Pulse, t4	(Notes 2, 4)	15	-	-	15	-	-	ns
$\overline{CS}$ to $\overline{OE}$ Setup Time, t5	(Note 2)	0	-	-	0	-	-	ns

Electrical Specifications AV_{CC} = +5V, DV_{CC} = +5V, AV_{EE} = -5V, DV_{EE} = -5V; Internal Reference Used Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	HI5800JCM/AID/JCD 0°C to +70°C -40°C to +85°C			HI5800KCM/BID/KCD 0°C to +70°C -40°C to +85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
$\overline{OE}$ to $\overline{CS}$ Setup Time, t6	(Note 2)	0	-	-	0	-	-	ns
IRQ Delay from Start Convert, t7	(Note 2)	10	20	25	10	20	25	ns
IRQ Pulse Width, t8		190	205	230	190	205	230	ns
Minimum Cycle Time for Conversion, t9		-	-	333	-	333	333	ns
IRQ to Data Valid Delay, t10	(Note 2)	-5	0	+5	-5	0	+5	ns
Minimum $\overline{A0}$ Pulse, t11	(Notes 2, 4)	10	-	-	10	-	-	ns
Data Access from $\overline{OE}$ Low, t12	(Note 2)	10	18	25	10	18	25	ns
LSB, Nibble Delay from $\overline{A0}$ High, t13	(Note 2)	-	10	20	-	10	20	ns
MSB Delay from $\overline{A0}$ Low, t14	(Note 2)	-	14	20	-	14	20	ns
$\overline{CS}$ to Float Delay, t15	(Note 2)	10	18	25	10	18	25	ns
Minimum $\overline{CS}$ Pulse, t16	(Notes 2, 4)	15	-	-	15	-	-	ns
$\overline{CS}$ to Data Valid Delay, t17	(Note 2)	10	18	25	10	18	25	ns
Output Fall Time, tf	(Note 2)	-	5	20	-	5	20	ns
Output Rise Time, tr	(Note 2)	-	5	20	-	5	20	ns
POWER SUPPLY CHARACTERISTICS								
IV_{CC}		-	180	220	-	180	220	mA
IV_{EE}		-	158	190	-	158	190	mA
IDV_{CC}		-	27	40	-	27	40	mA
IDV_{EE}		-	2.7	5	-	2.7	5	mA
Power Dissipation		-	1.8	2.2	-	1.8	2.2	W
PSRR	V_{CC}, V_{EE} ±5%	-	0.01	0.05	-	0.01	0.05	%/%

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
2. Parameter guaranteed by design or characterization and not production tested.
3. Recommended pulse width for $\overline{CONV}$ is 60ns.
4. Recommended minimum pulse width is 25ns.
5. This is the additional current available from the REF_{OUT} pin with the REF_{OUT} pin driving the REF_{IN} pin.
6. The $\overline{A0}$ pin V_{IH} at -40°C may exceed 2.0V by up to 0.4V at initial power up.
7. Excludes error due to internal reference temperature drift.

Timing Diagrams

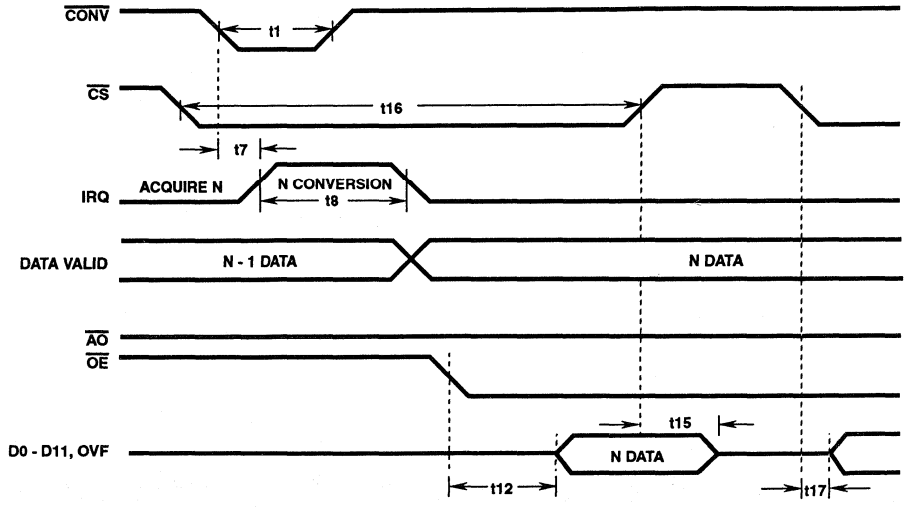


FIGURE 1. SINGLE SHOT TIMING

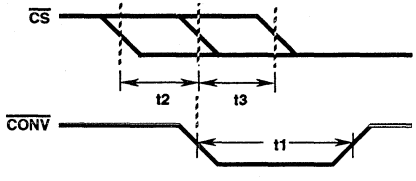


FIGURE 2A. START CONVERSION SETUP TIME

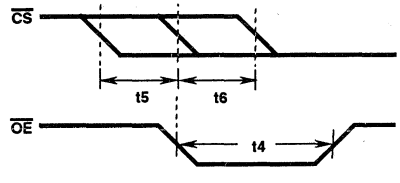


FIGURE 2B. OUTPUT ENABLE SETUP TIME

FIGURE 2.

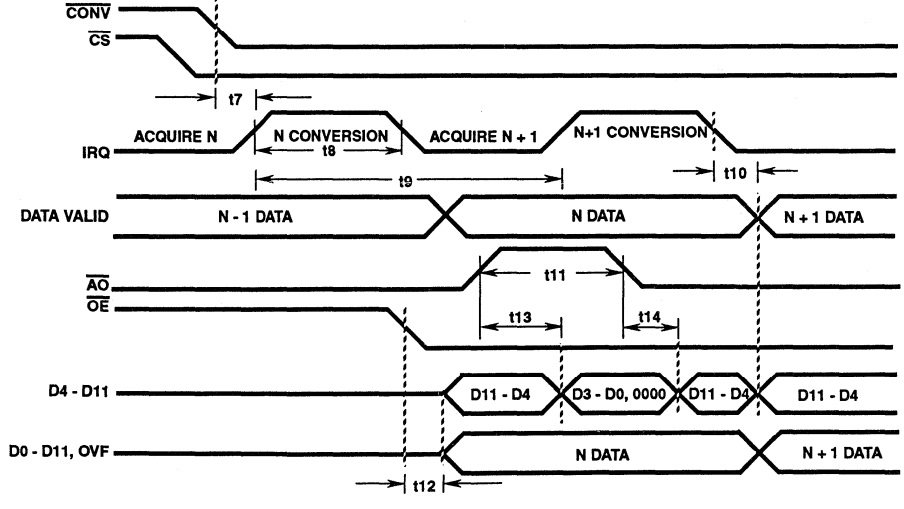


FIGURE 3. CONTINUOUS CONVERSION TIMING

Typical Performance Curves

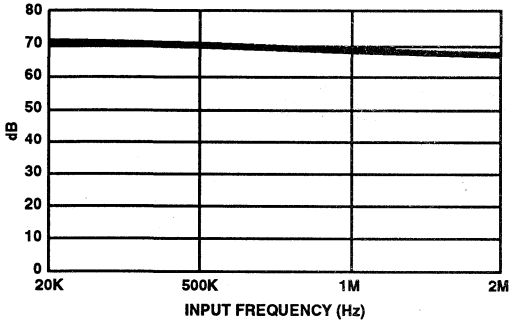


FIGURE 4. TYPICAL SNR vs INPUT FREQUENCY

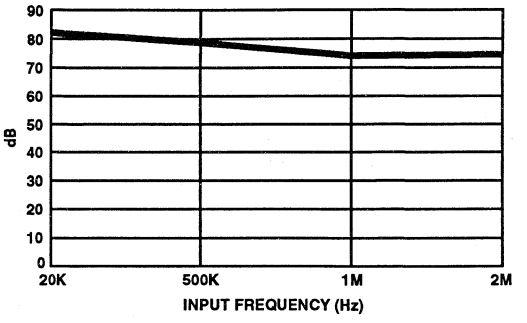


FIGURE 5. TYPICAL THD vs INPUT FREQUENCY

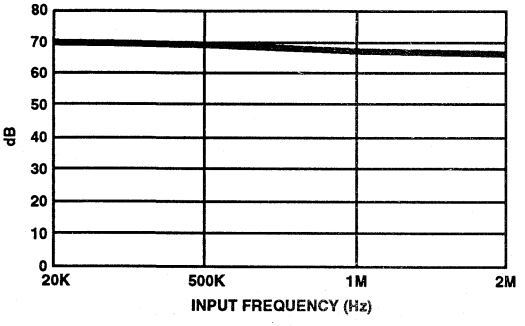


FIGURE 6. TYPICAL SND vs INPUT FREQUENCY

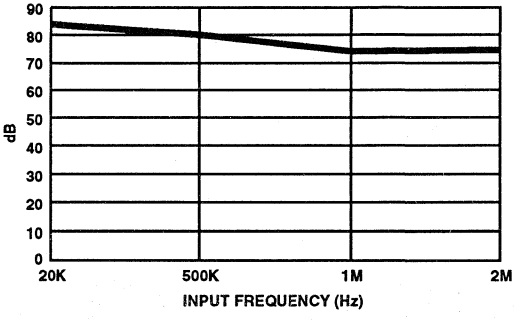


FIGURE 7. TYPICAL SFDR vs INPUT FREQUENCY

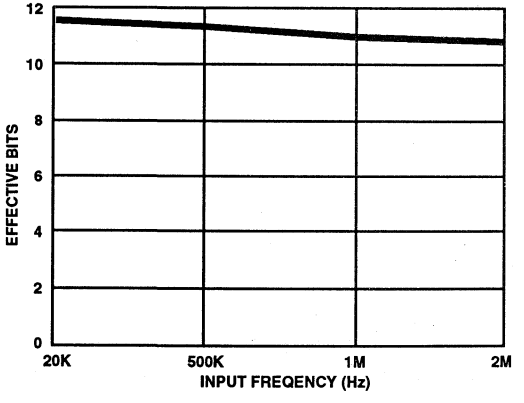


FIGURE 8. TYPICAL EFFECTIVE BITS vs INPUT FREQUENCY

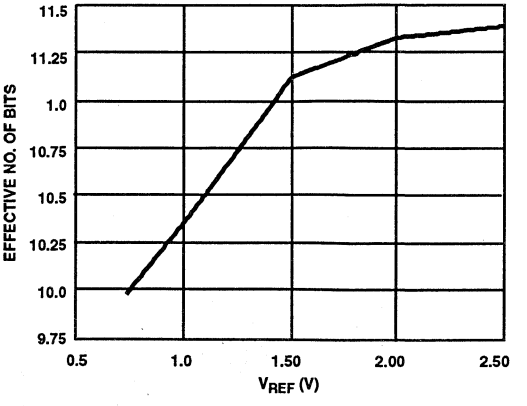


FIGURE 9. EFFECTIVE NUMBER OF BITS vs REFERENCE VOLTAGE (F_S = 3MHz, F_{IN} = 20kHz)

Typical Performance Curves (Continued)

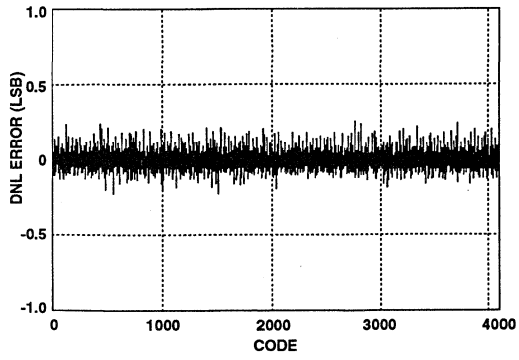


FIGURE 10. DIFFERENTIAL NON-LINEARITY

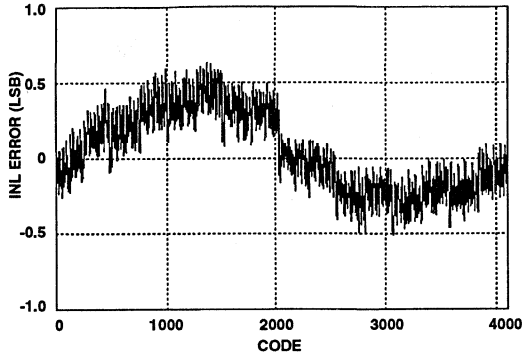


FIGURE 11. INTEGRAL NON-LINEARITY

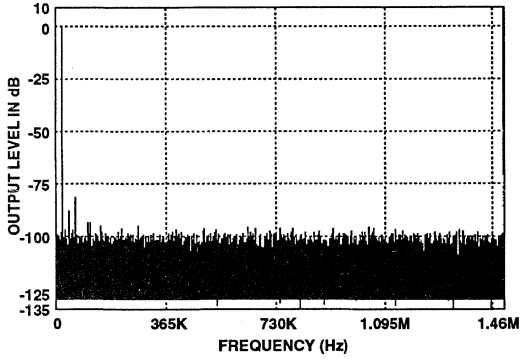


FIGURE 12. FFT SPECTRAL PLOT FOR F_{IN} = 20kHz, F_S = 3MHz

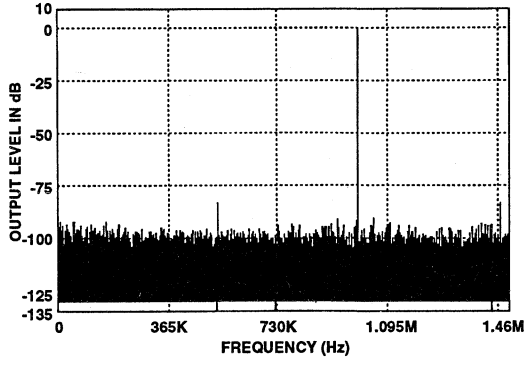


FIGURE 13. FFT SPECTRAL PLOT FOR F_{IN} = 1MHz, F_S = 3MHz

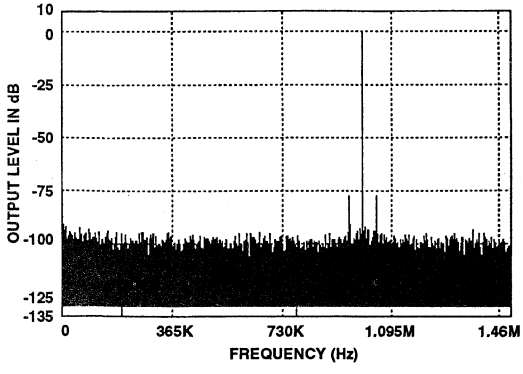


FIGURE 14. FFT SPECTRAL PLOT FOR F_{IN} = 2MHz, F_S = 3MHz

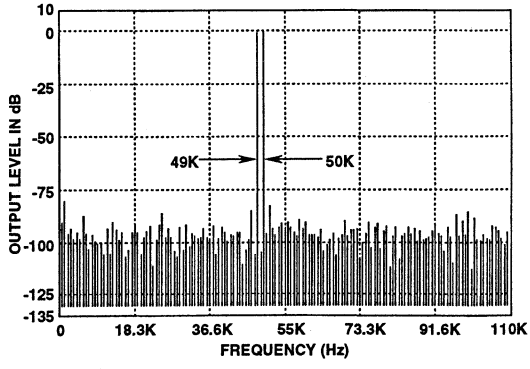


FIGURE 15. INTERMODULATION DISTORTION PLOT FOR F_{IN} = 49kHz, 50kHz at F_S = 3MHz

Pin Description

44 PIN PLCC	40 PIN DIP	PIN NAME	PIN DESCRIPTION
2	1	REF_{IN}	External reference input.
3	2	RO_{ADJ}	DAC offset adjust (Connect to AGND if not used).
4	3	RG_{ADJ}	DAC gain adjust (Connect to AGND if not used).
5	4	AV_{CC}	Analog positive power supply, +5V.
6	5	REF_{OUT}	Internal reference output, +2.5V.
1	-	NC	No connection.
7	6	V_{IN}	Analog input voltage.
8	7	AGND	Analog ground.
9	8	ADJ+	Sample/hold offset adjust (Connect to AGND if not used).
10	9	ADJ-	Sample/hold offset adjust (Connect to AGND if not used).
11	10	AV_{EE}	Analog negative power supply, -5V.
13	11	AV_{CC}	Analog positive power supply, +5V.
14	12	AGND	Analog ground.
15	13	AV_{EE}	Analog negative power supply, -5V.
16	14	A0	Output byte control input, active low. When low, data is presented as a 12 bit word or the upper byte (D11 - D4) in 8 bit mode. When high, the second byte contains the lower LSBs (D3 - D0) with 4 trailing zeroes. See Text.
17	15	CS	Chip Select input, active low. Dominates all control inputs.
12	-	NC	No connection.
18	16	OE	Output Enable input, active low.
19	17	CONV	Convert start input. Initiates conversion on the falling edge. If held low, continuous conversion mode overrides and remains in effect until the input goes high.
20	18	DV_{EE}	Digital negative power supply, -5V.
21	19	DGND	Digital ground.
22	20	DV_{CC}	Digital positive power supply, +5V.
24	21	AV_{CC}	Analog positive power supply, +5V.
25	22	D0	Data bit 0, (LSB).
26	23	D1	Data bit 1.
27	24	D2	Data bit 2.
28	25	D3	Data bit 3.
23	-	NC	No connection
29	26	D4	Data bit 4.
30	27	D5	Data bit 5.
31	28	D6	Data bit 6.
32	29	D7	Data bit 7.
33	30	AV_{EE}	Analog negative power supply, -5V.
35	31	AGND	Analog ground.
36	32	DGND	Digital ground.
37	33	DV_{CC}	Digital positive power supply, +5V.
38	34	D8	Data bit 8.
39	35	D9	Data bit 9.
34	-	NC	No connection.
40	36	D10	Data bit 10.
41	37	D11	Data bit 11 (MSB).
42	38	AV_{CC}	Analog positive power supply, +5V.
43	39	OVF	Overflow output. Active high when either an overrange or underrange analog input condition is detected.
44	40	IRQ	Interrupt ReQuest output. Goes low when a conversion is complete.

Description

The HI5800 is a 12-bit two step sampling analog to digital converter which uses a subranging technique with digital error correction. As illustrated in the block diagram, it uses a sample and hold front end, 7-bit R-2R D/A converter which is laser trimmed to 14 bits accuracy, a 7-bit BiCMOS flash converter, precision bandgap reference, digital controller and timing generator, error correction logic, output latches and BiCMOS output drivers.

The falling edge of the convert command signal puts the sample and hold (S/H) in the hold mode and the conversion process begins. At this point the Interrupt Request (IRQ) line is set high indicating that a conversion is in progress. The output of the S/H circuit drives the input of the 7-bit flash converter through a switch. After allowing the flash to settle, the intermediate output of the flash is stored in the latches which feed the D/A and error correction logic. The D/A reconstructs the analog signal and feeds the gain amplifier whose summing node subtracts the held signal of the S/H and amplifies the residue by 32. This signal is then switched to the flash for a second pass using the input switch. The output of the second flash conversion is fed directly to the error correction which reconstructs the twelve bit word from the fourteen bit input. The logic also decodes the overflow bit and the polarity of the overflow. The output of the error correction is then gated through the read controller to the output drivers. The data is ready on the bus as soon as the IRQ line goes low.

I/O Control Inputs

The converter has four active low inputs ($\overline{CS}$, $\overline{CONV}$, $\overline{OE}$ and $\overline{A0}$) and fourteen outputs (D0 - D11, IRQ and OVF). All inputs and outputs are TTL compatible and will also interface to the newer TTL compatible families. All four inputs are CMOS high input impedance stages and all outputs are BiMOS drivers capable of driving 100pF loads.

In order to initiate a conversion or read the data bus, $\overline{CS}$ should be held low. The conversion is initiated by the falling edge of the $\overline{CONV}$ command. The $\overline{OE}$ input controls the output bus directly and is independent of the conversion process. The data on the bus changes just before the IRQ goes low. Therefore if the $\overline{OE}$ line is held low all the time, the data on the bus will change just before the IRQ line goes low. The byte control signal $\overline{A0}$ is also independent of the conversion process and the byte can be manipulated anytime. When $\overline{A0}$ is low the 12 bits and overflow word is read on the bus. The bus can also be hooked up such that the upper byte (D11 - D4) is read when $\overline{A0}$ is low. When $\overline{A0}$ is high, the lower byte (D3 - D0) is output on the same eight pins with trailing zeros.

In order to minimize switching noise during a conversion, byte manipulations done using the $\overline{A0}$ signal should be done in the single shot mode and $\overline{A0}$ should be changed during the acquisition phase. For accuracy, allow sufficient time for settling from any glitches before the next conversion.

Once a conversion is started, the converter will complete the conversion and acquisition periods irrespective of the input states. If during these cycles another convert command is issued, it will be ignored until the acquire phase is complete.

Stand Alone Operation

The converter can be operated in a stand alone configuration with bus inputs controlling the converter. The conversion will be started on the negative edge of the convert ($\overline{CONV}$) pulse as long as this pulse is less than the converter throughput rate. If the converter is given multiple convert commands, it will ignore all but the first command until such time when the acquisition period of the next cycle is complete. At this point it will start a new conversion on the first negative edge of the input command. This allows the converter to be synchronized to a multiple of a faster external clock. The new output data of the conversion is available on the same cycle at the negative edge of the IRQ pulse and is valid until the next negative edge of the IRQ pulse. Data may be accessed at any time during these cycles. It should be noted that if the data bus is kept enabled all the time ($\overline{OE}$ is low), then the data will be updating just before the IRQ goes low. During this time, the data may not be valid for a few nanoseconds.

Continuous Convert Mode

The converter can be operated at its maximum rate by taking the $\overline{CONV}$ line low (supplying the first negative edge) and holding it low. This enables the continuous convert mode. During this time, at the end of the internal acquisition period, the converter automatically starts a new conversion. The data will be valid between the IRQ negative edges.

Note that there is no pipeline delay on the data. The output data is available during the same cycle as the conversion and is valid until the next conversion ends. This allows data access to both previous and present conversions in the same cycle.

When initiating a conversion or a series of conversions, the last signal ($\overline{CS}$ and $\overline{CONV}$) to arrive dominates the function. The same condition holds true for enabling the bus to read the data ($\overline{CS}$ and $\overline{OE}$). To terminate the bus operations, the first signal ($\overline{CS}$ and $\overline{OE}$) to arrive dominates the function.

Interrupt Request Output

The interrupt request line (IRQ) goes high at the start of each conversion and goes low to indicated the start of the acquisition. During the time that IRQ is high, the internal sample and hold is in hold mode. At the termination of IRQ, the sample and hold switches to acquire mode which lasts approximately 100ns. If no convert command is issued for a period of time, the sample and hold simply remains in acquire mode tracking the analog input signal until the next conversion cycle is initiated. The IRQ line is the only output that is not tri-stateable.

Analog Input, V_{IN}

The analog input of the HI5800 is coupled into the input stage of the Sample and Hold amplifier. The input is a high impedance bipolar differential pair complete with an ESD protection circuit. Typically it has >3MΩ input impedance. With this high input impedance circuit, the HI5800 is easily interfaced to any type of op-amp without a requirement for a high drive capability. Adequate precautions should be taken while driving the input from high voltage output op-amps to

ensure that the analog input pin is not overdriven above the specified maximum limits. For a +2.5V reference, the analog input range is ±2.5V. This input range scales with the value of the external reference voltage if the internal reference is not used. For best performance, the analog ground pin next to the analog input should be utilized for signal return.

Figures 4 and 5 illustrate the use of an input buffer as a level shifter to convert a unipolar signal to the bipolar input used by the HI5800. Figure 4 is an example of a non-inverting buffer that takes a 0 to 2.5V input and shifts it to ±2.5V. The gain can be calculated from

$$V_{OUT} = \left[1 + \frac{R_2}{(R_1 \| R_3)}\right] \times V_{IN} - \left[\frac{R_1}{R_1 + R_3}\right] \times V_{OFFSET}.$$

$$R_1 \| R_3 = \frac{R_1 R_3}{R_1 + R_3}$$

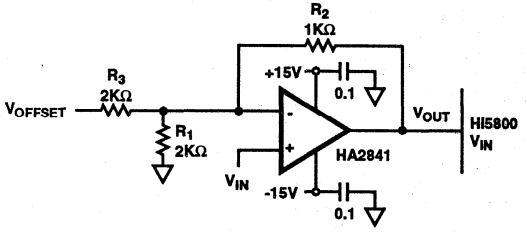


FIGURE 4. NON-INVERTING BUFFER

Figure 5 is an example of an inverting buffer that level shifts a 0V to 5V input to ±2.5V. Its gain can be calculated from

$$V_{OUT} = (-R_2/R_1) \times V_{IN} - (R_2/R_3) \times V_{OFFSET}.$$

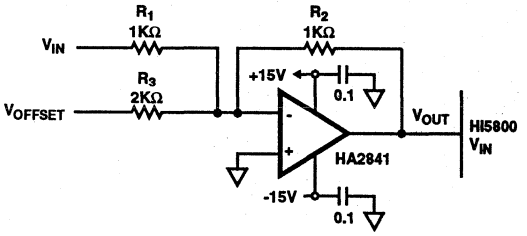


FIGURE 5. INVERTING BUFFER

Note that the correct op amp must be chosen in order to not degrade the overall dynamic performance of the circuit. Recommended op amps are called out in the figures.

Voltage Reference, REF_{OUT}

The HI5800 has a curvature corrected internal band-gap reference generator with a buffer amplifier capable of driving up to 15mA. The band-gap and amplifier are trimmed to give +2.50V. When connected to the reference input pin REF_{IN}, the reference is capable of driving up to 2mA externally. Further loading may degrade the performance of the output voltage. It is recommended that the output of the reference be decoupled with good quality capacitors to reduce the high-frequency noise.

Reference Input, REF_{IN}

The converter requires a voltage reference connected to the REF_{IN} pin. This can be the above internal reference or it can be an external reference. It is recommended that adequate high frequency decoupling is provided at the reference input pin in order to minimize overall converter noise.

A user trying to provide an external reference to a HI5800 is faced with two problems. First, the drift of the reference over temperature must be very low. Second, it must be capable of driving the 200Ω input impedance seen at the REF_{IN} pin of the HI5800. Figure 6 is a recommended circuit for doing this that is capable of 2ppm/°C drift over temperature.

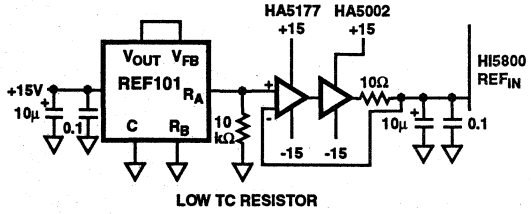


FIGURE 6. EXTERNAL REFERENCE

Supply and Ground Considerations

The HI5800 has separate analog and digital supply and ground pins to help keep digital noise out of the analog signal path. For the best performance, the part should be mounted on a board that provides separate low impedance planes for the analog and digital supplies and grounds. Only connect the two grounds together at one place preferably as close as possible to the part. The supplies should be driven by clean linear regulated supplies. The board should also have good high frequency decoupling capacitors mounted as close as possible to the HI5800.

If the part is powered off a single supply then the analog supply and ground pins should be isolated by ferrite beads from the digital supply and ground pins.

Refer to the Application Note "Using Harris High Speed A/D Converters" (AN9214) for additional suggestions to consider when using the HI5800.

Error Adjustments

For most applications the accuracy of the HI5800 is sufficient without any adjustments. In applications where accuracy is of utmost importance three external adjustments are possible: S/H offset, D/A offset and D/A gain. Figure 7 illustrates the use of external potentiometers to reduce the HI5800 errors to zero.

The D/A offset (RO_{ADJ}) and S/H offset (ADJ+ and ADJ-) trims adjust the voltage offset of the transfer curve while the D/A gain trim (RG_{ADJ}) adjusts the tilt of the transfer curve around the curve midpoint (code 2048). The 10KΩ potentiometers can be installed to achieve the desired adjustment in the following manner.

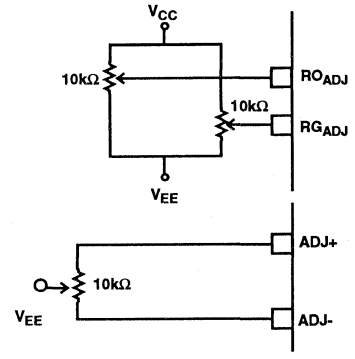


FIGURE 7. D/A OFFSET, D/A GAIN AND S/H OFFSET ADJUSTMENTS.

Typically only one of the offset trimpots needs to be used. The offset should first be adjusted to get code 2048 centered at a desired DC input voltage such as zero volts. Next the gain trim can be adjusted by trimming the gain pot until the 4094 to 4095 code transition occurs at the desired voltage (2.500 LSBs - 1.5 LSBs for a 2.5V reference). The gain trim can also be done by adjusting the gain pot until the code 0 to 1 transition occurs at a particular voltage (-2.5 LSBs + 0.5 LSBs for a 2.5V reference). If a nonzero offset is needed, then the offset pot can be adjusted after the gain trim is finished. The gain trim is simplified if an offset trim to zero is done first with a nonzero offset trim done after the gain trim is finished. The D/A offset and S/H offset trimpots have an identical effect on the converter except that the S/H offset is a finer resolution trim. The D/A offset and D/A gain typically have an adjustment range of ±30 LSBs and the S/H offset typically has an adjustment range of ±20 LSBs.

TABLE 2. I/O TRUTH TABLE

INPUTS				OUTPUT	
CS	CONV	OE	A0	IRQ	FUNCTION
1	X	X	X	X	No operation.
0	0	X	X	X	Continuous convert mode.
0	X	0	0	X	Outputs all 12-bits and OVF or upper byte D11 - D4 in 8 bit mode.
0	X	0	1	X	In 8 bit mode, outputs lower LSBs D3 - D0 followed by 4 trailing zeroes and OVF, (See text).
0	1	X	X	0	Converter is in acquisition mode.
0	X	X	X	1	Converter is busy doing a conversion.
0	X	1	X	X	Data outputs and OVF in high impedance state.

X's = Don't Care

TABLE 3. A/D OUTPUT CODE TABLE

CODE DESCRIPTION $LSB = \frac{2(REF_{IN})}{4096}$	(NOTE 1) INPUT VOLTAGE REF_{IN} = 2.5V (V)	OUTPUT DATA (OFFSET BINARY) MSB → LSB												
		OVF	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
≥+FS	≥ +2.5000	1	1	1	1	1	1	1	1	1	1	1	1	1
+FS - 1LSB	+2.49878	0	1	1	1	1	1	1	1	1	1	1	1	1
+3/4FS	+1.8750	0	1	1	1	0	0	0	0	0	0	0	0	0
+1/2FS	+1.2500	0	1	1	0	0	0	0	0	0	0	0	0	0
+1LSB	+0.00122	0	1	0	0	0	0	0	0	0	0	0	0	1
0	0.0000	0	1	0	0	0	0	0	0	0	0	0	0	0
-1 LSB	-0.00122	0	0	1	1	1	1	1	1	1	1	1	1	1
-1/2FS	-1.2500	0	0	1	0	0	0	0	0	0	0	0	0	0
-3/4FS	-1.8750	0	0	0	1	0	0	0	0	0	0	0	0	0
-FS + 1LSB	-2.49878	0	0	0	0	0	0	0	0	0	0	0	0	1
≤-FS	≤ -2.5000	1	0	0	0	0	0	0	0	0	0	0	0	0

NOTE:

1. The voltages listed above represent the ideal center of each output code shown as a function of the reference voltage.

If no external adjustments are required the following pins should be connected to analog ground (AGND) for optimum performance: RO_{ADJ}, RG_{ADJ}, ADJ+, and ADJ-.

Typical Application Schematic

A typical application schematic diagram for the HI5800 is shown with the block diagram. The adjust pins are shown with 10KΩ potentiometers used for gain and offset adjustments. These potentiometers may be left out and the respective pins should be connected to ground for best untrimmed performance.

Definitions

Static Performance Definitions

Offset, fullscale, and gain all use a measured value of the internal voltage reference to determine the ideal plus and minus fullscale values. The results are all displayed in LSB's.

Offset Error (VOS)

The first code transition should occur at a level $^1/_2$ LSB above the negative fullscale. Offset is defined as the deviation of the actual code transition from this point. Note that this is adjustable to zero.

Fullscale Error (FSE)

The last code transition should occur for a analog input that is $1^1/_2$ LSBs below positive fullscale. Fullscale error is defined as the deviation of the actual code transition from this point.

Differential Linearity Error (DNL)

DNL is the worst case deviation of a code width from the ideal value of 1 LSB. The converter is guaranteed for no missing codes over all temperature ranges.

Integral Linearity Error (INL)

INL is the worst case deviation of a code center from a best fit straight line calculated from the measured data.

Power Supply Rejection (PSRR)

Each of the power supplies are moved plus and minus 5% and the shift in the offset and fullscale error is noted. The number reported is the percent change in these parameters versus fullscale divided by the percent change in the supply.

Dynamic Performance Definitions

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance of the HI5800. A low distortion sine wave is applied to the input, it is sampled, and the output is stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the dynamic performance of the A/D. The sine wave input to the part is -0.5dB down from fullscale for all these tests. Distortion results are quoted in dBc (decibels with respect to carrier) and **DO NOT** include any correction factors for normalizing to full scale.

Signal-to-Noise Ratio (SNR)

SNR is the measured rms signal to rms noise at a specified input and sampling frequency. The noise is the rms sum of all of the spectral components except the fundamental and the first five harmonics.

Signal-to-Noise + Distortion Ratio (SINAD)

SINAD is the measured RMS signal to RMS sum of all other spectral components below the Nyquist frequency excluding DC.

Effective Number Of Bits (ENOB)

The effective number of bits (ENOB) is derived from the SINAD data. ENOB is calculated from:

$$ENOB = (SINAD - 1.76 + V_{CORR}) / 6.02$$

where: $V_{CORR} = 0.5dB$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first 5 harmonic components to the rms value of the measured input signal.

Spurious Free Dynamic Range (SFDR)

SFDR is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component If the harmonics are buried in the noise floor it is the largest peak.

Intermodulation Distortion (IMD)

Nonlinearities in the signal path will tend to generate intermodulation products when two tones, f1 and f2, are present on the inputs. The ratio of the measured signal to the distortion terms is calculated. The IMD products used to calculate the total distortion are (f2-f1), (f2+f1), (2f1-f2), (2f1+f2), (2f2-f1), (2f2+f1), (3f1-f2), (3f1+f2), (3f2-f1), (3f2+f1), (2f2-2f1), (2f2+2f1), (2f1), (2f2), (2f1), (2f2), (4f1), (4f2). The data reflects the sum of all the IMD products.

Full Power Input Bandwidth

Full power bandwidth is the frequency at which the amplitude of the fundamental of the digital output word has decreased 3dB below the amplitude of an input sine wave. The input sine wave has a peak-to-peak amplitude equal to the reference voltage. The bandwidth given is measured at the specified sampling frequency.

Die Characteristics

DIE DIMENSIONS:
202 x 283 x 19 ± 1mils

METALLIZATION:
Metal 1: Type: AlSiCu, Thickness: 6KÅ +1500Å/-750Å
Metal 1: Type: AlSiCu, Thickness: 16KÅ +2500Å/-1100Å

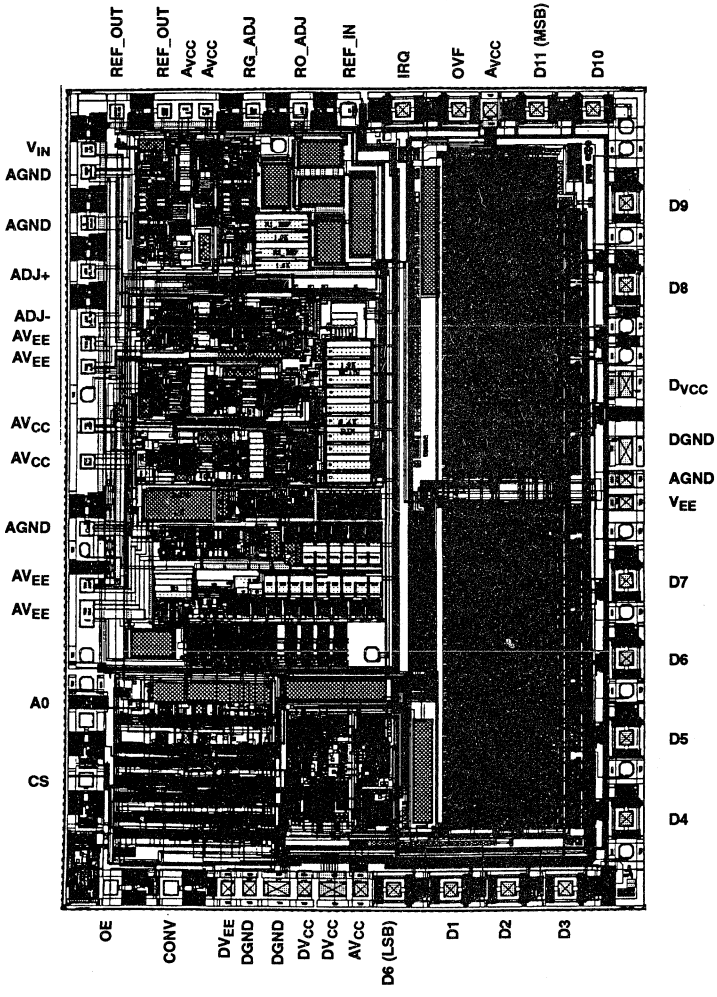
GLASSIVATION:
Type: Sandwich Passivation - Nitride + Undoped Si Glass (USG)
Thickness: Nitride - 4KÅ, USG - 8KÅ, Total - 12KÅ ±2KÅ

TRANSISTOR COUNT: 10K

SUBSTRATE POTENTIAL (POWERED UP): V_{EE}

Metallization Mask Layout

HI5800



HARRIS SEMICONDUCTOR

HI-7153

8 Channel, 10-Bit High Speed Sampling A/D Converter

December 1993

Features

- 5µs Conversion Time
- 8 Channel Input Multiplexer
- 200,000 Channels/Second Throughput Rate
- Over 9 Effective Bits at 20kHz
- No Offset or Gain Adjustments Necessary
- Analog and Reference Inputs Fully Buffered
- On-Chip Track and Hold Amplifier
- µP Compatible Interface
- 2's Complement Data Output
- 150mW Power Consumption
- Only a Single 2.5V Reference Required for a ±2.5V Input Range
- Out-of-Range Flag
- /883 Version Available

Applications

- µP Controlled Data Acquisition Systems
- DSP
  - Avionics
  - Sonar
- Process Control
  - Automotive Transducer Sensing
  - Industrial
- Robotics
- Digital Communications

Description

The HI-7153 is an 8 channel high speed 10 bit A/D converter which uses a Two Step Flash algorithm to achieve through-put rates of 200kHz. The converter features an 8 channel CMOS analog multiplexer with random channel addressing. A unique switched capacitor technique allows a new input voltage to be sampled while a conversion is taking place.

Internal high speed CMOS buffers at both the analog and reference inputs simplifies interface requirements.

A Track and Hold amplifier is included on the chip, consisting of two high speed amplifiers and an internal hold capacitor, reducing external circuitry.

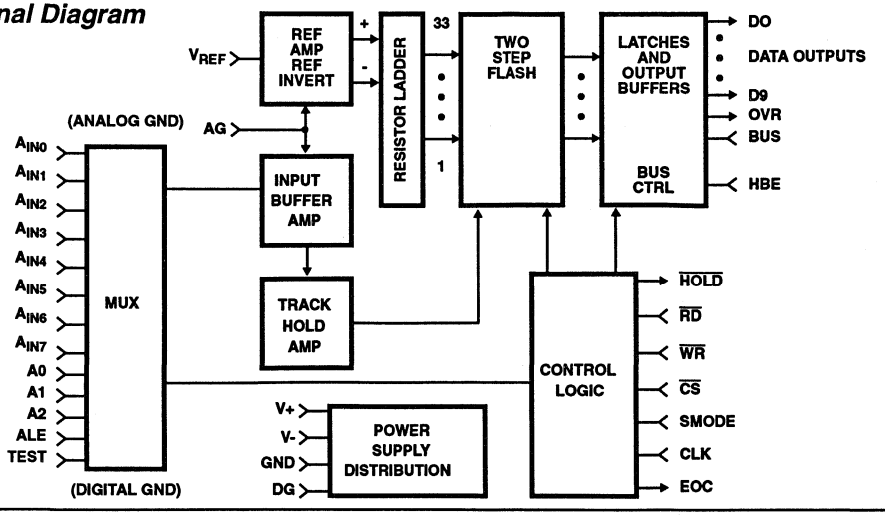
Microprocessor bus interfacing is simplified by the use of standard Chip Select, Read, and Write control signals. The digital three-state outputs are byte organized for bus interface to 8 or 16 bit systems. An Out-of-Range pin, together with the MSB bit, can be used to indicate an under or over-range condition.

The HI-7153 operates with ±5V supplies. Only a single +2.5V reference is required to provide a bipolar input range from -2.5V to +2.5V.

Ordering Information

PART NUMBER	LINEARITY (MAX ILE)	TEMPERATURE RANGE	PACKAGE
HI3-7153J-5	±1.0 LSB	0°C to +70°C	40 Lead Plastic DIP
HI3-7153A-9	±1.0 LSB	-40°C to +85°C	40 Lead Plastic DIP
HI1-7153S-2	±1.0 LSB	-55°C to +125°C	40 Lead Ceramic DIP

Functional Diagram

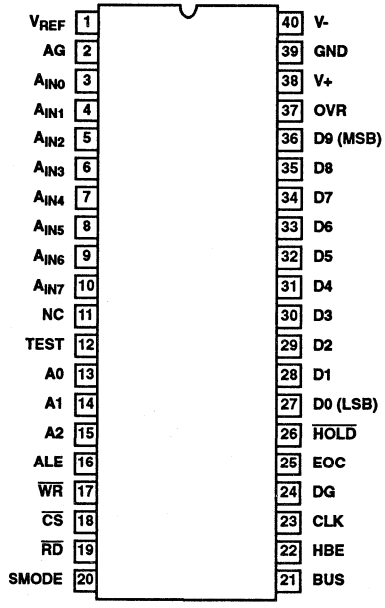


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 2787.3

Pinouts

HI-7153
(CDIP, PDIP)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage
V+ to GND (DG/AG/GND) ..... -0.3V < V+ < +5.7V
V- to GND (DG/AG/GND) ..... -5.7V < V- < +0.3V
Analog InputPins (Note 1)
(A_{IN0} - A_{IN7}, V_{REF}) ..... V- -0.3V < V_{INA} < V+ +0.3V
Digital I/O Pins (Note 1) ..... DG -0.3V < $V_{I/O}$ < V+ +0.3V
(D0 - D9, OVR, CLK, $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, ALE, SMODE, $\overline{HOLD}$, EOC, HBE, BUS, A0 - A2, TEST)
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic ..... 50°C/W
Operating Temperature Range
HI3-7153X-5 ..... 0°C to +70°C
HI3-7153X-9 ..... -40°C to +85°C
HI1-7153X-2 ..... -55°C to +125°C
Power Dissipation (Note 2) 500mW
Derate above +70°C at 10mW/°C

NOTES:

1. Input voltages may exceed the supply voltage, on input or channel at a time, provided the input current is limited to ±10mA
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +5V$, $V- = -5V$, $V_{REF} = +2.50V$, $f_{CLK} = 600kHz$, $t_R = t_F \leq 25ns$, 50% Duty Cycle. All Typical Values have been Characterized but are Not Tested.

(NOTE 4) PARAMETER	SYMBOL	TEMPERATURE	(NOTE 3) J, A, S GRADE MIN	TYP	MAX	UNITS
ACCURACY						
Resolution (Note 5)	RES	$T_A = +25°C$	10	-	-	Bits
		$T_{MIN} \leq T_A \leq T_{MAX}$	10	-	-	Bits
Integral Linearity Error	ILE	$T_A = +25°C$	-	±0.5	±1.0	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±0.75	±1.0	LSB
Differential Linearity Error	DLE	$T_A = +25°C$	-	±0.5	±1.0	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±0.75	±1.0	LSB
Bipolar Offset Error	V_{OS}	$T_A = +25°C$	-	±1.0	±2.5	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±1.5	±3.0	LSB
Unadjusted Gain Error	FSE	$T_A = +25°C$	-	±1.0	±2.5	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±1.5	±3.0	LSB
Channel to Channel Mismatch		$T_A = +25°C$	-	±0.002	-	LSB
		$T_{MIN} \leq T_A \leq T_{MAX}$	-	±0.002	-	LSB

NOTES:

1. Input voltages may exceed the supply voltage, one input or channel at a time, provided the input current is limited to 10mA.
2. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
3. See Ordering Information Table.
4. FSR (Full Scale Range) = 2 x V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.50V).
5. Parameter Not tested. Parameter guaranteed by design, simulation, or characterization.
6. T_{MIN} and T_{MAX} limits guaranteed by +25°C test.

Electrical Specifications T_A = +25°C, V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq$ 25ns, 50% Duty Cycle. All Typical Values have been Characterized but are Not Tested.

(NOTE 1) PARAMETER	SYMBOL	CONDITIONS	+25°C TYP	UNITS
DYNAMIC CHARACTERISTICS				
Signal to Noise Ratio	SNR	f_{IN} = 4.932kHz, ±2.5V	59	dB
		f_{IN} = 14.697kHz, ±2.5V	59	dB
		f_{IN} = 24.462kHz, ±2.5V	58	dB
		f_{IN} = 43.994kHz, ±2.5V	56	dB
Signal to Noise + Distortion	SINAD	f_{IN} = 4.932kHz, ±2.5V	59	dB
		f_{IN} = 14.697kHz, ±2.5V	58	dB
		f_{IN} = 24.462kHz, ±2.5V	55	dB
		f_{IN} = 43.994kHz, ±2.5V	48	dB
Total Harmonic Distortion	THD	f_{IN} = 4.932kHz, ±2.5V	-66	dBc
		f_{IN} = 14.697kHz, ±2.5V	-61	dBc
		f_{IN} = 24.462kHz, ±2.5V	-56	dBc
		f_{IN} = 43.994kHz, ±2.5V	-48	dBc
Spurious-Free Dynamic Range	SFDR	f_{IN} = 4.932kHz, ±2.5V	-76	dB
		f_{IN} = 14.697kHz, ±2.5V	-77	dB
		f_{IN} = 24.462kHz, ±2.5V	-77	dB
		f_{IN} = 43.994kHz, ±2.5V	-74	dB

NOTE:

1. FSR (Full Scale Range) = 2 x V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.50V)

DC Electrical Specifications T_A = +25°C, V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq$ 25ns, 50% Duty Cycle, Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested.

(NOTE 1) PARAMETER	SYMBOL	CONDITIONS	+25°C MIN	+25°C TYP	+25°C MAX	0°C to +75°C MIN	0°C to +75°C MAX	-40°C to +85°C MIN	-40°C to +85°C MAX	-55°C to +125°C MIN	-55°C to +125°C MAX	UNIT
ANALOG MULTIPLEXER INPUT												
Input Range	VIR		$-V_{REF}$	-	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	$-V_{REF}$	$+V_{REF}$	V
Input Resistance	R_{IN}		-	10	-	-	-	-	-	-	-	MΩ
Input Leakage Current	IBI	A_{IN} = 0V	-	0.01	100	-	100	-	100	-	100	nA
On Channel Input Capacitance	$CA_{IN(ON)}$	A_{IN} = 0V, Note 2	-	10	30	-	30	-	30	-	30	pF
Off Channel Input Capacitance	$CA_{IN(OFF)}$	A_{IN} = 0V, Note 2	-	8	20	-	20	-	20	-	20	pF
MUX On-Resistance	$R_{DS(ON)}$	A_{IN} = ±2.5V, I_{IN} =100µA	-	1.1	2.5	-	2.5	-	2.5	-	2.5	KΩ

DC Electrical Specifications T_A = +25°C, V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq$ 25ns, 50% Duty Cycle, Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested. **(Continued)**

(NOTE 1) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Greatest Change in $R_{DS(ON)}$ Between Any Two Channels	$\Delta R_{DS(ON)}$	-2.5V ≤ A_{IN} ≤ +2.5V	-	2.5	-	-	-	-	-	-	-	%
Off-Channel Isolation	OIRR	F_{IN} =100kHz, Note 4	-	-96	-	-	-	-	-	-	-	dB
Channel to Channel Isolation	CCRR	F_{IN} =100kHz, Note 4	-	-83	-	-	-	-	-	-	-	dB
REFERENCE INPUT												
Reference Input Range	VRR	Note 3	2.2	-	2.6	2.2	2.6	2.2	2.6	2.2	2.6	V
Reference Input Bias Current	IBR	V_{REF} = +2.50V	-	0.01	100	-	100	-	100	-	100	nA
Reference Input Capacitance	CV_R	Note 2	-	8	20	-	-	-	-	-	-	pF
LOGIC INPUTS												
Input High Voltage	V_{IH}		2.4	-	-	2.4	-	2.4	-	2.4	-	V
Input Low Voltage	V_{IL}		-	-	0.8	-	0.8	-	0.8	-	0.8	V
Logic Input Current	I_{IL}	V_{IN} = 0V, +5V	-	0.05	1	-	1	-	1	-	1	µA
Input Capacitance	C_{IN}	Note 2	-	7	17	-	-	-	-	-	-	pF
LOGIC OUTPUTS												
Output High Voltage	V_{OH}	I_{OH} = -200µA	2.4	-	-	2.4	-	2.4	-	2.4	-	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6mA	-	-	0.4	-	0.4	-	0.4	-	0.4	V
Output Leakage Current	I_{OL}	$\overline{RD}$ = +5V, V_{OUT} = +5V	-	0.04	1	-	10	-	10	-	10	µA
		$\overline{RD}$ = +5V, V_{OUT} = 0V	-1	-0.01	-	-10	-	-10	-	-10	-	µA
Output Capacitance	C_{OUT}	High-Z State, Note 2	-	7	15	-	-	-	-	-	-	pF
POWER SUPPLY VOLTAGE RANGE												
	V+	Functional Operation Only, Note 3	4.5	5.0	5.5	4.5	5.5	4.5	5.5	4.5	5.5	V
	V-		-4.5	-5.0	-5.5	-4.5	-5.5	-4.5	-5.5	-4.5	-5.5	V
POWER SUPPLY REJECTION												
V+, V- Gain Error	ΔFSE	V+ = 5V, V- = -4.75V, -5.25V	-	0.1	0.5	-	0.6	-	0.6	-	0.8	LSB
		V- = -5V, V+ = 4.75V, 5.25V	-	0.1	0.5	-	0.6	-	0.6	-	0.8	LSB

DC Electrical Specifications T_A = +25°C, V+ = +5V, V- = -5V, V_{REF} = +2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq 25$ns, 50% Duty Cycle, Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested. **(Continued)**

(NOTE 1) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
POWER SUPPLY REJECTION (Continued)												
V+, V- Offset Error	ΔVOS	V+ = 5V, V- = -4.75V, -5.25V	-	0.15	0.5	-	0.6	-	0.6	-	0.8	LSB
		V- = -5V, V+ = 4.75V, 5.25V	-	0.15	0.5	-	0.6	-	0.6	-	0.8	LSB
SUPPLY CURRENTS												
V+ Supply Current	I+	V+ = 5V, V- = -5V, V_{IN} = 0V, Digital Outputs Are Unloaded	-	20	30	-	30	-	30	-	30	mA
V- Supply Current	I-		-	-10	-15	-	-15	-	-15	-	-15	mA
GND Current	IGND		-	-8	-	-	-	-	-	-	-	mA
DG Current	IDG		-	-2	-	-	-	-	-	-	-	mA
AG Current	IAG		-	0.02	-	-	-	-	-	-	-	μA

NOTES:

1. FSR (Full Scale Range) = 2 x V_{REF} (5.00V at V_{REF} = 2.50V). LSB (Least Significant Bit) = FSR/1024 (4.88mV at V_{REF} = 2.50V)
2. Parameter Not tested. Parameter guaranteed by design, simulation, or characterization
3. Functionality is guaranteed by negative GAIN ERROR test.
4. Channel Isolation is tested with an input signal of ±2.5Vp-p, 100kHz and the measured pin is loaded with 100Ω to GND

DC Electrical Specifications T_A = +25°C, V+ = 5V ±10%, V- = -5V, V_{REF} = 2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq 25$ns, 50% Duty Cycle, C_L = 100pF (Including Stray for D0-D9, OVR, $\overline{HOLD}$), Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested.

(NOTE 4) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
TIMING CHARACTERISTICS												
Continuous Conversion Time	t_{SPS}	Note 2	-	-	5	-	5	-	5	-	5	μs
		Note 9	60	-	-	60	-	60	-	60	-	μs
		Notes 2, 8	-	-	$3t_{CLK}$	-	$3t_{CLK}$	-	$3t_{CLK}$	-	$3t_{CLK}$	μs
Conversion Time, First Conversion	t_{CONV}	Notes 1, 9	-	-	$4t_{CLK}$ + 0.63	-	$4t_{CLK}$ + 0.75	-	$4t_{CLK}$ + 0.75	-	$4t_{CLK}$ + 0.8	μs
Continuous Throughput	t_{CYC}	Note 2	-	-	$t_{CLK}/3$	-	$t_{CLK}/3$	-	$t_{CLK}/3$	-	$t_{CLK}/3$	CPS
Clock Period	t_{CLK}		-	$1/f_{CLK}$	-	-	-	-	-	-	-	-
Clock Input Duty Cycle	D	Note 9	45	50	55	45	55	45	55	45	55	%
ALE Pulse Width	t_{ALEW}	Note 9	30	15	-	40	-	40	-	50	-	ns
Address Setup Time	t_{AS}	Note 9	40	15	-	80	-	80	-	80	-	ns
Address Hold Time	t_{AH}		0	-16	-	0	-	0	-	0	-	ns
$\overline{WR}$ Pulse Width	t_{WRL}	Notes 1, 3, 9	100	20	$t_{CLK}/2$	100	$t_{CLK}/2$	100	$t_{CLK}/2$	100	$t_{CLK}/2$	ns

DC Electrical Specifications T_A = +25°C, V+ = 5V ±10%, V- = -5V, V_{REF} = 2.50V, f_{CLK} = 600kHz, $t_R = t_F \leq 25$ns, 50% Duty Cycle, C_L = 100pF (Including Stray for D0-D9, OVR, $\overline{HOLD}$), Unless Otherwise Specified. All Typical Values have been Characterized but are Not Tested. **(Continued)**

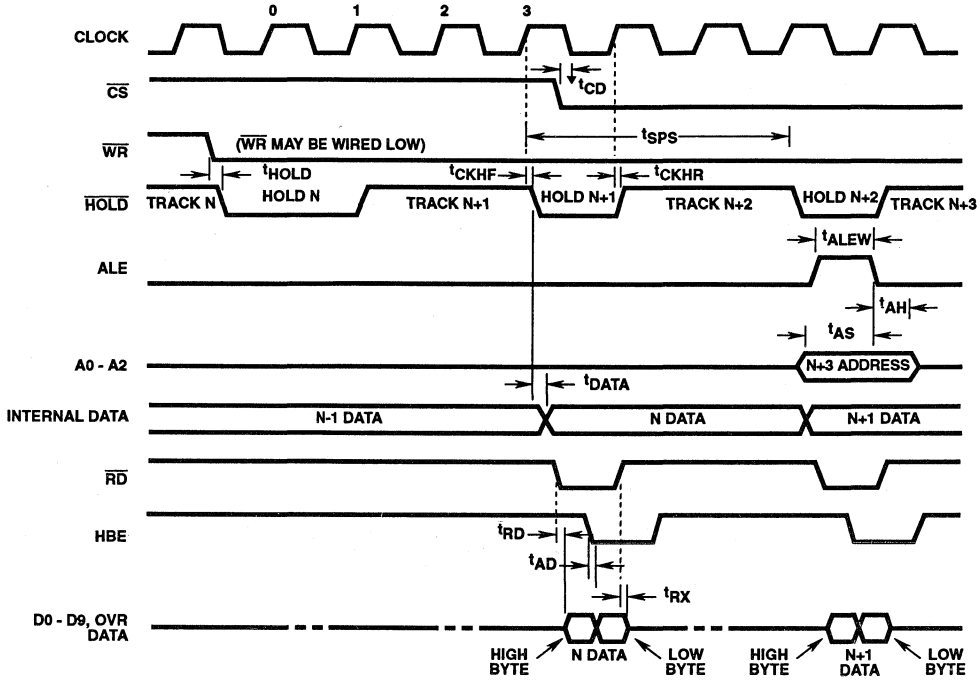
(NOTE 4) PARAMETER	SYMBOL	CONDITIONS	+25°C			0°C to +75°C		-40°C to +85°C		-55°C to +125°C		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$\overline{WR}$ to EOC Low	t_{WREOC}	Notes 1, 9	-	80	130	-	160	-	160	-	160	ns
$\overline{WR}$ to $\overline{HOLD}$ Delay	t_{HOLD}	Notes 1, 9	-	80	150	-	170	-	170	-	170	ns
Clock to $\overline{HOLD}$ Rise Delay	t_{CKHR}	Note 9	150	265	450	140	500	120	500	120	500	ns
Clock to $\overline{HOLD}$ Fall Delay	t_{CKHF}	Notes 2, 9	50	95	200	40	225	40	225	40	225	ns
Clock to EOC High	t_{CKEOC}	Notes 1, 9	-	460	630	-	750	-	750	-	800	ns
$\overline{HOLD}$ to DATA Change	t_{DATA}	Notes 2, 9	100	200	350	90	400	90	400	90	400	ns
$\overline{CS}$ to DATA	t_{CD}	Note 9	-	40	70	-	85	-	85	-	85	ns
HBE to DATA	t_{AD}	Note 9	-	30	50	-	70	-	70	-	70	ns
$\overline{RD}$ LOW to Active	t_{RD}	Notes 6, 9	-	70	100	-	125	-	125	-	125	ns
$\overline{RD}$ HIGH to Inactive	t_{RX}	Notes 7, 9	-	30	60	-	70	-	70	-	70	ns
Output Rise Time	t_R	Notes 5, 9	-	20	40	-	60	-	60	-	60	ns
Output Fall Time	t_F	Notes 5, 9	-	15	30	-	50	-	50	-	50	ns

NOTES:

1. Slow memory mode timing
2. Fast memory or DMA mode of operation, except the first conversion which is equal to t_{CONV}
3. Maximum specification to prevent multiple triggering with $\overline{WR}$
4. All input drive signals are specified with $t_R = t_F \leq 10$ns and shall swing from 0.4V to 2.4V for all timing specifications. A signal is considered to change state as it crosses a 1.4V threshold (except t_{RD} and t_{RX})
5. t_R and t_F load is C_L = 100pF (including stray capacitance) to DG and is measured from the 10% - 90% point
6. t_{RD} is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. High-Z to V_{OH} is measured with R_L = 2.5KΩ and C_L = 100pF (including stray) to DG. High-Z to V_{OL} is measured with R_L = 2.5KΩ to V+ and C_L = 100pF (including stray) to DG
7. t_{RX} is the time required for the data output level to change by 10% in response to $\overline{RD}$ crossing a voltage level of 1.4V. V_{OH} to High-Z is measured with R_L = 2.5KΩ and C_L = 10pF (including stray) to DG. V_{OL} to High-Z is measured with R_L = 2.5KΩ to V+ and C_L = 10pF (including stray) to DG
8. For clock frequencies other than 600kHz
9. Parameter Not Tested. Parameter guaranteed by design, simulation, or characterization

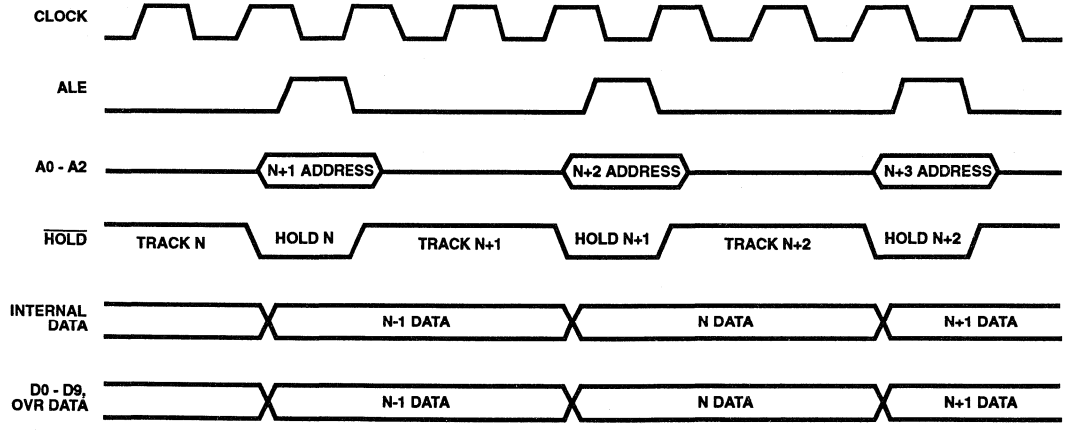
Timing Diagrams

FAST MEMORY MODE (8 BIT DATA BUS)



CONDITIONS: SMODE = DG. Bus = DG
NOTE: With SMODE = DG, the internal logic diables the output latches from being updated during a read. The EOC output is LOW continuously.

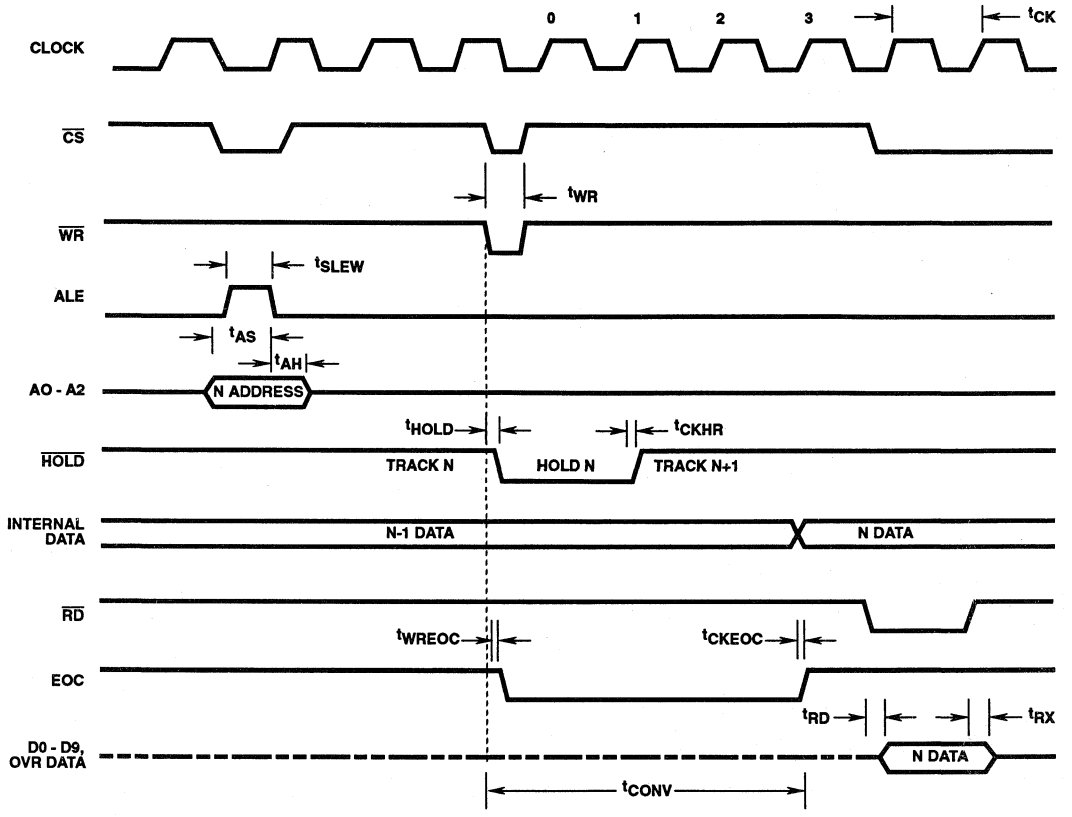
DMA MODE (16 BIT DATA BUS)



CONDITIONS: SMODE = V+, CS = WR = RD = DG, Bus = V+, HBE = DG or V+
NOTE: EOC output is low continuously

Timing Diagrams (Continued)

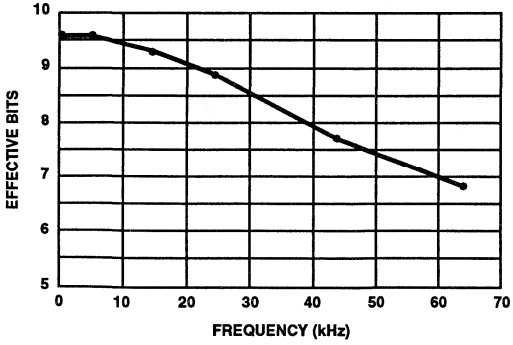
SLOW MEMORY MODE (16 BIT DATA BUS)



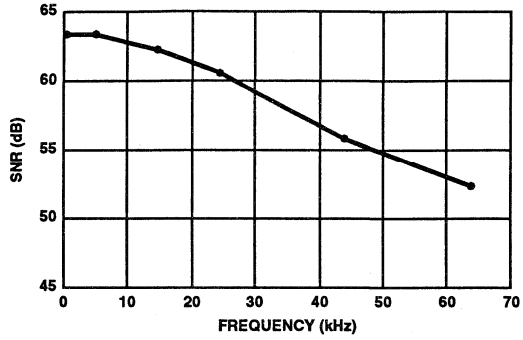
CONDITIONS: SMODE = V+, Bus = V+, HBE = DG or V+

Typical Dynamic Performance Characteristics

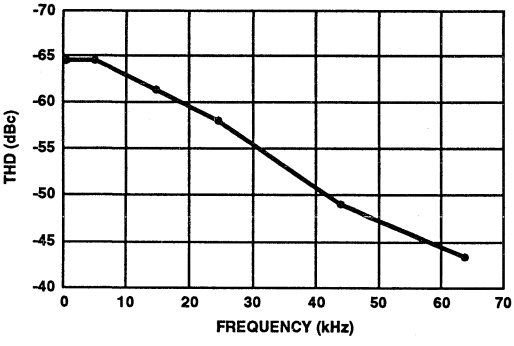
EFFECTIVE NUMBER OF BITS



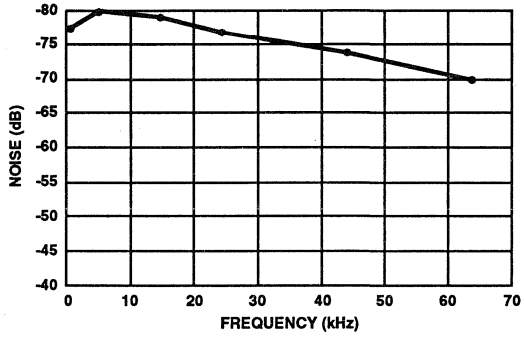
SIGNAL-TO-NOISE RATIO



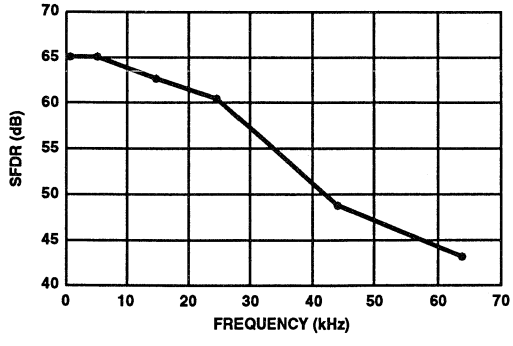
TOTAL HARMONIC DISTORTION



PEAK NOISE

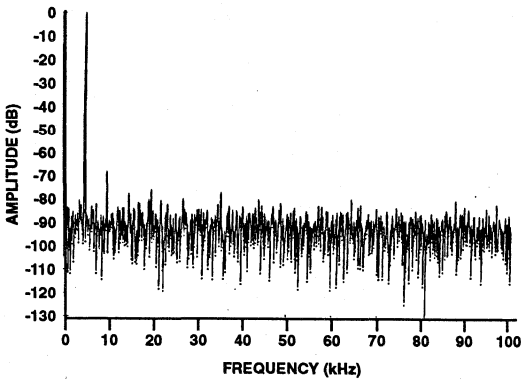


SPURIOUS-FREE DYNAMIC RANGE



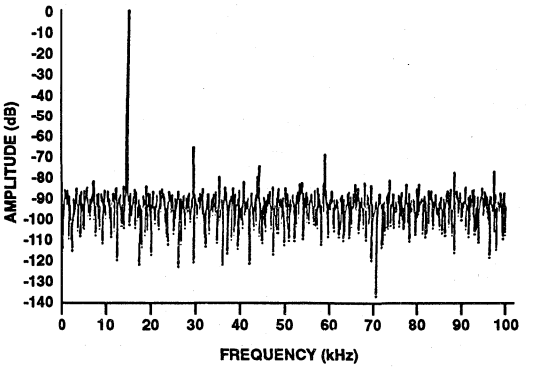
Typical Dynamic Performance Characteristics (Continued)

FFT SPECTRUMS



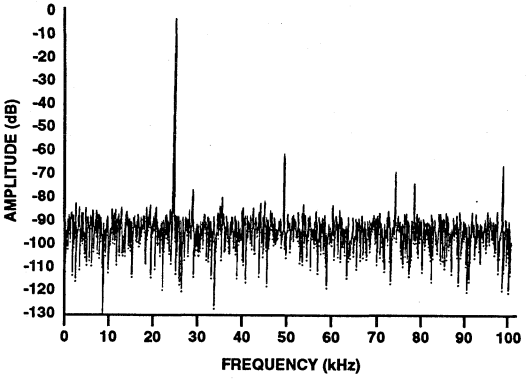
NOTES:

INPUT FREQUENCY: 4931Hz
SAMPLING RATE: 200kHz
SNR: 59.40dB
THD: -67.26dB
PEAK NOISE: -75.98dB
SPURIOUS FREE DYNAMIC RANGE: -68.36dB
3RD HARMONIC: -77.19dB



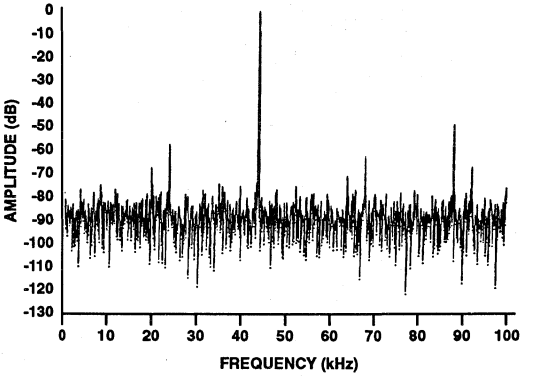
NOTES:

INPUT FREQUENCY: 14697Hz
SAMPLING RATE: 200kHz
SNR: 58.98dB
THD: -61.44dB
PEAK NOISE: -77.29dB
SPURIOUS FREE DYNAMIC RANGE: -63.42dB
3RD HARMONIC: -72.44dB



NOTES:

INPUT FREQUENCY: 24462Hz
SAMPLING RATE: 200kHz
SNR: 58.36dB
THD: -55.59dB
PEAK NOISE: -76.65dB
SPURIOUS FREE DYNAMIC RANGE: -57.72dB
3RD HARMONIC: -64.53dB



NOTES:

INPUT FREQUENCY: 4399Hz
SAMPLING RATE: 200kHz
SNR: 56.26dB
THD: -48.19dB
PEAK NOISE: -74.34dB
SPURIOUS FREE DYNAMIC RANGE: -48.66dB
3RD HARMONIC: -62.87dB

Pin Description

DIP PIN	SYMBOL	DESCRIPTION
1	V_{REF}	Reference voltage input (+2.50V)
2	AG	Analog ground reference (0V)
3	A_{IN0}	Analog input channel 0
4	A_{IN1}	Analog input channel 1
5	A_{IN2}	Analog input channel 2
6	A_{IN3}	Analog input channel 3
7	A_{IN4}	Analog input channel 4
8	A_{IN5}	Analog input channel 5
9	A_{IN6}	Analog input channel 6
10	A_{IN7}	Analog input channel 7
11	NC	No connect or tie to V+ only
12	TEST	Test pin. Connect to DG for normal operation
13	A0	Mux address input. (LSB) Active high.
14	A1	Mux address input. (LSB) Active high.
15	A2	Mux address input. (MSB) Active high.
16	ALE	Mux address enable. When high, the latch is transparent. Address data is latched on the falling edge.
17	$\overline{WR}$	Write input. With $\overline{CS}$ low, starts conversion when pulsed low; continuous conversions when kept low.
18	$\overline{CS}$	Chip select input. Active low.
19	$\overline{RD}$	Read input. With $\overline{CS}$ low, enables output buffers when pulsed low; outputs updated at the end of conversion.
20	SMODE	Slow memory mode input. Active high.

DIP PIN	SYMBOL	DESCRIPTION
21	BUS	Bus select input. High = all outputs enabled together D0-D9, OVR Low = Outputs enabled by HBE
22	HBE	Byte select (HBE/LBE) input for 8 bit bus. High = High byte select, D8 - D9, OVR Low = Low byte select, D0 - D7
23	CLK	Clock input. TTL compatible.
24	DG	Digital ground (0V)
25	EOC	End-of-conversion status. Pulses high at the end-of-conversion.
26	$\overline{HOLD}$	Start of conversion status. Pulses low at the start-of-conversion.
27	D0	Bit 0 (LSB)
28	D1	Bit 1
29	D2	Bit 2 Output
30	D3	Bit 3 Data
31	D4	Bit 4 Bits
32	D5	Bit 5
33	D6	Bit 6
34	D7	Bit 7
35	D8	Bit 8
36	D9	Bit 9 (MSB)
37	OVR	Out of Range flag. Valid at end of conversion when output exceeds full scale.
38	V+	Positive supply voltage input (+5.0V)
39	GND	Ground return for comparators (0V)
40	V-	Negative supply voltage input (-5.0V)

Detailed Description

The HI-7153 is an 8 channel high speed 10 bit A/D converter which achieves throughput rates of 200kHz by use of a Two Step Flash algorithm. A pipelined operation has been achieved through the use of switched capacitor techniques which allows the device to sample a new input voltage while a conversion is taking place. The 8 channel multiplexer can be randomly addressed. The HI-7153 requires a single reference input of +2.5V, which is internally inverted to -2.5V, thereby allowing an input range of -2.5V to +2.5V. The ten bits are two's complement coded. The analog and reference inputs are internally buffered by high speed CMOS buffers, which greatly simplifies the external analog drive requirements for the device.

Analog to Digital

Section The HI-7153 uses a conversion technique which is generally called a "Two Step Flash" algorithm. This algorithm enables very fast conversion rates without the penalty of high power dissipation or high cost. A detailed functional diagram is presented in Figure 1.

The reference input to the HI-7153 is buffered by a high speed CMOS amplifier which is used to drive one end of the resistor string. Another high speed amplifier configured in the inverting unity gain mode inverts the reference voltage with respect to analog ground and forces it onto the other end of the resistor string. Both reference amplifiers are offset trimmed during manufacturing in order to increase the accuracy of the HI-7153 and to simplify its usage.

The input voltage is first converted into a 5 bit result (plus Out of Range information) by the flash converter. This flash converter consists of an array of 33 auto-zeroed comparators which perform a comparison between the input voltage and subdivisions of the reference voltage. These subdivisions of the reference voltage are formed by forcing the reference voltage and its negative on the two ends of a string of 32 resistors.

The 5 bit result of the first flash conversion is latched into the upper five bits of double buffered latches. It is also converted back into an analog signal by choosing the ladder voltage which is closest to but less than the input voltage. The selected voltage (VTAP) is then subtracted from the input voltage. The residual is then amplified by a factor of 32 and referenced to the negative reference voltage (VSCA = 32(VIN - VTAP) + V_{REF-}). This subtraction and amplification operation is performed by a Switched Capacitor amplifier (SCA). The output of the SCA amplifier is between the positive and negative reference voltages and can therefore be digitized by the original 5 bit flash converter (second flash conversion).

The 5 bit result of the second flash conversion is latched into the lower five bits of double buffered latches. At the end of a conversion, 10 bits of data plus an Out of Range bit are latched into the second level of latches and can then be put on the digital output pins.

The conversion takes place in three clock cycles and is illustrated in Figure 2. When the conversion begins, the track and hold goes into its hold mode for 1 clock cycle. During the first half clock cycle the comparator array is in its auto-zero mode and it samples the input voltage. During the second half clock cycle, the comparators make a comparison between the input voltage and the ladder voltages. At the beginning of the third half clock cycle, the first most significant 5 bit result becomes available. During the first clock cycle, the SCA was sampling the input voltage. After the first flash result becomes available and a ladder tap voltage has been selected the SCA amplifies the residue between the input and ladder tap voltages. During the next three half clock cycles, while the SCA output is settling to its required accuracy, the comparators go into their auto-zero mode and sample this voltage. During the sixth half clock cycle, the comparators perform another comparison whose 5 bit result becomes available on the next clock edge.

Reference Input

The reference input to the HI-7153 is buffered by a high speed CMOS amplifier. The reference input range is 2.2V to 2.6V. The reference input voltage should be applied following the application of V+ and V- supplies.

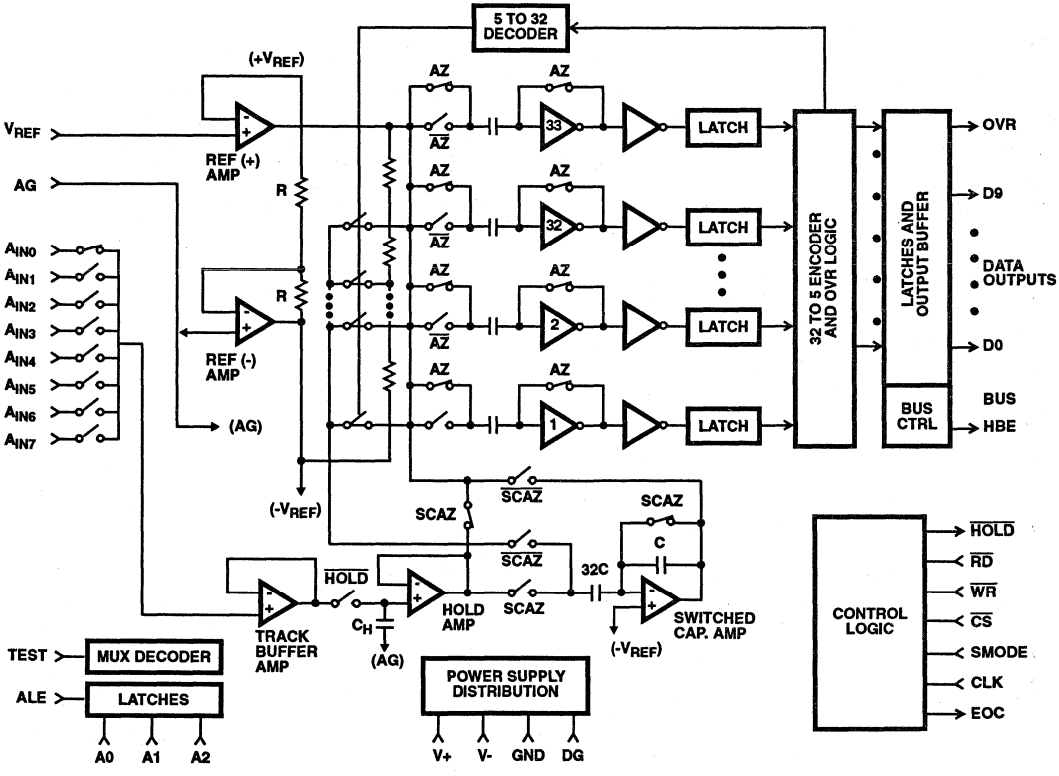


FIGURE 1. DETAILED BLOCK DIAGRAM

Analog Multiplexer

The multiplexer channel assignments are shown in Table 1 and can be randomly addressed. Address inputs A0 - A2 are binary coded and are TTL/CMOS compatible. During power up the circuit is initialized and multiplexer channel A_{IN0} is selected. The multiplexer address is transparent when ALE is high and $\overline{CS}$ is low. The address data is latched on the falling edge of the ALE signal. The multiplexer channel acquisition timing (Timing Diagrams, Slow Memory Mode) occurs approximately 500ns after the rising edge of HOLD. The multiplexer features a typical break-before-make switch action of 44ns.

Track And Hold

A Track and Hold amplifier has been fully integrated on the front end of the A/D converter. Because of the sampling nature of this A/D converter, the input is required to stay constant only during the first clock cycle. Therefore, the Track and Hold (T/H) amplifier "holds" the input voltage only during the first clock cycle and it acquires the input voltage for the next conversion during the remaining two clock cycles. The high input impedance of the T/H input amplifier simplifies analog interfacing. Input signals up to $\pm V_{REF}$ can be directly connected to the A/D without buffering. The T/H amplifier typically settles to within $^1/_4$ LSB in 1.5µs. The A/D output code table is presented in Table 2.

The timing signals for the Track and Hold amplifier are generated internally, and are also provided externally (HOLD) for synchronization purposes.

All of the internal amplifiers are offset trimmed during manufacturing to give improved accuracy and to minimize the number of external components. If necessary, offset error can be adjusted by using digital post correction.

TABLE 1. MULTIPLEXER CHANNEL SELECTION

ADDRESS AND CONTROL INPUTS					ANALOG CHANNEL SELECTED
A2	A1	A0	$\overline{CS}$	ALE	
0	0	0	0	1	A_{IN0}
0	0	1	0	1	A_{IN1}
0	1	0	0	1	A_{IN2}
0	1	1	0	1	A_{IN3}
1	0	0	0	1	A_{IN4}
1	0	1	0	1	A_{IN5}
1	1	0	0	1	A_{IN6}
1	1	1	0	1	A_{IN7}

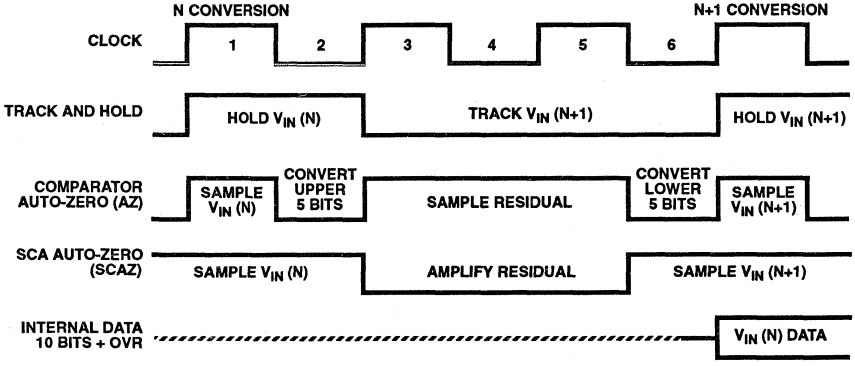


FIGURE 2. INTERNAL ADC TIMING DIAGRAM

TABLE 2. A/D OUTPUT CODE TABLE

ANALOG INPUT*		OUTPUT DATA (2'S COMPLEMENT)										
LSB = $2(V_{REF})/1024$	V_{REF} = 2.500V	OVR	MSB 9	8	7	6	5	4	3	2	1	LSB 0
≥ $+V_{REF}$	2.500 to V+ (+OVR)	1	0	0	0	0	0	0	0	0	0	0
$+V_{REF}$ - 1LSB	2.49512 (+Full Scale)	0	0	1	1	1	1	1	1	1	1	1
+1LSB	0.00488	0	0	0	0	0	0	0	0	0	0	1
0	0.000	0	0	0	0	0	0	0	0	0	0	0
-1LSB	-0.00488	0	1	1	1	1	1	1	1	1	1	1
$-V_{REF}$	-2.500 (-Full Scale)	0	1	0	0	0	0	0	0	0	0	0
≤ $-V_{REF}$ - 1LSB	2.50488 to V- (-OVR)	1	1	0	0	0	0	0	0	0	0	0

* The voltages listed above are the ideal centers of each output code shown as a function of its associated reference voltage.

Dynamic Performance

Fast Fourier Transform (FFT) techniques are used to evaluate the dynamic performance for one channel of the A/D system. A low distortion sine wave is applied to the input of the A/D converter. The input is sampled by the A/D and its output stored in RAM. The data is then transformed into the frequency domain with a 4096 point FFT and analyzed to evaluate the converters dynamic performance such as SNR and THD. See typical performance characteristics.

Signal-To-Noise Ratio

The signal to noise ratio (SNR) is the measured rms signal to rms sum of noise at a specified input and sampling frequency. The noise is the rms sum of all except the fundamental and the first five harmonic signals. The SNR is dependent on the number of quantization levels used in the converter. The theoretical SNR for an N-bit converter with no differential or integral linearity error is: SNR = (6.02N + 1.76)dB. For an ideal 10 bit converter the SNR is 62dB. Differential and integral linearity errors will degrade SNR.

$$SNR = 10\log\frac{\text{Sinewave Signal Power}}{\text{Total Noise Power}}$$

Signal-To-Noise + Distortion Ratio

SINAD is the measured rms signal to rms sum of noise plus harmonic power and is expressed by the following.

$$SINAD = 10\log\frac{\text{Sinewave Signal Power}}{\text{Noise + Harmonic Power (2nd thru 6th)}}$$

Effective Number of Bits

The effective number of bits (ENOB) is derived from the SINAD data;

$$ENOB = \frac{SINAD - 1.76}{6.02}$$

Total Harmonic Distortion

The total harmonic distortion (THD) is the ratio of the RMS sum of the second through sixth harmonic components to the fundamental RMS signal for a specified input and sampling frequency.

$$THD = 10\log\frac{\text{Total Harmonic Power (2nd - 6th harmonics)}}{\text{Sinewave Signal Power}}$$

Spurious-Free Dynamic Range

The spurious-free dynamic range (SFDR) is the ratio of the fundamental RMS amplitude to the RMS amplitude of the next largest spur or spectral component. It is usually determined by the largest harmonic. However, if the harmonics are buried in the noise floor it is the largest peak.

$$SFDR = 10\log\frac{\text{Sinewave Signal Power}}{\text{Highest Spurious Signal Power}}$$

Clock

The clock input is TTL compatible. The converter will function with clock inputs between 10kHz and 800kHz.

Microprocessor Interface

The HI-7153 can be interfaced to microprocessors through the use of standard Write, Read, Chip Select, and HBE control pins. The digital outputs are two's complement coded, three-state gated, and byte organized for bus interface with 8 and 16 bit systems. The digital outputs (D0 - D9, OVR) may be accessed under control of BUS, byte enable input HBE, chip select, and read inputs for a simple parallel bus interface. The microprocessor can read the current data in the output latches in typically 60ns/byte (t_{RD}). An over-range pin (OVR) together with the MSB (D9) pin set to either a logic 0 or 1 will indicate a positive or negative over-range condition respectively. All digital output buffers are capable of driving one TTL load. The multiplexer can be interfaced to either multiplexed or separate address and data bus systems.

The HI-7153 can be interfaced to a microprocessor using one of three modes: slow memory, fast memory, or DMA mode.

Slow Memory Mode

In slow memory mode, the conversion will be initiated by the microprocessor by selecting the chip ($\overline{CS}$) and pulsing $\overline{WR}$ low. This mode is selected by hardwiring the SMODE pin to V+. Note that the converter will change to the DMA interface mode if the $\overline{WR}$ to $\overline{RD}$ active timing is less than 100ns. The end-of-conversion (EOC) output signals an interrupt for the microprocessor to jump to a read subroutine at the end of conversion. When the 8 bit bus operation is selected, high and low byte data may be accessed in either order. An I/O truth table is presented in Table 3 for the slow memory mode of operation.

Fast Memory Mode

The fast memory mode of operation is selected by tying the SMODE and $\overline{WR}$ pins to DG. In this mode, the chip performs continuous conversions and only $\overline{CS}$ and $\overline{RD}$ are required to read the data. Whenever the SMODE pin is low, $\overline{WR}$ is independent of $\overline{CS}$ in starting a conversion cycle. During the first conversion cycle, $\overline{HOLD}$ follows $\overline{WR}$ going low. $\overline{HOLD}$ will be one clock period wide for subsequent conversion cycles.

Data can be read a byte at a time or all 11 bits at once. When the 8 bit bus operation is selected, high and low byte data may be accessed in either order. EOC is continuously low in this mode of operation. The conversion data can be read after $\overline{HOLD}$ has gone low. An I/O truth table is presented in Table 4 for the fast memory mode of operation.

DMA Mode

This is a hardwired mode where the HI-7153 continuously converts. The user implements hardware to store the results in memory, bypassing the microprocessor. This mode is recognized by the chip when SMODE is connected to V+ and $\overline{CS}$, $\overline{RD}$, $\overline{WR}$ are connected to DG. When 8 bit bus operation is selected, high and low byte data may be accessed in either order. EOC is continuously low in this mode. The conversion data can be read approximately 300ns after $\overline{HOLD}$ has gone low. An I/O truth table is presented in Table 5 for the DMA mode of operation.

TABLE 3. SLOW MEMORY MODE I/O TRUTH TABLE (SMODE = V+)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	ALE	FUNCTION
0	0	X	X	X	X	Initiates a conversion.
0	X	X	X	X	1	Selects mux channel. Address data is latched on falling edge of ALE. Latch is transparent when ALE is high.
1	X	X	X	X	X	Disables all chip commands.
0	X	0	1	X	X	Enables D0 - D9 and OVR.
0	X	0	0	0	X	Low byte enable: D0 - D7
0	X	0	0	1	X	High byte enable: D8 - D9, OVR
X	X	1	X	X	X	Disables all outputs (high impedance).

X = Don't Care

TABLE 4. FAST MEMORY MODE I/O TRUTH TABLE (SMODE = DG)

$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	BUS	HBE	ALE	FUNCTION
0	0	X	X	X	X	Continuous conversion, $\overline{WR}$ may be tied to DG.
0	X	X	X	X	1	Selects mux channel. Address data is latched on falling edge of ALE. Latch is transparent when ALE is high.
1	X	X	X	X	X	Disables all chip commands.
0	X	0	1	X	X	Enables D0 - D9 and OVR.
0	X	0	0	0	X	Low byte enable: D0 - D7
0	X	0	0	1	X	High byte enable: D8 - D9, OVR
X	X	1	X	X	X	Disables all outputs (high impedance).

X = Don't Care

TABLE 5. DMA MODE I/O TRUTH TABLE (SMODE = V+, $\overline{CS}$ = $\overline{WR}$ = $\overline{RD}$ = DG)

BUS	HBE	ALE	FUNCTION
X	X	1	Selects mux channel. Address data is latched on falling edge of ALE. Latch is transparent when ALE is high.
1	X	X	Enables D0 - D9 and OVR.
0	0	X	Low byte enable: D0 - D7
0	1	X	High byte enable: D8 - D9, OVR

X = Don't Care

Optimizing System Performance

The HI-7153 has three ground pins (AG, DG, GND) for improved system accuracy. Proper grounding and bypassing is illustrated in Figure 3. The AG pin is a ground pin and is used internally as a reference ground. The reference input and analog input should be referenced to the analog ground (AG) pin. The digital inputs and outputs should be referenced to the digital ground (DG) pin. The GND pin is a return point for the supply current of the comparator array. The comparator array is designed such that this current is approximately constant at all times and does not vary with input voltage. By virtue of the switched capacitor nature of the comparators, it is necessary to hold GND firmly at zero volts at all times. Therefore, the system ground star connection should be located as close to this pin as possible.

As in any analog system, good supply bypassing is necessary in order to achieve optimum system performance. The power supplies should be bypassed with at least a 20µF tantalum and a 0.1µF ceramic capacitor to GND. The reference input should be bypassed with a 0.1µF ceramic capacitor to AG. The capacitor leads should be as short as possible.

The pins on the HI-7153 are arranged such that the analog pins are well isolated from the digital pins. In spite of this arrangement, there is always some pin-to-pin coupling. Therefore the analog inputs to the device should not be driven from very high output impedance sources. PC board layout should screen the analog and reference inputs with guard rings on both sides of the PC board, connected to AG. Using a solder mask is good practice and helps reduce leakage due to moisture contamination on the PC board.

Applications

Figure 4 illustrates an application where the HI-7153 is used to form a multi-channel data acquisition system. Either slow memory or fast memory modes of operation can be selected. Fast memory mode should be selected for maximum throughput. The output data is configured for 16 bit bus operation in these applications. By tying BUS to DG and connecting the HBE input to the system address decoder, the output data can be configured for 8 bit bus systems.

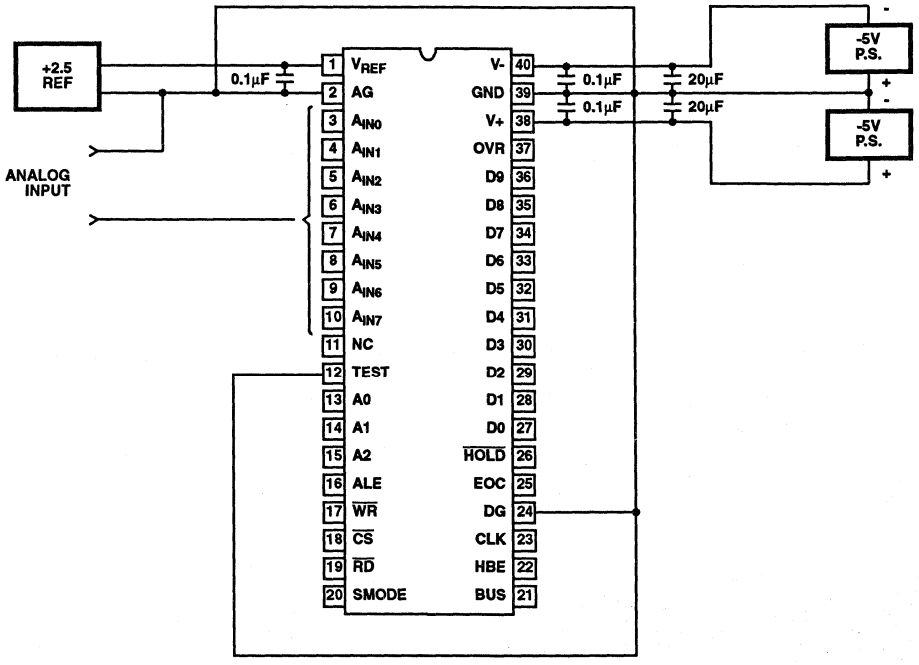


FIGURE 3. GROUND AND POWER SUPPLY DECOUPLING

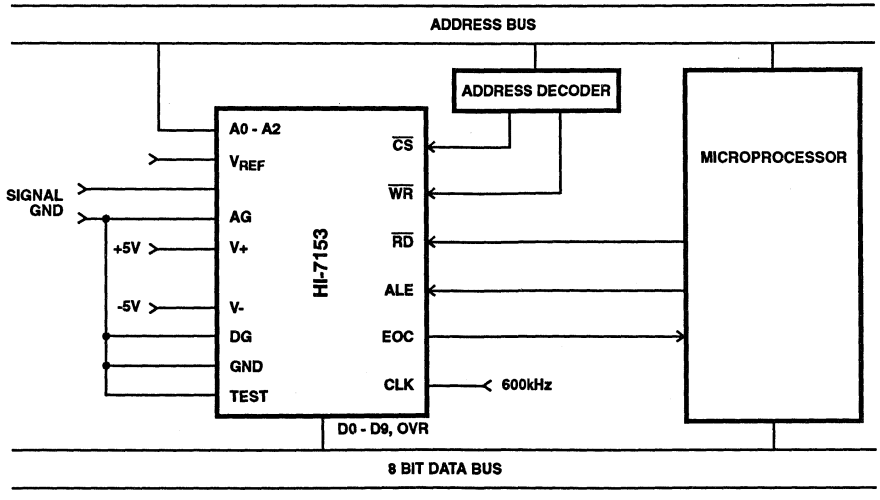


FIGURE 4. MULTI-CHANNEL DATA ACQUISITION SYSTEM

DATA ACQUISITION 8

D/A CONVERTERS

NOTE: Bold Type Designates a New Product from Harris.

DIGITAL TO ANALOG CONVERTERS

DEVICE (NOTES 2, 3)	SUFFIX CODES	MIL SPEC	INL LSB	DNL LSB	SETTLING TIME (µs)	TECHNOLOGY	MULTIPLYING	OUTPUT I/V	INPUT BUFFER	REFERENCE	FEATURES
8-BIT CMOS											
AD7523J	N		±1/2	Monotonic	200 Max	CMOS-JI	X	I	No	External	
AD7523K			±1/4								
AD7523L			±1/8								
HIGH SPEED 8-BIT, 10-BIT											
CA3338A	D	M	±3/4	±1/2	20 Typ	CMOS-SOS		V	Yes	External	8-Bit Video Speed, Low Glitch
	E										
CA3338	D	M	±1	±3/4							
	E										
HI1171	JCB		±1.3	±1/4	25 Typ	CMOS		I	Yes	External	8-Bit Video Speed, Low Glitch, Low Power, Low Cost
HI20201	JCB		±1	±1/2	5.2 Typ	CMOS	Yes	I	Yes	External	10-Bit 160MHz D/A with ECL Inputs,Low Glitch, Low Power
	JCP										
HI20203	JCB		±1	±1/2	4.3 Typ	CMOS	Yes	I	Yes	External	8-Bit 160MHz D/A with ECL Inputs,Low Glitch, Low Power
	JCP										
10-BIT CMOS											
AD7520J	D		±2		500 Typ	CMOS-JI	X	I	No	External	Full Input Static Protection
AD7520J	N		±2								
AD7520K	D		±1								
AD7520K	N		±1								
AD7520L	D		±1/2								
AD7520L	N		±1/2								
AD7520S	D	AD7520SD/883B	±2								
AD7520T	D		±1								
AD7520U	D	AD7520UD/883B	±1/2								

DIGITAL TO ANALOG CONVERTERS (Continued)

DEVICE (NOTES 2, 3)	SUFFIX CODES	MIL SPEC	INL LSB	DNL LSB	SETTLING TIME (µs)	TECHNOLOGY	MULTIPLYING	OUTPUT I/V	INPUT BUFFER	REFERENCE	FEATURES
10-BIT CMOS (Continued)											
AD7530J	N		±2		500 Typ	CMOS-JI	X	I	No	External	Full Input Static Protection
AD7530K			±1								
AD7530L			±1/2								
AD7533J	N		±2		800 Max	CMOS-JI	X	I	No	External	Full Input Static Protection
AD7533K			±1								
AD7533L			±1/2								
12-BIT CMOS											
HI3-DAC80V	-5		±1/2	±3/4	1.5 Max	Bipolar		V	No	Internal	Low Cost, Internal Op Amp
HI3-DAC85V	-4, -9		±1/2	±1/2							
HI1-565AJD	-5	HI1-565ASD/883	±1/2	±3/4	0.5 Typ	Bipolar-DI		I	No	Internal	
HI1-565AKD		HI1-565ATD/883	±1/4	±1/2							
HI1-565ASD	-2		±1/2	±3/4							
HI1-565ATD			±1/4	±1/2							
AD7521J	N		±8		0.5 Typ	CMOS-JI	X	I	No	External	
AD7521K			±4								
AD7521L			±2								
AD7531J	N		±8		0.5 Max	CMOS-JI	X	I	No	External	
AD7531K			±4								
AD7531L			±2								
AD7541A	D		±1		1.0 Max	CMOS-JI	X	I	No	External	
AD7541B			±1/2								
AD7541J	N		±1								
AD7541K			±1/2								
AD7541L			±1/2	Monotonic							
AD7541S	D		±1								
AD7541T			±1/2								

Selection Guide (Continued)

DIGITAL TO ANALOG CONVERTERS (Continued)

DEVICE (NOTES 2, 3)	SUFFIX CODES	MIL SPEC	INL LSB	DNL LSB	SETTLING TIME (µs)	TECHNOLOGY	MULTIPLYING	OUTPUT I/V	INPUT BUFFER	REFERENCE	FEATURES
12-BIT CMOS (Continued)											
AD7545A	D		±2	±4.0	2.0 Max	CMOS-JI	X	I	Yes	External	
AD7545A	N		±2	±4.0							
AD7545B	D		±1	±1.0							
AD7545B	N		±1	±1.0							
AD7545J	N		±2	±4.0							
AD7545K	N		±1	±1.0							
AD7545S	D	AD7545SQ/883B	±2	±4.0							

HARRIS SEMICONDUCTOR

AD7520, AD7530 AD7521, AD7531

December 1993

10-Bit, 12-Bit Multiplying D/A Converters

Features

- **AD7520/AD7530 10 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **AD7521/AD7531 12 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **Low Power Dissipation of 20mW (Max)**
- **Low Nonlinearity Tempco at 2ppm of FSR/°C**
- **Current Settling Time 1.0μs to 0.05% of FSR**
- **±5V to +15V Supply Voltage Range**
- **TTL/CMOS Compatible**
- **Full Input Static Protection**
- **/883B Processed Versions Available**

Description

The AD7520/AD7530 and AD7521/AD7531 are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). Harris' thin-film on CMOS processing gives up to 10-bit accuracy with TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by diodes to ground and positive supply.

Typical applications include digital/analog interfacing, multiplication and division, programmable power supplies, CRT character generation, digitally controlled gain circuits, integrators and attenuators, etc.

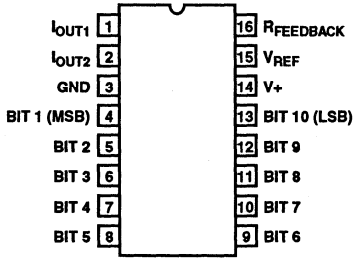
The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

Ordering Information

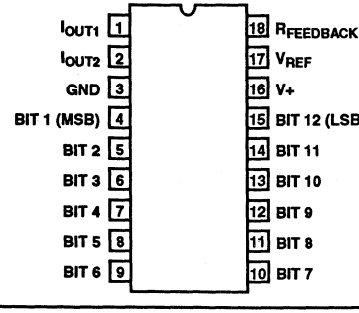
PART NUMBER	NONLINEARITY	TEMPERATURE RANGE	PACKAGE
AD7520JN, AD7530JN	0.2% (8-Bit)	0°C to +70°C	16 Lead Plastic DIP
AD7520KN, AD7530KN	0.1% (9-Bit)	0°C to +70°C	16 Lead Plastic DIP
AD7521JN, AD7531JN	0.2% (8-Bit)	0°C to +70°C	18 Lead Plastic DIP
AD7521KN, AD7531KN	0.1% (9-Bit)	0°C to +70°C	18 Lead Plastic DIP
AD7520LN, AD7530LN	0.05% (10-Bit)	-40°C to +85°C	16 Lead Plastic DIP
AD7521LN, AD7531LN	0.05% (10-Bit)	-40°C to +85°C	18 Lead Plastic DIP
AD7520JD	0.2% (8-Bit)	-25°C to +85°C	16 Lead Ceramic DIP
AD7520KD	0.1% (9-Bit)	-25°C to +85°C	16 Lead Ceramic DIP
AD7520LD	0.05% (10-Bit)	-25°C to +85°C	16 Lead Ceramic DIP
AD7520SD, AD7520SD/883B	0.2% (8-Bit)	-55°C to +125°C	16 Lead Ceramic DIP
AD7520TD	0.1% (9-Bit)	-55°C to +125°C	16 Lead Ceramic DIP
AD7520UD, AD7520UD/883B	0.05% (10-Bit)	-55°C to +125°C	16 Lead Ceramic DIP

Pinouts

AD7520, AD7530 (CDIP, PDIP)
TOP VIEW



AD7521, AD7531 (PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3104**

Absolute Maximum Ratings

Supply Voltage (V+ to GND) ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V+ to GND
Output Voltage Compliance ..... -100mV to V+
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... 300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
16 Lead Plastic DIP	100°C/W	-
18 Lead Plastic DIP	90°C/W	-
16 Lead Ceramic DIP	80°C/W	24°C/W

Maximum Power Dissipation
Up to +75°C 450mW
Derate Above +75°C at 6mW/°C

Operating Temperature
JN, KN, LN Versions ..... 0°C to +70°C
JD, KD, LD Versions ..... -25°C to +85°C
SD, TD, UD Versions ..... -55°C to +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and $R_{FEEDBACK}$.

Electrical Specifications

V+ = +15V, V_{REF} = +10V, T_A = +25°C Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	AD7520/AD7530 MIN	AD7520/AD7530 TYP	AD7520/AD7530 MAX	AD7521/AD7531 MIN	AD7521/AD7531 TYP	AD7521/AD7531 MAX	UNITS
SYSTEM PERFORMANCE (Note 1)									
Resolution			10	10	10	12	12	12	Bits
Nonlinearity	J, S	S Over -55°C to +125°C (Notes 2, 5) (Figure 2)	-	-	±0.2 (8-Bit)	-	-	±0.2 (8-Bit)	% of FSR
	K, T	T Over -55°C to +125°C (Figure 2)	-	-	±0.1 (9-Bit)	-	-	±0.1 (9-Bit)	% of FSR
	L, U	-10V ≤ V_{REF} ≤ +10V U Over -55°C to +125°C (Figure 2)	-	-	±0.05 (10-Bit)	-	-	±0.05 (10-Bit)	% of FSR
Nonlinearity Tempco		-10V ≤ V_{REF} ≤ +10V (Notes 2, 3)	-	-	±2	-	-	±2	ppm of FSR/°C
Gain Error			-	±0.3	-	-	±0.3	-	% of FSR
Gain Error Tempco			-	-	±10	-	-	±10	ppm of FSR/°C
Output Leakage Current (Either Output)		Over the Specified Temperature Range	-	-	±200 (±300)	-	-	±200 (±300)	nA
DYNAMIC CHARACTERISTICS									
Output Current Settling Time		To 0.05% of FSR (All Digital Inputs Low To High And High To Low) (Note 3) (Figure 7)	-	1.0	-	-	1.0	-	µs
Feedthrough Error		V_{REF} = 20V_{P-P}, 10kHz (50kHz) All Digital Inputs Low (Note 3) (Figure 6)	-	-	10	-	-	10	mV_{P-P}
REFERENCE INPUT									
Input Resistance		All Digital Inputs High I_{OUT1} at Ground	5	10	20	5	10	20	kΩ
ANALOG OUTPUT									
Output Capacitance	I_{OUT1}	All Digital Inputs High (Note 3) (Figure 5)	-	200	-	-	200	-	pF
	I_{OUT2}		-	75	-	-	75	-	pF
	I_{OUT1}	All Digital Inputs Low (Note 3) (Figure 5)	-	75	-	-	75	-	pF
	I_{OUT2}		-	200	-	-	200	-	pF

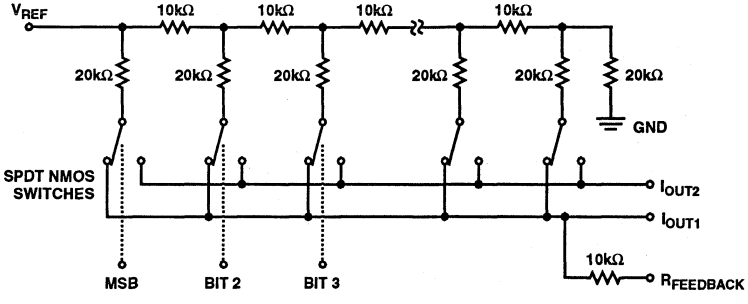
Electrical Specifications $V+ = +15V$, $V_{REF} = +10V$, $T_A = +25°C$ Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	AD7520/AD7530			AD7521/AD7531			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Noise	Both Outputs (Note 3) (Figure 4)	-	Equivalent to 10kΩ	-	-	Equivalent to 10kΩ	-	Johnson Noise
DIGITAL INPUTS								
Low State Threshold, V_{IL}	Over the Specified Temperature Range V_{IN} = 0V or +15V	-	-	0.8	-	-	0.8	V
High State Threshold, V_{IH}		2.4	-	-	2.4	-	-	V
Input Current, I_{IL}, I_{IH}		-	-	±1	-	-	±1	µA
Input Coding	See Tables 1 & 2	Binary/Offset Binary						
POWER SUPPLY CHARACTERISTICS								
Power Supply Rejection	V+ = 14.5V to 15.5V (Note 2) (Figure 3)	-	±0.005	-	-	±0.005	-	% FSR/% ΔV+
Power Supply Voltage Range		+5 to +15			+5 to +15			V
I+	All Digital Inputs at 0V or V+ Excluding Ladder Network	-	±1	-	-	±1	-	µA
	All Digital Inputs High or Low Excluding Ladder Network	-	-	2	-	-	2	mA
Total Power Dissipation	Including the Ladder Network	-	20	-	-	20	-	mW

NOTES:

1. Full scale range (FSR) is 10V for Unipolar and ±10V for Bipolar modes.
2. Using internal feedback resistor $R_{FEEDBACK}$.
3. Guaranteed by design, or characterization and not production tested.
4. Accuracy not guaranteed unless outputs at GND potential.
5. Accuracy is tested and guaranteed at V+ = 15V only.

Functional Diagram



Switches shown for Digital Inputs "High".

Resistor values are typical.

Pin Descriptions

AD7520/30	AD7521/31	PIN NAME	DESCRIPTION
1	1	I_{OUT1}	Current Out summing junction of the R2R ladder network.
2	2	I_{OUT2}	Current Out virtual ground, return path for the R2R ladder network
3	3	GND	Digital Ground. Ground potential for digital side of D/A.
4	4	Bits 1(MSB)	Most Significant Digital Data Bit
5	5	Bit 2	Digital Bit 2
6	6	Bit 3	Digital Bit 3
7	7	Bit 4	Digital Bit 4
8	8	Bit 5	Digital Bit 5
9	9	Bit 6	Digital Bit 6
10	10	Bit 7	Digital Bit 7
11	11	Bit 8	Digital Bit 8
12	12	Bit 9	Digital Bit 9
13	13	Bit 10	Digital Bit 10 (AD7521/31), Least Significant Digital Data Bit (AD7520/30)
-	14	Bit 11	Digital Bit 11 (AD7521/31)
-	15	Bit 12	Least Significant Digital Data Bit (AD7521/31)
14	16	V+	Power Supply +5 to +15 Volts
15	17	V_{REF}	Voltage Reference Input to set the output range. Supplies the R2R resistor ladder.
16	18	$R_{FEEDBACK}$	Feedback resistor used for the current to voltage conversion when using and external OP-Amp.

Definition of Terms

Nonlinearity: Error contributed by deviation of the DAC transfer function from a "best straight line" through the actual plot of transfer function. Normally expressed as a percentage of full scale range or in (sub)multiples of 1 LSB.

Resolution: It is addressing the smallest distinct analog output change that a D/A converter can produce. It is commonly expressed as the number of converter bits. A converter with resolution of n bits can resolve output changes of 2^{-N} of the full-scale range, e.g. 2^{-N} V_{REF} for a unipolar conversion. Resolution by no means implies linearity.

Settling Time: Time required for the output of a DAC to settle to within specified error band around its final value (e.g. 1/2 LSB) for a given digital input change, i.e. all digital inputs LOW to HIGH and HIGH to LOW.

Gain Error: The difference between actual and ideal analog output values at full-scale range, i.e. all digital inputs at HIGH state. It is expressed as a percentage of full-scale range or in (sub)multiples of 1 LSB.

Feedthrough Error: Error caused by capacitive coupling from V_{REF} to I_{OUT1} with all digital inputs LOW.

Output Capacitance: Capacitance from I_{OUT1}, and I_{OUT2} terminals to ground.

Output Leakage Current: Current which appears on I_{OUT1}, terminal when all digital inputs are LOW or on I_{OUT2} terminal when all digital inputs are HIGH.

Detailed Description

The AD7520, AD7530, AD7521 and AD7531 are monolithic, multiplying D/A converters. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit, CMOS level shifters permit low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in the Functional Diagram. The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} buses which must be held either at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduce offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with positive feedback from the output of the second to the first, see Figure 1. This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and highly accurate leg currents.

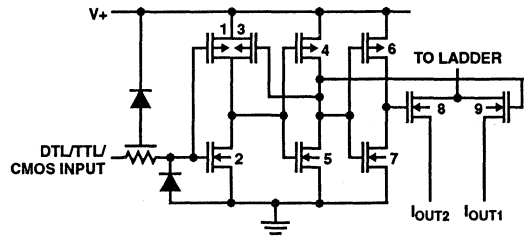


FIGURE 1. CMOS SWITCH

Test Circuits The following test circuits apply for the AD7520. Similar circuits are used for the AD7530, AD7521 and AD7531.

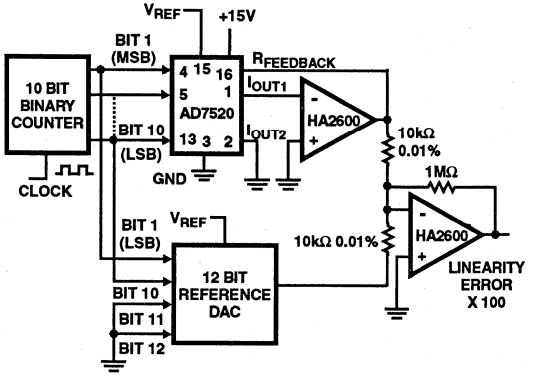


FIGURE 2. NONLINEARITY

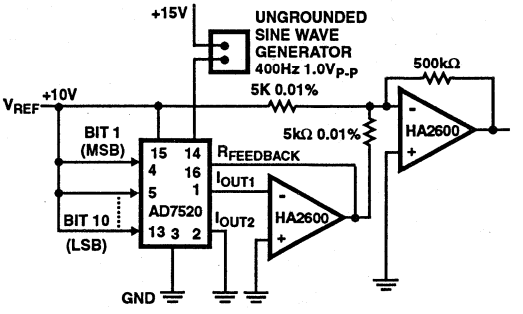


FIGURE 3. POWER SUPPLY REJECTION

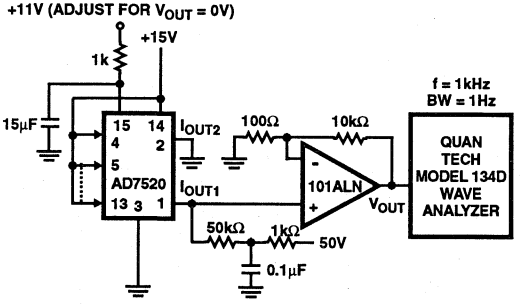


FIGURE 4. NOISE

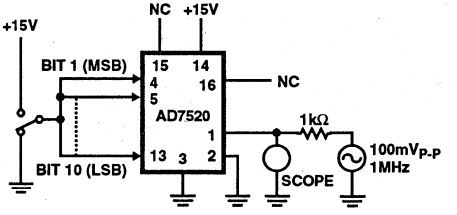


FIGURE 5. OUTPUT CAPACITANCE

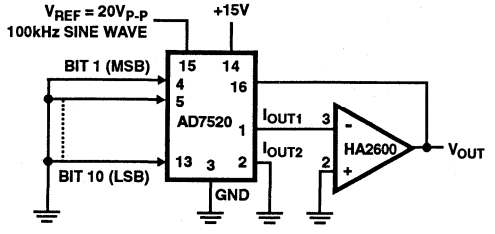


FIGURE 6. FEEDTHROUGH ERROR

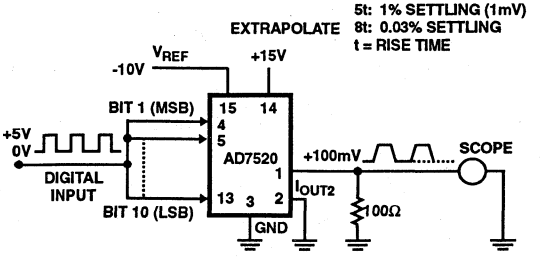


FIGURE 7. OUTPUT CURRENT SETTLING TIME

Applications

Unipolar Binary Operation

The circuit configuration for operating the AD7520 in unipolar mode is shown in Figure 8. Similar circuits can be used for AD7521, AD7530 and AD7531. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

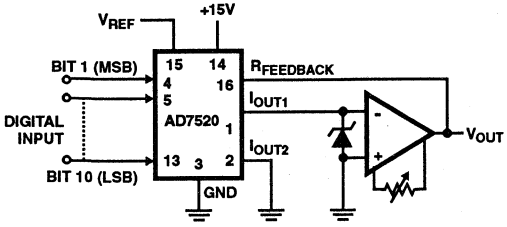


FIGURE 8. UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION

TABLE 1. CODE TABLE - UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-N})$
1000000001	$-V_{REF}(1/2+2^{-N})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF}(1/2-2^{-N})$
0000000001	$-V_{REF}(2^{-N})$
0000000000	0

NOTES:
1. $LSB = 2^{-N} V_{REF}$
2. N = 10 for 7520, 7530
   N = 12 for 7521, 7531

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V+.
2. Monitor VOUT for a $-V_{REF}(1-2^{-N})$ reading. (N = 10 for AD7520/30 and N = 12 for AD7521/31).
3. To decrease V_{OUT}, connect a series resistor (0 to 250Ω) between the reference voltage and the V_{REF} terminal.
4. To increase V_{OUT}, connect a series resistor (0 to 250Ω) in the I_{OUT1} amplifier feedback loop.

Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7520 in the bipolar mode is given in Figure 9. Similar circuits can be used for AD7521, AD7530 and AD7531. Using offset binary digital input codes and positive and negative reference voltage values, 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

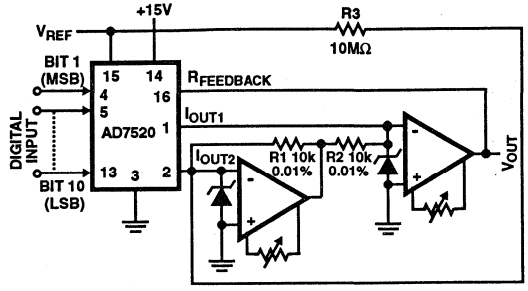


FIGURE 9. BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

TABLE 2. BIPOLAR (OFFSET BINARY) CODE TABLE

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-(N-1)})$
1000000001	$-V_{REF}(2^{-(N-1)})$
1000000000	0
0111111111	$V_{REF}(2^{-(N-1)})$
0000000001	$V_{REF}(1-2^{-(N-1)})$
0000000000	V_{REF}

NOTES:
1. $LSB = 2^{-(N-1)} V_{REF}$
2. N = 10 for 7520, 7521
   N = 12 for 7530,7531

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistor, (10MΩ), from V_{REF} to I_{OUT2}.

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset adjust trimpot for 0V ±1mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset adjust trimpot for 0V ±1mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}(1-2^{-(N-1)})$ volts reading. (N = 10 for AD7520 and AD7530, and N = 12 for AD7521 and AD7531).
3. To increase V_{OUT}, connect a series resistor of up to 250Ω between V_{OUT} and $R_{FEEDBACK}$.
4. To decrease V_{OUT}, connect a series resister of up to 250Ω between the reference voltage and the V_{REF} terminal.

Die Characteristics

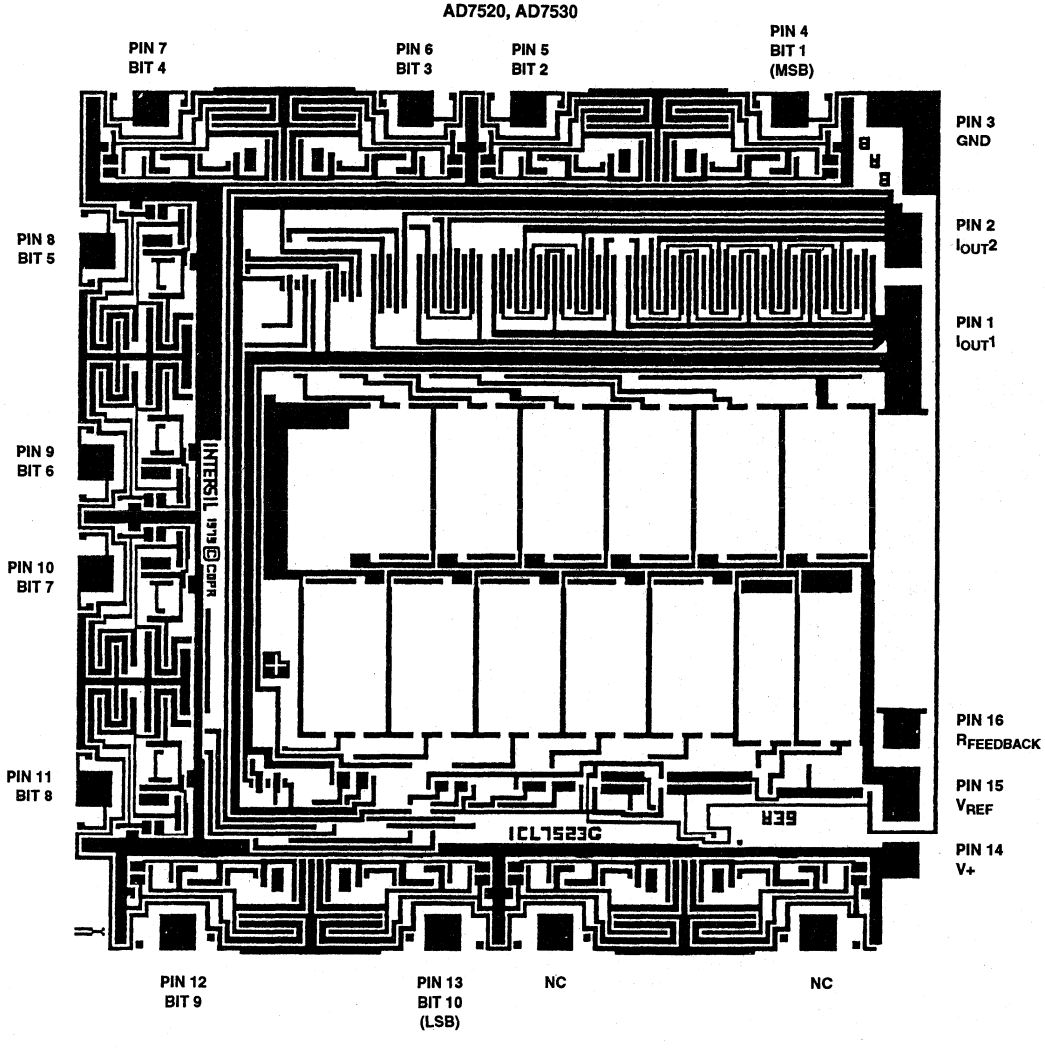
DIE DIMENSIONS:
101 x 103mils (2565 x 2616micrms)

METALLIZATION:
Type: Pure Aluminum
Thickness: 10 ± 1kÅ

GLASSIVATION:
Type: PSG/NITRIDE
PSG: 7 ± 1.4kÅ
NITRIDE: 8 ± 1.2kÅ

PROCESS: CMOS Metal Gate

Metallization Mask Layout



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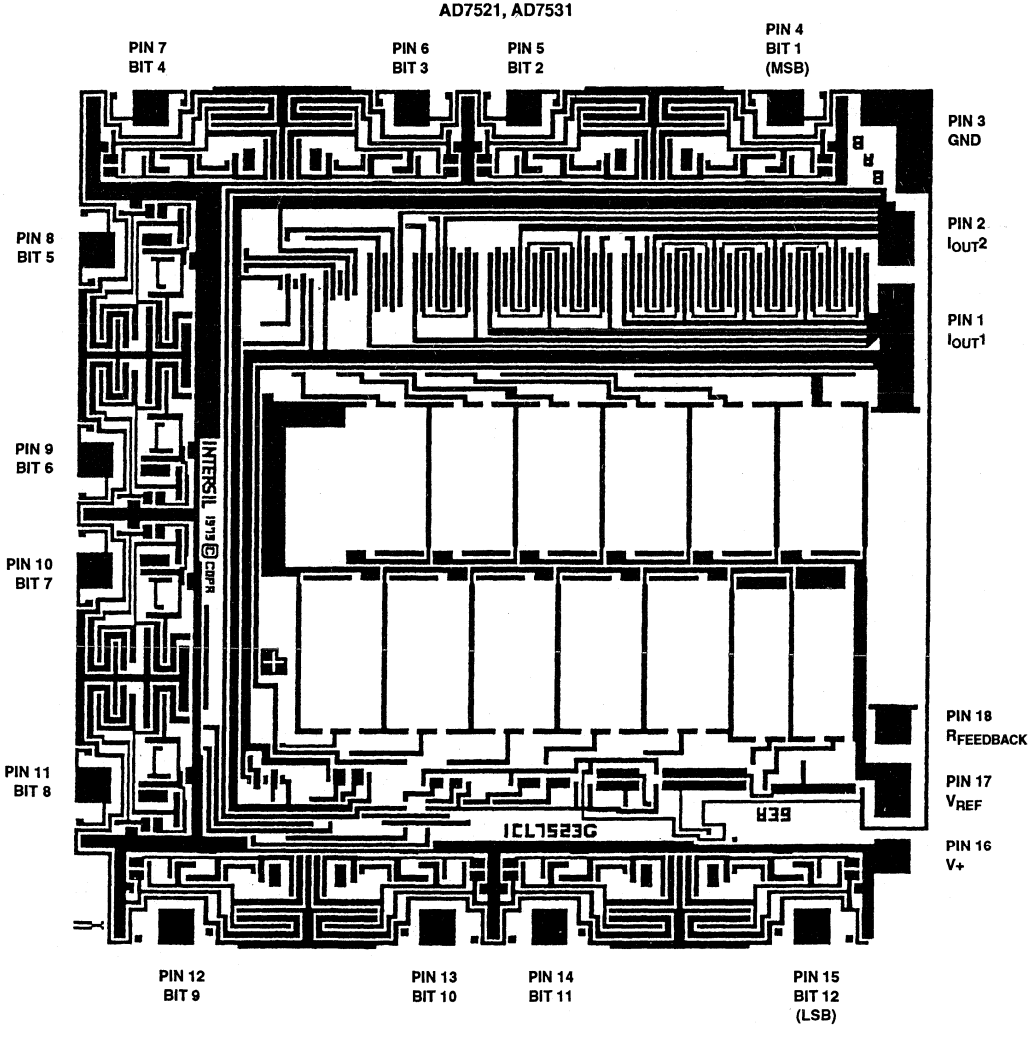


AD7523, AD7533

December 1993

8-Bit Multiplying D/A Converters

Features

- 8, 9 and 10-Bit Linearity
- Low Gain and Linearity Temperature Coefficients
- Full Temperature Range Operation
- Static Discharge Input Protection
- TTL/CMOS Compatible
- +5V to +15V Supply Range
- Fast Settling Time: 150ns Max at +25°C
- Four Quadrant Multiplication
- AD7533 Direct AD7520 Equivalent

Description

The AD7523 and AD7533 monolithic, low cost, high performance, 8-bit and 10-bit accurate, multiplying digital-to-analog converter (DAC), in a 16 pin DIP.

Harris' thin film resistors on CMOS circuitry provide 10-bit resolution (8, 9 and 10-bit accuracy), with TTL/CMOS compatible operation.

The AD7523 and AD7533s accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND, and very low power dissipation make it a very versatile converter.

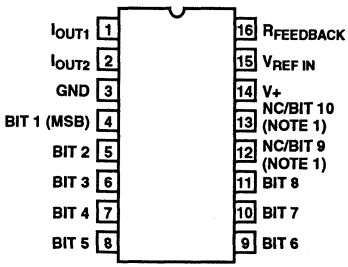
Low noise audio gain controls, motor speed controls, digitally controlled gain and digital attenuators are a few of the wide range of applications of the AD7523 and AD7533.

Ordering Information

PART NUMBER	NONLINEARITY	TEMPERATURE RANGE	PACKAGE
AD7523JN, AD7533JN	0.2% (8-Bit)	0°C to +70°C	16 Lead Plastic DIP
AD7523KN, AD7533KN	0.1% (9-Bit)	0°C to +70°C	16 Lead Plastic DIP
AD7523LN, AD7533LN	0.05% (10-Bit)	0°C to +70°C	16 Lead Plastic DIP

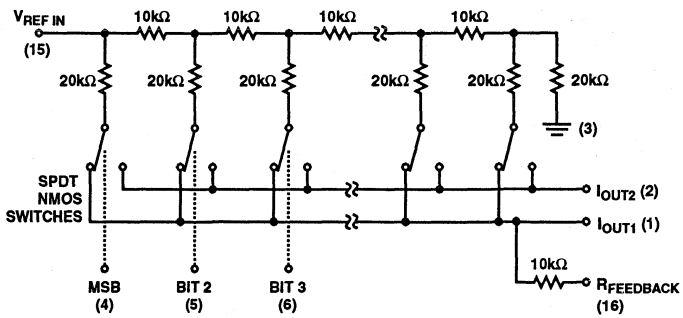
Pinout

AD7523, AD7533 (CDIP, PDIP)
TOP VIEW



NOTE:
1. NC for AD7523 only.

Functional Block Diagram



Switches shown for digital inputs "High"

8 D/A CONVERTERS

File Number 3105

Absolute Maximum Ratings

Supply Voltage (V+ to GND) ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V+ to GND
Output Voltage Compliance ..... -100mV to V+
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package ..... 100°C/W
Operating Temperature
JN, KN, LN Versions ..... 0°C to +70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	AD7523				AD7533				UNITS
			T_A +25°C		T_A MIN-MAX		T_A +25°C		T_A MIN-MAX		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
SYSTEM PERFORMANCE											
Resolution			8	-	8	-	10	-	10	-	Bits
Nonlinearity	J	-10V ≤ V_{REF} ≤ +10V V_{OUT1} = V_{OUT2} = 0V (Note 1, 2, 5)	-	±0.2	-	±0.2	-	±0.2	-	±0.2	% of FSR
	K, T		-	±0.1	-	±0.1	-	±0.1	-	±0.1	% of FSR
	L		-	±0.05	-	±0.05	-	±0.05	-	±0.05	% of FSR
Monotonicity			Guaranteed				Guaranteed				
Gain Error		All Digital Inputs High (Note 2)	-	±1.5	-	±1.8	-	±1.4	-	±1.8	% of FSR
Nonlinearity Tempco		-10V ≤ V_{REF} ≤ + 10V (Notes 2, 3)	-	±2	-	±2	-	±2	-	±2	ppm of FSR/°C
Gain Error Tempco			-	±10	-	±10	-	±10	-	±10	ppm of FSR/°C
Output Leakage Current (Either Output)		V_{OUT1} = V_{OUT2} = 0	-	±50	-	±200	-	±50	-	±200	nA
DYNAMIC CHARACTERISTICS											
Power Supply Rejection		V+ = 14.0V to 15.0V (Note 2)	-	±0.02	-	±0.03	-	±0.005	-	±0.008	% of FSR/% of ΔV+
Output Current Settling Time		To 0.2% of FSR, R_L = 100Ω (Note 3)	-	150	-	200	-	600	-	800	ns
Feedthrough Error		V_{REF} = 20Vpp, 200kHz Sine Wave, All Digital Inputs Low (Note 3)	-	±1/2	-	±1	-	±0.05	-	±0.1	LSB
REFERENCE INPUTS											
Input Resistance (Pin 15)		All Digital Inputs High I_{OUT1} at Ground (Note 3)	5	-	5	-	5	-	5	-	kΩ
			-	20	-	20	-	20	-	20	kΩ
Temperature Coefficient			-	-500	-	-500	-	-300	-	-300	ppm/°C

Electrical Specifications V+ = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER		TEST CONDITIONS	AD7523				AD7533				UNITS
			T_A +25°C		T_A MIN-MAX		T_A +25°C		T_A MIN-MAX		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
ANALOG OUTPUT											
Output Capacitance	C_{OUT1}	All Digital Inputs High (Note 3)	-	100	-	100	-	100	-	100	pF
	C_{OUT2}		-	30	-	30	-	35	-	35	pF
	C_{OUT1}	All Digital Inputs Low (Note 3)	-	30	-	30	-	35	-	35	pF
	C_{OUT2}		-	100	-	100	-	100	-	100	pF
DIGITAL INPUTS											
Low State Threshold, V_{IL}			-	0.8	-	0.8	-	0.8	-	0.8	V
High State Threshold, V_{IH}			2,4	-	2,4	-	2.4	-	2.4	-	V
Input Current (Low or High), I_{IL}, I_{IH}		V_{IN} = 0V or + 15V	-	±1	-	±1	-	±1	-	±1	µA
Input Coding		See Tables 1 & 3	Binary/Offset Binary				Binary/Offset Binary				
Input Capacitance		(Note 3)	-	4	-	4	-	4	-	4	pF
POWER SUPPLY CHARACTERISTICS											
Power Supply Voltage Range		(Note 5)	+5 to +16				+5 to +16				V
I+		All Digital Inputs High or Low (Excluding Ladder Network)	-	2	-	2.5	-	2	-	2.5	mA

NOTES:

1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design or characterization and not production tested.
4. Accuracy not guaranteed unless outputs at ground potential.
5. Accuracy is tested and guaranteed at V+ = +15V, only.

Definition of Terms

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Settling Time: Time required for the output of a DAC to settle to within specified error band around its final value (e.g. 1/2 LSB) for a given digital input change, i.e. all digital inputs LOW to HIGH and HIGH to LOW.

Gain Error: The difference between actual and ideal analog output values at full-scale range, i.e. all digital inputs at HIGH state. It is expressed as a percentage of full-scale range or in (sub)multiples of 1 LSB.

Feedthrough Error: Error caused by capacitive coupling from V_{REF} to I_{OUT1} with all digital inputs LOW.

Output Capacitance: Capacitance from I_{OUT1}, and I_{OUT2} terminals to ground.

Output Leakage Current: Current which appears on I_{OUT1}, terminal when all digital inputs are LOW or on I_{OUT2} terminal when all digital inputs are HIGH.

For further information on the use of this device, see the following Application Notes:

A002 "Principles of Data Acquisition and Conversion"

A018 "Do's and Don'ts of Applying A/D Converters", by Peter Bradshaw and Skip Osgood

A042 "Interpretation of Data Conversion Accuracy Specifications"

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Converter errors are further reduced by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduce offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with positive feedback from the output of the second to the first, see Figure 1. This configuration results in TTL/CMOS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binarily weighted for an ON resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors and high accurate leg currents.

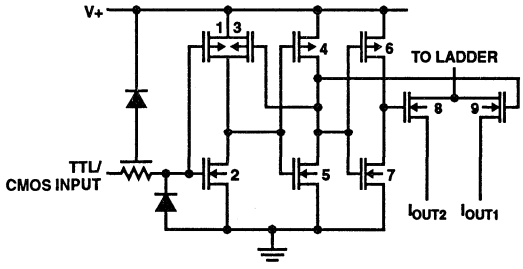
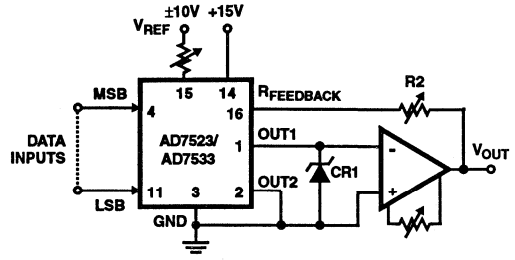


FIGURE 1. CMOS SWITCH

Typical Applications

Unipolar Binary Operation - AD7523 (8 Bit DAC)

The circuit configuration for operating the AD7523 in unipolar mode is shown in Figure 2. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.



NOTES:

1. R1 and R2 used only if gain adjustment is required.
2. CF1 protects AD7523 and AD7533 against negative transients.

FIGURE 2. UNIPOLAR BINARY OPERATION

TABLE 1. UNIPOLAR BINARY CODE - AD7523

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{255}{256}\right)$
10000001	$-V_{REF}\left(\frac{129}{256}\right)$
10000000	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111	$-V_{REF}\left(\frac{127}{256}\right)$
00000001	$-V_{REF}\left(\frac{1}{256}\right)$
00000000	$-V_{REF}\left(\frac{0}{256}\right) = 0$

NOTES:

1. 1 LSB $= (2^{-8})(V_{REF}) = \left(\frac{1}{256}\right)(V_{REF})$

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±1mV (max) at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}$ $(1 - 1/2^8)$ reading.
3. To increase V_{OUT}, connect a series resistor, R2, (0Ω to 250Ω) in the I_{OUT1} amplifier feedback loop.
4. To decrease V_{OUT}, connect a series resistor, R1, (0Ω to 250Ω) between the reference voltage and the V_{REF} terminal.

Unipolar Binary Operation - AD7533 (10 Bit DAC)

The circuit configuration for operating the AD7533 in unipolar mode is shown in Figure 2. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 2.

TABLE 2. UNIPOLAR BINARY CODE - AD7533

DIGITAL INPUT MSB LSB	(NOTE 1) NOMINAL ANALOG OUTPUT
1111111111	$-V_{REF}(\frac{1023}{1024})$
1000000001	$-V_{REF}(\frac{513}{1024})$
1000000000	$-V_{REF}(\frac{512}{1024}) = -\frac{V_{REF}}{2}$
0111111111	$-V_{REF}(\frac{511}{1024})$
0000000001	$-V_{REF}(\frac{1}{1024})$
0000000000	$-V_{REF}(\frac{0}{1024}) = 0$

NOTES:

1. V_{OUT} as shown in the Functional Diagram.
2. Nominal Full Scale for the circuit of Figure 2 is given by
   $FS = -V_{REF}(\frac{1023}{1024})$
3. Nominal LSB magnitude for the circuit of Figure 2 is given by
   $LSB = V_{REF}(\frac{1}{1024})$

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±1mV (max) at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}(1 - 1/2^{10})$ reading.
3. To increase V_{OUT}, connect a series resistor, R2, (0Ω to 250Ω) in the I_{OUT1} amplifier feedback loop.
4. To decrease V_{OUT}, connect a series resistor, R1, (0Ω to 250Ω) between the reference voltage and the V_{REF} terminal.

Bipolar (Offset Binary) Operation - AD7523

The circuit configuration for operating the AD7523 in the bipolar mode is given in Figure 3. Using offset binary digital input codes and positive and negative reference voltage values, Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 3.)

TABLE 3. BIPOLAR (OFFSET BINARY) CODE - AD7523

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}(\frac{127}{128})$
10000001	$-V_{REF}(\frac{1}{128})$
10000000	0
01111111	$+V_{REF}(\frac{1}{128})$
00000001	$+V_{REF}(\frac{127}{128})$
00000000	$+V_{REF}(\frac{128}{128})$

NOTES:

1. 1 LSB $= (2^{-7})(V_{REF}) = (\frac{1}{128})(V_{REF})$

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the

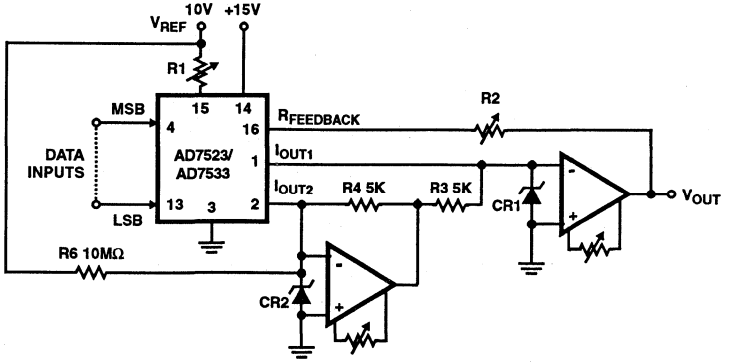


FIGURE 3. BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT} output sums the two currents. This configuration doubles the output range. The difference current resulting at zero offset binary code, (MSB = "Logic 1", all other bits = "Logic 0"), is corrected by suing an external resistor, (10MΩ), from V_{REF} to I_{OUT2} (Figure 3).

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset adjust trimpot for 0V ±1mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset adjust trimpot for 0V ±1mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}$ $(1 - 1/2^8)$ volts reading.
3. To increase V_{OUT}, connect a series resistor, R2, of up to 250Ω between V_{OUT} and $R_{FEEDBACK}$.
4. To decrease V_{OUT}, connect a series resistor, R1, of up to 250Ω between the reference voltage and the V_{REF} terminal.

Bipolar (Offset Binary) Operation - AD7533

The circuit configuration for operating the AD7533 in the bipolar mode is given in Figure 3. Using offset binary digital input codes and positive and negative reference voltage values, 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 4.

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range. The difference current resulting at zero offset binary code, (MSB = "Logic 1", all other bits = "Logic 0"), is corrected by using an external resistor, (10MΩ), from V_{REF} to I_{OUT2}.

TABLE 4. UNIPOLAR BINARY CODE - AD7533

DIGITAL INPUT MSB LSB	(NOTE 1) NOMINAL ANALOG OUTPUT
1111111111	$-V_{REF}(\frac{511}{512})$
1000000001	$-V_{REF}(\frac{1}{512})$
1000000000	0
0111111111	$+V_{REF}(\frac{1}{512})$
0000000001	$+V_{REF}(\frac{511}{512})$
0000000000	$+V_{REF}(\frac{512}{512})$

NOTES:

1. V_{OUT} as shown in the Functional Diagram.
2. Nominal Full Scale for the circuit of Figure 6 is given by
$$FSR = V_{REF}(\frac{1023}{512})$$
3. Nominal LSB magnitude for the circuit of Figure 3 is given by
$$LSB = V_{REF}(\frac{1}{512})$$

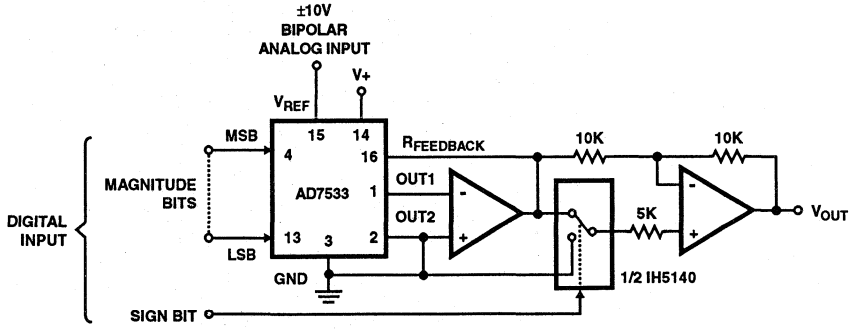


FIGURE 4. 10-BIT AND SIGN MULTIPLYING DAC

Offset Adjustment

1. Adjust V_{REF} to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust I_{OUT2} amplifier offset adjust trimpot for 0V ±1mV at I_{OUT2} amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust I_{OUT1} amplifier offset adjust trimpot for 0V ±1mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V+.
2. Monitor V_{OUT} for a $-V_{REF}(1 - 2^{-9})$ volts reading.
3. To increase V_{OUT}, connect a series resistor of up to 250Ω between V_{OUT} and $R_{FEEDBACK}$.
4. To decrease V_{OUT}, connect a series resistor of up to 250Ω between the reference voltage and the V_{REF} terminal.

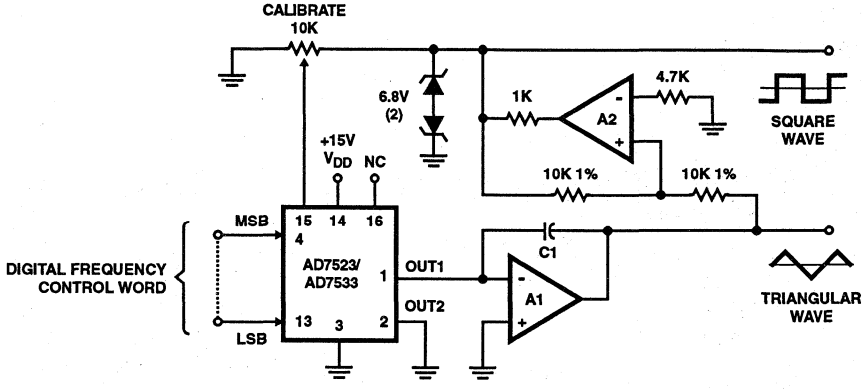
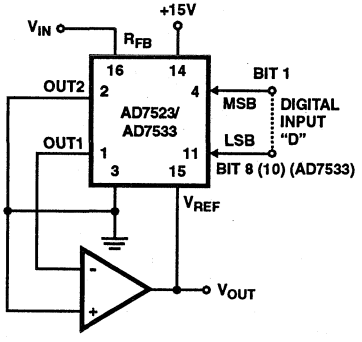


FIGURE 5. PROGRAMMABLE FUNCTION GENERATOR

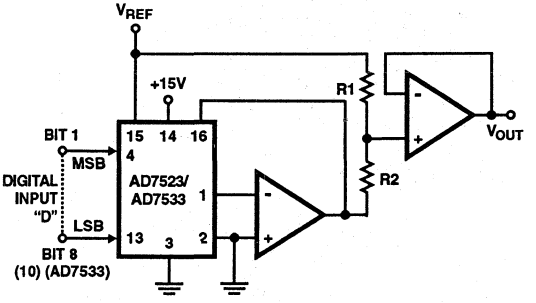


$V_{OUT} = -V_{IN/D}$
Where:

$$D = \frac{Bit1}{2^1} + \frac{Bit2}{2^2} + \ldots \frac{Bit8}{2^2}$$

$$\left(0 \leq D \leq \frac{255}{256}\right)$$

FIGURE 6. DIVIDER (DIGITALLY CONTROLLED GAIN)



$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1 + R_2}\right) - \left(\frac{R_1 D}{R_1 + R_2}\right)\right]$$

$$\text{Where } D = \frac{Bit\ 1}{2^1} + \frac{Bit\ 2}{2^2} + \ldots \frac{Bit\ 8}{2^8}$$

$$\left(0 \leq D \leq \frac{255}{256}\right)$$

FIGURE 7. MODIFIED SCALE FACTOR AND OFFSET

Die Characteristics

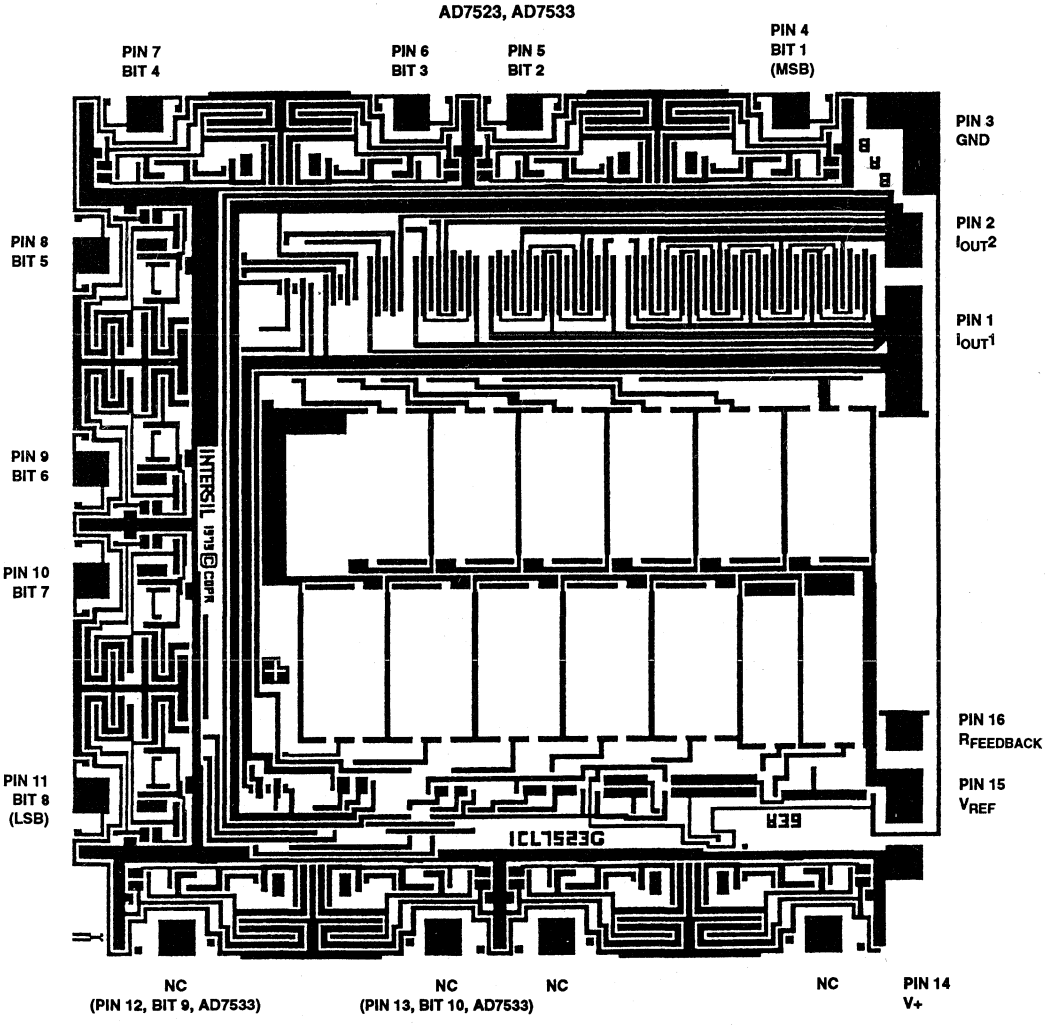
DIE DIMENSIONS:
101 x 103mils (2565 x 2616micrms)

METALLIZATION:
Type: Pure Aluminum
Thickness: 10 ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
PSG: 7 ± 1.4kÅ
Nitride: 8 ± 1.2kÅ

PROCESS: CMOS Metal Gate

Metallization Mask Layout



HARRIS SEMICONDUCTOR

AD7541

December 1993

12-Bit Multiplying D/A Converter

Features

- 12-Bit Linearity 0.01%
- Pretrimmed Gain
- Low Gain and Linearity Tempcos
- Full Temperature Range Operation
- Full Input Static Protection
- TTL/CMOS Compatible
- +5V to +15V Supply Range
- 20mW Low Power Dissipation
- Current Settling Time 1μs to 0.01% of FSR
- Four Quadrant Multiplication

Description

The AD7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

Harris' wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V+ and ground, large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Harris AD7541.

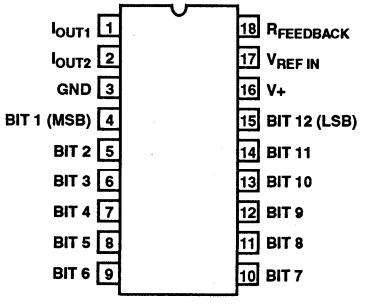
Pin compatible with AD7521, this DAC provides accurate four quadrant multiplication over the full military temperature range.

Ordering Information

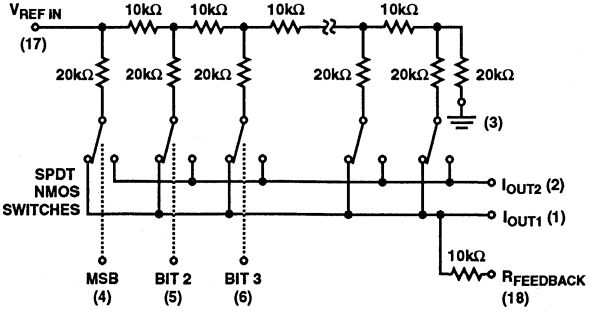
PART NUMBER	NONLINEARITY	TEMPERATURE RANGE	PACKAGE
AD7541AD	0.02% (11-Bit)	-25°C to +85°C	18 Lead Plastic DIP
AD7541BD	0.01% (12-Bit)	-25°C to +85°C	18 Lead Plastic DIP
AD7541JN	0.02% (11-Bit)	0°C to +70°C	18 Lead Plastic DIP
AD7541KN	0.01% (12-Bit)	0°C to +70°C	18 Lead Plastic DIP
AD7541LN	0.01% (12-Bit) Guaranteed Monotonic	0°C to +70°C	18 Lead Plastic DIP
AD7541SD	0.02% (11-Bit)	-55°C to +125°C	18 Lead Plastic DIP
AD7541TD	0.01% (12-Bit)	-55°C to +125°C	18 Lead Plastic DIP

Pinout

AD7541
(PDIP)
TOP VIEW



Functional Diagram



Switches shown are for Digital Inputs "High"

File Number 3107

Absolute Maximum Ratings

Supply Voltage (V+ to GND) ..... +17V
V_{REF} ..... ±25V
Digital Input Voltage Range ..... V+ to GND
Output Voltage Compliance ..... -100mV to V+
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic DIP Package ..... 90°C/W
Operating Temperature
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD Versions ..... -25°C to +85°C
SD, TD Version ..... -55°C to +125°C
Maximum Power Dissipation
Plastic DIP Package up to +70°C 670mW
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, T_A = +25°C, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	T_A +25°C MIN	T_A +25°C TYP	T_A +25°C MAX	T_A MIN-MAX MIN	T_A MIN-MAX MAX	UNITS
SYSTEM PERFORMANCE								
Resolution			12	-	-	12	-	Bits
Nonlinearity	A, S, J	-10V ≤ V_{REF} ≤ +10V V_{OUT1} = V_{OUT2} = 0V See Figure 3 (Note 4)	-	-	±0.024	-	±0.024	% of FSR
	B, T, K		-	-	±0.012	-	±0.012	% of FSR
	L		-	-	±0.012	-	±0.012	% of FSR
Monotonicity			Guaranteed					
Gain Error		-10V ≤ V_{REF} ≤ +10V (Note 4)	-	-	±0.3	-	±0.4	% of FSR
Output Leakage Current (Either Output)		V_{OUT1} = V_{OUT2} = 0	-	-	±50	-	±200	nA
DYNAMIC CHARACTERISTICS								
Power Supply Rejection		V+ = 14.5V to 15.5V See Figure 5, (Note 4)	-	-	±0.005	-	±0.01	% of FSR/% of ΔV+
Output Current Settling Time		To 0.1% of FSR See Figure 9, (Note 5)	-	-	1	-	1	µs
Feedthrough Error		V_{REF} = $20V_{PP}$, 10kHz All Digital Inputs Low See Figure 8, (Note 5)	-	-	1	-	1	mV_{P-P}
REFERENCE INPUTS								
Input Resistance		All Digital Inputs High I_{OUT1} at Ground	5	10	20	5	20	kΩ
ANALOG OUTPUT								
Voltage Compliance		Both Outputs, See Maximum Ratings (Note 6)	-100mV to V+					
Output Capacitance	C_{OUT1}	All Digital Inputs High See Figure 7, (Note 5)	-	-	200	-	200	pF
	C_{OUT2}		-	-	60	-	60	pF
	C_{OUT1}	All Digital Inputs Low) See Figure 7, (Note 5)	-	-	60	-	60	pF
	C_{OUT2}		-	-	200	-	200	pF
Output Noise (Both Outputs)		See Figure 6	Equivalent to 10kΩ Johnson Noise					
DIGITAL INPUTS								
Low State Threshold, V_{IL}		(Note 1, 5)	-	-	0.8	-	0.8	V
High State Threshold, V_{IH}			2.4	-	-	2.4	-	V

Electrical Specifications V+ = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = 0V, T_A = +25°C, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	T_A +25°C			T_A MIN-MAX		UNITS
		MIN	TYP	MAX	MIN	MAX	
Input Current	V_{IN} = 0V or V+ (Note 5)	-	-	±1	-	±1	µA
Input Coding	See Tables 1 & 2 (Note 5)	Binary/Offset Binary					
Input Capacitance	(Note 5)	-	-	8	-	8	pF
POWER SUPPLY CHARACTERISTICS							
Power Supply Voltage Range	Accuracy is not guaranteed over this range	+5 to +16					V
I+	All Digital Inputs High or Low (Excluding Ladder Network)	-	-	2.0	-	2.5	mA
Total Power Dissipation	(Including Ladder Network)	-	20	-	-	-	mW

NOTES:

1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} and $R_{FEEDBACK}$.
3. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
4. Using internal feedback resistor, $R_{FEEDBACK}$.
5. Guaranteed by design or characterization and not production tested.
6. Accuracy not guaranteed unless outputs at ground potential.

Definition of Terms

Nonlinearity: Error contributed by deviation of the DAC transfer function from a "best fit straight line" function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

Resolution: Value of the LSB. For example, a unipolar converter with n bits has a resolution of LSB = $(V_{REF})/2^{-N}$. A bipolar converter of n bits has a resolution of LSB = $(V_{REF})/2^{-(N-1)}$. Resolution in no way implies linearity.

Settling Time: Time required for the output function of the DAC to settle to within $^1/_2$ LSB for a given digital input stimulus, i.e., 0 to Full Scale.

Gain Error: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

Feedthrough Error: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

Output Capacitance: Capacitance from I_{OUT1}, and I_{OUT2} terminals to ground.

Output Leakage Current: Current which appears on I_{OUT1}, terminal when all digital inputs are LOW or on I_{OUT2} terminal when all inputs are HIGH.

Detailed Description

The AD7541 is a 12-bit, monolithic, multiplying D/A converter. A highly stable thin film R-2R resistor ladder network and NMOS SPDT switches form the basis of the converter circuit. CMOS level shifters provide low power TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications. A simplified equivalent circuit of the DAC is shown on page 1, (Functional Diagram). The NMOS SPDT switches steer the ladder leg currents between I_{OUT1} and I_{OUT2} buses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code. Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12-bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to first (Figure 1). This configuration results in TTL/COMS compatible operation over the full military temperature range. With the ladder SPDT switches driven by the level shifter, each switch is binary weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistor, resulting in accurate leg currents.

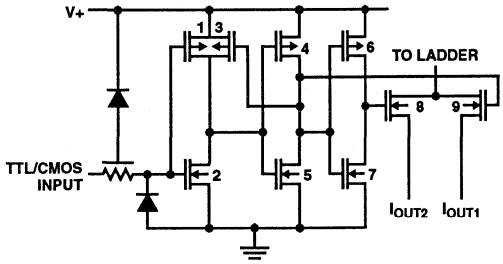


FIGURE 1. CMOS SWITCH

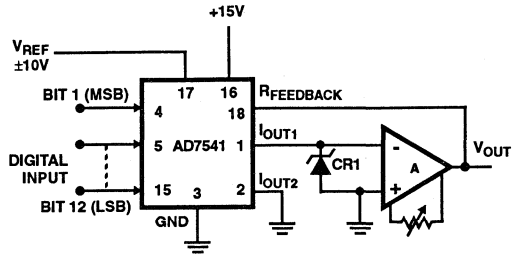


FIGURE 2. UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Typical Applications

General Recommendations

Static performance of the AD7541 depends on I_{OUT1} and I_{OUT2} (pin 1 and pin 2) potentials being exactly equal to GND (pin3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than ±200µV).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point, using separate connections.

The V+ (pin 18) power supply should have a low noise level and should not have any transients exceeding +17V.

Unused digital inputs must be connected to GND or V_{DD} for proper operation.

A high value resistor (~1MΩ) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

Unipolar Binary Operation

The circuit configuration for operating the AD7541 in unipolar mode is shown in Figure 2. With positive and negative V_{REF} values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1. A Schottky diode (HP5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

Zero Offset Adjustment

1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±0.5mV (max) at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V_{DD}.
2. Monitor V_{OUT} for a $-V_{REF}$ $(1 - {}^1/_2{}^{12})$ reading.
3. To increase V_{OUT}, connect a series resistor, (0Ω to 250Ω), in the I_{OUT1} amplifier feedback loop.
4. To decrease V_{OUT}, connect a series resistor, (0Ω to 250Ω), between the reference voltage and the V_{REF} terminal.

TABLE 1. CODE TABLE - UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}$ $(1 - {}^1/_2{}^{12})$
100000000001	$-V_{REF}$ $({}^1/_2 + {}^1/_2{}^{12})$
100000000000	$-V_{REF}/2$
011111111111	$-V_{REF}$ $({}^1/_2 - {}^1/_2{}^{12})$
000000000001	$-V_{REF}$ $({}^1/_2{}^{12})$
000000000000	0

Bipolar (Offset Binary) Operation

The circuit configuration for operating the AD7541 in the bipolar mode is given in Figure 3. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to I_{OUT1} bus. A "Logic 0" input forces the bit current to I_{OUT2} bus. For any code the I_{OUT1} and I_{OUT2} bus currents are complements of one another. The current amplifier at I_{OUT2} changes the polarity of I_{OUT2} current and the transconductance amplifier at I_{OUT1} output sums the two currents. This configuration doubles the output range of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistive divider, from V_{REF} to I_{OUT2}.

Offset Adjustment

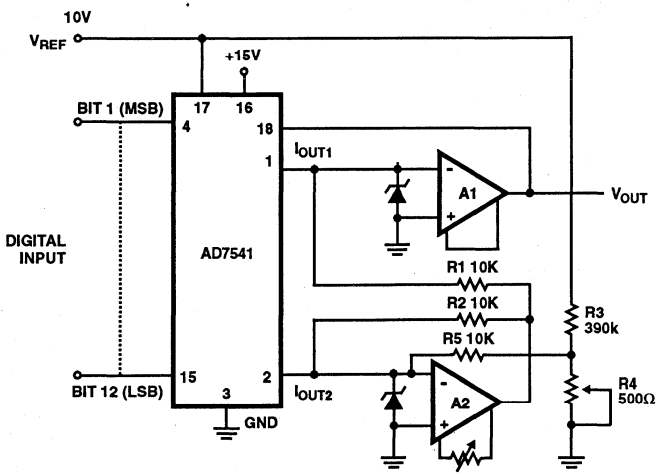
1. Adjust V_{REF} to approximately +10V.
2. Set R4 to zero.
3. Connect all digital inputs to "Logic 1".
4. Adjust I_{OUT1} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT2} amplifier output.
5. Connect a short circuit across R2.
6. Connect all digital inputs to "Logic 0".
7. Adjust I_{OUT2} amplifier offset zero adjust trimpot for 0V ±0.1mV at I_{OUT1} amplifier output.
8. Remove short circuit across R2.
9. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
10. Adjust R4 for 0V ±0.2mV at V_{OUT}.

Gain Adjustment

1. Connect all digital inputs to V_{DD}.
2. Monitor V_{OUT} for a $-V_{REF}$ $(1 - {}^1/_2{}^{11})$ volts reading.
3. To increase V_{OUT}, connect a series resistor, (0Ω to 250Ω), in the I_{OUT1} amplifier feedback loop.
4. To decrease V_{OUT}, connect a series resistor, (0Ω to 250Ω), between the reference voltage and the V_{REF} terminal.

TABLE 2. CODE TABLE - BIPOLAR (OFFSET BINARY) OPERATION

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}$ $(1 - {}^1/_2{}^{11})$
100000000001	$-V_{REF}$ $({}^1/_2{}^{11})$
100000000000	0
011111111111	V_{REF} $({}^1/_2{}^{11})$
000000000001	V_{REF} $(1 - {}^1/_2{}^{11})$
000000000000	V_{REF}



NOTE: R1 AND R2 SHOULD BE 0.01%, LOW-TCR RESISTORS

FIGURE 3. BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Test Circuits

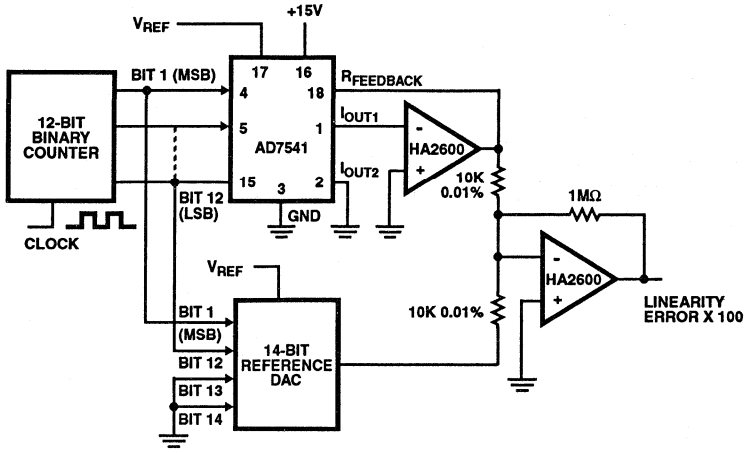


FIGURE 4. NONLINEARITY TEST CIRCUIT

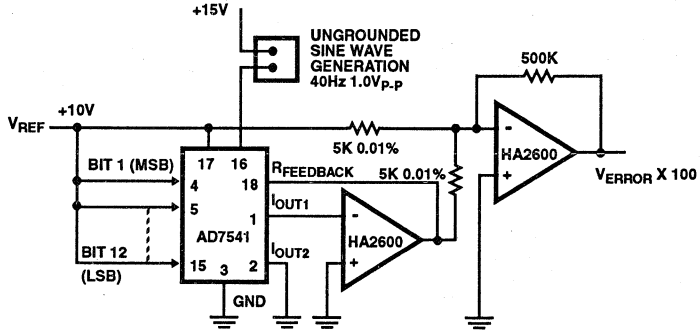


FIGURE 5. POWER SUPPLY REJECTION TEST CIRCUIT

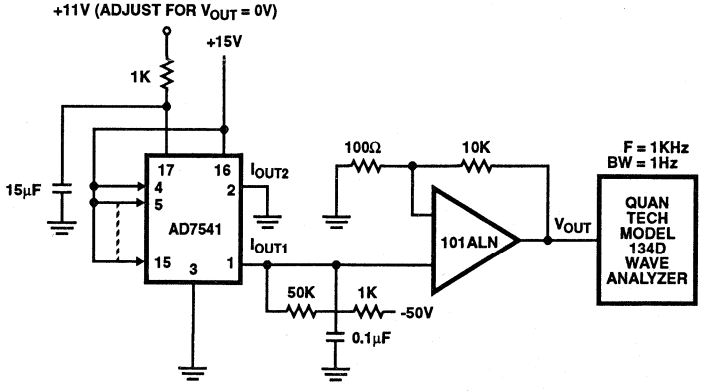


FIGURE 6. NOISE TEST CIRCUIT

Test Circuits (Continued)

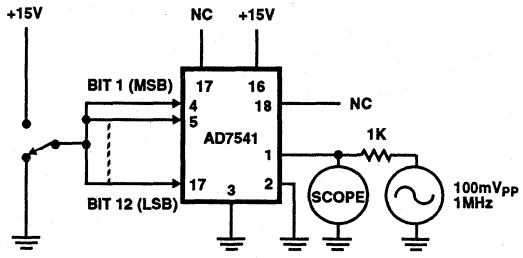


FIGURE 7. OUTPUT CAPACITANCE TEST CIRCUIT

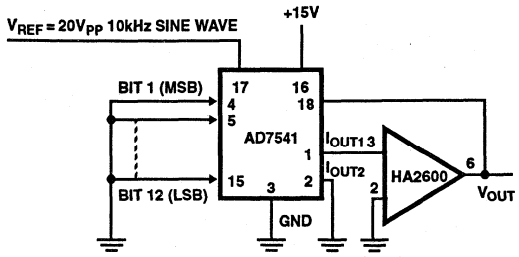


FIGURE 8. FEEDTHROUGH ERROR TEST CIRCUIT

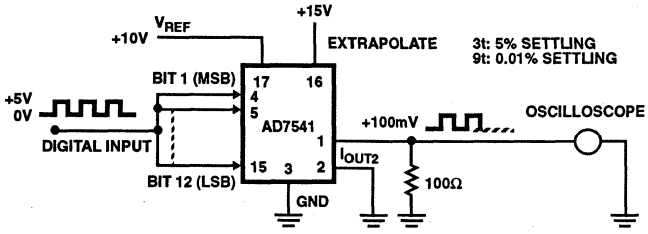


FIGURE 9. OUTPUT CURRENT SETTLING TIME TEST CIRCUIT

Dynamic Performance

The dynamic performance of the DAC, also depends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, open-loop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.

The output impedance of the AD7541 looking into I_{OUT1} varies between 10kΩ ($R_{FEEDBACK}$ alone) and 5KΩ ($R_{FEEDBACK}$ in parallel with the ladder resistance).

Similarly the output capacitance varies between the minimum and the maximum values depending on the input code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

A capacitor in parallel with the feedback resistor (as shown in Figure 10) provides the necessary phase compensation to critically damp the output.

A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.

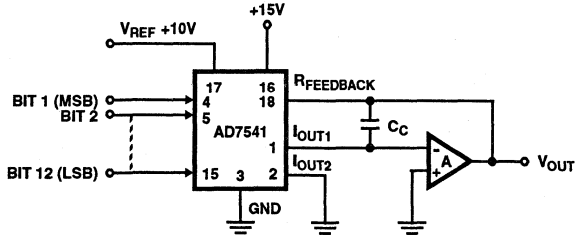


FIGURE 10. GENERAL DAC CIRCUIT WITH COMPENSATION CAPACITOR, C_C

HARRIS SEMICONDUCTOR

AD7545

12-Bit Buffered Multiplying CMOS DAC

December 1993

Features

- 12-Bit Resolution
- Low Gain T.C. 2ppm/°C Typ
- Fast TTL/CMOS Compatible Data Latches
- Single +5V to +15V Supply
- Low Power
- Low Cost
- /883 Processed Versions Available

Description

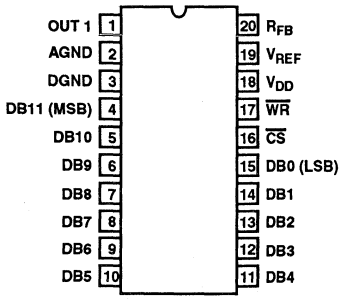
The AD7545 is a low cost monolithic 12-bit CMOS multiplying DAC with on-board data latches. Data is loaded in a single 12-bit wide word which allows interfacing directly to most 12-bit and 16-bit bus systems. Loading of the input latches is under the control of the CS and WR inputs. A logic low on these control inputs makes the input latches transparent allowing direct unbuffered operation of the DAC.

Ordering Information

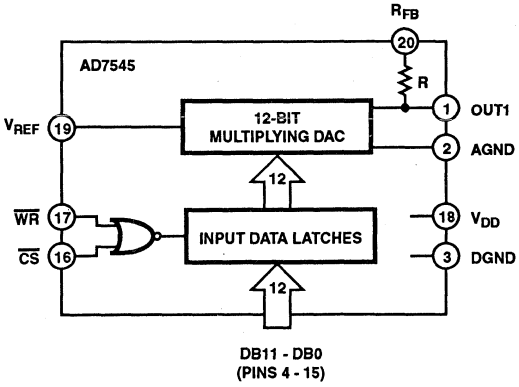
PART NUMBER	TEMPERATURE RANGE	PACKAGE
AD7545JN	0°C to +70°C	20 Lead Plastic DIP
AD7545KN	0°C to +70°C	20 Lead Plastic DIP
AD7545AN	-40°C to +85°C	20 Lead Plastic DIP
AD7545BN	-40°C to +85°C	20 Lead Plastic DIP
AD7545AD	-40°C to +85°C	20 Lead Ceramic DIP
AD7545BD	-40°C to +85°C	20 Lead Ceramic DIP
AD7545SD	-55°C to +125°C	20 Lead Ceramic DIP

Pinout

AD7545
(PDIP, CDIP)
TOP VIEW



Functional Diagram



File Number 3108

Absolute Maximum Ratings

Supply Voltage (V_{DD} to DGND) ..... -0.3V, +17V
Digital Input Voltage to DGND ..... -0.3V, V_{DD} +0.3V
V_{RFB}, V_{REF} to DGND ..... ±25V
V_{PIN1} to DGND ..... -0.3V, V_{DD} +0.3V
AGND to DGND ..... -0.3V, V_{DD} +0.3V
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	71°C/W	17°C/W
Plastic DIP Package	120°C/W	-

Operating Temperature
Commercial (J, K, Grades) ..... 0°C to +70°C
Industrial (A, B, Grades) ..... -40°C to +85°C
Extended (S Grades) ..... -55°C to +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = See Note 1, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND, Unless Otherwise Specified

PARAMETER		TEST CONDITIONS	V_{DD} = +5V			V_{DD} = +15V			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
STATIC PERFORMANCE									
Resolution			12			12			Bits
Relative Accuracy	J, A, S		-	-	±2	-	-	±2	LSB
	K, B		-	-	±1	-	-	±1	LSB
Differential Nonlinearity	J, A, S	10-Bit Monotonic T_{MIN} to T_{MAX}	-	-	±4	-	-	±4	LSB
	K, B	12-Bit Monotonic T_{MIN} to T_{MAX}	-	-	±1	-	-	±1	LSB
Gain Error (Using Internal RFB)	J, A, S	DAC Register Loaded with 1111 1111 1111	-	-	±20	-	-	±25	LSB
	K, B	Gain Error is Adjustable Using the Circuits of Figure 5 and 6, (Note 2)	-	-	±10	-	-	±15	LSB
Gain Temperature Coefficient ΔGain/ΔTemperature		Typical Value is 2ppm/°C for V_{DD} = +5V, (Note 3)	-	-	±5	-	-	±10	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD}		ΔV_{DD} = ±5%	0.015	-	0.03	0.01	-	0.02	%
Output Leakage Current at OUT1	J, K	DB0 - DB11 = 0V; $\overline{WR}$, $\overline{CS}$ = 0V (Note 1)	-	-	50	-	-	50	nA
	A, B		-	-	50	-	-	50	nA
	S		-	-	200	-	-	200	nA
DYNAMIC CHARACTERISTICS									
Current Setting Time		To $^1/_2$ LSB OUT1 LOAD = 100Ω, DAC output measured from falling edge of $\overline{WR}$, $\overline{CS}$ = 0V, (Note 3)	-	-	2	-	-	2	µs
Propagation Delay from Digital Input Change to 90% of Final Analog Output		OUT1 LOAD = 100Ω C_{EXT} = 13pF (Note 3 and 4)	-	-	300	-	-	250	ns
Digital to Analog Glitch Impulse		V_{REF} = AGND	-	400	-	-	250	-	nV sec
AC Feedthrough At OUT1		V_{REF} = ±10V, 10kHz Sinewave, (Note 5)	-	5	-	-	5	-	mV_{P-P}
ANALOG OUTPUTS									
Output Capacitance C_{OUT1}		DB0 - DB11 = 0V, $\overline{WR}$, $\overline{CS}$ = 0V, (Note 3)	-	-	70	-	-	70	pF
C_{OUT1}		DB0 - DB11 = V_{DD}, $\overline{WR}$, $\overline{CS}$ = 0V, (Note 3)	-	-	200	-	-	200	pF

Electrical Specifications T_A = See Note 1, V_{REF} = +10V, V_{OUT1} = 0V, AGND = DGND, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	V_{DD} = +5V			V_{DD} = +15V			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
REFERENCE INPUT								
Input Resistance, (Pin 19 to GND)	Input Resistance TC = -300ppm/°C typ	7	-	-	7	-	-	kΩ
	Typical Input Resistance = 11kΩ	-	-	25	-	-	25	kΩ
DIGITAL INPUTS								
Input High Voltage, V_{IH}		2.4	-	-	-	-	13.5	V
Input Low Voltage, V_{IL}		-	-	0.8	-	-	1.5	V
Input Current, I_{IN}	V_{IN} = 0 or V_{DD}, (Note 6)	±1		±10	±1		±10	µA max
Input Capacitance								
DB0 - DB11	V_{IN} = 0, (Note 3)	-	-	7	-	-	7	pF
$\overline{WR}$, $\overline{CS}$	V_{IN} = 0, (Note 3)	-	-	20	-	-	20	pF
SWITCHING CHARACTERISTICS (Note 3)								
Chip Select to Write Setup Time, t_{CS}	See Figure 1	380	200	-	200	120	-	ns
Chip Select to Write Hold Time, t_{CH}	See Figure 1	0	-	-	0	-	-	ns
Write Pulse Width, t_{WR}	$t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$, See Figure 1	400	175	-	240	100		ns
Data Setup Time, t_{DS}	See Figure 1	210	100	-	120	60	-	ns
Data Hold Time, t_{DH}	See Figure 1	10	-	-	10	-	-	ns
POWER SUPPLY CHARACTERISTICS								
I_{DD}	All Digital Inputs V_{IL} or V_{IH}	-	-	2	-	-	2	mA
	All Digital Inputs 0V or V_{DD}	-	100	500	-	100	500	µA
	All Digital Inputs 0V or V_{DD}	-	10	-	-	10	-	µA

NOTES:

1. Temperature Ranges as follows: J, K versions: 0°C to +70°C
   A, B versions: -20°C to +85°C
   S version: -55°C to +125°C
   T_A = +25°C for TYP Specifications. MIN and MAX are measured over the specified operating range.
2. This includes the effect of 5ppm maximum gain TC.
3. Parameter not tested. Parameter guaranteed by design, simulation, or characterization.
4. DB0 - DB11 = 0V to V_{DD} or V_{DD} to 0V in plastic and sidebraze package.
5. Feedthrough can be further reduced by connecting the metal lid on the ceramic package to DGND.
6. Logic inputs are MOS gates. Typical input current (+25°C) is less than 1nA.
7. Typical values are not guaranteed but reflect mean performance specification.
   Specifications subject to change without notice.

Timing Diagram

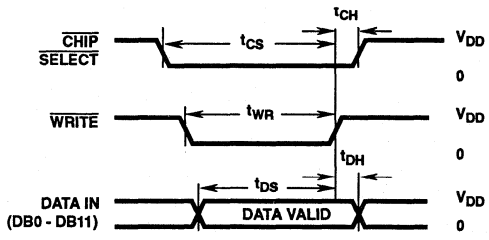


FIGURE 1A. TYPICAL WRITE CYCLE

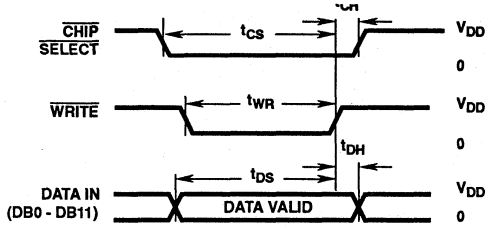


FIGURE 1B. PREFERRED WRITE CYCLE

FIGURE 1. WRITE CYCLE TIMING DIAGRAM

MODE SELECTION	
WRITE MODE:	HOLD MODE:
$\overline{CS}$ and $\overline{WR}$ low, DAC responds to data bus (DB0 - DB11) inputs	Either $\overline{CS}$ or $\overline{WR}$ high, data bus (DB0 - DB11) is locked out; DAC holds last data present when $\overline{WR}$ or $\overline{CS}$ assumed high state.

NOTES:

1. V_{DD} = +5V; $t_R = t_F$ = 20ns
2. V_{DD} = +15V; $t_R = t_F$ = 40ns
3. All input signal rise and fall times measured from 10% to 90% of V_{DD}.
4. Timing measurement reference level is $(V_{IH} + V_{IL})/2$.
5. Since input data latches are transparent for $\overline{CS}$ and $\overline{WR}$ both low, it is preferred to have data valid before $\overline{CS}$ and $\overline{WR}$ both go low. This prevents undesirable changes at the analog output while the data inputs settle.

Circuit Information - D/A Converter Section

Figure 2 shows a simplified circuit of the D/A converter section of the AD7545. Note that the ladder termination resistor is connected to AGND. R is typically 11kΩ.

The binary weighted currents are switched between the OUT1 bus line and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state. One of the current switches is shown in Figure 3.

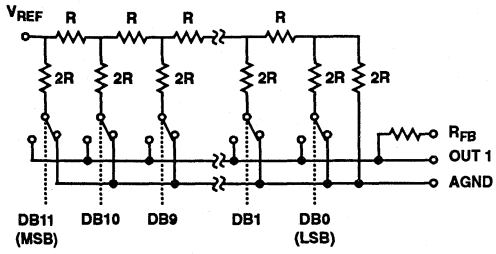


FIGURE 2. SIMPLIFIED D/A CIRCUIT OF AD7545

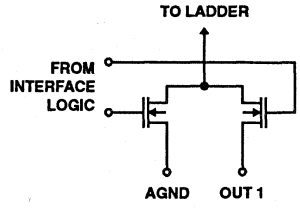


FIGURE 3. N-CHANNEL CURRENT STEERING SWITCH

The capacitance at the OUT1 bus line, C_{OUT1}, is code dependent and varies from 70pF (all switches to AGND) to 200pF (all switches to OUT1).

The input resistance at V_{REF} (Figure 2) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristic resistance and is equal to the value "R"). Since R_{IN} at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external R_{FB} is recommended to define scale factor)Circuit Information - Digital Section.

Figure 4 shows the digital structure for one bit. The digital signals CONTROL and $\overline{CONTROL}$ are generated from $\overline{CS}$ and $\overline{WR}$.

The input buffers are simple CMOS inverters designed such that when the AD7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When V_{IN} is in the region of 2.0V to 3.5V the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7545 may be operated with any supply voltage in the range 5V ≤ V_{DD} ≤ 15V. With V_{DD} = +15V the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V.

Application

Output Offset

CMOS current-steering D/A converters exhibit a code dependent output resistance which in turn causes a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which depends on V_{OS} where V_{OS} is the amplifier input offset voltage. To maintain monotonic operation it is recommended that V_{OS} be no greater than (25×10^{-6}) (V_{REF}) over the temperature range of operation.

General Ground Management

AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7545. In more complex systems where the AGND and DGND connection is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7545 AGND and DGND pins (1N914 or equivalent).

Digital Glitches

When $\overline{WR}$ and $\overline{CS}$ are both low the latched are transparent and the D/A converter inputs follow the data inputs. In some bus systems, data on the data bus is not always valid for the whole period during which $\overline{WR}$ is low and as a result invalid data can briefly occur at the D/A converter inputs during a write cycle. Such invalid data can cause unwanted glitches at the output of the D/A converter. The solution to this problem, if it occurs, is to retime the write pulse ($\overline{WR}$) so that it only occurs when data is valid.

Another cause of digital glitches is capacitive coupling from the digital lines to the OUT1 and AGND terminals. This should be minimized by isolating the analog pins of the AD7545 (Pins 1, 2, 19, 20) from the digital pins by a ground track run between pins 2 and 3 and between pins 18 and 19 of the AD7545. Note how the analog pins are at one end of the package and separated from the digital pins by V_{DD} and DGND to aid isolation at the board level. On-chip capacitive coupling can also give rise to crosstalk from the digital to analog sections of the AD7545, particularly in circuits with high currents and fast rise and fall times. This type of crosstalk is minimized by using V_{DD} = +5V. However, great care should be taken to ensure that the +5V used to power the AD7545 is free from digitally induces noise.

Temperature Coefficients

The gain temperature coefficient of the AD7545 has a maximum value of 5ppm/°C and a typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account.

Basic Applications

Figures 5 and 6 show simple unipolar and bipolar circuits using the AD7545. Resistor R1 is used to trim for full scale. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. Note that the circuits of Figures 5 and 6 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 5 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0V to $-V_{IN}$ (note the inversion introduced by the op amp) or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20V \leq V_{IN} \leq +20V$ (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table 2 shows the code relationship for the circuit of Figure 5.

Figure 6 and Table 3 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code and inverter U_1 on the MSB line converts 2's complement input code to offset binary code. If appropriate, inversion of the MSB may be done in software using an exclusive -OR instruction and the inverter omitted. R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

The choice of the operational amplifiers in Figure 5 and Figure 6 depends on the application and the trade off between required precision and speed. Below is a list of operational amplifiers which are good candidates for many applications. The main selection criteria for these operational amplifiers is to have low V_{OS}, low V_{OS} drift, low bias current and low settling time.

These amplifiers need to maintain the low nonlinearity and monotonic operation of the D/A while providing enough speed for maximum converter performance.

Operational Amplifiers

HA5127 Ultra Low Noise, Precision
HA5137 Ultra Low Noise, Precision, Wide Band
HA5147 Ultra Low Noise, Precision, High Slew Rate
HA5170 Precision, JFET Input

TABLE 1. RECOMMENDED TRIM RESISTOR VALUES vs GRADES FOR V_{DD} = +5V

TRIM RESISTOR	J, A, S	K, B
R1	500Ω	200Ω
R2	150Ω	68Ω

TABLE 2. UNIPOLAR BINARY CODE TABLE FOR CIRCUIT OF FIGURE 5

BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT
1111	1111	1111	$-V_{IN}\{\frac{4095}{4096}\}$
1000	0000	0000	$-V_{IN}\{\frac{2048}{4096}\} = -\frac{1}{2}V_{IN}$
0000	0000	0001	$-V_{IN}\{\frac{1}{4096}\}$
0000	0000	0000	0V

TABLE 3. 2'S COMPLEMENT CODE TABLE FOR CIRCUIT OF FIGURE 6

DATA INPUT			ANALOG OUTPUT
0111	1111	1111	$+V_{IN} \bullet \{\frac{2047}{2048}\}$
0000	0000	0001	$+V_{IN} \bullet \{\frac{1}{2048}\}$
0000	0000	0000	0V
1111	1111	1111	$-V_{IN} \bullet \{\frac{1}{2048}\}$
1000	0000	0000	$-V_{IN} \bullet \{\frac{2048}{2048}\}$

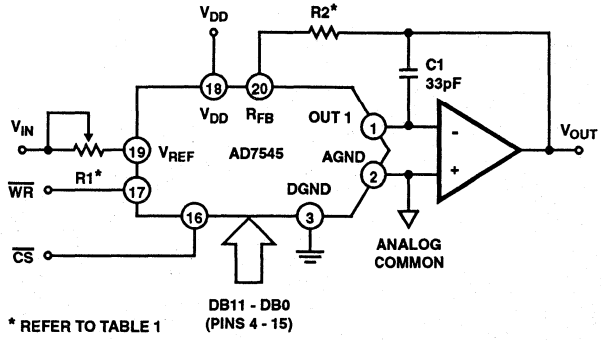


FIGURE 5. UNIPOLAR BINARY OPERATION

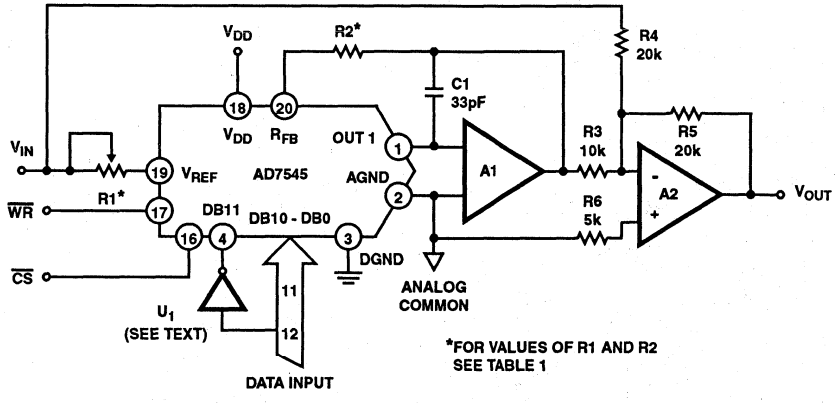


FIGURE 6. BIPOLAR OPERATION (2'S COMPLEMENT CODE)

Die Characteristics

DIE DIMENSIONS:
121 x 123mils (3073 x 3124micrms)

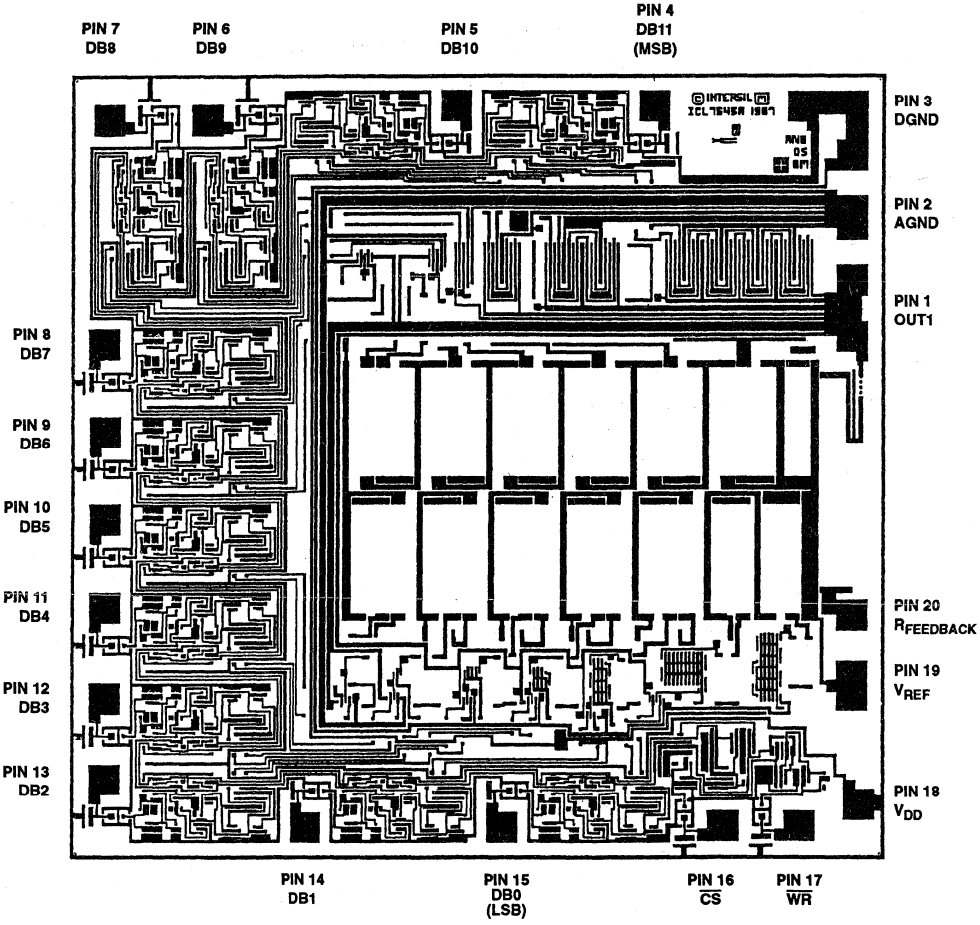
METALLIZATION:
Type: Pure Aluminum
Thickness: 10 ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
PSG: 7 ± 1.4kÅ
Nitride: 8 ± 1.2kÅ

PROCESS: CMOS Metal Gate

Metallization Mask Layout

AD7545



CA3338, CA3338A

CMOS Video Speed 8-Bit R2R D/A Converter

December 1993

Features

- CMOS/SOS Low Power
- R2R Output, Segmented for Low "Glitch"
- CMOS/TTL Compatible Inputs
- Fast Settling: 20ns (Typ) to $^1/_2$ LSB
- Feedthrough Latch for Clocked or Unclocked Use
- ±0.5 LSB Accuracy (Typ)
- Data Complement Control
- High Update Rate 50MHz (Typ)
- Unipolar or Bipolar Operation

Applications

- TV/Video Display
- High Speed Oscilloscope Display
- Digital Waveform Generator
- Direct Digital Synthesis

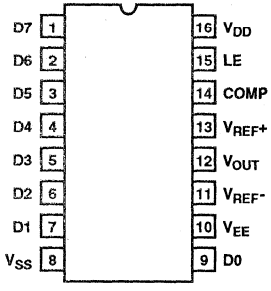
Description

The CA3338 family are CMOS/SOS high speed R2R voltage output digital-to-analog converters. They can operate from a single +5V supply, at video speeds, and can produce "rail-to-rail" output swings. Internal level shifters and a pin for an optional second supply provide for an output range below digital ground. The data complement control allows the inversion of input data while the latch enable control provides either feedthrough or latched operation. Both ends of the R2R ladder network are available externally and may be modulated for gain or offset adjustments. In addition, "glitch" energy has been kept very low by segmenting and thermometer encoding of the upper 3 bits.

The CA3338 is manufactured on a sapphire substrate to give low dynamic power dissipation, low output capacitance, and inherent latch-up resistance.

Pinout

CA3338, CA3338A
(PDIP, CDIP, SOIC)
TOP VIEW



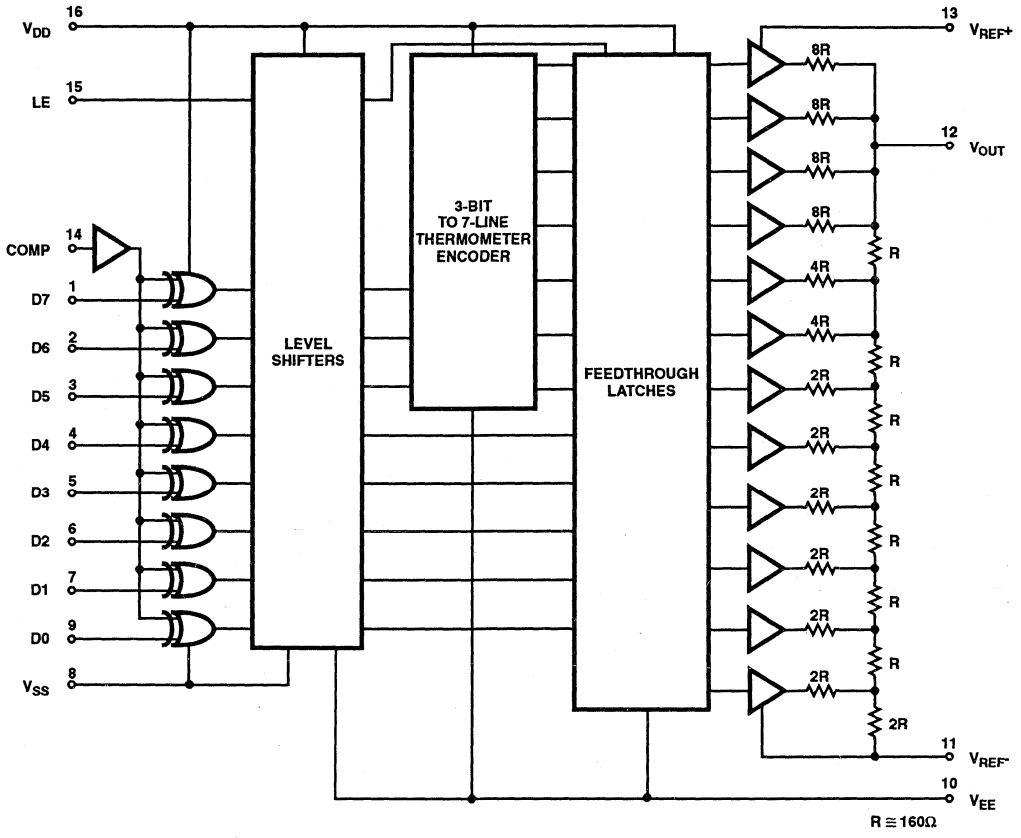
Ordering Information

PART NUMBER	LINEARITY (INL, DNL)	TEMPERATURE RANGE	PACKAGE
CA3338E	±1.0 LSB	-40°C to +85°C	16 Lead Plastic DIP
CA3338AE	±0.75 LSB	-40°C to +85°C	16 Lead Plastic DIP
CA3338D	±1.0 LSB	-55°C to +125°C	16 Lead Ceramic DIP
CA3338AD	±0.75 LSB	-55°C to +125°C	16 Lead Ceramic DIP
CA3338M	±1.0 LSB	-40°C to +85°C	16 Lead Plastic SOIC (W)
CA3338AM	±0.75 LSB	-40°C to +85°C	16 Lead Plastic SOIC (W)

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 1850.1

Functional Diagram



Die Characteristics

DIE DIMENSIONS:
2.050µm x 2.200µm x 530 ± 50µm

METALLIZATION:
Type: Al with 0.8% Si
Thickness: 11kÅ ± 1kÅ

GLASSIVATION:
Type: 3% PSG
Thickness: 13kÅ ± 2.6kÅ

Absolute Maximum Ratings

DC Supply-Voltage Range ..... -0.5V to +8V
(V_{DD} - V_{SS} or V_{DD} - V_{EE}, whichever is greater)
Input Voltage Range
Digital Inputs (LE, COMP D0 - D7) ..... V_{SS} - 0.5V to V_{DD} + 0.5V
Analog Pins (V_{REF}+, V_{REF}-, V_{OUT}) ..... V_{DD} - 8V to V_{DD} + 0.5V
DC Input Current
Digital Inputs (LE, COMP, D0 - D7) ..... ±20mA
Recommended Supply Voltage Range ..... 4.5V to 7.5V
Storage Temperature Range, T_{STG} ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	77°C/W	12°C/W
Plastic DIP Package	100°C/W	-
SOIC Package	100°C/W	-

Maximum Power Dissipation, P_D
T_A = -55°C to +55°C 315mW
Operating Temperature Range (T_A)
Ceramic Package, D suffix ..... -55°C to +125°C
Plastic Package, E suffix, M suffix ..... -40°C to +85°C
Junction Temperature
Ceramic Package ..... +175°C
Plastic Package ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V_{DD} = 5V, V_{REF}+ = 4.608V, V_{SS} = V_{EE} = V_{REF}- = GND, LE clocked at 20MHz, $R_L \geq 1$ MΩ, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ACCURACY					
Resolution		8	-	-	Bits
Integral Linearity Error	See Figure 4				
CA3338		-	-	±1	LSB
CA3338A		-	-	±0.75	LSB
Differential Linearity Error	See Figure 4				
CA3338		-	-	±0.75	LSB
CA3338A		-	-	±0.5	LSB
Gain Error	Input Code = FF_{HEX}, See Figure 3				
CA3338		-	-	±0.75	LSB
CA3338A		-	-	±0.5	LSB
Offset Error	Input Code = 00_{HEX}; See Figure 3	-	-	±0.25	LSB
DIGITAL INPUT TIMING					
Update Rate	To Maintain $^1/_2$ LSB Settling	DC	50	-	MHz
Update Rate	V_{REF}- = V_{EE} = -2.5V, V_{REF}+ = +2.5V	DC	20	-	MHz
Set Up Time T_{SU1}	For Low Glitch	-	-2	-	ns
Set Up Time T_{SU2}	For Data Store	-	8	-	ns
Hold Time T_H	For Data Store	-	5	-	ns
Latch Pulse Width T_W	For Data Store	-	5	-	ns
Latch Pulse Width T_W	V_{REF}- = V_{EE} = -2.5V, V_{REF}+ = +2.5V	-	25	-	ns
OUTPUT PARAMETERS	R_L Adjusted for $1V_{P-P}$ Output				
Output Delay T_{D1}	From LE Edge	-	25	-	ns
Output Delay T_{D2}	From Data Changing	-	22	-	ns
Rise Time T_R	10% to 90% of Output	-	4	-	ns
Settling Time T_S	10% to Settling to $^1/_2$ LSB	-	20	-	ns
Output Impedance	V_{REF}+ = 6V, V_{DD} = 6V	120	160	200	Ω
Glitch Area		-	150	-	pV-s
Glitch Area	V_{REF}- = V_{EE} = -2.5V, V_{REF}+ = +2.5V	-	250	-	pV-s

Electrical Specifications $T_A = +25°C$, $V_{DD} = 5V$, $V_{REF}+ = 4.608V$, $V_{SS} = V_{EE} = V_{REF}- = GND$, LE clocked at 20MHz, $R_L \geq 1 M\Omega$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE VOLTAGE					
$V_{REF}+$ Range	(+) Full Scale, Note 1	$V_{REF}- + 3$	-	V_{DD}	V
$V_{REF}-$ Range	(-) Full Scale, Note 1	V_{EE}	-	$V_{REF}+ - 3$	V
$V_{REF}+$ Input Current	$V_{REF}+ = 6V$, $V_{DD} = 6V$	-	40	50	mA
SUPPLY VOLTAGE					
Static I_{DD} or I_{EE}	LE = Low, D0 - D7 = High	-	100	220	µA
	LE = Low, D0 - D7 = Low	-	-	100	µA
Dynamic I_{DD} or I_{EE}	V_{OUT} = 10MHz, 0V to 5V Square Wave	-	20	-	mA
Dynamic I_{DD} or I_{EE}	V_{OUT} = 10MHz, ±2.5V Square Wave	-	25	-	mA
V_{DD} Rejection	50kHz Sine Wave Applied	-	3	-	mV/V
V_{EE} Rejection	50kHz Sine Wave Applied	-	1	-	mV/V
DIGITAL INPUTS D0 - D7, LE, COMP					
High Level Input Voltage	Note 1	2	-	-	V
Low Level Input Voltage	Note 1	-	-	0.8	V
Leakage Current		-	±1	±5	µA
Capacitance		-	5	-	pF
TEMPERATURE COEFFICIENTS					
Output Impedance		-	200	-	ppm/°C

NOTE:

1. Parameter not tested. but guaranteed by design or characterization.

Pin Descriptions

PIN	NAME	DESCRIPTION
1	D7	Most Significant Bit
2	D6	Input
3	D5	Data
4	D4	Bits
5	D3	(High = True)
6	D2	
7	D1	
8	V_{SS}	Digital Ground
9	D_0	Least Significant Bit. Input Data Bit
10	V_{EE}	Analog Ground
11	$V_{REF}-$	Reference Voltage Negative Input
12	V_{OUT}	Analog Output
13	$V_{REF}+$	Reference Voltage Positive Input
14	COMP	Data Complement Control input. Active High
15	LE	Latch Enable Input. Active Low
16	V_{DD}	Digital Power Supply, +5V

Digital Signal Path

The digital inputs (LE, COMP, and D0 - D7) are of TTL compatible HCT High Speed CMOS design: the loading is essentially capacitive and the logic threshold is typically 1.5V.

The 8 data bits, D0 (weighted 2^0) through D7 (weighted 2^7), are applied to Exclusive OR gates (see Functional Diagram). The COMP (data complement) control provides the second input to the gates: if COMP is high, the data bits will be inverted as they pass through.

The input data and the LE (latch enable) signals are next applied to a level shifter. The inputs, operating between the levels of V_{DD} and V_{SS}, are shifted to operate between V_{DD} and V_{EE}. V_{EE} optionally at ground or at a negative voltage, will be discussed under bipolar operation. All further logic elements except the output drivers operate from the V_{DD} and V_{EE} supplies.

The upper 3 bits of data, D5 through D7, are input to a 3-to-7 line bar graph encoder. The encoder outputs and D0 through D4 are applied to a feedthrough latch, which is controlled by LE (latch enable).

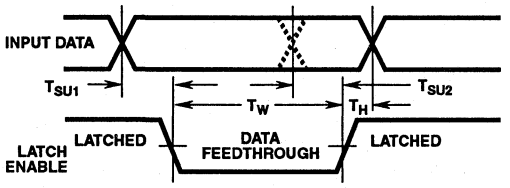


FIGURE 1. DATA TO LATCH ENABLE TIMING

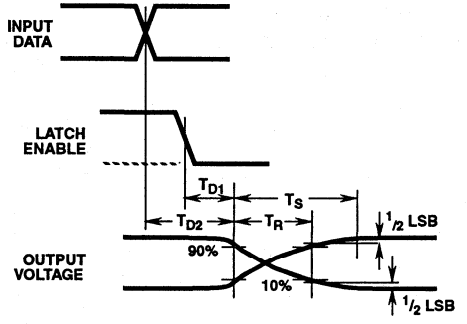


FIGURE 2. DATA AND LATCH ENABLE TO OUTPUT TIMING

Latch Operation

Data is fed from input to output while LE is low: LE should be tied low for non-clocked operation.

Non-clocked operation or changing data while LE is low is not recommended for applications requiring low output "glitch" energy: there is no guarantee of the simultaneous changing of input data or the equal propagation delay of all bits through the converter. Several parameters are given if the converter is to be used in either of these modes: T_{D2} gives the delay from the input changing to the output changing (10%), while T_{SU2} and T_H give the set up and hold times (referred to LE rising edge) needed to latch data. See Figures 1 and 2.

Clocked operation is needed for low "glitch" energy use. Data must meet the given T_{SU1} set up time to the LE falling edge, and the T_H hold time from the LE rising edge. The delay to the output changing, T_{D1}, is now referred to the LE falling edge.

There is no need for a square wave LE clock; LE must only meet the minimum T_W pulse width for successful latch operation. Generally, output timing (desired accuracy of settling) sets the upper limit of usable clock frequency.

Output Structure

The latches feed data to a row of high current CMOS drivers, which in turn feed a modified R2R ladder network.

The "N" channel (pull down) transistor of each driver plus the bottom "2R" resistor are returned to V_{REF}- this is the (-) full-scale reference. The "P" channel (pull up) transistor of each driver is returned to V_{REF}+, the (+) full-scale reference.

In unipolar operation, V_{REF}- would typically be returned to analog ground, but may be raised above ground (see specifications). There is substantial code dependent current that flows from V_{REF}+ to V_{REF}- (see V_{REF}+ input current in specifications), so V_{REF}- should have a low impedance path to ground.

In bipolar operation, V_{REF}- would be returned to a negative voltage (the maximum voltage rating to V_{DD} must be observed). V_{EE}, which supplies the gate potential for the output drivers, must be returned to a point at least as negative as V_{REF}-. Note that the maximum clocking speed decreases when the bipolar mode is used.

Static Characteristics

The ideal 8-bit D/A would have an output equal to V_{REF}- with an input code of 00_{HEX} (zero scale output), and an output equal to 255/256 of V_{REF}+ (referred to V_{REF}-) with an input code of FF_{HEX} (full-scale output). The difference between the ideal and actual values of these two parameters are the OFFSET and GAIN errors, respectively; see Figure 3.

If the code into an 8-bit D/A is changed by 1 count, the output should change by 1/255 (full-scale output-zero scale output). A deviation from this step size is a differential linearity error, see Figure 4. Note that the error is expressed in fractions of the ideal step size (usually called an LSB). Also note that if the (-) differential linearity error is less (in absolute numbers) than 1 LSB, the device is monotonic. (The output will always increase for increasing code or decrease for decreasing code).

If the code into an 8-bit D/A is at any value, say "N", the output voltage should be N/255 of the full-scale output (referred to the zero-scale output). Any deviation from that output is an integral linearity error, usually expressed in LSBs. See Figure 4.

Note that OFFSET and GAIN errors do not affect integral linearity, as the linearity is referenced to actual zero and full-scale outputs, not ideal. Absolute accuracy would have to also take these errors into account.

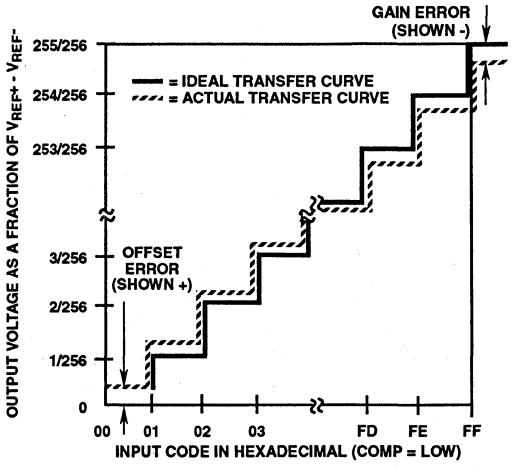


FIGURE 3. D/A OFFSET AND GAIN ERROR

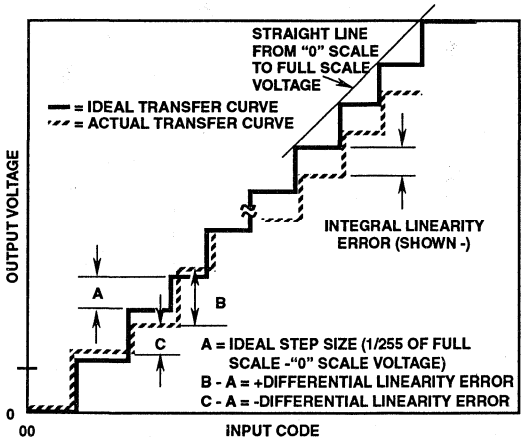


FIGURE 4. D/A INTEGRAL AND DIFFERENTIAL LINEARITY ERROR

Dynamic Characteristics

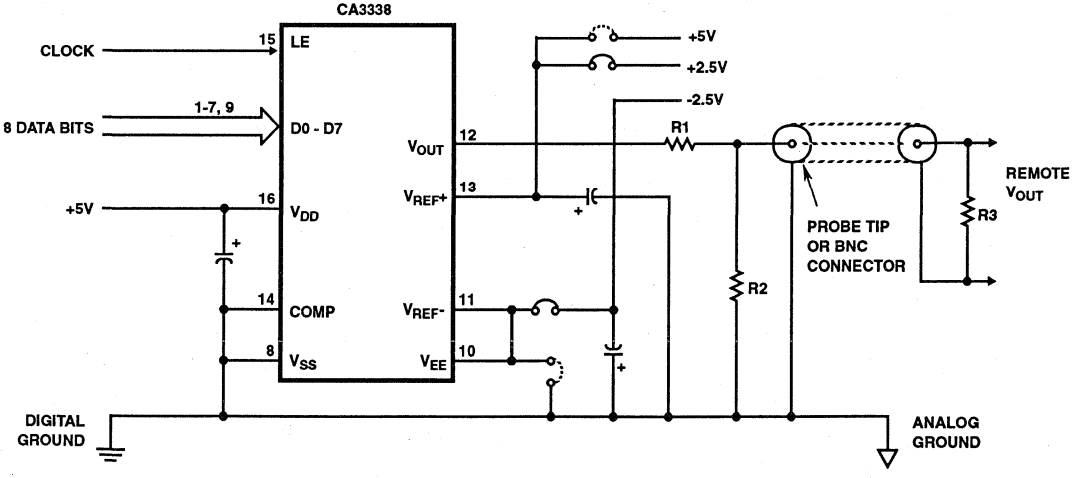
Keeping the full-scale range ($V_{REF}+ - V_{REF}-$) as high as possible gives the best linearity and lowest "glitch" energy (referred to 1V). This provides the best "P" and "N" channel gate drives (hence saturation resistance) and propagation delays. The $V_{REF}+$ (and $V_{REF}-$ if bipolar) terminal should be well bypassed as near the chip as possible.

"Glitch" energy is defined as a spurious voltage that occurs as the output is changed from one voltage to another. In a binary input converter, it is usually highest at the most significant bit transition ($7F_{HEX}$ to 80_{HEX} for an 8 bit device), and can be measured by displaying the output as the input code alternates around that point. The "glitch" energy is the area between the actual output display and an ideal one LSB step voltage (subtracting negative area from positive), at either the positive or negative-going step. It is usually expressed in pV-s.

The CA3338 uses a modified R2R ladder, where the 3 most significant bits drive a bar graph decoder and 7 equally weighted resistors. This makes the "glitch" energy at each 1/8 scale transition ($1F_{HEX}$ to 20_{HEX}, $3F_{HEX}$ to 40_{HEX}, etc.) essentially equal, and far less than the MSB transition would otherwise display.

For the purpose of comparison to other converters, the output should be resistively divided to 1V full-scale. Figure 5 shows a typical hook-up for checking "glitch" energy or settling time.

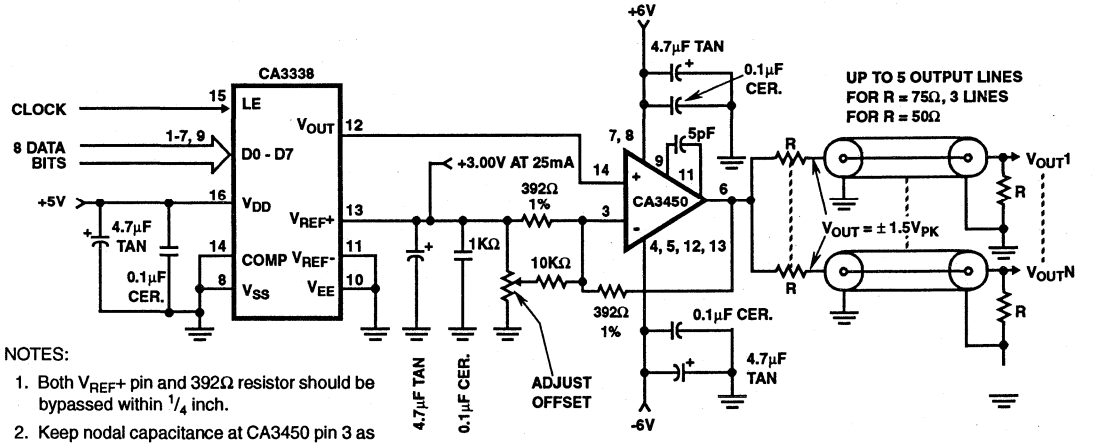
The settling time of the A/D is mainly a function of the output resistance (approximately 160Ω in parallel with the load resistance) and the load plus internal chip capacitance. Both "glitch" energy and settling time measurements require very good circuit and probe grounding: a probe tip connector such as Tektronix part number 131-0258-00 is recommended.



FUNCTION	CONNECTOR	R1	R2	R3	V_{OUT} (PK-PK)
Oscilloscope Display	Probe Tip	82Ω	62Ω	N/C	1V
Match 93Ω Cable	BNC	75	160	93	1V
Match 75Ω Cable	BNC	18	130	75	1V
Match 50Ω Cable	BNC	Short	75	50	0 79V

NOTES:
1. V_{OUT}(PK) is approximate, and will vary as R_{OUT} of D/A varies.
2. All drawn capacitors are 0.1µF multilayer ceramic/4.7µF tantalum.
3. Dashed connections are for unipolar operation. Solid connection are for bipolar operation.

FIGURE 5. CA3338 DYNAMIC TEST CIRCUIT



NOTES:

1. Both V_{REF}+ pin and 392Ω resistor should be bypassed within $^1/_4$ inch.
2. Keep nodal capacitance at CA3450 pin 3 as low as possible.
3. V_{OUT} Range = ±3V at CA3450.

FIGURE 6. CA3338 AND CA3450 FOR DRIVING MULTIPLE COAXIAL LINES

TABLE 1. OUTPUT VOLTAGE vs INPUT CODE AND V_{REF}

V_{REF}+ V_{REF}- STEP SIZE	5.12V 0 0.0200V	5.00V 0 0.0195V	4.608V 0 0.0180V	2.56V -2.56V 0.0200V	2.50V -2.50V 0.0195V
Input Code					
$11111112 = FF_{HEX}$	5.1000V	4.9805V	4.5900V	2.5400V	2.4805V
$11111102 = FE_{HEX}$	5.0800	4.9610	4.5720	2.5200	2.4610
•					
•					
•					
$10000001_2 = 81_{HEX}$	2.5800	2.5195	2.3220	0.0200	0.0195
$10000000_2 = 80_{HEX}$	2.5600	2.5000	2.3040	0.0000	0.0000
$01111111_2 = 7F_{HEX}$	2.5400	2.4805	2.2860	- 0.0200	-0.0195
•					
•					
•					
$00000001_2 = 01_{HEX}$	0.0200	0.0195	0.0180	-2.5400	-2.4805
$00000000_2 = 00_{HEX}$	0.0000	0.0000	0.0000	-2.5600	-2.5000

Applications

The output of the CA3338 can be resistively divided to match a doubly terminated 50Ω or 75Ω line, although peak-to-peak swings of less than 1V may result. The output magnitude will also vary with the converter's output impedance. Figure 5 shows such an application. Note that because of the HCT input structure, the CA3338 could be operated up to +7.5V V_{DD} and V_{REF}+ supplies and still accept 0V to 5V CMOS input voltages.

If larger voltage swings or better accuracy is desired, a high speed output buffer, such as the HA-5033, HA-2542, or CA3450, can be employed. Figure 6 shows a typical application, with the output capable of driving ±2V into multiple 50Ω terminated lines.

Operating and Handling Considerations

1. Handling

All inputs and outputs of CMOS devices have a network for electrostatic protection during handling. Recommended handling practices for CMOS devices are described in AN6525. "Guide to Better Handling and Operation of CMOS Integrated Circuits."

2. Operating

Operating Voltage

During operation near the maximum supply voltage limit, care should be taken to avoid or suppress power supply turn-on and turn-off transients, power supply ripple, or ground noise; any of these conditions must not cause the absolute maximum ratings to be exceeded.

Input Signals

To prevent damage to the input protection circuit, input signals should never be greater than V_{DD} nor less than V_{SS}. Input currents must not exceed 20mA even when the power supply is off.

Unused Inputs

A connection must be provided at every input terminal. All unused input terminals must be connected to either V_{CC} or GND, whichever is appropriate.

HARRIS SEMICONDUCTOR

HI-565A

High Speed Monolithic D/A Converter with Reference

December 1993

Features

- 12-Bit DAC and Reference on a Single Chip
- Pin Compatible With AD565A
- Very High Speed: Settles to ±0.5 LSB in 250ns, Max. Full Scale Switching Time 30ns, Typ.
- Guaranteed For Operation With ±12V Supplies
- Monotonicity Guaranteed Over Temperature
- ±0.5 LSB Max. Nonlinearity Guaranteed Over Temp
- Low Gain Drift (Max., DAC Plus Ref) 25ppm/°C
- Low Power Dissipation 250mW

Applications

- CRT Displays
- High Speed A/D Converters
- Signal Reconstruction
- Waveform Synthesis

Description

The HI-565A is a fast, 12 bit current output, digital to analog converter. The monolithic chip includes a precision voltage reference, thin-film R2R ladder, reference control amplifier and twelve high speed bipolar current switches.

The Harris dielectric isolation process provides latch free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code dependent ground currents.

HI-565A dice are laser trimmed for a maximum integral non-linearity error of ±0.5 LSB at +25°C. In addition, the low noise buried zener reference is trimmed both for absolute value and temperature coefficient. Power dissipation is typically 250mW, with ±15V supplies.

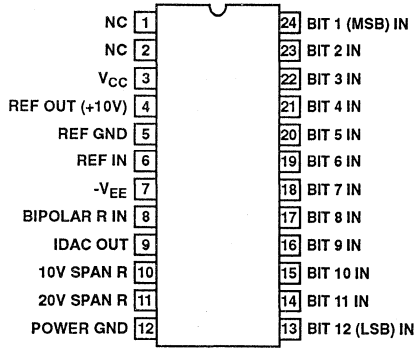
The HI-565A is offered in both commercial and military grades. See Ordering Information.

Ordering Information

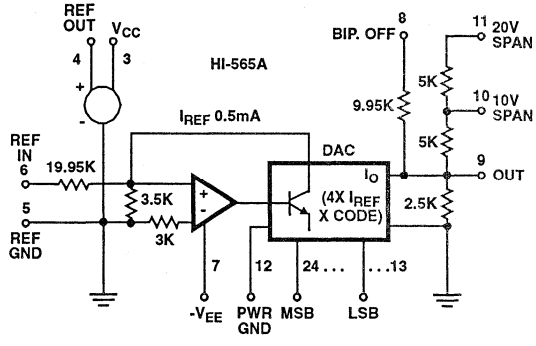
PART NUMBER	LINEARITY (INL)	LINEARITY (DNL)	TEMPERATURE RANGE	PACKAGE
HI1-565AJD-5	0.50 LSB	0.75 LSB	0°C to +75°C	24 Lead Ceramic Side Brazed DIP
HI1-565AKD-5	0.25 LSB	0.50 LSB	0°C to +75°C	24 Lead Ceramic Side Brazed DIP
HI1-565ASD-2	0.50 LSB	0.75 LSB	-55°C to +125°C	24 Lead Ceramic Side Brazed DIP
HI1-565ATD-2	0.25 LSB	0.50 LSB	-55°C to +125°C	24 Lead Ceramic Side Brazed DIP
HI1-565ASD/883	0.50 LSB	0.50 LSB	-55°C to +125°C	24 Lead Ceramic Side Brazed DIP
HI1-565ATD/883	0.25 LSB	0.50 LSB	-55°C to +125°C	24 Lead Ceramic Side Brazed DIP

Pinout

HI-565A (CDIP, SOIC)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3109

Absolute Maximum Ratings

V_{CC} to Power GND ..... 0V to +18V
V_{EE} to Power GND ..... 0V to -18V
Voltage on DAC Output (Pin 9) ..... -3V to +12V
Digital Inputs (Pins 13-24) to Power GND ..... -1V to +7.0V
REF In to REF GND ..... ±12V
Bipolar Offset to REF GND ..... ±12V
10V Span R to REF GND ..... ±12V
20V Span R to REF GND ..... ±24V
REF Out ..... Indefinite Short to Power GND
Momentary Short to V_{CC}
Transistor Count 200
Process ..... Bipolar-DI

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic Side Brazed DIP Package	63°C/W	12°C/W

Maximum Package Power Dissipation
Ceramic Side Brazed DIP Package 500mW
SOIC Package 500mW
Operating Temperature Range
HI-565AS,T-2 ..... -55°C to +125°C
H1-565AJ, K-5 ..... 0°C to +75°C
Junction Temperature ..... 175°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, Unless Otherwise Specified)

PARAMETER	TEST CONDITIONS	HI-565AJ, HI565AS			HI-565AK, HI-565AT			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DATA INPUTS (Pins 13 to 24) (Note 1)								
Input Voltage Bit ON Logic "1"	(T_{MIN} to T_{MAX})	+2.0	-	+5.5	+2.0	-	+5.5	V
Input Voltage Bit OFF Logic "0"	(T_{MIN} to T_{MAX})	-	-	+0.8	-	-	+0.8	V
Logic Current Bit ON Logic "1"	(T_{MIN} to T_{MAX})	-	0.01	+1.0	-	0.01	+1.0	µA
Logic Current Bit OFF Logic "0"	(T_{MIN} to T_{MAX})	-	-2.0	-20	-	-2.0	-20	µA
Resolution		12	-	-	12	-	-	Bits
OUTPUT								
Unipolar Current	(All Bits ON)	-1.6	-2.0	-2.4	-1.6	-2.0	-2.4	mA
Bipolar Current	(All Bits ON or OFF)	±0.8	±1.0	±1.2	±0.8	±1.0	±1.2	mA
Resistance	(Exclusive of Span Resistors)	1.8K	2.5K	3.2K	1.8K	2.5K	3.2K	Ω
Unipolar Offset at +25°C ±0.07°C Over Temperature		-	0.01	0.05	-	0.01	0.05	% of F.S.
Bipolar Offset at ±0.2 (T), ±0.25 (S) Over Temperature	(Figure 2, R_3 = 50Ω Fixed)	-	0.05	0.15	-	0.05	0.1	% of F.S.
Capacitance		-	20	-	-	20	-	pF
Compliance Voltage	(T_{MIN} to T_{MAX})	-1.5	-	+10	-1.5	-	+10	V
ACCURACY (Error Relative to Full Scale)								
Integral Non-Linearity	(+25°C) End Point Method	-	±0.25 (0.006)	±0.50 (0.012)	-	±0.12 (0.003)	±0.12 (0.006)	LSB % of F.S.
Integral Non-Linearity	(T_{MIN} to T_{MAX}) End Point Method	-	±0.50 (0.012)	±0.75 (0.018)	-	±0.25 (0.006)	±0.50 (0.012)	LSB % of F.S.
Differential Non-Linearity	+25°C	-	±0.50	±0.75	-	±0.25	±0.50	LSB
Differential Non-Linearity	T_{MIN} to T_{MAX}	MONOTONICITY GUARANTEED						
TEMPERATURE COEFFICIENTS								
With Internal Reference Unipolar Zero		-	1	2	-	1	2	ppm/°C
With Internal Reference Bipolar Zero		-	5	10	-	5	10	ppm/°C
With Internal Reference Gain (Full Scale)		-	15	40	-	10	25	ppm/°C

Electrical Specifications (T_A = +25°C, V_{CC} = +15V, V_{EE} = -15V, Unless Otherwise Specified) **(Continued)**

PARAMETER	TEST CONDITIONS	HI-565AJ, HI565AS			HI-565AK, HI-565AT			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
With Internal Reference Differential Nonlinearity		-	2	-	-	2	-	ppm/°C
SETTLING TIME T0 ±0.5 LSB								
With High, Z External Load	(Note 2)	-	350	500	-	350	500	ns
With 75Ω External Load		-	150	250	-	150	250	ns
FULL SCALE TRANSITION (From 50% of Logic Input to 90% of Analog Output)								
Rise Time		-	15	30	-	15	30	ns
Fall Time		-	30	50	-	30	50	ns
POWER REQUIREMENTS								
V_{CC}	(+11.4 to +16.5VDC)	-	9.0	11.8	-	9.0	11.8	mA
V_{EE}	(+11.4 to -16.5VDC)	-	-9.5	-14.5	-	-9.5	-14.5	mA
POWER SUPPLY GAIN SENSITIVITY (Note 3)								
V_{CC}	(+11.4 to +16.5VDC)	-	3	10	-	3	10	ppm of F.S./%
V_{EE}	(+11.4 to -16.5VDC)	-	15	25	-	15	25	ppm of F.S./%
PROGRAMMABLE OUTPUT RANGES (See Table 2)								
Unipolar 5	(Note 1)	0 to +5			0 to +5			V
Bipolar 5	(Note 1)	-2.5 to +2.5			-2.5 to +2.5			V
Unipolar 10	(Note 1)	0 to +10			0 to +10			V
Bipolar 10	(Note 1)	-5 to +5			-5 to +5			V
Bipolar 20	(Note 1)	-10 to +10			-10 to +10			V
EXTERNAL ADJUSTMENTS								
Gain Error with Fixed 50Ω Resister for R2 (Figure 1)		-	±0.1	±0.25	-	±0.1	±0.25	% of F.S.
Bipolar Zero Error with Fixed 50Ω Resister for R3 (Figure 2)		-	±0.05	±0.15	-	±0.05	±0.1	% of F.S.
Gain Adjustment Range (Figure 1)		±0.25	-	-	±0.25	-	-	% of F.S.
Bipolar Zero Adjustment Range		±0.15	-	-	±0.15	-	-	% of F.S.
REFERENCE INPUT								
Input Impedance		15K	20K	25K	15K	20K	25K	-
REFERENCE OUTPUT								
Voltage		9.90	10.00	10.10	9.90	10.00	10.10	V
Current (Available for External Loads)		1.5	2.5	-	1.5	2.5	-	mA

NOTES:

1. Guaranteed by characterization or design but not tested over the operating temperature range.
2. See settling time discussion and Figure 3.
3. The Power Supply Gain Sensitivity is tested in reference to a V_{CC}, V_{EE} of ±15V.

Definitions of Specifications

Digital Inputs

The HI-565A accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement (Note 1), or Offset Binary, (See Operating Instructions).

TABLE 1.

DIGITAL INPUT	ANALOG OUTPUT		
	STRAIGHT BINARY	OFFSET BINARY	(NOTE 1) TWO'S COMPLEMENT
MSB...LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	$^1/_2$FS	Zero	-FS
111...111	+FS - 1 LSB	+FS - 1 LSB	Zero - 1 LSB
011...111	1/2FS - 1 LSB	Zero - 1 LSB	+FS - 1 LSB

NOTE:
1. Invert MSB with external inverter to obtain Two's Complement Coding.

Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON) (End Point Method).

Differential Nonlinearity for a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases for an increasing input.

Settling Time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition, settling to within ±0.5 LSB of final value.

Gain Drift is the change in full scale analog output over the specified temperature range, expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst-case drift.

Offset Drift is the change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only, and makes no claims to accuracy.

Glitch a glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Detailed Description

Op Amp Selection

The HI-565As current output may be converted to voltage using the standard connections shown in Figures 1 and 2. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy.

For highest precision, use an HA-5130. This amplifier contributes negligible error, but requires about 11µs to settle within ±0.1% following a 10V step.

The Harris Semiconductor HA-2600 is the best all-around choice for this application, and it settles in 1.5µs (also to ±0.1% following a 10V step). Remember, settling time for the DAC amplifier combination is the square root of t_D^2 plus t_A^2, where t_D, t_A are settling times for the DAC and amplifier.

No-Trim Operation

The HI-565A will perform as specified without calibration adjustments. To operate without calibration, substitute 50Ω resistors for the 100Ω trimming potentiometers: In Figure 1 replace R2 with 50Ω also remove the network on pin 8 and connect 50Ω to ground. For bipolar operation in Figure 2, replace R3 and R4 with 50Ω resistors.

With these changes, performance is guaranteed as shown under Specifications, "External Adjustments". Typical unipolar zero will be ±0.5 LSB plus the op amp offset.

The feedback capacitor C must be selected to minimize settling time.

Calibration

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero. For the HI-565A, these adjustments are similar whether the current output is used, or whether an external op amp is added to convert this current to a voltage. Refer to Table 2 for the voltage output case, along with Figure 1 or Figure 2.

Calibration is a two step process for each of the five output ranges shown in Table 2. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum value is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

TABLE 2. OPERATING MODES AND CALIBRATION

MODE	CIRCUIT CONNECTIONS				CALIBRATION		
	OUTPUT PRANGE	PIN 10 TO	PIN 11 TO	RESISTOR (R)	APPLY INPUT CODE	ADJUST	TO SET V_O
Unipolar (See Figure 1)	0 to +10V	V_O	Pin 10	1.43K	All 0's All 1's	R1 R2	0V +9.99756V
	0 to +5V	V_O	Pin 9	1.1K	All 0's All 1's	R1 R2	0V +4.99878V
Bipolar (See Figure 2)	±10V	NC	V_O	1.69K	All 0's All 1's	R3 R4	-10V +9.99512V
	±5V	V_O	Pin 10	1.43K	All 0's All 1's	R3 R4	-5V +4.99756V
	±2.5V	V_O	Pin 9	1.1K	All 0's All 1's	R3 R4	-2.5V +2.49878V

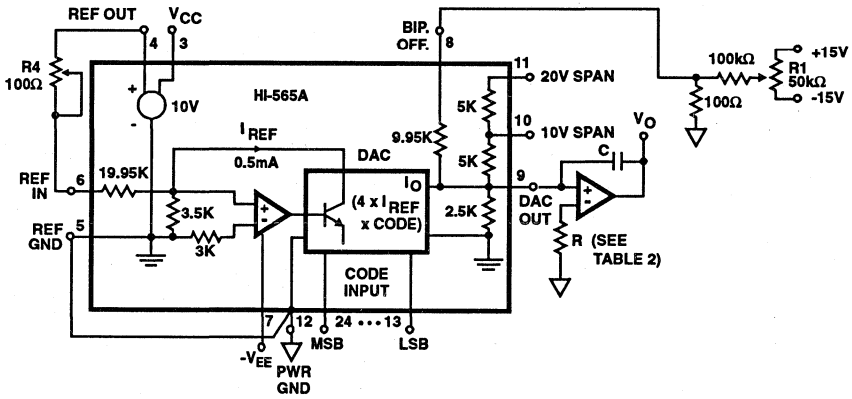


FIGURE 1. UNIPOLAR VOLTAGE OUTPUT

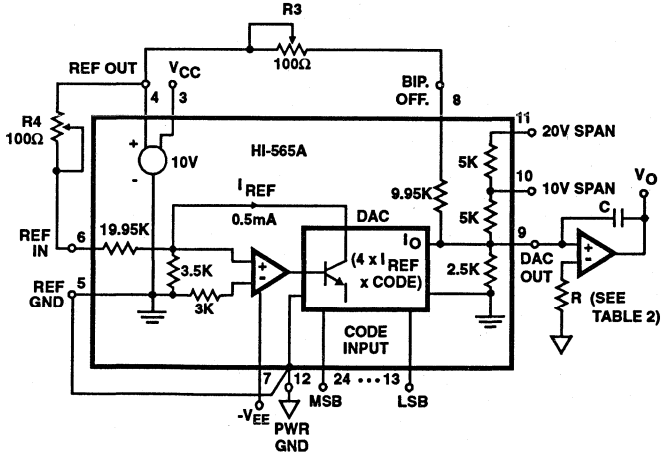


FIGURE 2. BIPOLAR VOLTAGE OUTPUT

Settling Time

This is a challenging measurement, in which the result depends on the method chosen, the precision and quality of test equipment and the operating configuration of the DAC (test conditions). As a result, the different techniques in use by converter manufacturers can lead to consistently different results. An engineer should understand the advantage and limitations of a given test method before using the specified settling time as a basis for design.

The approach used for several years at Harris Analog Products Division calls for a strobed comparator to sense final perturbations of the DAC output waveform. This gives the LSB a reasonable magnitude (814µV for the HI-565A), which provides the comparator with enough overdrive to establish an accurate ±0.5 LSB window about the final settled value. Also, the required test conditions simulate the DACs environment for a common application - use in a successive approximation A/D converter. Considerable experience has shown this to be a reliable and repeatable way to measure settling time.

The usual specification is based on a 10V step, produced by simultaneously switching all bits from off-to-on (t_{ON}) or on-to-off (t_{OFF}). The slower of the two cases is specified, as measured from 50% of the digital input transition to the final entry within a window of ±0.5 LSB about the settled value. Four measurements characterize a given type of DAC:

(a) t_{ON}, to final value +0.5 LSB

(b) t_{ON}, to final value –0.5 LSB

(c) t_{OFF}, to final value +0.5 LSB

(d) t_{OFF}, to final value –0.5 LSB

(Cases (b) and (c) may be eliminated unless the overshoot exceeds 0.5 LSB). For example, refer to Figure 3 for the measurement of case (d).

Procedure

As shown in Figure 3B, settling time equals t_X plus the comparator delay (t_D = 15ns). To measure t_X:

- Adjust the delay on generator No. 2 for a t_X of several microseconds. This assures that the DAC output has settled to its final value.
- Switch on the LSB (+5V).
- Adjust the V_{LSB} supply for 50% triggering at COMPARATOR OUT. This is indicated by traces of equal brightness on the oscilloscope display as shown in Figure 3B. Note DVM reading.
- Switch the LSB to Pulse (P).
- Readjust the V_{LSB} supply for 50% triggering as before, and note DVM reading. One LSB equals one tenth the difference in the DVM readings noted above.
- Adjust the V_{LSB} supply to reduce the DVM reading by 5 LSBs (DVM reads 10X, so this sets the comparator to sense the final settled value minus 0.5 LSB). Comparator output disappears.
- Reduce generator No. 2 delay until comparator output reappears, and adjust for "equal brightness".
- Measure t_X from scope as shown in Figure 3B. Settling time equals $t_X + t_D$, i.e. t_X + 15ns.

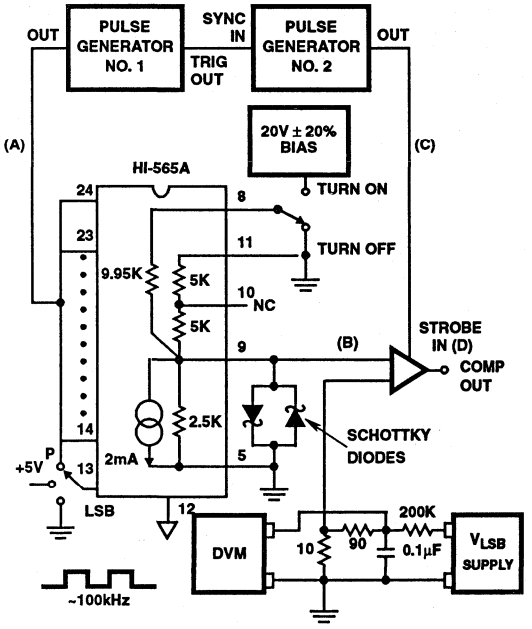


FIGURE 3A.

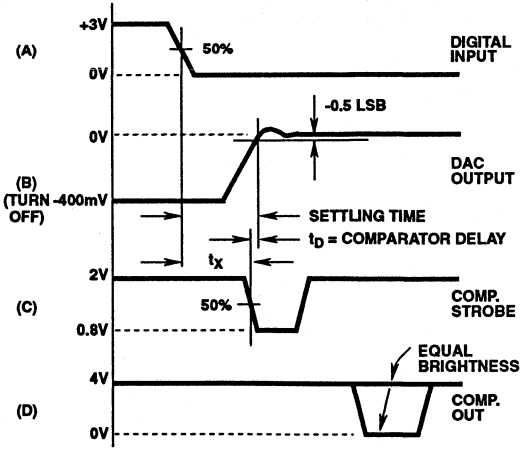


FIGURE 3B.

FIGURE 3.

Other Considerations

Grounds

The HI-565A has two ground terminals, pin 5 (REF GND) and pin 12 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 5 and 12).

The current through pin 5 is near-zero DC (Note 1); but pin 12 carries up to 1.75mA of code - ependent current from bits 1, 2, and 3. The general rule is to connect pin 5 directly to the system "quiet" point, usually called signal or analog ground. Connect pin 12 to the local digital or power ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

Layout

Connections to pin 9 (I_{OUT}) on the HI-565A are most critical for high speed performance. Output capacitance of the DAC is only 20pF, so a small change or additional capacitance may alter the op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should be short on the side connecting to pin 9 (as for feedback capacitor C). See the Settling Time section.

Bypass Capacitors

Power supply bypass capacitors on the op amp will serve the HI-565A also. If no op amp is used, a 0.01µF ceramic capacitor from each supply terminal to pin 12 is sufficient, since supply current variations are small.

Current Cancellation

Current cancellation is a two step process within the H1-565A in which code dependent variations are eliminated, then the resulting DC current is supplied internally. First an auxiliary 9 bit R-2R ladder is driven by the complement of the DACs input code. Together, the main and auxiliary ladders draw a continuous 2.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 5).

Die Characteristics

DIE DIMENSIONS:
179mils x 107mils x 19 mills ± 1mils

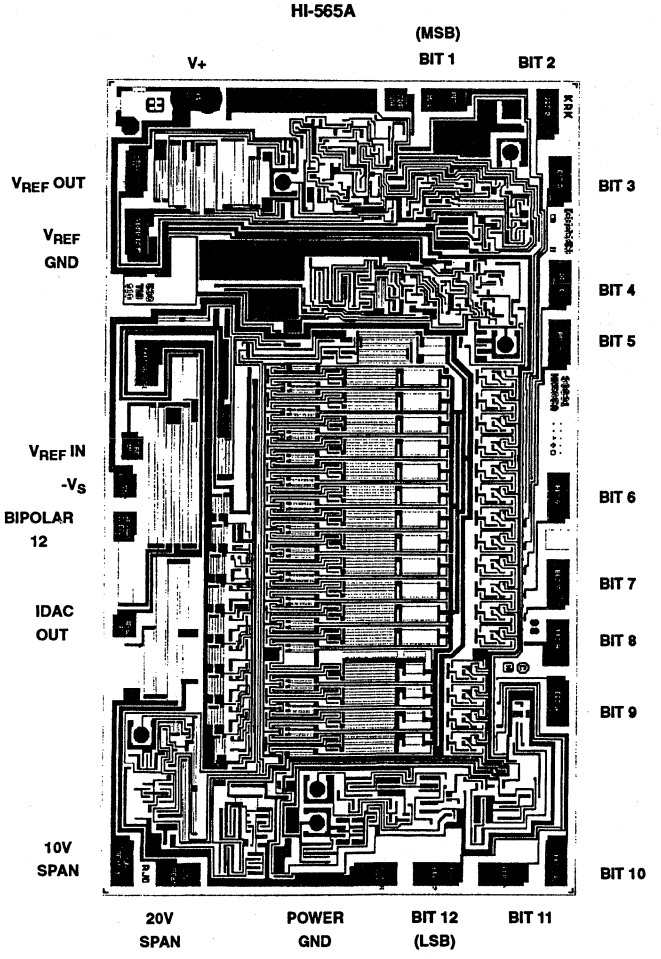
METALLIZATION:
Type: Al
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ± 0.5kÅ
Silox Thickness: 12kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:
0.75×10^5 A/cm^2

Transistor Count:
200

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HI-DAC80V
HI-DAC85V

December 1993

12-Bit, Low Cost, Monolithic D/A Converter

Features

- DAC 80V/DAC 85V Alternative Source
- Monolithic Construction
- Fast Settling Time 1.5µs (typ.)
- Guaranteed Monotonicity
- Wafer Laser Trimmed Linearity, Gain, Offset
- Span Resistors On-Chip
- On-Board Reference
- ±12V Supply Operation

Applications

- High Speed A/D Converters
- Precision Instrumentation
- CRT Display Generation

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-DAC80V-5	0°C to +75°C	24 Lead Plastic DIP
HI3-DAC80V-7	0°C to +75°C	24 Lead Plastic DIP
HI3-DAC85V-4	-25°C to +85°C	24 Lead Plastic DIP
HI3-DAC85V-9	-40°C to +85°C	24 Lead Plastic DIP

Description

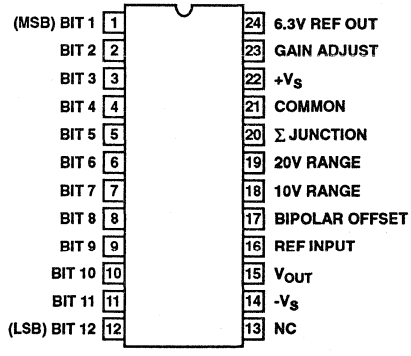
The HI-DAC80V is a monolithic direct replacement for the popular DAC80 and AD DAC80. The HI-DAC85V is a monolithic direct replacement for the popular DAC85 and AD DAC85 as well as the HI-5685V. Single chip construction along with several design innovations make the HI-DAC80V the optimum choice for low cost, high reliability applications. Harris' unique Dielectric Isolation (DI) processing reduces internal parasitics resulting in fast switching times and minimum glitch. On board span resistors are provided for good tracking over temperature, and are laser trimmed to high accuracy.

Internally the HI-DAC80V/HI-DAC85V eliminates code dependent ground currents by routing current from the positive supply to the internal ground node, as determined by an auxiliary R2R ladder. This results in a cancellation of code dependent ground currents allowing virtually zero variation in current through the package common, pin 21.

The HI-DAC80V is available as a voltage output device which is guaranteed over the 0°C to +75°C temperature range. An extended burn in screening of 96 hours is available in the HI-DAC80V-7 model. The HI-DAC85V is available as a voltage output device which is guaranteed over the -25°C to +85°C temperature range. It includes a buried zener reference featuring a low temperature coefficient as well as an on board operational amplifier. The HI-DAC80V requires only two power supplies and will operate in the range of ± (11.4V to 16.5V).

Pinout

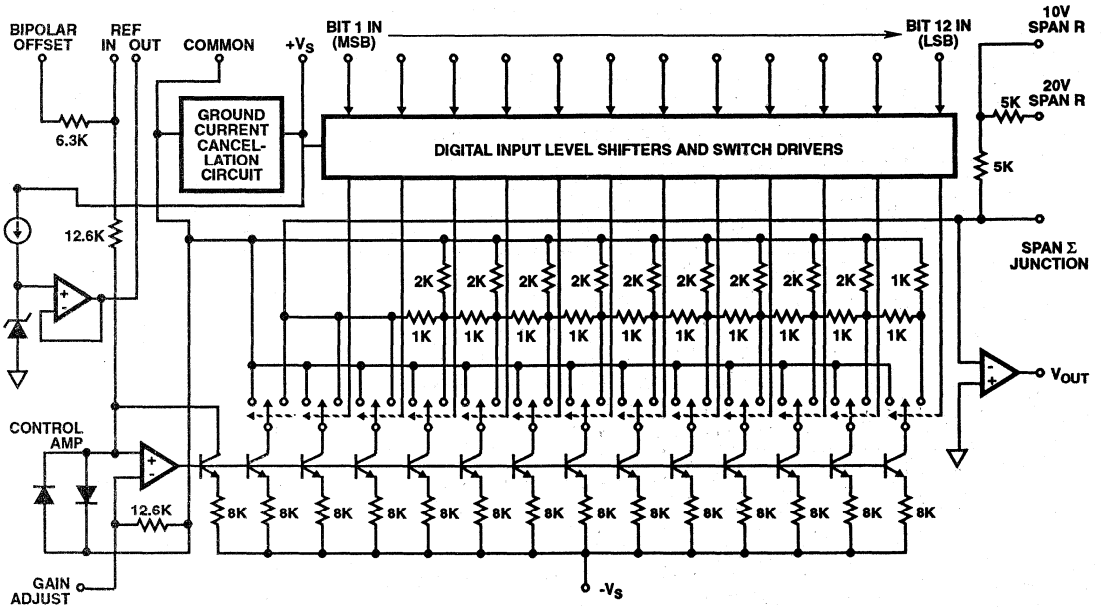
HI-DAC80V/HI-DAC85V
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3110

Functional Block Diagram



Absolute Maximum Ratings

Power Supply Inputs
- $+V_S$ ..... +20V
- $-V_S$ ..... -20V

Reference
- Input (Pin 16) ..... $+V_S$
- Output Drain 2.5mA

Digital Inputs (Bits 1 to 12) ..... -1V to $+V_S$
Process ..... Bipolar-DI
Transistor Count 214
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance θ_{JA}
- Plastic DIP Package ..... 75°C/W

Maximum Power Dissipation
- Plastic DIP Package 550mW

Operating Temperature Range
- HI-DAC80V ..... 0°C to +75°C
- HI-DAV85V ..... -40°C to +85°C

Max Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V_S ±12V to ±15V (Note 4), Pin 16 to Pin 24, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	HI-DAC80V-5, HI-DAC85V-5			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution		-	-	12	Bits
ACCURACY (Note 2)					
Linear Error	Full Temperature	-	±1/4	±1/2	LSB
Differential Linearity Error	Full Temperature	-	±1/2	±3/4	LSB
Monotonicity	Full Temperature		Guaranteed		
Gain Error	Full Temperature (Notes 1, 3)	-	±0.1	±0.3	% FSR
Offset Error	Full Temperature (Note 1)		±0.05	±0.15	% FSR
ANALOG OUTPUT					
Output Ranges		-	±2.5	-	V
		-	±5	-	V
		-	±10	-	V
		-	0 to 5	-	V
		-	0 to 10	-	V
Output Current		±5	-	-	mA
Output Resistance		-	0.05	-	Ω
Short Circuit Duration	To Common		Continuous		-
DRIFT (Note 2)					
Total Bipolar Drift (Includes Gain, Offset and Linearity Drifts)	Full Temperature	-	-	±20	ppm/°C
Total Error					
Unipolar	Full Temperature (Note 5)	-	±0.08	±0.15	% FSR
Bipolar	Full Temperature (Note 5)	-	±0.06	±0.1	% FSR
Gain	With Internal Reference	-	±15	±30	ppm/°C
	Without Internal Reference	-	±7	-	ppm/°C
Unipolar Offset		-	±1	±3	ppm/°C
Bipolar Offset			±5	±10	ppm/°C

Electrical Specifications T_A = +25°C, V_S ±12V to ±15V (Note 4), Pin 16 to Pin 24, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	HI-DAC80V-5, HI-DAC85V-5 MIN	TYP	MAX	UNITS
CONVERSION SPEED					
Settling Time	Full Scale Transition All Bits ON to OFF or OFF to ON to ±0.01% or FSR (Note 2)				
With 10K Feedback		-	3	-	µs
With 5K Feedback		-	1.5	-	µs
For 1 LSB Change		-	1.5	-	µs
Slew Rate		10	15	-	V/µs
INTERNAL REFERENCE					
Output Voltage		6.250	+6.3	6.350	V
Output Impedance		-	1.5	-	Ω
External Current		-	-	+2.5	mA
Tempco of Drift		-	5	-	ppm/°C
DIGITAL INPUT (Note 2)					
Logic Levels					
Logic "1"	TTL Compatible At +1µA	+2	-	+5.5	V
Logic "0"	TTL Compatible At -100µA	0	-	+0.8	V
POWER SUPPLY SENSITIVITY (Notes 2, 4)					
+15V Supply		-	0.001	0.002	% FSR / % V_S
-15V Supply		-	0.001	0.002	% FSR / % V_S
POWER SUPPLY CHARACTERISTICS (Note 4)					
Voltage Range					
$+V_S$	Full Temperature	+11.4	+15	+16.5	V
$-V_S$	Full Temperature	-11.4	-15	-16.5	V
Current					
$+I_S$	Full Temperature, V_S = ±15V	-	+12	+15	mA
$-I_S$	Full Temperature, V_S = ±15V	-	-15	-20	mA

NOTES:

1. Adjustable to zero using external potentiometers.
2. See Definitions.
3. FSR is "Full Scale Range: and is 20V for ±10V range, 10V for ±5V range, etc.
4. The HI-DAC80V/HI-DAC85V will operate with supply voltages as low as ±11.4V.It is recommended that output voltage range -10V to +10V not be used if the supply voltages are less than ±12.5V.
5. With Gain and Offset errors adjusted to zero at +25°C

Definitions of Specifications

Digital Inputs

The HI-DAC80V accepts digital input codes in complementary binary, complementary offset binary, and complementary two's complement binary.

Settling Time

That interval between application of a digital step input, and final entry of the analog output within a specified window about the settled value. Harris Semiconductor usually specifies a unipolar 10V full scale step, to be measured from 50% of the input digital transition, and a window of $\pm^1/_2$ LSB about

TABLE 1.

DIGITAL INPUT	ANALOG OUTPUT COMPLEMENTARY STRAIGHT BINARY	COMPLEMENTARY OFFSET BINARY	COMPLEMENTARY TWO'S COMPLEMENT†
MSB...LSB			
000...000	+ Full Scale	+ Full Scale	-LSB
100...000	Mid Scale-1 LSB	-1 LSB	+ Full Scale
111...111	Zero	- Full Scale	Zero
011...111	$+^1/_2$ Full Scale	Zero	- Full Scale

†Invert MSB with external inverter to obtain CTC Coding

the final value. The device output is then rated according to the worst (longest settling) case: low to high, or high to low. In a 12-bit system $\pm^1/_2$ LSB = ±0.012% of FSR.

Thermal Drift

Thermal drift is based on measurements at +25°C, at high (T_H) and low (T_L) temperatures. Drift calculations are made for the high (T_H -25°C) and low (+25°C-T_L) ranges, and the larger of the two values is given as a specification representing worst case drift.

Gain Drift, Offset Drift, Reference Drift and Total Bipolar Drift are calculated in parts per million per °C as follows:

$$\text{Gain Drift} = \frac{\Delta FSR/\Delta°C}{FSR} \times 10^6$$

$$\text{Offset Drift} = \frac{\Delta Offset/\Delta°C}{FSR} \times 10^6$$

$$\text{Reference Drift} = \frac{\Delta V_{REF}/(\Delta°C)}{V_{REF}} \times 10^6$$

$$\text{Total Bipolar Drift} = \frac{\Delta V_O/(\Delta°C)}{FSR} \times 10^6$$

NOTE: FSR = Full Scale Output Voltage - Zero Scale Output Voltage

ΔFSR = FSR (T_H) - FSR (+25°C)
or FSR (+25°C) - FSR (T_L)
V_O = Steady State response to any input code.

Total Bipolar Drift is the variation of output voltage with temperature, in the bipolar mode of operation. It represents the net effect of drift in Gain, Offset, Linearity and Reference Voltage. Total Bipolar Drift values are calculated, based on measurements as explained above. Gain and Offset need not be calibrated to zero at +25°C. The specified limits for TBD apply for any input code and for any power supply setting within the specified operating range.

Accuracy

Linearity Error (Short for "Integral Linearity Error." Also, sometimes called "Integral Nonlinearity" and "Nonlinearity".) The maximum deviation of the actual transfer characteristic from an ideal straight line. The ideal line is positioned according to end-point linearity for D/A converter products from Harris Semiconductor, i.e. the line is drawn between the end-points of the actual transfer characteristic (codes 00...0 and 11...1).

Differential Linearity Error The difference between one LSB and the output voltage change corresponding to any two consecutive codes. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity.

Monotonicity The property of a D/A converter's transfer function which guarantees that the output derivative will not change sign in response to a sequence of increasing (or decreasing) input codes. That is, the only output response to a code change is to remain constant, increase for Increasing code, or decrease for decreasing code.

Total Error The net output error resulting from all internal effects (primarily non-ideal Gain, Offset, Linearity and Reference Voltage). Supply voltages may be set to any values within the specified operating range. Gain and offset errors must be calibrated to zero at +25°C. Then the specified limits for Total Error apply for any input code and for any temperature within the specified operating range.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -V_S, or +V_S supplies. It is specified under DC conditions and expressed as full scale range percent of change divided by power supply percent change.

$$PSS = \frac{\dfrac{\Delta \text{Full Scale Range} \times 100}{FSR\,(\text{Nominal})}}{\dfrac{\Delta V_S \times 100}{V_S(\text{Nominal})}}$$

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale i.e. the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably. (Measured as one half the Product of duration and amplitude.)

Decoupling and Grounding

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-DAC80V/HI-DAC85V (preferably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

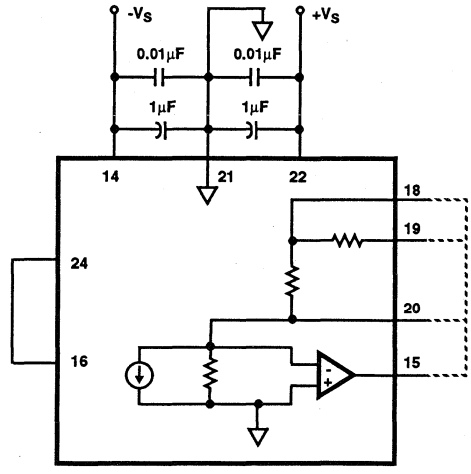


FIGURE 1.

Reference Supply

An internal 6.3 volt reference is provided on board the HI-DAC80V/HI-DAC85V. The voltage (pin 24) is accurate to ±0.8% and must be connected to the reference input (pin 16) for specified operation. This reference may be used externally, provided current drain is limited to 2.5mA. An external buffer amplifier is recommended if this reference is to be used to drive other system components. Otherwise, variations in the load driven by the reference will result in gain variations of the HI-DAC80V/HI-DAC85V. All gain adjustments should be made under constant load conditions.

Output Voltage Ranges

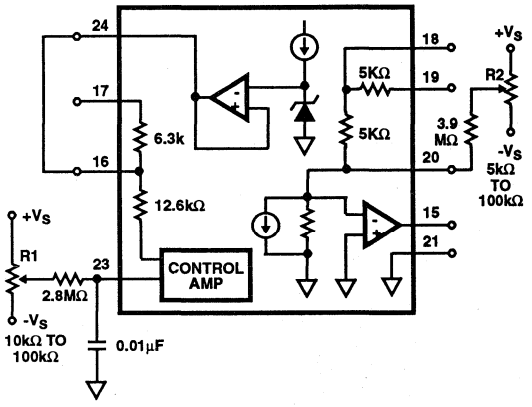


FIGURE 2. HI-DAC80V/HI-DAC85V

TABLE 2. RANGE CONNECTIONS

		CONNECT		
	RANGE	PIN 15	PIN 17	PIN 19
Unipolar	0 to +5V	18	NC	20
	0 to +10V	18	NC	NC
Bipolar	±2.5V	18	20	20
	±5V	18	20	NC
	±10V	19	20	15

TABLE 3. GAIN AND OFFSET CALIBRATIONS

UNIPOLAR CALIBRATION	
Step 1:	Offset Turn all bits OFF (11 . . . 1) Adjust R2 for 0V out
Step 2:	Gain Turn all bits ON (00 . . . 0) Adjust R1 for FS - 1 LSB That is: 4.9988 for 0 to +5V range 9.9976 for 0 to +10V range
BIPOLAR CALIBRATION	
Step 1:	Offset Turn all bits OFF (11 . . . 1) Adjust R2 for Negative FS That is: -10V for ±10V range -5V for ±5V range -2.5V for ±2.5V range
Step 2:	Gain Turn all bits ON (00 . . . 0) Adjust R1 for positive FS - 1 LSB That is: +9.9951V for ±10V range +4.9976V for ±5V range +2.4988V for ±2.5V range
This Bipolar procedure adjusts the output range end points. The maximum error at zero (half scale) will not exceed the Linearity error. See the "Accuracy" Specifications.	

Die Characteristics

DIE DIMENSIONS:
108 x 163 mils

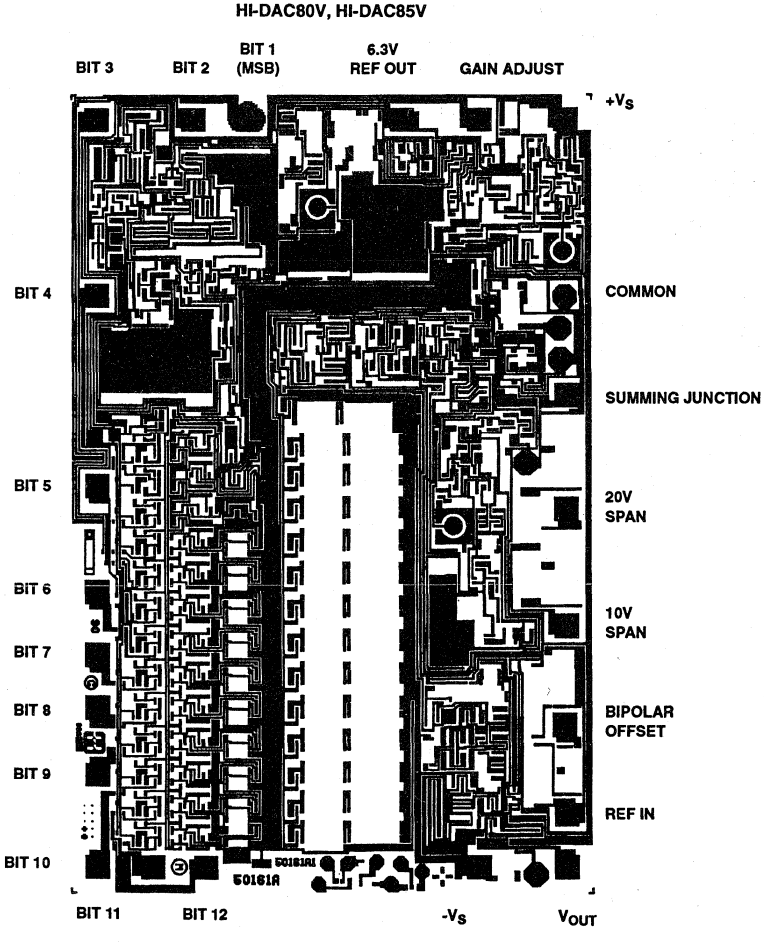
METALLIZATION:
Type: AL
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Nitride Thickness: 3.5kÅ ± 0.5kÅ
Silox Thickness: 12kÅ ± 1.5kÅ

WORST CASE CURRENT DENSITY:
0.95 x 10^5A/cm^2

TIE SUBSTRATE TO:
Ground

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HI1171

December 1993

8-Bit, 40MSPS High Speed D/A Converter

Features

- 40MSPS Throughput Rate
- 8-Bit Resolution
- 0.25 LSB Integral Linearity Error
- Low Glitch Noise
- Single +5V Supply Operation
- Low Power Consumption 80mW (Max)

Applications

- Wireless Telecommunications
- NTSC, PAL, or SECAM
- Signal Reconstruction
- Direct Digital Synthesis
- Imaging
- Presentation and Broadcast Video
- Graphics Displays
- Signal Generators

Description

The HI1171 is an 8-bit 40MHz high speed D/A converter. The converter incorporates an 8 bit input data register with blanking capability, and current outputs. The HI1171 features low glitch outputs. The architecture is a current cell arrangement to provide low linearity errors.

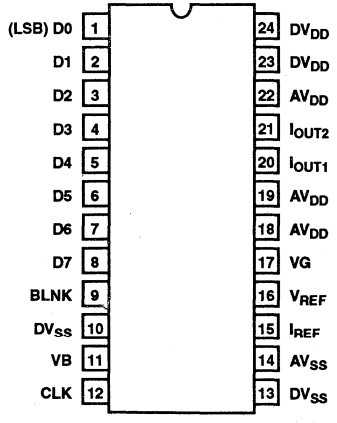
The HI1171 is available in a Commercial temperature range and is offered in a 24 lead (200 mil) SOIC plastic package.

Ordering Information

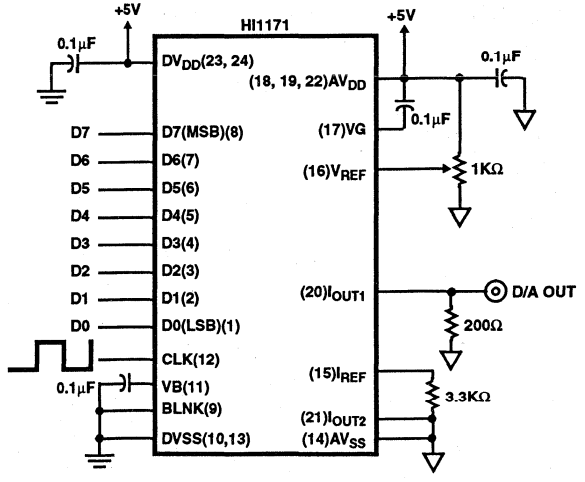
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1171JCB	-20°C to 75°C	24 Lead SOIC (200 mil)

Pinout

HI1171
(SOIC)
TOP VIEW



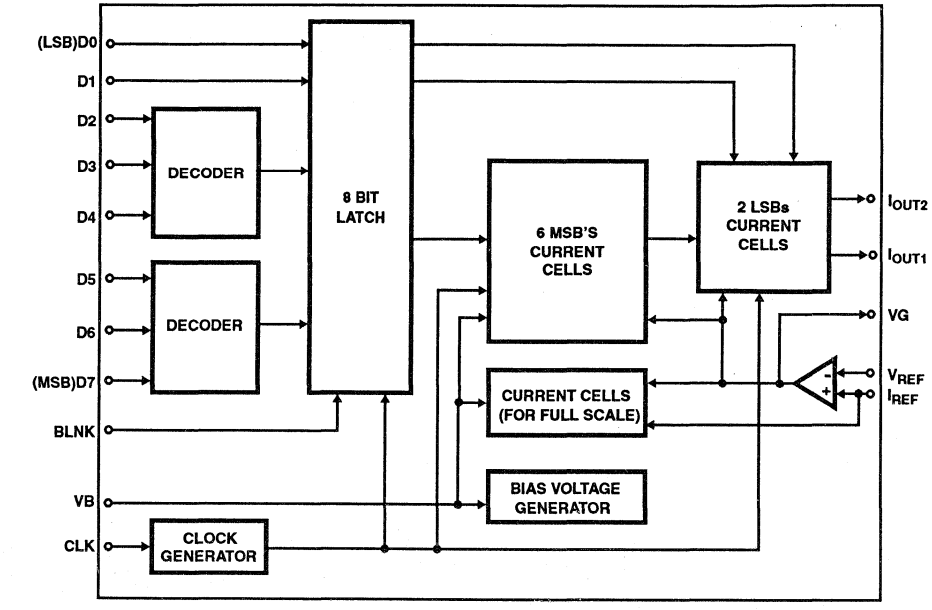
Typical Applications Circuit



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3580.1

Functional Block Diagram



Absolute Maximum Ratings

Digital Supply Voltage DV_{DD} to DV_{SS} ..... +7.0V
Analog Supply Voltage AV_{DD} to AV_{SS} ..... +7.0V
Input Voltage..... V_{DD} to V_{SS} V
Output Current .....0mA to 15mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s)..... +300°C

Thermal Information

Thermal Resistance (Typ, Note 1) θ_{JA}
SOIC Package..... 98°C/W
Maximum Power Dissipation
HI1171JCB 160mW
Operating Temperature Range ..... -20°C to +75°C
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{DD} = +4.75 to +5.25V, DV_{DD} = +4.75 to +5.25V, V_{REF} = +2.0V, f_S = 40MHz, CLK Pulse Width = 12.5ns, T_A = +25°C (Note 4).

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
SYSTEM PERFORMANCE					
Resolution		8	-	-	Bits
Integral Linearity Error, INL	f_S = 40MHz (End Point)	-0.5	-	1.3	LSB
Differential Linearity Error, DNL	f_S = 40MHz	-	-	±0.25	LSB
Offset Error, V_{OS}	(Note 2)	-	-	0.125	LSB
Full Scale Error, FSE (Adjustable to Zero)	(Note 2)	-	-	±13	LSB
Full Scale Output Current, I_{FS}		-	10	15	mA
Full Scale Output Voltage, V_{FS}		1.9	2.0	2.1	V
Output Voltage Range, V_{FSR}		0.5	2.0	2.1	V
DYNAMIC CHARACTERISTICS					
Throughput Rate	See Figure 7	40.0	-	-	MSPS
Glitch Energy, GE	R_{OUT} = 75Ω	-	30	-	pV-s
Differential Gain, ΔA_V (Note 3)		-	1.2	-	%
Differential Phase, $\Delta\phi$ (Note 3)		-	0.5	-	Degree
REFERENCE INPUT					
Voltage Reference Input Range		0.5	-	2.0	V
Reference Input Resistance	(Note 3)	1.0	-	-	MΩ
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}	(Note 3)	3.0	-	-	V
Input Logic Low Voltage, V_{IL}	(Note 3)	-	-	1.5	V
Input Logic Current, I_{IL}, I_{IH}	(Note 3)	-	-	±5.0	µA
Digital Input Capacitance, C_{IN}	(Note 3)	-	5.0	-	pF
TIMING CHARACTERISTICS					
Data Setup Time, t_{SU}	See Figure 1	5	-	-	ns
Data Hold Time, t_{HLD}	See Figure 1	10	-	-	ns
Propagation Delay Time, t_{PD}	See Figure 9	-	10	-	ns
Settling Time, t_{SET} (to 1/2 LSB)	See Figure 1	-	10	15	ns
CLK Pulse Width, T_{PW1}, T_{PW2}	See Figure 1	12.5	-	-	ns

Electrical Specifications AV_{DD} = +4.75 to +5.25V, DV_{DD} = +4.75 to +5.25V, V_{REF} = +2.0V, f_S = 40MHz, CLK Pulse Width = 12.5ns, T_A = +25°C (Note 4). **(Continued)**

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNITS
POWER SUPPLY CHARACTERISITICS					
IAV_{DD}	14.3MHz, at Color Bar Data Input	-	10.9	11.5	mA
IDV_{DD}	14.3MHz, at Color Bar Data Input	-	4.2	4.8	mA
Power Dissipation	200Ω load at $2V_{P-P}$ Output	-	-	80	mW

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board
2. Excludes error due to external reference drift.
3. Parameter guaranteed by design or characterization and not production tested.
4. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagram

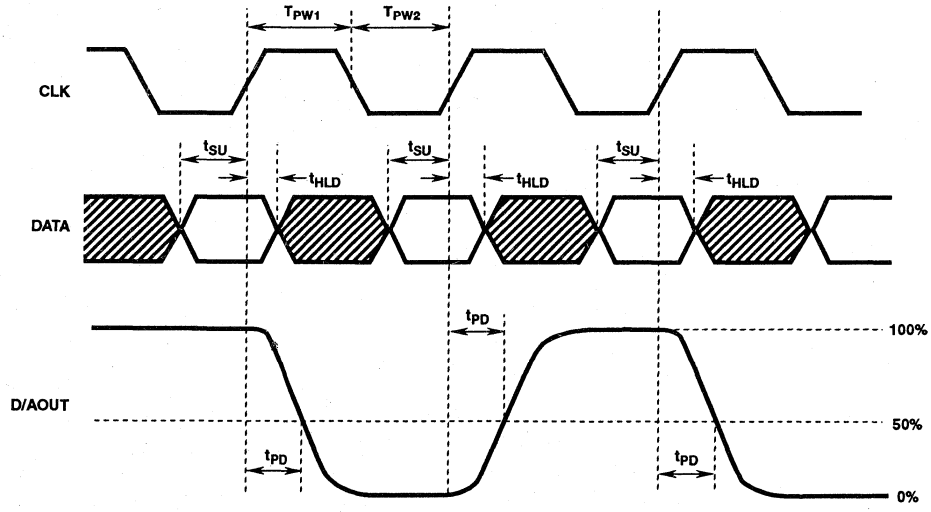


FIGURE 1.

Typical Performance Curves

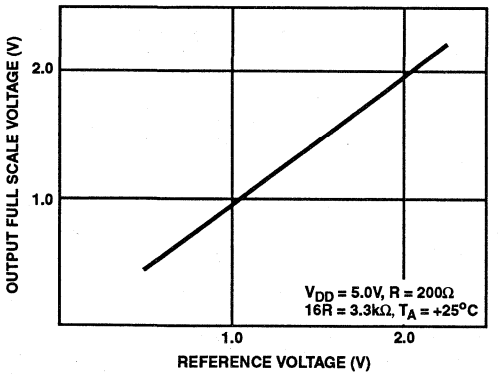


FIGURE 4. OUTPUT FULL SCALE VOLTAGE vs REFERENCE VOLTAGE

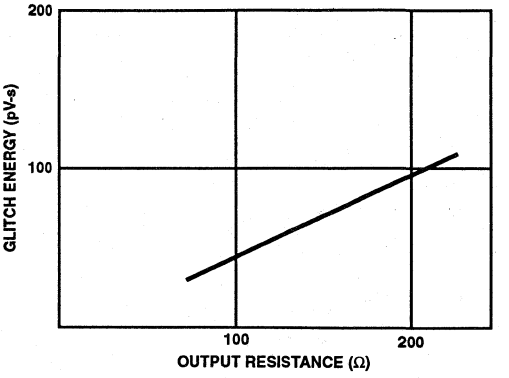


FIGURE 5. OUTPUT RESISTANCE vs GLITCH ENERGY

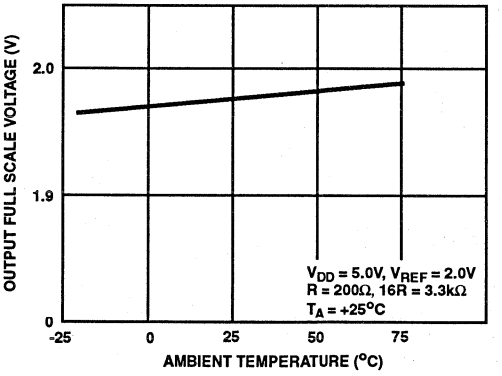


FIGURE 6. OUTPUT FULL SCALE VOLTAGE vs AMBIENT TEMPERATURE

Pin Description

24 PIN SOIC	PIN NAME	PIN DESCRIPTION
1-8	D0(LSB) thru D7(MSB)	Digital Data Bit 0, the Least Significant Bit thru Digital Data Bit 7, the Most Significant Bit
9	BLNK	Blanking Line, used to clear the internal data register to the zero condition when High, normal operation when Low.
10, 13	DV_{SS}	Digital Ground
11	VB	Voltage Bias, connect a 0.1µF capacitor to DV_{SS}
12	CLK	Data Clock Pin 100kHz to 40MHz
14	AV_{SS}	Analog Ground
15	I_{REF}	Current Reference, used to set the current range. Connect a resistor to AV_{SS} that is 16 times greater than the resistor on I_{OUT1}. (See Typical Applications Circuit)
16	V_{REF}	Input Reference Voltage used to set the output full scale range.
17	VG	Voltage Ground, connect a 0.1µF capacitor to AV_{DD}.
18, 19, 22	AV_{DD}	Analog Supply 4.75V to 7V
20	I_{OUT1}	Current Output Pin.
21	I_{OUT2}	Current Output pin used for a virtual ground connection. Usually connected to AV_{SS}
23, 24	DV_{DD}	Digital Supply 4.75V to 7V

Detailed Description

The HI1171 is an 8 bit, current out D/A converter. The DAC can convert at 40MSPS and run on a single +5V supply. The architecture is an encoded, switched current cell arrangement.

Voltage Output Mode

The output current of the HI1171 can be converted into a voltage by connecting an external resistor to I_{OUT1}. To calculate the output resistor use the following equation:

$$R_{OUT} = V_{FS} / I_{FS}$$

where V_{FS} can range from +0.5V to +2.0V and I_{FS} can range from 0mA to 15mA

In setting the output current the I_{REF} pin should have a resistor connected to it that is 16 times greater than the output resistor.

$$R_{REF} = 16 \times R_{OUT}$$

As the values of both R_{OUT} and R_{REF} increase, power consumption is decreased, but glitch energy and output settling time is increased.

Clock Phase Relationship

The internal latch is closed when the clock line is high. The latch can be cleared by the BLNK line. When BLNK is set (HIGH) the contents of the internal data latch will be cleared. When BLNK is low data is updated by the CLK.

Noise Reduction

To reduce power supply noise separate analog and digital power supplies should be used with 0.1µF ceramic capacitors placed as close to the body of the HI1171 as possible. The analog (AV_{SS}) and digital (DV_{SS}) ground returns should be connected together back at the power supply to ensure proper operation from power up.

Test Circuits

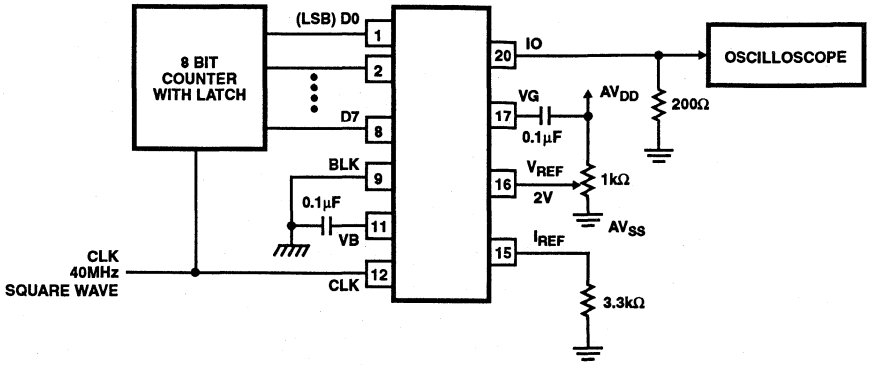


FIGURE 7. MAXIMUM CONVERSION SPEED TEST CIRCUIT

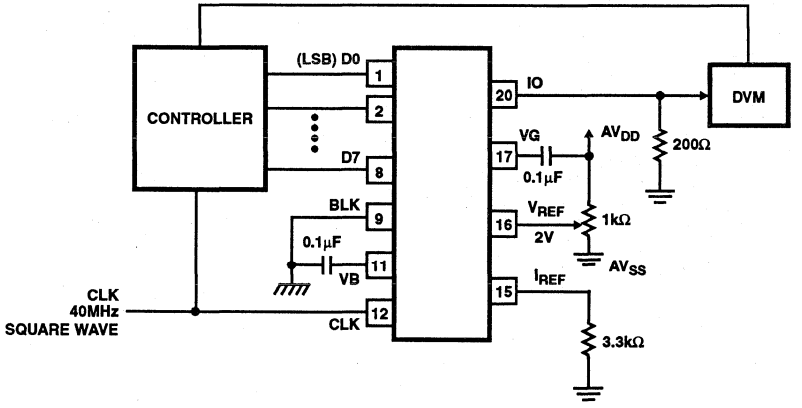


FIGURE 8. DC CHARACTERISTICS TEST CIRCUIT

Test Circuits (Continued)

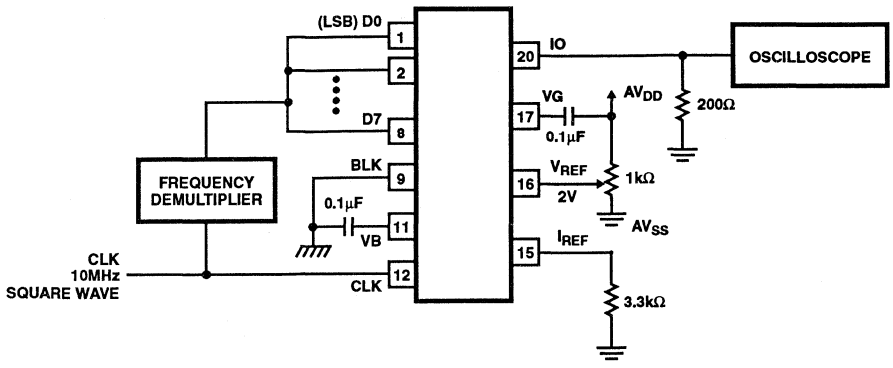


FIGURE 9. PROPAGATION DELAY TIME TEST CIRCUIT

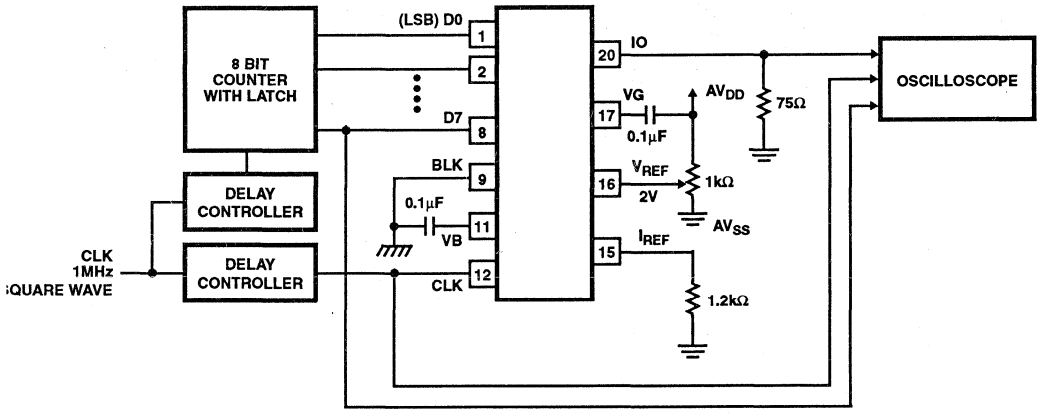


FIGURE 10. SET UP HOLD TIME AND GLITCH ENERGY TEST CIRCUIT

HI20201, HI20203

10/8-Bit, 160MSPS Ultra High Speed D/A Converter

December 1993

Features

- 160MSPS Throughput Rate
- 10 (HI20201) & 8 (HI20203) Bit Resolution
- 0.5 LSB Differential Linearity Error
- Low Glitch Noise
- Analog Multiplying Function
- Low Power Consumption 420mW
- Evaluation Board Available

Applications

- Wireless Communications
- Signal Reconstruction
- Direct Digital Synthesis
- High Definition Video Systems
- Digital Measurement Systems
- Radar

Description

The HI20201/03 is a 160MHz ultra high speed D/A converter. The converter is based on an R2R switched current source architecture that includes an input data register with a complement feature and is Emitter Coupled Logic (ECL) compatible.

The HI20201 is a 10 bit accurate D/A with a linearity error of 1 LSB. The HI20203 is an 8 bit accurate D/A with a linearity error of 0.5 LSB.

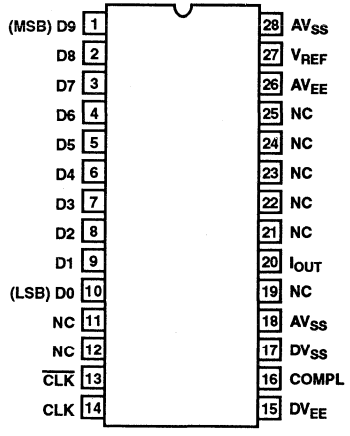
The HI20201/03 are available in a commercial temperature range and are offered in a 28 lead plastic SOIC (300 mil) and a 28 lead plastic DIP package.

Ordering Information

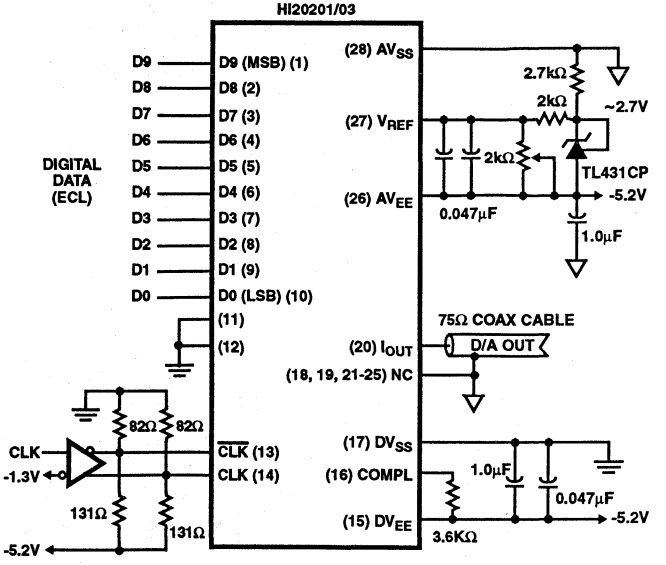
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI20201JCB	-20°C to +75°C	28 Lead SOIC (300 mil)
HI20203JCB	-20°C to +75°C	28 Lead SOIC (300 mil)
HI20201JCP	-20°C to +75°C	28 Lead Plastic DIP
HI20203JCP	-20°C to +75°C	28 Lead Plastic DIP

Pinout

HI20201, HI20203
(PDIP, SOIC)
TOP VIEW



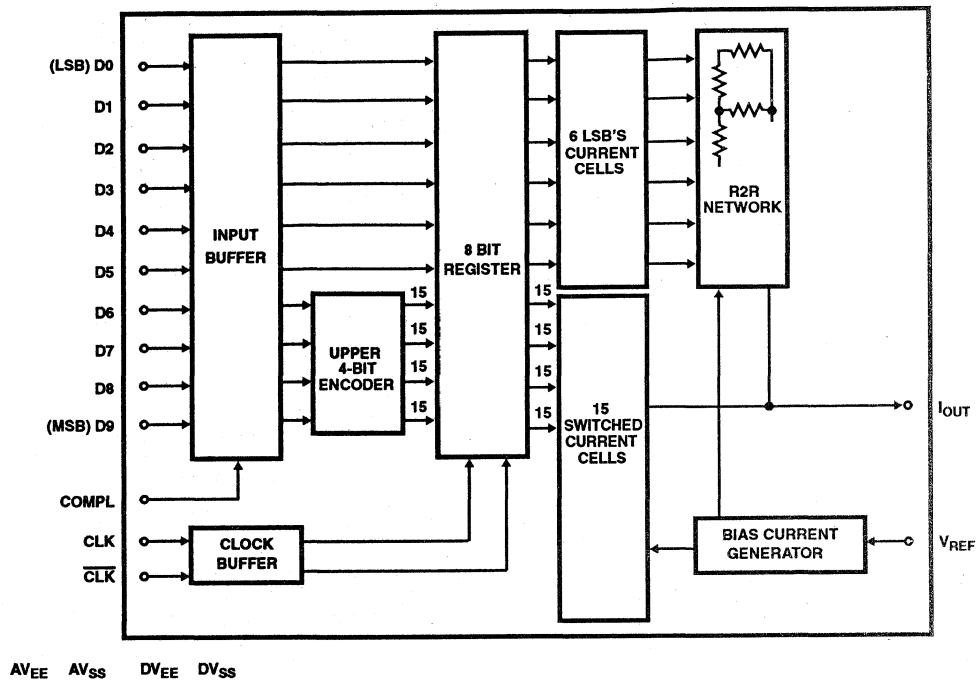
Typical Applications Circuit



8 D/A CONVERTERS

File Number 3581.1

Functional Block Diagram



Absolute Maximum Ratings

Digital Supply Voltage DV_{EE} to DV_{SS} ..... -7.0V
Analog Supply Voltage AV_{DD} to AV_{SS} ..... -7.0V
Digital Input Voltage ..... +0.3 to DV_{EE} V
Reference Input Voltage ..... +0.3 to AV_{EE} V
Output Current 20mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance (Typ, See Note 1) θ_{JA}
SOIC Package ..... 70°C/W
Plastic DIP Package ..... 60°C/W
Maximum Power Dissipation
HI20201JCB 575mW
HI20203JCB 575mW
Operating Temperature Range ..... -20°C to +75°C
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

AV_{EE} = -4.75 to -5.25V, DV_{EE} = -4.75 to -5.25V, V_{REF} = AV_{EE} +0.5 to AV_{EE} +1.5V, f_S = 160MHz, Logic Levels V_{IH} = -1.0 to -0.7V, V_{IL} = -1.9 to -1.6V R_{LOAD} = ∞, V_{OUT} = -1V, T_A = +25°C (Note 4).

PARAMETER	TEST CONDITION	HI20201JCB/JCP			HI20203JCB/JCP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SYSTEM PERFORMANCE								
Resolution		10	-	-	8	-	-	Bits
Integral Linearity Error, INL	f_S = 160MHz (End Point)	-	-	±1.0	-	-	±0.5	LSB
Differential Linearity Error, DNL	f_S = 160MHz	-	-	±0.50	-	-	±0.50	LSB
Offset Error, V_{OS} (Adjustable to Zero)	(Note 3)	-	7	-	-	1.8	-	LSB
Full Scale Error, FSE (Adjustable to Zero)	(Note 3)	-	-	±102	-	-	±26	LSB
Full Scale Output Current, I_{FS}		-	-	20	-	-	20	mA
DYNAMIC CHARACTERISTICS								
Throughput Rate	See Figure 11	160	-	-	160	-	-	MSPS
Glitch Energy, GE	R_{OUT} = 75Ω	-	15	-	-	15	-	pV-s
REFERENCE INPUT								
Voltage Reference Input Range	With respect to AV_{EE}	+0.5	-	+1.4	+0.5	-	+1.4	V
Reference Input Current	V_{REF} = -4.58V	-0.1	-0.4	-3.0	-0.1	-0.4	-3.0	µA
Voltage Reference to Output Small Signal Bandwidth	-3dB point 1V p-p Input	-	14.0	-	-	14.0	-	MHz
Output Rise Time, t_R	R_{LOAD} = 75Ω	-	1.5	-	-	1.5	-	ns
Output Fall Time, t_F	R_{LOAD} = 75Ω	-	1.5	-	-	1.5	-	ns
DIGITAL INPUTS								
Input Logic High Voltage, V_{IH}	(Note 2)	-1.0	-0.89		-1.0	-0.89		V
Input Logic Low Voltage, V_{IL}	(Note 2)		-1.75	-1.6		-1.75	-1.6	V
Input Logic Current, I_{IL} I_{IH} (For D9 thru D6, COMPL)	(Note 2) V_{IH} = -0.89V V_{IL} = -1.75V	0.1	1.5	6.0	0.1	1.5	6.0	µA
Input Logic Current, I_{IL} I_{IH} (For D5 thru D0)	(Note 2) V_{IH} = -0.89V V_{IL} = -1.75V	0.1	0.75	3.0	0.1	0.75	3.0	µA

Electrical Specifications AV_{EE} = -4.75 to -5.25V, DV_{EE} = -4.75 to -5.25V, V_{REF} = AV_{EE} +0.5 to AV_{EE} +1.5V, f_S = 160MHz, Logic Levels V_{IH} = -1.0 to -0.7V, V_{IL} = -1.9 to -1.6V R_{LOAD} = ∞, V_{OUT} = -1V, T_A = +25°C (Note 4).**(Continued)**

PARAMETER	TEST CONDITION	HI20201JCB/JCP			HI20203JCB/JCP			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
TIMING CHARACTERISTICS								
Data Setup Time, t_{SU}	See Figure 11	5	-	-	5	-	-	ns
Data Hold Time, t_{HLD}	See Figure 11	1	-	-	1	-	-	ns
Propagation Delay Time, t_{PD}	See Figure 11	-	3.8	-	-	3.8	-	ns
Settling Time, t_{SET} (to 1/2 LSB)	See Figure 11	-	5.2	-	-	4.3	-	ns
POWER SUPPLY CHARACTERISITICS								
I_{EE}		-60	-75	-90	-60	-75	-90	mA
Power Dissipation	75Ω load	-	420	470	-	420	470	mW

NOTES:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board
2. Parameter guaranteed by design or characterization and not production tested.
3. Excludes error due to reference drift.
4. Electrical specifications guaranteed only under the stated operating conditions.

Timing Diagram

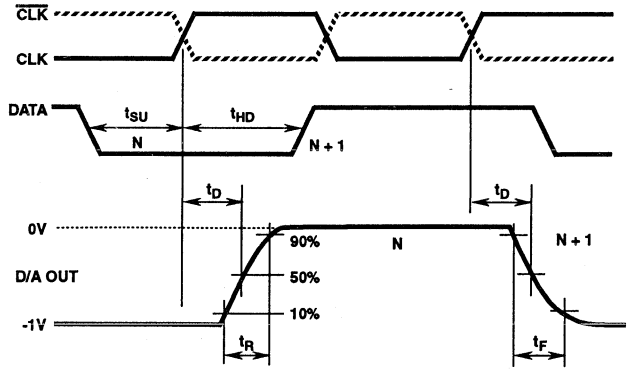


FIGURE 1. LADDER SETTLING TIME FULL POWER BANDWIDTH (LS)

Typical Performance Curves

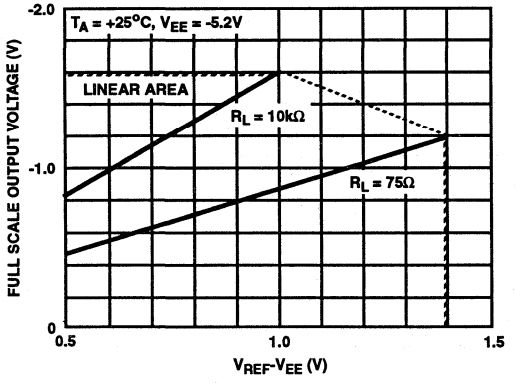


FIGURE 2. $V_{O(FS)}$ RATIO vs (V_{REF}-V_{EE})

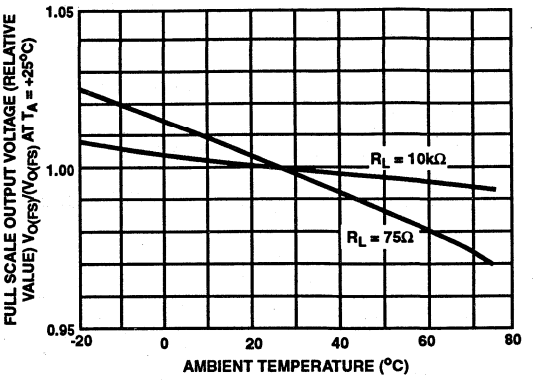


FIGURE 3. FULL SCALE OUTPUT VOLTAGE vs AMBIENT TEMPERATURE

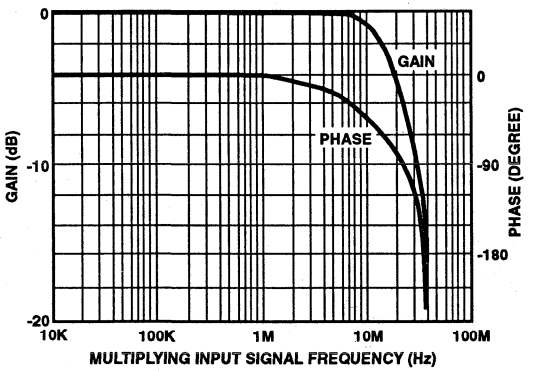


FIGURE 4. OUTPUT CHARACTERISTICS vs MULTIPLYING INPUT SIGNAL FREQUENCY

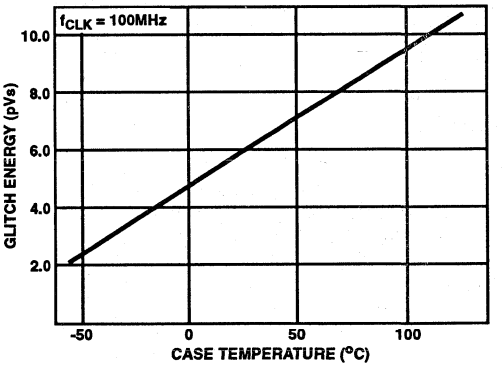


FIGURE 5. GLITCH ENERGY vs CASE TEMPERATURE (FULL SCALE - 1023mV)

Pin Description

28 PIN SOIC	PIN NAME	PIN DESCRIPTION
1-10	D0 (LSB)-D9 (MSB)	Digital Data Bit 0, the Least Significant Bit thru Digital Data Bit 9, the Most Significant Bit.
11, 12, 19, 21- 25	NC	No connect, not used.
13	$\overline{CLK}$	Negative differential Clock input.
14	CLK	Positive differential Clock input
15	DV_{EE}	Digital (ECL) Power Supply -4.75V to -7V.
16	COMPL	Data Complement Pin. When set to a (ECL) logic High the input data is complemented in the input buffer. When cleared to a (ECL) logic Low the input data is not complemented.
17	DV_{SS}	Digital Ground
18	AV_{SS}	Analog Ground
20	I_{OUT}	Current Output Pin.
26	AV_{EE}	Analog Supply -4.75V to -7V.
27	V_{REF}	Input Reference Voltage used to set the output full scale range.
28	AV_{SS}	Analog Ground

Detailed Description

The HI20201 is a 10 bit, current output D/A converter. The DAC can run at 160MSPS and is ECL compatible. The architecture is segmented/R2R combination to reduce glitch and improve linearity.

The HI20203 is an 8 bit, current output D/A converter. The converter has 10 data bits but yields 8 bit performance.

Architecture

The HI2020/031 is a combined R2R/segmented current source design. The 6 least significant bits of the converter are derived by a traditional R2R network to binary weight the 1mA current sources. The upper 4 most significant bits are implemented as segmented or thermometer encoded current sources. The encoder converts the incoming 4 bits to 15 control lines to enable the most significant current sources. The thermometer encoder will convert binary to individual control lines. See Table 1.

TABLE 1. THERMOMETER ENCODER

MSB	BIT 8	BIT 7	BIT 6	THERMOMETER CODE 1 = ON, 0 = OFF I_{15} - I_0
0	0	0	0	000 0000 0000 0000
0	0	0	1	000 0000 0000 0001
0	0	1	0	000 0000 0000 0011
0	0	1	1	000 0000 0000 0111
0	1	0	0	000 0000 0000 1111
0	1	0	1	000 0000 0001 1111
0	1	1	0	000 0000 0011 1111
0	1	1	1	000 0000 0111 1111
1	0	0	0	000 0000 1111 1111
1	0	0	1	000 0001 1111 1111
1	0	1	0	000 0011 1111 1111
1	0	1	1	000 0111 1111 1111
1	1	0	0	000 1111 1111 1111
1	1	0	1	001 1111 1111 1111
1	1	1	0	011 1111 1111 1111
1	1	1	1	111 1111 1111 1111

The architecture of the HI20201/03 is designed to minimize glitch while providing a manufacturable 10 bit design that does not require laser trimming to achieve good linearity.

Glitch

Glitch is caused by the time skew between bits of the incoming digital data. Typically the switching time of digital inputs are asymmetrical meaning that the turn off time is faster than the turn on time (TTL designs). In an ECL system where the logic levels switch from one non-saturated level to another, the switching times can be considered close to symmetrical. This helps to reduce glitch in the D/A. Unequal delay paths through the device can also cause one current source to change before another. To minimize this the Harris HI20201/03 employes an internal register, just prior to the current sources, that is updated on the clock edge. Lastly the worst case glitch usually happens at the major transition i.e. 01 1111 1111 to 10 0000 0000. But in the HI20201/03 the glitch is moved to the 00 0001 1111 to 11 1110 0000 transition. This is achieved by the split R2R/segmented current source architecture. This decreases the amount of current switching at any one time and makes the glitch practically constant over the entire output range. By making the glitch a constant size over the entire output range this effectively integrates this error out of the end application.

In measuring the output glitch of the HI20201/03 the output is terminated into a 75Ω load. The glitch is measured at the major carry's throughout the DACs output range.

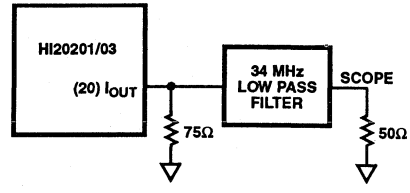


FIGURE 6. HI20201/03 GLITCH TEST CIRCUIT

The glitch energy is calculated by measuring the area under the voltage-time curve. Figure 7 shows the area considered as glitch when changing the DAC output. Units are typically specified in picoVolt-seconds (pV-sec).

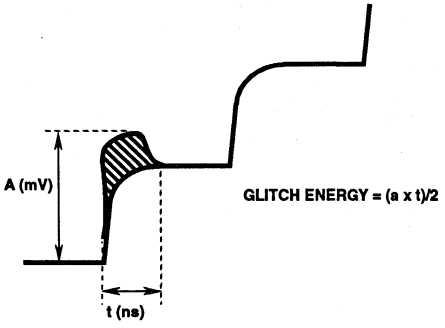


FIGURE 7. GLITCH ENERGY

Setting Full Scale

The Full Scale output voltage is set by the Voltage Reference pin (27). The output voltage performance will vary as shown in Figure 2.

The output structure of the HI20201 can handle down to a 75Ω load effectively. To drive a 50Ω load Figure 8 is suggested. Note the equivalent output load is ~75Ω.

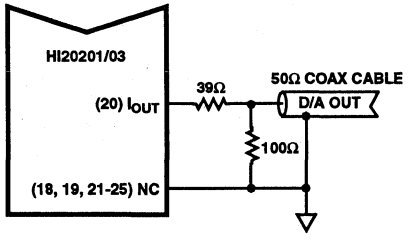


FIGURE 8. HI20201/03 DRIVING A 50Ω LOAD

Variable Attenuator Capability

The HI20201/03 can be used in a multiplying mode with a variable frequency input on the V_{REF} pin. In order for the part to operate correctly a DC bias must be applied and the incoming AC signal should be coupled to the V_{REF} pin. See Figure 13 for the application circuit. The user must first adjust the DC reference voltage. The incoming signal must be attenuated so as not to exceed the maximum (+1.4V) and minimum (+0.5V) reference input. The typical output Small Signal Bandwidth is 14MHz.

Integral Linearity

The Integral Linearity is measured using the End Point method. In the End Point method the gain is adjusted. A line is then established from the zero point to the end point or Full Scale of the converter. All codes along the transfer curve must fall within an error band of 1 LSB of the line. Figure 10 shows the linearity test circuit.

Differential Linearity

The Differential Linearity is the difference from the ideal step. To guarantee monotonicity a maximum of 1 LSB differential error is allowed. When more than 1 LSB is specified the converter is considered to be missing codes. Figure 10 shows the linearity test circuit.

Clock Phase Relationship

The HI20201/03 are designed to be operated at very high speed (i.e. 160MHz). The clock lines should be driven with ECL100K logic for full performance. Any external data drivers and clock drivers should be terminated with 50Ω to minimize reflections and ringing.

Internal Data Register

The HI20201/03 incorporates a data register as shown in the Functional Block Diagram. This register is updated on the rising edge of the CLK line. The state of the Complement bit (COMPL) will determine the data coding. See Table 2.

TABLE 2. INPUT CODING TABLE

INPUT CODE	OUTPUT CODE	
	COMPL = 1	COMPL = 0
00 0000 0000	0	-1
10 0000 0000	-0.5	-0.5
11 1111 1111	-1	0

Thermal Considerations

The temperature coefficient of the full scale output voltage and zero offset voltage depend on the load resistance connected to I_{OUT}. The larger the load resistor the better (i.e. smaller) the temperature coefficient of the D/A. See Figure 3 in the performance curves section.

Noise Reduction

Digital switching noise must be minimized to guarantee system specifications. Since 1 LSB corresponds to 1mV for 10 bit resolution, care must be taken in the layout of a circuit board.

Separate ground planes should be used for DV_{SS} and AV_{SS}. They should be connected back at the power supply.

Separate power planes should be used for DV_{EE} and AV_{EE}. They should be decoupled with a 1µF tantalum capacitor and a ceramic 0.047µF capacitor positioned as close to the body of the IC as possible.

Test Circuits

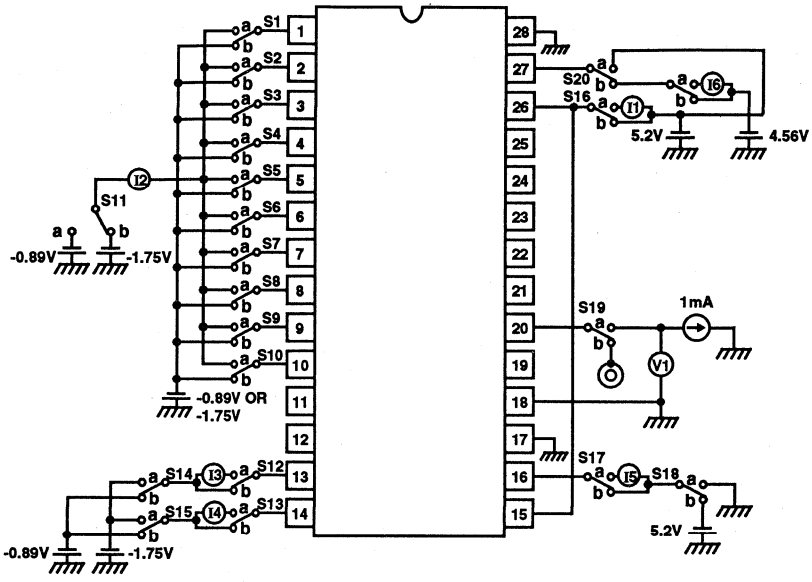
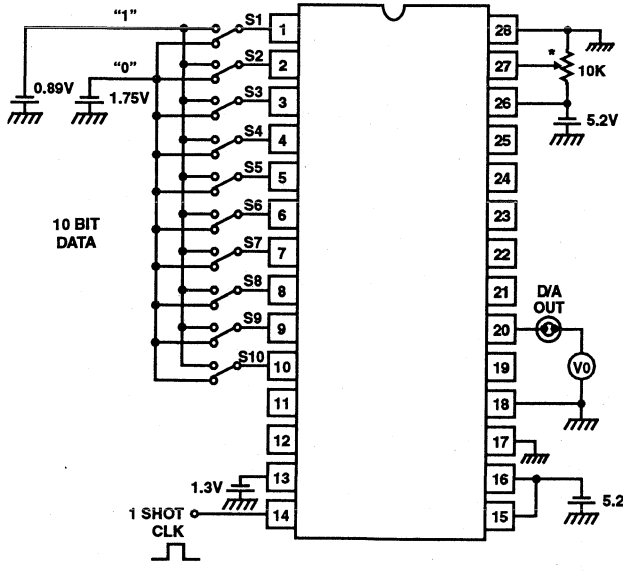


FIGURE 9. CURRENT CONSUMPTION, INPUT CURRENT AND OUTPUT RESISTANCE



LINEARITY ERRORS ARE MEASURED AS FOLLOWS						
S1	S2	S3	••••	S9	S10	D/A OUT
0	0	0	••••	0	0	V_0
0	0	0	••••	0	1	V_1
0	0	0	••••	1	0	V_2
			⋮			⋮
1	1	1	••••	1	1	V_{1023}

INTEGRAL LINEARITY ERROR	DIFFERENTIAL LINEARITY ERROR
V_0	
V_1	$V_1 - V_0$
V_2	$V_2 - V_1$
V_4	$V_4 - V_3$
V_8	$V_8 - V_7$
V_{16}	$V_{16} - V_{15}$
V_{32}	$V_{32} - V_{31}$
V_{64}	$V_{64} - V_{63}$
V_{128}	$V_{128} - V_{127}$
V_{192}	$V_{192} - V_{191}$
⋮	⋮
V_{960}	$V_{960} - V_{959}$
V_{1023}	

Error at individual measurement points are calculated according to the following definition.

$(V_{1023} - V_0)/1023 = V_{O(FS)}/1023 \equiv 1$ LSB.

FIGURE 10. DIFFERENTIAL LINEARITY ERROR AND LINEARITY ERROR

Test Circuits (Continued)

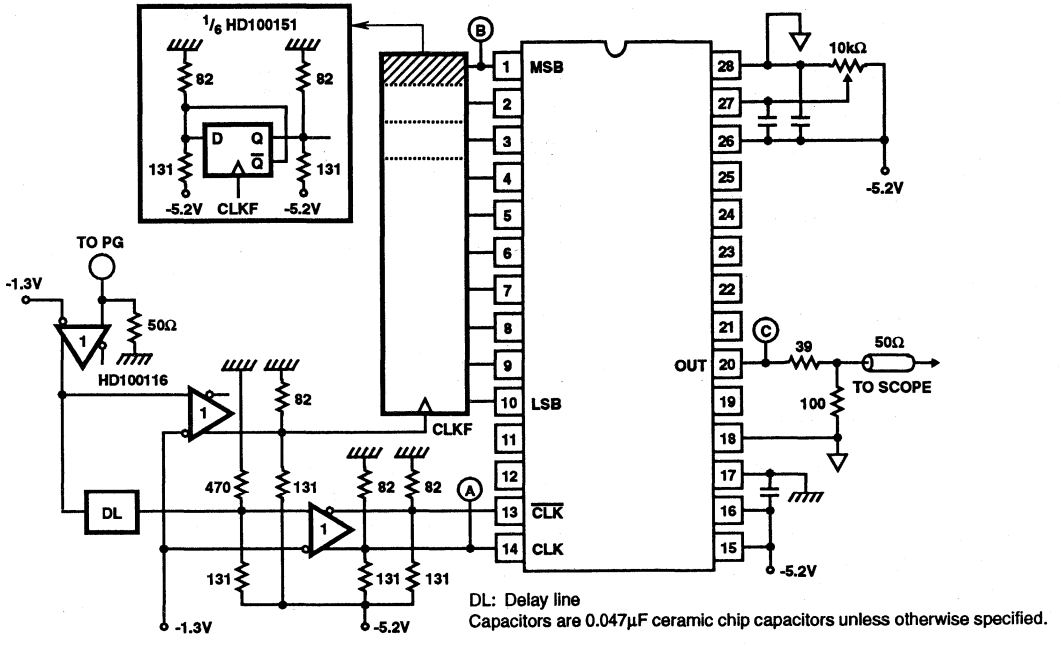


FIGURE 11. MAXIMUM CONVERSION RATE, RISE TIME, FALL TIME, PROPAGATION DELAY, SETUP TIME, HOLD TIME AND SETTLING TIME

Measuring Settling Time

Settling time is measured as follows. The relationship between V and $V_{0(FS)}$ as shown in the D/A output waveform in Figure 12 is expressed as

$$V = V_{0(FS)} (1 - e^{-t\tau}).$$

The settling time for respective accuracy of 10, 9 and 8-bit is specified as

$V = 0.9995\ V_{0(FS)}$
$V = 0.999\ V_{0(FS)}$
$V = 0.999\ V_{0(FS)}$

which results in the following:

$t_S = 7.60\tau$ for 10-bit,
$t_S = 6.93\tau$ for 9-bit, and
$t_S = 6.24\tau$ for 8-bit,

Rise time (t_R) and fall time (t_F) are defined as the time interval to slew from 10% to 90% of full scale voltage ($V_{0(FS)}$):

$V = 0.1\ V_{0(FS)}$
$V = 0.9\ V_{0(FS)}$

and calculated as $t_R = t_F = 2.20\tau$.

The settling time is obtained by combining these expressions:

$t_S = 3.45t_R$ for 10-bit,
$t_S = 3.15t_R$ for 9-bit, and
$t_S = 6.24t_R$ for 8-bit

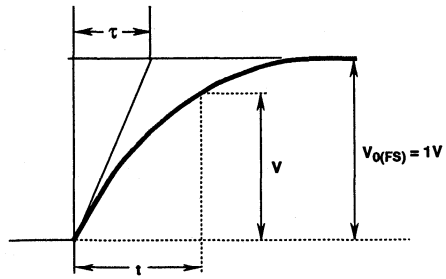


FIGURE 12. D/A OUTPUT WAVEFORM

Test Circuits (Continued)

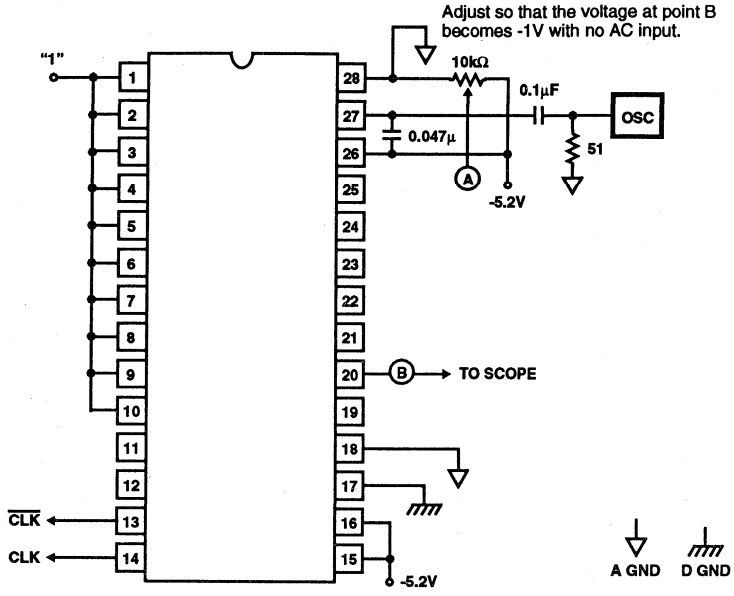


FIGURE 13A.

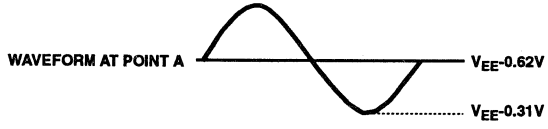


FIGURE 13B.

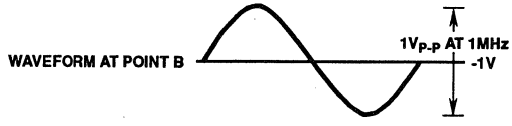


FIGURE 13C.

FIGURE 13. MULTIPLYING BANDWIDTH

DATA ACQUISITION 9

SWITCHES

NOTE: Bold Type Designates a New Product from Harris.

Switches (Continued)

NOTE: Bold Type Designates a New Product from Harris.

SINGLE POLE SINGLE THROW (SPST, FIGURE 1)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
HI1-5040	-2, -5, -7	HI1-5040/883	75	3.0	0.8	36V CMOS-DI	0.8	370	280	
IH5140	MJE, CJE, CPE	IH5140MJE/883B	75	2.4	0.8	36V CMOS-JI	5.0	175	150	
HI1-0301	-2, -5, -7	HI1-0301/883	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Very Low Leakage, TTL Inputs
HI2-0301	-2, -5	HI2-0301/883								
HI3-0301	-5									
HI9P0301	-5									
HI9P0301	-9									
HI1-0305	-2, -5	HI1-0305/883	50	11.0	3.5	44V CMOS-DI	0.04	160	100	CMOS Logic Very Low Leakage
HI2-0305	-2, -5	HI2-0305/883								
HI3-0305	-5									
HI9P0305	-5									
HI9P0305	-9									

DUAL SINGLE POLE SINGLE THROW (2 x SPST, FIGURE 2)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
DG200	AA, AK BA, BK CK	DG200AA/883B DG200AK/883B	80	2.4	0.8	36V CMOS-JI	5.0	1000	500	
DG300A	AA, AK BA, BK CJ, CK	DG300AAA/883B DG300AAK/883B	50	4.0	0.8	44V CMOS-JI	0.1	150	130	
DG401	DJ, DY	DG401AK/883	45	2.4	0.8	44V CMOS-JI	-0.01	100	60	Very Low $R_{DS(ON)}$

DUAL SINGLE POLE SINGLE THROW (2 x SPST, FIGURE 2) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
HI1-0200	-2, -4, -5, -7	HI1-0200/883	80	0.8	2.4	44V CMOS-DI	1.0	240	500	
HI2-0200	-2, -4, -5, -7	HI2-0200/883								
HI3-0200	-5									
HI9P0200	-5, -9									
HI1-0300	-2, -5	HI1-0300/883	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Very Low Leakage
HI2-0300	-2, -5	HI2-0300/883								
HI3-0300	-5									
HI9P0300	-5, -9									
HI1-0304	-2, -5	HI1-0304/883	50	11.0	3.5	44V CMOS-DI	0.04	160	100	CMOS Logic Very Low Leakage
HI2-0304	-2, -5	HI2-0304/883								
HI3-0304	-5									
HI9P0304	-5, -9									
HI1-0381	-2, -5	HI1-0381/883	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Very Low Leakage
HI2-0381	-2, -5	HI2-0381/883								
HI3-0381	-5									
HI9P0381	-5, -9									
HI1-5041	-2, -5, -7, -8	HI1-5041/883	75	3.0	0.8	36V CMOS-DI	0.8	370	280	10Ω $R_{DS(ON)}$ Matching
HI3-5041	-5									
HI1-5048	-2, -5, -7	HI1-5048/883	45	3.0	0.8	36V CMOS-DI	0.8	370	280	5Ω $R_{DS(ON)}$ Matching
HI3-5048	-5									
IH5141	CJE, CPE MJE	IH5141MJE/883B	75	2.4	0.8	36V CMOS-JI	5.0	150	125	
IH5341	CPD, ITW, MTW	IH5341MTW/883B	75	2.4	0.8	36V CMOS-JI	1.0	150	80	RF Video T-Switch

QUAD SINGLE POLE SINGLE THROW (4 x SPST, FIGURE 3)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
DG201	AK, BK, CJ	DG201AK/883B	100	2.4	0.8	36V CMOS-JI	0.01	480	370	Very Low Leakage
DG201A	AK, BK, CJ, CK	DG201AAK/883B	115 Typ	0.8	2.4	44V CMOS-JI	0.01	480	370	Very Low Leakage
DG201A	BY, CY									
DG202	AK, BK, CJ, CK	DG202AK/883B	115 Typ	2.4	0.8	44V CMOS-JI	0.01	480	370	
DG211	CJ, CY		150 Typ	0.8	2.4	44V CMOS-JI	0.01	460	360	Low Cost
DG212	CJ, CY		150 Typ	2.4	0.8	44V CMOS-JI	0.01	460	360	Low Cost
DG308A	AK, BK CJ, CK, CY	DG308AAK/883B	60 Typ	11.0	3.5	44V CMOS-JI	0.01	130	90	CMOS Logic, Single or Dual Supply Operation
DG309	AK, BK, CJ, CK, CY	DG309AK/883B	60 Typ	3.5	11.0	44V CMOS-JI	0.1	130	90	CMOS Logic, Single or Dual Supply Operation
DG411	DJ, DY	DG411AK/883	35	2.4	0.8	44V CMOS-JI	-0.1	110	100	Very Low $R_{DS(ON)}$
DG412	DJ, DY	DG412AK/883	35	2.4	0.8	44V CMOS-JI	-0.1	110	100	Very Low $R_{DS(ON)}$
DG413	DJ, DY	DG413AK/883	35	2.4	0.8	44V CMOS-JI	-0.1	110	100	Very Low $R_{DS(ON)}$
DG441	DJ, DY	DG441AK/883	85	2.4	0.8	44V CMOS-JI	0.01	150	90	Low $R_{DS(ON)}$, Low Leakage
DG442	DJ, DY	DG442AK/883	85	2.4	0.8	44V CMOS-JI	0.01	150	110	Low $R_{DS(ON)}$, Low Leakage
DG444	DJ, DY		85	2.4	0.8	44V CMOS-JI	0.01	150	90	Low $R_{DS(ON)}$, Low Leakage
DG445	DJ, DY		85	2.4	0.8	44V CMOS-JI	0.01	150	110	Low $R_{DS(ON)}$, Low Leakage
HI1-0201	-2, -4, -5, -7, -8	HI1-0201/883	80	0.8	2.4	44V CMOS-DI	2.0	185	220	
HI3-0201	-5									
HI4P0201	-5									
HI9P0201	-5, -9									
		HI4-0201/883								

QUAD SINGLE POLE SINGLE THROW (4 x SPST, FIGURE 3) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
HI1-0201HS	-2, -4, -5, -7, -8	HI1-0201HS/883	50	0.8	2.4	33V CMOS-DI	0.3	30	40	High Speed, Low $R_{DS(ON)}$
HI3-0201HS	-4, -5									
HI4P0201HS	-5									
HI9P0201HS	-5, -9									
		HI4-0201HS/883								
IH5052	CDE, MDE		80	0.8	2.4	36V CMOS-JI	5.0	1000	500	
IH5053	CDE, MDE		80	2.4	0.8	36V CMOS-JI	5.0	1000	500	
IH5352	CPE, IJE, MJE	IH5352MJE/883B	75	2.4	0.8	36V CMOS-JI	2.0	150	80	RF Video T-Switch
IH5352	CBP, IBP									

FOUR POLE SINGLE THROW (4PST, FIGURE 4)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
HI1-5047	-2, -5, -7	HI1-5047/883	75	3.0	0.8	36V CMOS-JI	0.8	370	280	10Ω Max $R_{DS(ON)}$ Matching
HI3-5047	-5									
HI1-5047A	-2, -5, -7, -8	HI1-5047A/883	45	3.0	0.8	36V CMOS-JI	0.8	370	280	5Ω Max $R_{DS(ON)}$ Matching
HI3-5047A	-5									
HI4P5047A	-5									

SINGLE POLE DOUBLE THROW (SPDT, FIGURE 5)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
DG301A	AA, AK BA, BK CA, CJ, CK	DG301AAA/883B DG301AAK/883B	50	2.4	0.8	44V CMOS-JI	0.1	150	130	Channel 1 "ON", Channel 2 "OFF", TTL Inputs
DG303A	BY, CY									
HI1-0387	-2, -5	HI1-0387/883	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Channel 1 "ON", Channel 2 "OFF", Very Low Leakage
HI2-0387	-2, -5	HI2-0387/883								
HI3-0387	-5									
HI9P0387	-5									
HI1-5042	-2, -5, -7	HI1-5042/883	75	3.0	0.8	36V CMOS-DI	0.8	370	280	Channel 1 "ON", Channel 2 "OFF", 10Ω Max RDS Matching
HI3-5042	-5									
HI1-5050	-2, -5, -7	HI1-5050/883	45	3.0	0.8	36V CMOS-DI	0.8	370	280	Channel 1 "ON", Channel 2 "OFF", 5Ω Max RDS Matching
HI3-5050	-5									

DUAL SINGLE POLE DOUBLE THROW (2 x SPDT, FIGURE 6)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
DG403	DJ, DY	DG403AK/883	45	2.4	0.8	44V CMOS-JI	-0.01	100	60	
HI1-0303	-2, -5	HI1-0303/883	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Channel 1 "ON", Channel 2 "OFF", Very Low Leakage, TTL Inputs
HI3-0303	-5									
HI9P0303	-5, -9									

DUAL SINGLE POLE DOUBLE THROW (2 x SPDT, FIGURE 6) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
HI1-0307	-2, -5, -7	HI1-0307/883	50	11.0	3.5	44V CMOS-DI	0.04	160	100	Channel 1 "ON", Channel 2 "OFF", Very Low Leakage
HI3-0307	-5									
HI9P0307	-5, -9									
HI1-0390	-2, -5	HI1-0390/883	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Channel 1 "ON", Channel 2 "OFF", Very Low Leakage
HI3-0390	-5									
HI9P0390	-5, -9									
HI1-5043	-2, -5 -8	HI1-5043/883	75	2.4	0.8	36V CMOS-DI	0.8	370	280	Channel 1 "ON" Channel 2 "OFF" 10Ω Max $R_{DS(ON)}$ Matching
HI3-5043	-5									
HI9P5043	-5, -9									
HI1-5051	-2, -5, -7, -8	HI1-5051/883	45	3.0	0.8	36V CMOS-DI	0.84	370	280	Channel 1 "ON" Channel 2 "OFF" 5Ω Max $R_{DS(ON)}$ Matching
HI3-5051	-5									
HI4P5051	-5									
HI9P5051	-5, -9									
IH5043	CDE, CJE, CPE, CY, MJE	IH5043MJE/883B	80	3.0	0.8	36V MCOS-JI	5.0	1000	500	Channel 1 "ON" Channel 2 "OFF"

DOUBLE POLE SINGLE THROW (DPST, FIGURE 7)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
HI1-5044	-2, -5, -7	HI1-5044/883	75	3.0	0.8	36V CMOS-DI	0.8	370	280	10Ω Max $R_{DS(ON)}$ Matching
HI3-5044	-5									
IH5144	CJE, CPE, MJE	IH5144MJE/883B	75	2.4	0.8	36V CMOS-JI	5.0	250	150	

DUAL DOUBLE POLE SINGLE THROW (2 x DPST, FIGURE 8)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
DG302A	AK, BK, CK, CJ	DG302AAK/883B	50	4.0	0.8	44V CMOS-JI	0.1	150	130	TTL Inputs
DG405	DJ, DY	DG405AK/883	45	2.4	0.8	44V CMOS-JI	-0.01	100	60	Very Low $R_{DS(ON)}$
HI1-0302	-2, -5	HI1-0302/883	50	4.0	0.8	44V CMOS-DI	0.1	210	160	TTL Inputs
HI3-0302	-5									
HI9P0302	-5, -9									
HI1-0306	-2, -5	HI1-0306/883	50	11.0	3.5	44V CMOS-DI	0.1	160	100	CMOS Logic
HI3-0306	-5									
HI9P0306	-5, -9									
HI1-0384	-2, -5	HI1-0384/883	50	4.0	0.8	44V CMOS-DI	0.04	210	160	Very Low Leakage
HI3-0384	-5									
HI9P0384	-5, -9									
HI1-5045	-2, -5, -7	HI1-5045/883	75	4.0	0.8	36V CMOS-DI	0.04	210	160	Very Low Leakage
HI3-5045	-5									
		HI4-5045/883								
HI95045	-5, -9									
HI1-5049	-2, -5, -7	HI1-5049/883	45	3.0	0.8	36V CMOS-DI	0.8	370	280	5Ω $R_{DS(ON)}$ Matching
HI3-5049	-5									
IH5145	CJE, CPE, MJE	IH5145MJE/883B	75	2.4	0.8	36V CMOS-JI	5.0	150	125	

DUAL DOUBLE POLE DOUBLE THROW (2 x DPDT, FIGURE 9)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
HI1-5046	-2, -5, -7	HI1-5046/883	75	0.8	2.4	36V CMOS-DI	0.8	370	280	Channel 1 "ON" Channel 2 "OFF" 10Ω Max $R_{DS(ON)}$ Matching
HI3-5046	-5									
HI1-5046A	-2, -5, -7	HI1-5046A/883	45	3.0	0.8	36V CMOS-DI	0.8	370	280	Channel 1 "ON" Channel 2 "OFF" 5Ω Max $R_{DS(ON)}$ Matching
HI3-5046A	-5									

RF/VIDEO "T" SWITCHES ("T" SWITCH , FIGURE 10)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ Ω MAX	SWITCH "ON" (V)	SWITCH "OFF" (V)	TECHNOLOGY	I_{SOFF} (±nA) TYP	T_{ON} (ns) TYP	T_{OFF} (ns) TYP	FEATURES
IH5341	ITW, MTW	IH5341MTW/883B	75	2.4	0.8	36V CMOS-JI	1.0	150	80	Dual SPST
IH5341	CPD									
IH5352	IJE, MJE	IH5352MJE/883B	75	2.4	0.8	36V CMOS-JI	2.0	150	80	Quad SPST
IH5352	CPE									
IH5352	CBP									
IH5352	IBP									

NOTES:

1. The $R_{DS(ON)}$ of a CMOS switch varies as a function of supply voltage, analog signal voltage, and temperature. Values shown are maximum (unless noted "Typ" = typical) at +25°C.
   SWITCH "ON" V: Digital Threshold to "CLOSE" a particular switch. (Minimum if greater than "OFF". Maximum if less than "OFF").
   SWITCH "OFF" V: Digital Threshold to "OPEN" a particular switch. (Minimum if greater than "ON". Maximum if less than "ON").
   V_{INL}: Digital Threshold to represent a "Low" select signal. (Maximum, voltage levels greater than this value are not guaranteed to produce a "LOW").
   V_{INH}: Digital Threshold to represent a "HIGH" select signal. (Minimum, voltage levels less than this value are not guaranteed to produce a "HIGH").
2. Package codes:
   DG Types - SUFFIX:
   - A 10 Lead TO-100
   - J Plastic DIP
   - K Ceramic DIP
   - P Ceramic DIP

   IH Types - Middle SUFFIX Letter:
   - J Ceramic DIP
   - P Plastic DIP
   - T TO-100 Can
   - B SOIC

   HI Types - PREFIX:
   - HI1 Ceramic DIP
   - HI2 Metal Can
   - HI3 Plastic DIP
   - HI4 Ceramic LCC
   - HI4P PLCC
   - HI9P SOIC
3. Temperature Code Suffix:
   - -1: 0° to +200°C
   - -2, A, or M: -55°C to +125°C
   - -4 or B: -25°C to +85°C
   - -5: 0°C to +75°C
   - C: 0°C to +70°C
   - -7: 0°C to +75°C with Burn-In
   - -8: -55°C to +125°C with Burn-In
   - -9: -40°C to +85°C
   - /883: Mil-Std-883, Class B, -55°C to +125°C with Burn-In
   - I: Industrial, -25°C or -40°C to +85°C, see data sheet
4. Double Throw switches have one switch ON and the other switch OFF for each input state. See data sheet.

Selection Guide (Continued)

FIGURE 1. SPST

FIGURE 2. DUAL SPST

FIGURE 3. QUAD SPST

FIGURE 4. 4PST

FIGURE 5. SPDT

FIGURE 6. DUAL SPDT

FIGURE 7. DPST

FIGURE 8. DUAL DPST

FIGURE 10. "T" SCHEMATIC

FIGURE 9. DPDT

FIGURE 11. "T" SWITCH

HARRIS SEMICONDUCTOR

DG200, DG201

December 1993

CMOS Dual/Quad SPST Analog Switches

Features

- Switches Greater than 28V_{P-P} Signals with ±15 Supplies
- Break-Before-Make Switching t_{OFF} 250ns, t_{ON} 700ns Typical
- TTL, DTL, CMOS, PMOS Compatible
- Non-Latching with Supply Turn-Off
- Complete Monolithic Construction
- Industry Standard (DG200, DG201)

Applications

- Data Acquisition
- Sample and Hold Circuits
- Operational Amplifier Gain Switching Networks

Description

The DG200 and DG201 solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. They provide ease-of-use and performance advantages not previously available from solid state switches. Destructive latch-up of solid state analog gates has been eliminated by Harris's CMOS technology.

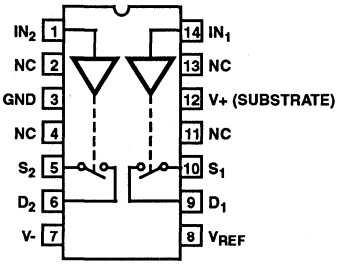
The DG200 and DG201 are completely specification and pinout compatible with the industry standard devices.

Ordering Information

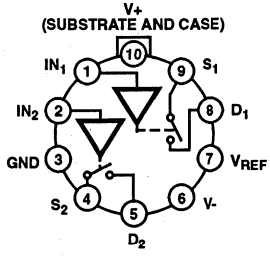
PART NUMBER	TEMPERATURE	PACKAGE
DG200AA	-55°C to +125°C	10 Pin Metal Can
DG200AK	-55°C to +125°C	14 Lead Ceramic DIP
DG200BA	-25°C to +85°C	10 Pin Metal Can
DG200BK	-25°C to +85°C	14 Lead Ceramic DIP
DG200CJ	0°C to +70°C	14 Lead Plastic DIP
DG200AA/883B	-55°C to +125°C	10 Pin Metal Can
DG200AK/883B	-55°C to +125°C	14 Lead Ceramic DIP
DG201AK	-55°C to +125°C	16 Lead Ceramic DIP
DG201BK	-25°C to +85°C	16 Lead Ceramic DIP
DG201CJ	0°C to +70°C	16 Lead Plastic DIP
DG201AK/883B	-55°C to +125°C	16 Lead Ceramic DIP

Pinouts

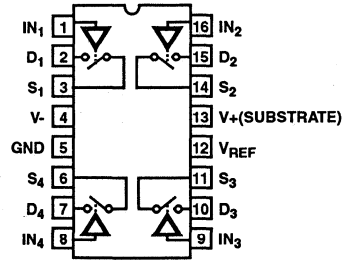
DG200
(CDIP, PDIP)
TOP VIEW



DG200
(TO-100 METAL CAN)
TOP VIEW



DG201
(CDIP, PDIP)
TOP VIEW

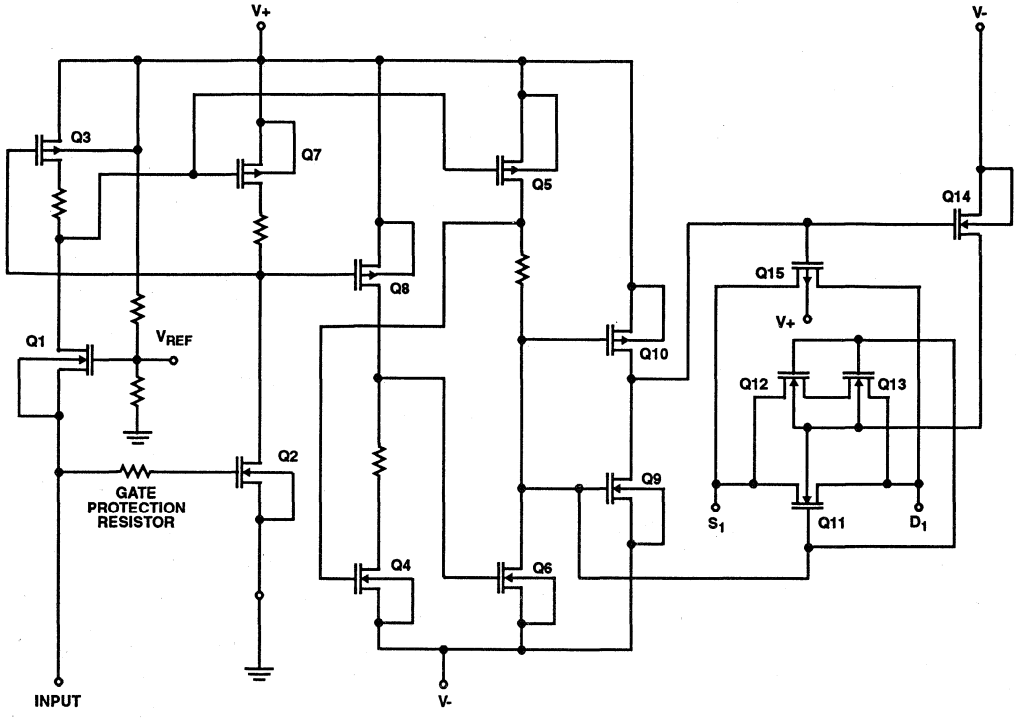


9 SWITCHES

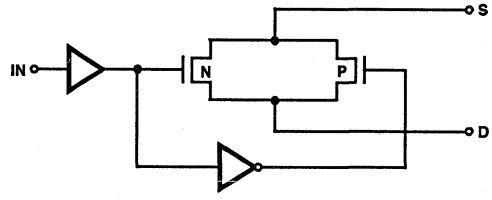
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3115**

Schematic Diagram ($^1/_2$ DG200, $^1/_4$ DG201)



Functional Diagram



DG200, DG201 SWITCH CELL

Absolute Maximum Ratings

$V+, V-$ ..... <36V
$V+ - V_D$ ..... <30V
$V_D - V-$ ..... <30V
$V_D - V_S$ ..... <28V
V_{IN} - GND ..... <20V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	95°C/W	24°C/W
Plastic DIP Package	100°C/W	-
Metal Can Package	136°C/W	65°C/W

Operating Temperature Range
"A" Suffix ..... -55°C to +125°C
"B" Suffix ..... -25°C to +85°C
"C" Suffix ..... 0°C to +70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications (T_A = +25°C, V+ = +15V, V- = -15V)

PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL / INDUSTRIAL			UNITS
		-55°C	+25°C	+125°C	0°C TO -25°C	+25°C	+70°C TO +85°C	
Input Logic Current, $I_{IN(ON)}$	V_{IN} = 0.8V (Notes 2, 3)	±10	±1	±10	-	±10	±10	µA
Input Logic Current, $I_{N(OFF)}$	V_{IN} = 2.4V (Notes 2, 3)	±10	±1	±10	-	±10	±10	µA
Drain-Source On Resistance, $r_{DS(ON)}$	I_S = 10mA, V_{ANALOG} = ±10V	70	70	100	80	80	100	Ω
Channel-to-Channel $r_{DS(ON)}$ Match, $r_{DS(ON)}$		-	25 (Typ)	-	-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}		-	±15V	-	-	±15V	-	V
Switch OFF Leakage Current, $I_{D(OFF)}$	V_{ANALOG} = -14V to +14V	-	±2	100	-	±5	100	nA
Switch OFF Leakage Current, $I_{S(OFF)}$	V_{ANALOG} = -14V to +14V	-	±2	100	-	±5	100	nA
Switch ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$	$V_D = V_S$ = -14V to +14V	-	±2	200	-	±10	200	nA
Switch "ON" Time (Note 1), t_{ON}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V (Figure 5)	-	1.0	-	-	1.0	-	µs
Switch "OFF" Time, t_{OFF}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V (Figure 5)	-	0.5	-	-	0.5	-	µs
Charge Injection, $Q_{(INJ.)}$	Figure 6	-	15 (Typ)	-	-	20 (Typ)	-	mV
Minimum Off Isolation Rejection Ratio, OIRR	f = 1MHz, R_L = 100Ω, $C_L \leq$ 5pF (Figure 7, Note 1)	-	54 (Typ)	-	-	50 (Typ)	-	dB
+Power Supply Quiescent Current, I_{V1}	V_{IN} = 0V or V_{IN} = 5V	1000	1000	2000	1000	1000	2000	µA
-Power Supply Quiescent Current, I_{V2}		1000	1000	2000	1000	1000	2000	µA
Minimum Channel to Channel Cross Coupling Rejection Ratio, CCRR	One Channel Off	-	54 (Typ)	-	-	50 (Typ)	-	dB

NOTES:

1. Pull Down Resistor must be ≤ 2kΩ.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the minimum range for switching properly. Peak input current required for transition is typically -120µA.

Absolute Maximum Ratings

V+ to V- ..... <36V
V+ to V_D ..... <30V
V_D to V- ..... <30V
V_D to V_S ..... <28V
V_{REF} to V- ..... <33V
V_{REF} to V_{IN} ..... <30V
V_{REF} to GND ..... <20V
V_{IN} to GND ..... <20V
Current (Any Terminal) ..... <30mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	80°C/W	24°C/W
Plastic DIP Package	145°C/W	-

Operating Temperature Range
"A" Suffix ..... -55°C to +125°C
"B" Suffix ..... -25°C to +85°C
"C" Suffix ..... 0°C to +70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications (T_A = +25°C, V+ = +15V, V- = -15V)

PARAMETER	TEST CONDITIONS	MILITARY			COMMERCIAL / INDUSTRIAL			UNITS
		-55°C	+25°C	+125°C	0°C TO -25°C	+25°C	+70°C TO +85°C	
Input Logic Current, $I_{IN(ON)}$	V_{IN} = 0.8V (Note 1)	10	±1	10	±1	±1	10	µA
Input Logic Current, $I_{N(OFF)}$	V_{IN} = 2.4V (Note 1)	10	±1	10	±1	±1	10	µA
Drain-Source On Resistance, $r_{DS(ON)}$	I_S = 10mA, V_{ANALOG} = ±10V	80	80	125	100	100	125	Ω
Channel-to-Channel $r_{DS(ON)}$ Match, $r_{DS(ON)}$		-	25 (Typ)	-	-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}		-	±15 (Typ)	-	-	±15 (Typ)	-	V
Switch OFF Leakage Current, $I_{D(OFF)}$	V_{ANALOG} = -14V to +14V	-	±1	100	-	±5	100	nA
Switch OFF Leakage Current, $I_{S(OFF)}$	V_{ANALOG} = -14V to +14V	-	±1	100	-	±5	100	nA
Switch ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$	$V_D = V_S$ = -14V to +14V	-	±2	200	-	±5	200	nA
Switch "ON" Time (Note 2), t_{ON}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V (Figure 5)	-	1.0	-	-	1.0	-	µs
Switch "OFF" Time (Note 2), t_{OFF}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V (Figure 5)	-	0.5	-	-	0.5	-	µs
Charge Injection, $Q_{(INJ.)}$	Figure 6	-	15 (Typ)	-	-	20 (Typ)	-	mV
Minimum Off Isolation Rejection Ratio, OIRR	f = 1MHz, R_L = 100Ω, $C_L \leq$ 5pF, (Figure 7)	-	54 (Typ)	-	-	50 (Typ)	-	dB
+Power Supply Quiescent Current, I_{+Q}	V_{IN} = 0V or V_{IN} = 5V	2000	1000	2000	2000	1000	2000	µA
-Power Supply Quiescent Current, I_{-Q}		2000	1000	2000	2000	1000	2000	µA
Minimum Channel to Channel Cross Coupling Rejection Ratio, CCRR	One Channel Off	-	54 (Typ)	-	-	50 (Typ)	-	dB

NOTES:

1. Typical values are for design aid only, not guaranteed and not subject to production testing.
2. All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the minimum range for switching properly. Peak input current required for transition is typically -120µA.

Performance Curves

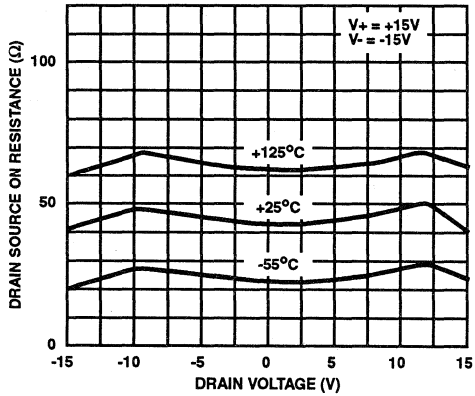


FIGURE 1. $R_{DS(ON)}$ vs V_D AND TEMPERATURE

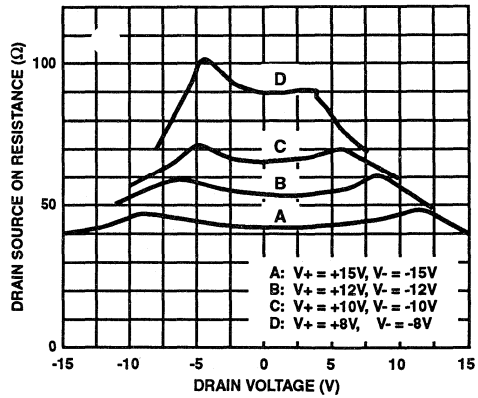


FIGURE 2. $r_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

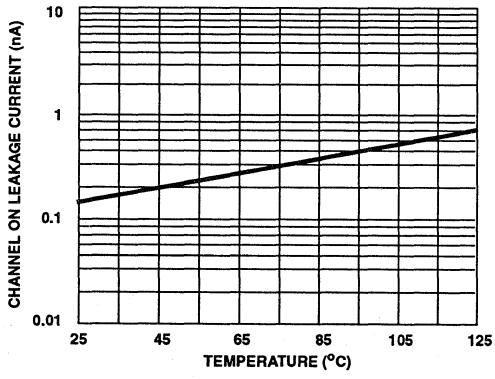


FIGURE 3. $I_{D(ON)}$ vs TEMPERATURE

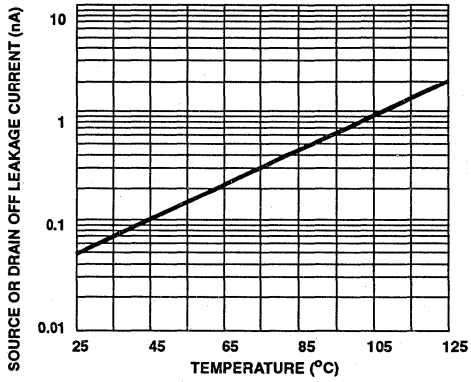


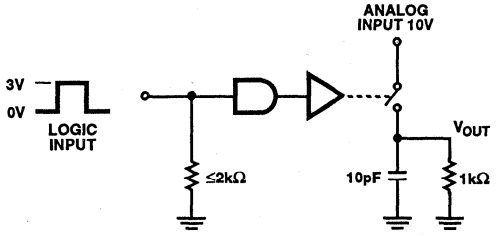
FIGURE 4. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE

Pin Description

DG200 (14 LEAD DIP)		
PIN	SYMBOL	DESCRIPTION
1	IN_2	Logic control for switch 2
2	NC	No Connection
3	GND	Ground Terminal (Logic Common)
4	NC	No Connection
5	S_2	Source (input) terminal for switch 2
6	D_2	Drain (output) terminal for switch 2
7	V-	Negative power supply terminal
8	V_{REF}	Logic reference voltage
9	D_1	Drain (output) terminal for switch 1
10	S_1	Source (input) terminal for switch 1
11	NC	No Connection
12	V+	Positive power supply terminal (substrate)
13	NC	No Connection
14	IN_1	Source (input) terminal for switch 1

DG201 (16 LEAD DIP)		
PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic control for switch 1
2	D_1	Drain (output) terminal for switch 1
3	S_1	Source (input) terminal for switch 1
4	V-	Negative power supply terminal
5	GND	Ground terminal (Logic Common)
6	S_4	Source (input) terminal for switch 4
7	D_4	Drain (output) terminal for switch 4
8	IN_4	Logic control for switch 4
9	IN_3	Logic control for switch 3
10	D_3	Drain (output) terminal for switch 3
11	S_3	Source (input) terminal for switch 3
12	V_{REF}	Logic reference voltage
13	V+	Positive power supply terminal (substrate)
14	S_2	Source (input) terminal for switch 2
15	D_2	Drain (output) terminal for switch 2
16	IN_2	Logic control for switch 2

Test Circuits



NOTE: All channels are turned off by high "1" logic inputs and all channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the minimum range for switching properly. Peak input current required for transition is typically -120μA.

FIGURE 5.

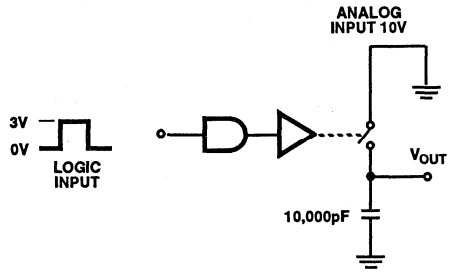
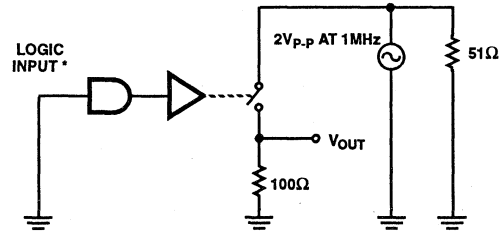


FIGURE 6.



* Pull Down Resistor must be ≤ 2kΩ.

FIGURE 7.

Typical Applications

Using the V_{REF} Terminal

The DG200 and DG201 have an internal voltage divider setting the TTL threshold on the input control lines for V+ equal to +15V. The schematic shown in Figure 8 with nominal resistor values, gives approximately 2.4V on the V_{REF} pin. As the TTL input signal goes from +0.8V to +2.4V, Q1 and Q2 switch states to turn the switch ON and OFF.

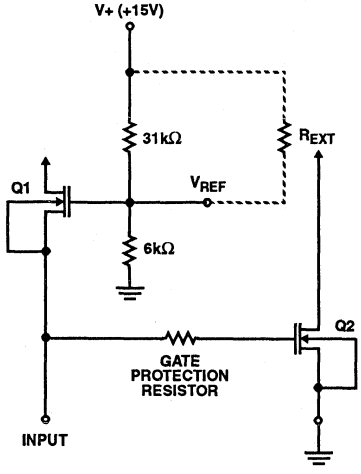


FIGURE 8.

If the power supply voltage is less than +15V, then a resistor must be added between V+ and the V_{REF} pin, to restore +2.4V at V_{REF}. The table shows the value of this resistor for various supply voltages, to maintain TTL compatibility. If CMOS logic levels on a +5V supply are being used, the threshold shifts are less critical, but a separate column of suitable values is given in the table. For logic swings of -5V to + 5V, no resistor is needed.

In general, the "low" logic level should be <0.8V to prevent Q1 and Q2 from both being ON together (this will cause incorrect switch function).

TABLE 1.

V+ SUPPLY (V)	TTL RESISTOR (kΩ)	CMOS RESISTOR (kΩ)
+15	-	-
+12	100	-
+10	51	-
+9	(34)	34
+8	(27)	27
+7	18	18

Metallization Topology

DIE DIMENSIONS:
74 x 77 x 14 ± 1mils

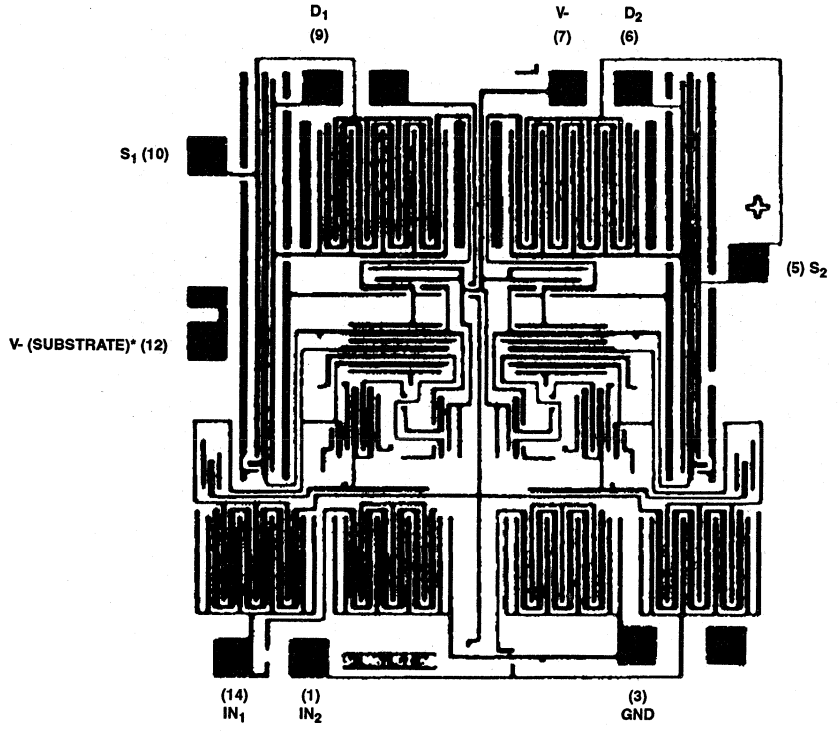
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2/Si_3N_4
SiO_2 Thickness: 7kÅ ± 1.4kÅ
Si_3N_4 Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
1×10^5 A/cm^2

Metallization Mask Layout

DG200



* Backside of Chip is V+

Metallization Topology

DIE DIMENSIONS:
94 x 101 x 14 ± 1mils

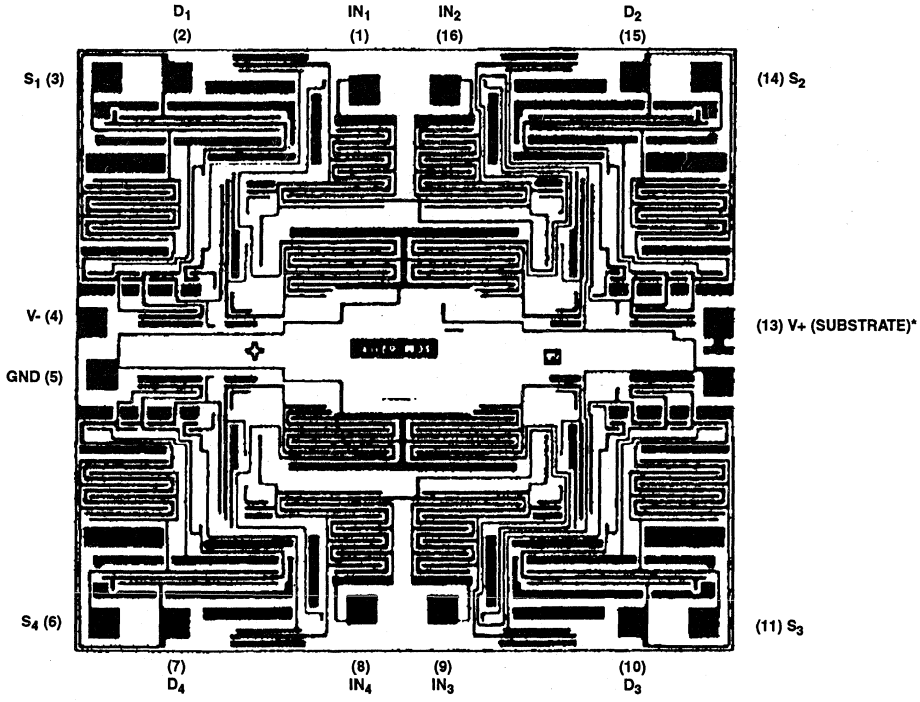
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: SiO_2/Si_3N_4
SiO_2 Thickness: 7kÅ ± 1.4kÅ
Si_3N_4 Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
1×10^5 A/cm^2

Metallization Mask Layout

DG201



* Backside of Chip is V+

HARRIS SEMICONDUCTOR

DG201A, DG202

Quad SPST CMOS Analog Switches

December 1993

Features

- ±15V Input Signal Range
- Low $R_{DS(ON)}$ (≤175Ω)
- TTL, CMOS Compatible
- Latch Proof
- True Second Source
- 44V Maximum Supply Ratings
- Logic Inputs Accept Negative Voltages

Description

The DG201A (normally open) and DG202 (normally closed) quad SPST analog switches are designed using Harris' 44V CMOS process. These bidirectional switches are latch-proof and feature break-before-make switching. Designed to block signals up to 30V peak-to-peak in the OFF state, the DG201A and DG202 offer the advantages of low on resistance (≤175Ω), wide input signal range (±15V) and provide both TTL and CMOS compatibility.

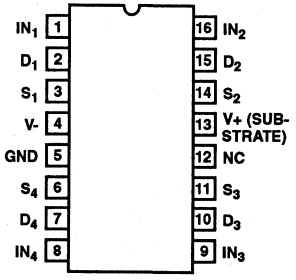
The DG201A and DG202 are specification and pinout compatible with the industry standard devices.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG201AAK	-55°C to +125°C	16 Lead Ceramic DIP
DG201ABK	-25°C to +85°C	16 Lead Ceramic DIP
DG201AAK/883B	-55°C to +125°C	16 Lead Ceramic DIP
DG201ABY	-25°C to +85°C	16 Lead SOIC (W)
DG201ACK	0°C to +70°C	16 Lead Ceramic DIP
DG201ACJ	0°C to +70°C	16 Lead Plastic DIP
DG201ACY	0°C to +70°C	16 Lead SOIC (W)
DG202AK	-55°C to +125°C	16 Lead Ceramic DIP
DG202AK/883B	-55°C to +125°C	16 Lead Ceramic DIP
DG202BK	-25°C to +85°C	16 Lead Ceramic DIP
DG202CK	0°C to +70°C	16 Lead Ceramic DIP
DG202CJ	0°C to +70°C	16 Lead Plastic DIP

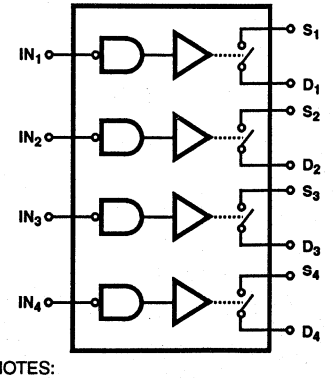
Pinout

DG201A, DG202
(CDIP, PDIP, SOIC)
TOP VIEW

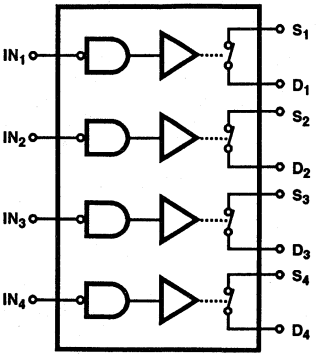


Functional Diagrams

DG201A



DG202



NOTES:
1. Four SPST switches per package.
2. Switches shown for logic "1" input

TRUTH TABLE

LOGIC	DG201A	DG202
0	ON	OFF
1	OFF	ON

Logic "0" ≤0.8V, Logic "1" ≥ 2.4V

9 SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3117

Absolute Maximum Ratings

V+ to V- 44V
V- to Ground ..... -25V
V_{IN} to Ground (Note 1) ..... (V- -2V), (V+ +2V)
V_S or V_D to V+ (Note 1) ..... +2, (V- -2V)
V_S or V_D to V- (Note 1) ..... -2, (V+ +2V)
Current, any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max) 70mA
Lead Temperature (Soldering 10s) ..... +300°C
Storage Temperature Range
C Suffix ..... -65°C to +125°C
A & B Suffix ..... -65°C to +150°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	80°C/W	24°C/W
Plastic DIP Package	100°C/W	-
SOIC Package	100°C/W	-

Junction Temperature
Ceramic DIP Package ..... +175°C
Plastic DIP Package ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = 15V, V- = -15V, GND = 0V, T_A = Over Operating Temperature Range

PARAMETERS	TEST CONDITIONS		DG201AA/DG202A MIN	DG201AA/DG202A (NOTE 2) TYP	DG201AA/DG202A MAX	DG201AB, C/DG202B, C MIN	DG201AB, C/DG202B, C (NOTE 2) TYP	DG201AB, C/DG202B, C MAX	UNITS
DYNAMIC CHARACTERISTICS									
Turn-On Time, t_{ON}	See Figure 1		-	480	600	-	480	600	ns
Turn-Off Time, t_{OFF}	See Figure 1		-	370	450	-	370	450	ns
Charge Injection, Q	C_L = 1000pF, R_S = 0, V_S = 0V		-	20	-	-	20	-	pC
Source OFF Capacitance, $C_{S(OFF)}$	f = 140kHz, V_{IN} = 5V, V_S = 0V		-	5.0	-	-	5.0	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	f = 140kHz, V_{IN} = 5V, V_D = 0V		-	5.0	-	-	5.0	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$	f = 140kHz, V_{IN} = 5V, $V_S = V_D$ = 0V		-	16	-	-	16	-	pF
OFF Isolation, OIRR	V_{IN} = 5V, Z_L = 75Ω, V_S = 2.0V, f = 100kHz		-	70	-	-	70	-	dB
Crosstalk (Channel to Channel), CCRR			-	90	-	-	90	-	dB
INPUT									
Input Current with Voltage High, I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004	-	-1.0	-0.0004	-	µA
	V_{IN} = 15V		-	0.003	1.0	-	0.003	1.0	µA
Input Current with Voltage Low, I_{INL}	V_{IN} = 0V		-1.0	-0.0004	-	-1.0	-0.0004	-	µA
SWITCH									
Analog Signal Range, V_{ANALOG}			-15	-	15	-15	-	15	V
Drain Source On Resistance, $R_{DS(ON)}$	V_D = ±10V, V_{IN} = 0.8V (DG201A) I_S = 1mA, V_{IN} = 2.4V (DG202)		-	115	175	-	115	200	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 2.4V (DG201A) V_{IN} = 0.8V (DG202)	V_S = 14V, V_D = -14V	-	0.01	1.0	-	0.01	5.0	nA
		V_S = -14V, V_D = 14V	-1.0	-0.02	-	-5.0	-0.02	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	0.01	1.0	-	0.01	5.0	nA
		V_S = 14V, V_D = -14V	-1.0	-0.02	-	-5.0	-0.02	-	nA
Drain ON Leakage Current, $I_{D(ON)}$ (Note 4)	V_{IN} = 0.8V (DG201A) V_{IN} = 2.4V (DG202)	$V_D = V_S$ = 14V	-	0.1	1.0	-	0.1	5.0	µA
		$V_D = V_S$ = -14V	-1.0	-0.15	-	-5.0	-0.15	-	µA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I+	All Channels ON or OFF		-	0.9	2	-	0.9	2	mA
Negative Supply Current, I-			-1	-0.3	-	-1	-0.3	-	mA

Electrical Specifications V+ = 15V, V- = -15V, GND = 0V, T_A = Over Operating Temperature Range **(Continued)**

PARAMETERS	TEST CONDITIONS		DG201AA/DG202A MIN	DG201AA/DG202A (NOTE 2) TYP	DG201AA/DG202A MAX	DG201AB, C/DG202B, C MIN	DG201AB, C/DG202B, C (NOTE 2) TYP	DG201AB, C/DG202B, C MAX	UNITS
INPUT									
Input Current with Voltage High, I_{INH}	V_{IN} = 2.4V		-10	-	-	-10	-	-	µA
	V_{IN} = 15V		-	-	10	-	-	10	µA
Input Current with Voltage Low, I_{INL}	V_{IN} = 0V		-10	-	-	-10	-	-	µA
SWITCH									
Analog Signal Range, V_{ANALOG}			-15	-	15	-15	-	15	V
Drain Source On Resistance, $R_{DS(ON)}$	V_D = ±10V, V_{IN} = 0.8V (DG201A) I_S = 1mA, V_{IN} = 2.4V (DG202)		-	-	250	-	-	250	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 2.4V (DG201A) V_{IN} = 0.8V (DG202)	V_S = 14V, V_D = -14V	-	-	100	-	-	100	nA
		V_S = -14V, V_D = 14V	-100	-	-	-100	-	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	-	100	-	-	100	nA
		V_S = 14V, V_D = -14V	-100	-	-	-100	-	-	nA
Drain ON Leakage Current, $I_{D(ON)}$ (Note 4)	V_{IN} = 0.8V (DG201A) V_{IN} = 2.4V (DG202)	V_D = V_S = 14V	-	-	200	-	-	200	µA
		V_D = V_S = -14V	-200	-	-	-200	-	-	µA

NOTES:

1. Signals on V_S, V_D, or V_{IN} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. $I_{D(ON)}$ is leakage from driver into ON switch.

Test Circuits

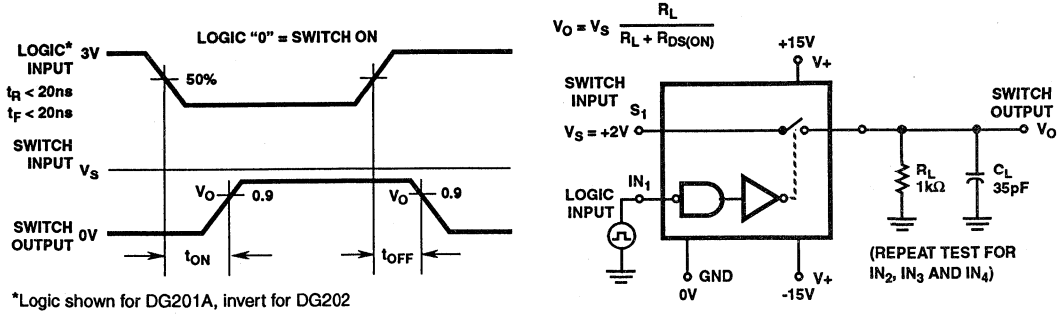
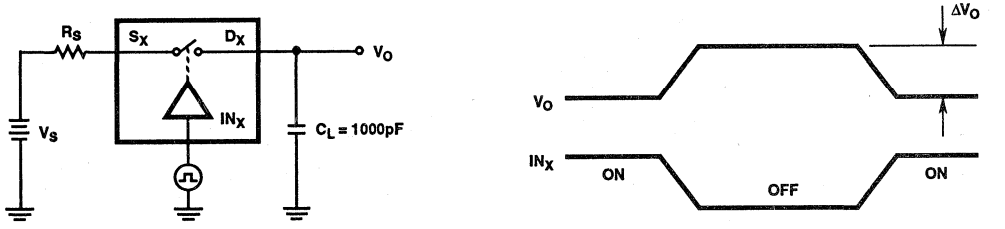


FIGURE 1. T_{ON} AND T_{OFF} SWITCHING TEST



NOTES:

1. ΔV_O = Measured voltage error due to charge injection.
2. The error voltage in coulombs is $\Delta Q = C_L \times \Delta V_O$.

FIGURE 2. CHARGE INJECTION TEST CIRCUIT

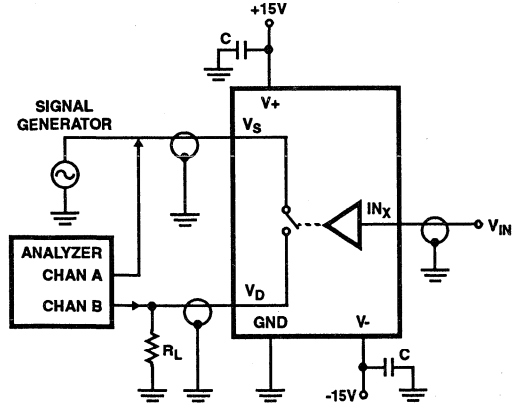


FIGURE 3. OFF ISOLATION TEST CIRCUIT

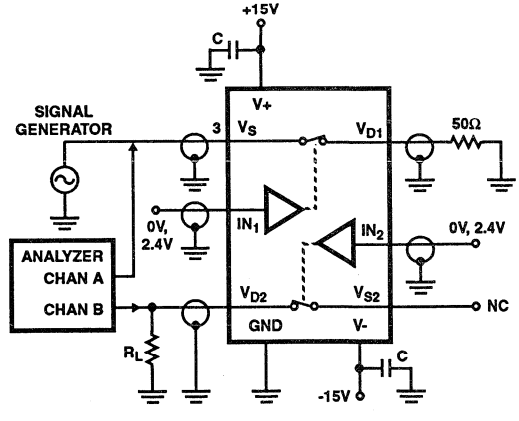


FIGURE 4. CHANNEL TO CHANNEL CROSSTALK TEST CIRCUIT

DG211, DG212

December 1993

SPST 4 Channel Analog Switch

Features

- **Switches ±15V Analog Signals**
- **TTL Compatibility**
- **Logic Inputs Accept Negative Voltages**
- **R_{ON} ≤175Ω**

Description

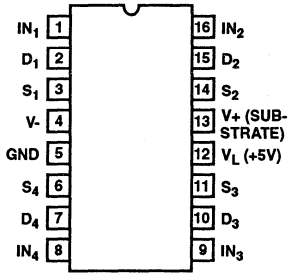
The DG211 and DG212 are low cost, CMOS monolithic, Quad SPST analog switches. These can be used in general purpose switching applications for communications, instrumentation, process control and computer peripheral equipment. Both devices provide true bidirectional performance in the ON condition and will block signals to 30V peak-to-peak in the OFF condition. The DG211 and DG212 differ only in that the digital control logic is inverted, as shown in the truth table.

Ordering Information

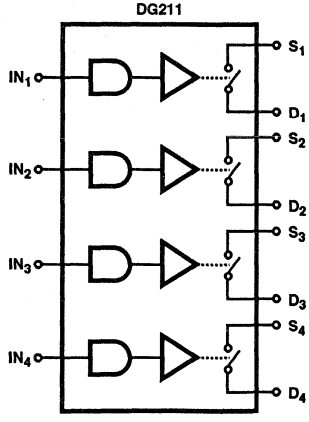
PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG211CJ	0°C to +70°C	16 Lead Plastic DIP
DG212CJ	0°C to +70°C	16 Lead Plastic DIP
DG211CY	0°C to +70°C	16 Lead SOIC (N)
DG212CY	0°C to +70°C	16 Lead SOIC (N)

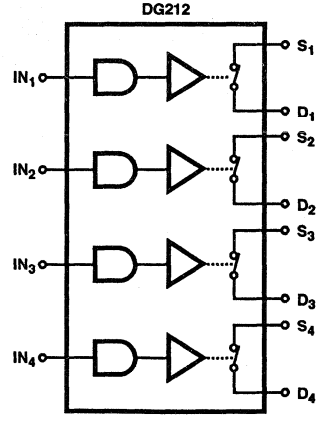
Pinout

DG211, DG212
(PDIP, SOIC)
TOP VIEW



Functional Diagrams





NOTES:
1. Four SPST switches per package.
2. Switches shown for logic "1" input

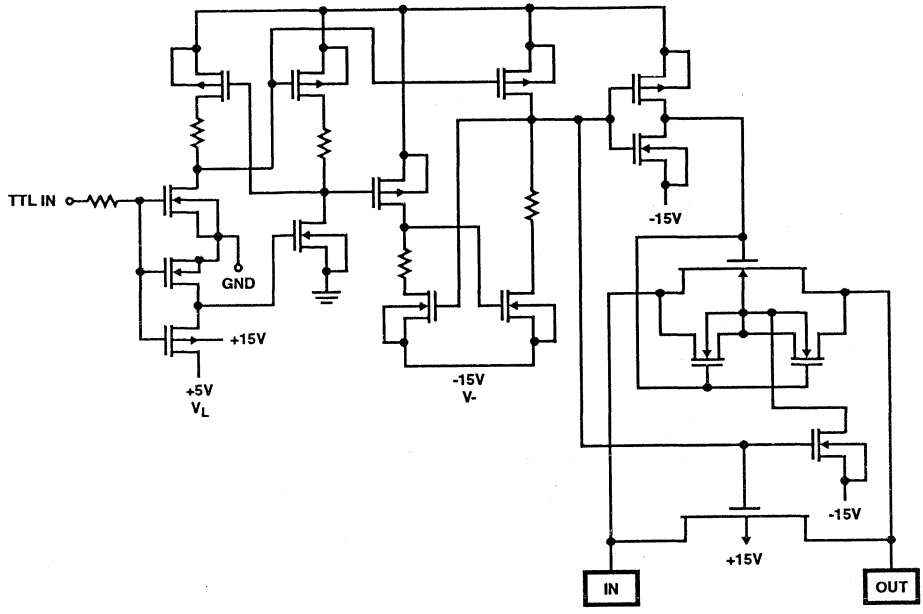
TRUTH TABLE

LOGIC	DG211	DG212
0	ON	OFF
1	OFF	ON

Logic "0" ≤0.8V, Logic "1" ≥ 2.4V

Schematic Diagram

DG211 ($^1/_4$ AS SHOWN)



Absolute Maximum Ratings

V+ to V- 44V
V_{IN} to Ground ..... V-, V+
V_L to Ground ..... -0.3V, 25V
V_S or V_D to V+ ..... 0, -36V
V_S or V_D to V- 0, 36V
V+ to Ground 25V
V- to Ground ..... -25V
Current, any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max) 70mA
Lead Temperature (Soldering 10s) ..... +300°C
Storage Temperature Range ..... -65°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA}
Plastic DIP Package	100°C/W
SOIC Package	120°C/W
Junction Temperature	+150°C
Operating Temperature	0°C to +70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +15V, V- = -15V, V_L = +5V, GND, T_A = +25°C

PARAMETERS	TEST CONDITIONS		(NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-On Time, t_{ON}	See Figure 1 V_S = 10V, R_L = 1kΩ, C_L = 35pF		-	460	1000	ns
Turn-Off Time, t_{OFF1}			-	360	500	ns
t_{OFF2}			-	450	-	ns
Source OFF Capacitance, $C_{S(OFF)}$	V_S = 0V, V_{IN} = 5V, f = 1MHz (Note 2)		-	5	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	V_D = 0V, V_{IN} = 5V, f = 1MHz (Note 2)		-	5	-	pF
Channel ON Capacitance, $C_{D+S(ON)}$	V_D = V_S = 0V, V_{IN} = 0V, f = 1MHz (Note 2)		-	16	-	pF
OFF Isolation, OIRR (Note 4)	V_{IN} = 5V, R_L = 1kΩ, C_L = 15pF, V_S = $1V_{RMS}$, f = 100kHz (Note 2)		-	70	-	dB
Crosstalk (Channel to Channel), CCRR			-	90	-	dB
INPUT						
Input Current with Voltage High, I_{INH}	V_{IN} = 2.4V		-1.0	-0.0004	-	µA
	V_{IN} = 15V		-	0.003	1.0	µA
Input Current with Voltage Low, I_{INL}	V_{IN} = 0V		-1.0	-0.0004	-	µA
SWITCH						
Analog Signal Range, V_{ANALOG}	V- = -15V, V_L = +5V		-15	-	15	V
Drain Source On Resistance, $R_{DS(ON)}$	V_D = ±10V, V_{IN} = 2.4V (DG212) I_S = 1mA, V_{IN} = 0.8V (DG211)		-	150	175	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 2.4V (DG211) V_{IN} = 0.8V (DG212)	V_S = 14V, V_D = -14V	-	0.01	5.0	nA
		V_S = -14V, V_D = 14V	-5.0	-0.02	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	0.01	5.0	nA
		V_S = 14V, V_D = -14V	-5.0	-0.02	-	nA
Drain ON Leakage Current, $I_{D(ON)}$ (Note 3)	V_S = V_D = -14V, V_{IN} = 0.8V (DG211) V_{IN} = 2.4V (DG212)		-	0.1	5.0	nA
			-5.0	-0.15	-	nA

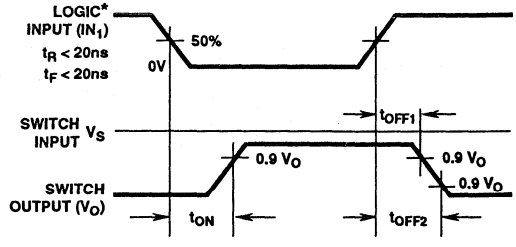
Electrical Specifications V+ = +15V, V- = -15V, V_L = +5V, GND, T_A = +25°C **(Continued)**

PARAMETERS	TEST CONDITIONS	(NOTE 1) MIN	(NOTE 2) TYP	MAX	UNITS
POWER SUPPLY CHARACTERISTICS					
Positive Supply Current, I+	V_{IN} = 0V and 2.4V	-	0.1	10	µA
Negative Supply Current, I-		-	0.1	10	µA
Logic Supply Current, I_L		-	0.1	10	µA

NOTES:
1. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
2. For design reference only, not 100% tested.
3. $I_{D(ON)}$ is leakage from driver into ON switch.
4. OFF Isolation = $20\log\frac{V_S}{V_D}$, V_S = Input to OFF switch, V_D = output
5. Switching times only sampled.

Test Circuits

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note the V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



* Logic shown for DG211. Invert for DG212.

FIGURE 1. SWITCHING TIME TEST WAVEFORMS

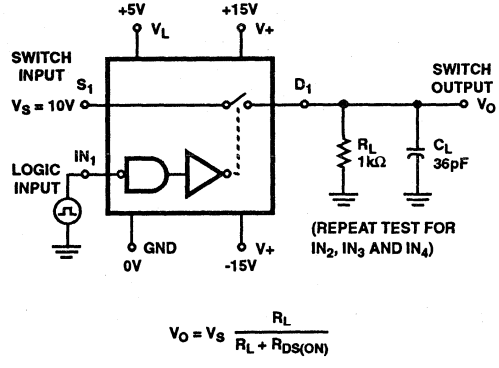


FIGURE 2. SWITCHING TIME TEST CIRCUIT

Metallization Topology

DIE DIMENSIONS:
2159µm x 2235µm

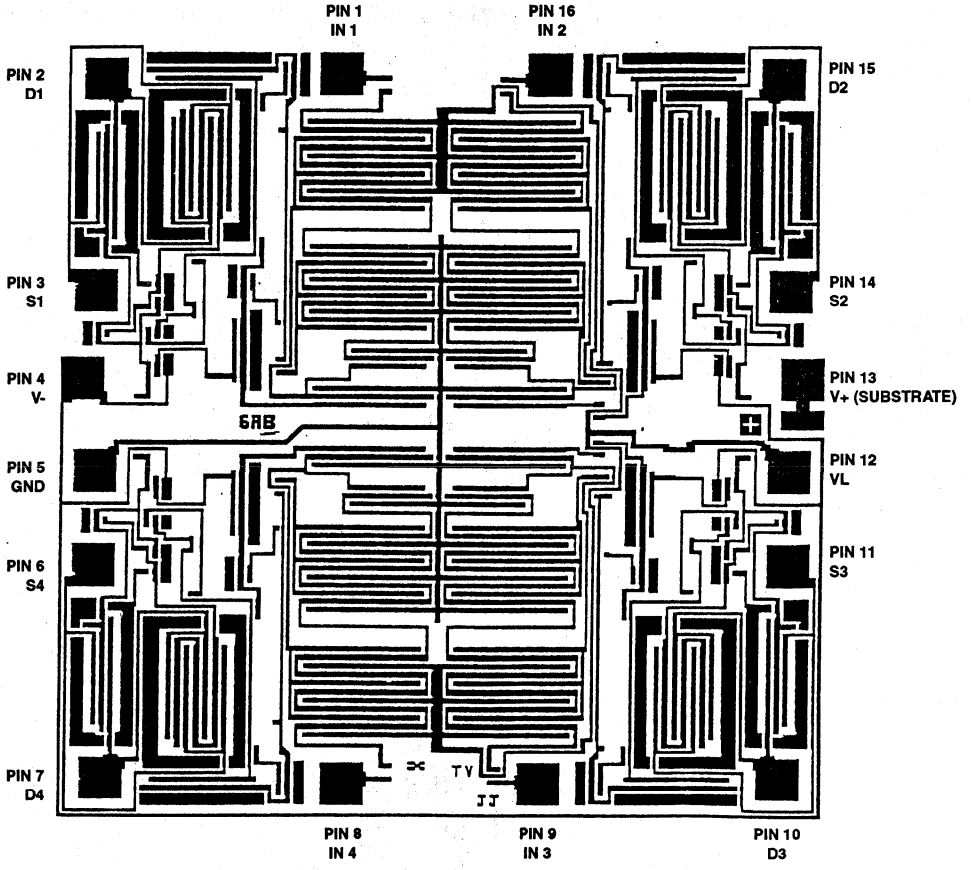
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG211, DG212



HARRIS SEMICONDUCTOR

DG300A, DG301A DG302A, DG303A

TTL Compatible CMOS Analog Switches

December 1993

Features

- Low Power Consumption
- Break-Before-Make Switching t_{OFF} 130ns, t_{ON} 150ns Typical
- TTL, CMOS Compatible
- Low $R_{DS(ON)}$ ($\leq 50\Omega$)
- Single Supply Operation
- True Second Source

Description

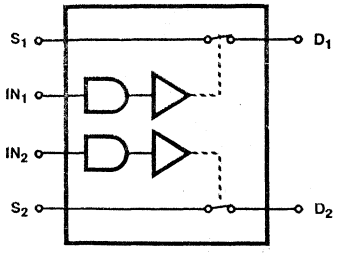
The DG300A through DG303A family of monolithic CMOS switches are truly compatible second source of the original manufacturer. The switches are latch-proof and are designed to block signals up to $30V_{P-P}$ when OFF. Featuring low leakage and low power consumption, these switches are ideally suited for precision application in instrumentation, communication, data acquisition and battery powered applications. Other key features include Break-Before-Make switching, TTL and CMOS compatibility, and low ON resistance. Single supply operation (for positive switch voltages) is possible by connecting V- to 0V.

Ordering Information

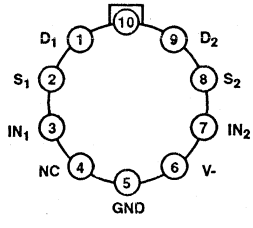
PART NUMBER	TEMPERATURE	PACKAGE
DG300AAK	-55°C to +125°C	14 Lead Ceramic DIP
DG301AAK	-55°C to +125°C	14 Lead Ceramic DIP
DG302AAK	-55°C to +125°C	14 Lead Ceramic DIP
DG303AAK	-55°C to +125°C	14 Lead Ceramic DIP
DG300ABK	-25°C to +85°C	14 Lead Ceramic DIP
DG301ABK	-25°C to +85°C	14 Lead Ceramic DIP
DG302ABK	-25°C to +85°C	14 Lead Ceramic DIP
DG303ABK	-25°C to +85°C	14 Lead Ceramic DIP
DG300ACK	0°C to +70°C	14 Lead Ceramic DIP
DG301ACK	0°C to +70°C	14 Lead Ceramic DIP
DG302ACK	0°C to +70°C	14 Lead Ceramic DIP
DG303ACK	0°C to +70°C	14 Lead Ceramic DIP
DG300ACJ	0°C to +70°C	14 Lead Plastic DIP
DG301ACJ	0°C to +70°C	14 Lead Plastic DIP
DG302ACJ	0°C to +70°C	14 Lead Plastic DIP
DG303ACJ	0°C to +70°C	14 Lead Plastic DIP
DG300AAA	-55°C to +125°C	10 Pin Metal Can
DG301AAA	-55°C to +125°C	10 Pin Metal Can
DG300ABA	-25°C to +85°C	10 Pin Metal Can
DG301ABA	-25°C to +85°C	10 Pin Metal Can
DG300ACA	0°C to +70°C	10 Pin Metal Can
DG301ACA	0°C to +70°C	10 Pin Metal Can
DG303ACY	0°C to +70°C	16 Lead SOIC (W)
DG300AAA/883B	-55°C to +125°C	10 Pin Metal Can
DG300AAK/883B	-55°C to +125°C	14 Lead Ceramic DIP
DG301AAA/883B	-55°C to +125°C	10 Pin Metal Can
DG301AAK/883B	-55°C to +125°C	14 Lead Ceramic DIP
DG302AAK/883B	-55°C to +125°C	14 Lead Ceramic DIP
DG303AAK/883B	-55°C to +125°C	14 Lead Ceramic DIP

Pinouts and Functional Diagrams

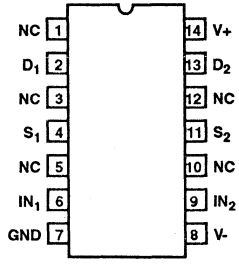
DG300A



DG300A (METAL CAN)
TOP VIEW
V+ (SUBSTRATE AND CASE)



DG300A (CDIP, PDIP)
TOP VIEW



TRUTH TABLE

LOGIC	SWITCH
0	OFF
1	ON

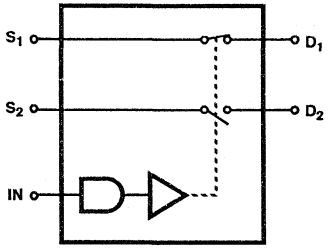
Logic "0" $\leq$ 0.8V, Logic "1" $\geq$ 4.0V; Two SPST switches per package (switches shown for Logic "1" input)

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

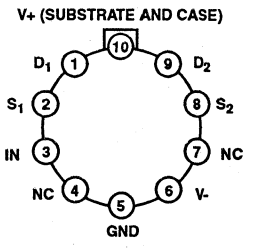
File Number **3119**

Pinouts and Functional Diagrams (Continued)

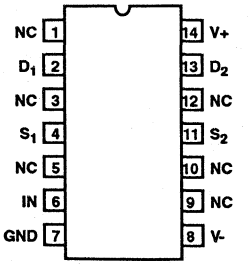
DG301A



DG301A (METAL CAN)
TOP VIEW



DG301A (CDIP, PDIP)
TOP VIEW

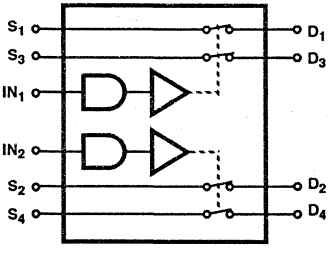


TRUTH TABLE

LOGIC	SWITCH 1	SWITCH 2
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8V, Logic "1" ≥ 4.0V; One SPDT switch per package (switches shown for Logic "1" input)

DG302A

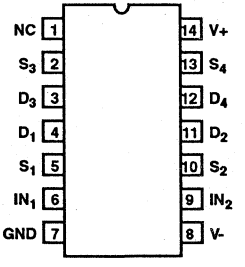


TRUTH TABLE

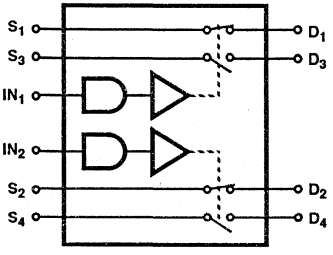
LOGIC	SWITCH
0	OFF
1	ON

Logic "0" ≤ 0.8V, Logic "1" ≥ 4.0V; Two DPST switch per package (switches shown for Logic "1" input)

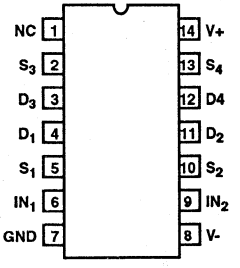
DG302A (CDIP, PDIP)
TOP VIEW



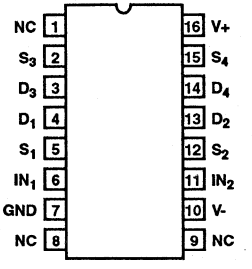
DG303A



DG303A (CDIP, PDIP)
TOP VIEW



DG303ACY (SOIC)
TOP VIEW



TRUTH TABLE

LOGIC	SWITCH 1 AND 2	SWITCH 3 AND 4
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8V, Logic "1" ≥ 4.0V; Two SPDT switch per package (switches shown for Logic "1" input)

Absolute Maximum Ratings

V+ to V- ..... +44.0V
V- to GND ..... -25V
V_{IN} to Ground (Note 1) ..... (V- - 2V), (V+ + 2V)
V_S or V_D to V+ (Note 1) ..... +2, (V- - 2V)
V_S or V_D to V- (Note 1) ..... -2, (V+ + 2V)
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 30mA
Peak Current, S or D
(Pulsed at 1ms, 10% Duty Cycle Max) 100mA
Storage Temperature Range
(C Suffix) ..... -65°C to +125°C
(A & B Suffix) ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... 300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
SOIC	100°C/W	-
Plastic DIP	145°C/W	-
Ceramic DIP	80°C/W	24°C/W
Metal Can	136°C/W	65°C/W

Junction Temperature
Ceramic DIP, Metal Can ..... +175°C
Plastic DIP, SOIC ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... ±15V
Operating Temperature Range
(C Suffix) ..... 0°C to +70°C
(B Suffix) ..... -25°C to +85°C
(A Suffix) ..... -55°C to +125°C

Input Low Voltage ..... 0.8V MAX
Input High Voltage ..... 4.0V MIN
Input Rise and Fall Time ..... <20ns

Electrical Specifications V+ = +15V, V- = -15V, GND = 0V, T_A = +25°C

PARAMETER	TEST CONDITION		DG300A - DG303AA MIN	DG300A - DG303AA (NOTE 6) TYP	DG300A - DG303AA MAX	DG300A - DG303AB/C MIN	DG300A - DG303AB/C (NOTE 6) TYP	DG300A - DG303AB/C MAX	UNITS
DYNAMIC CHARACTERISTICS									
Turn-ON Time, t_{ON}	See Figure 3		-	150	300	-	150	-	ns
Turn-OFF Time, t_{OFF}	See Figure 3		-	130	250	-	130	-	ns
Break-Before-Make Interval, t_{ON} - t_{OFF}	See Figure 2, DG301A/DG303A		-	50	-	-	50	-	ns
Charge Injection, Q	C_L = 10nF, R_S = 0, V_S = 0		-	3	-	-	3	-	mV
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz, V_{IN} = 0.8V or V_{IN} = 4.0V	V_S = 0	-	14	-	-	14	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$		V_D = 0	-	14	-	-	14	-	pF
Channel ON Capacitance, $C_{D(ON)}$ + $C_{S(ON)}$		V_S = V_D = 0	-	40	-	-	40	-	pF
Input Capacitance, C_{IN}	f = 1MHz	V_{IN} = 0	-	6	-	-	6	-	pF
		V_{IN} = 15V	-	7	-	-	7	-	pF
OFF Isolation (Note 8)	V_{IN} = 0, R_L = 1k, V_S = $1V_{RMS}$, f = 500kHz		-	62	-	-	62	-	dB
Crosstalk (Channel-to-Channel)			-	74	-	-	74	-	dB
INPUT									
Input Current with Voltage High, I_{INH}	V_{IN} = 5.0V		-1	-0.001	-	-1	-0.001	-	µA
	V_{IN} = 15.0V		-	0.001	1	-	0.001	1	µA
Input Current with Voltage Low, I_{INL}	V_{IN} = 0V		-1	-0.001	-	-1	-0.001	-	µA
ANALOG SWITCH									
Analog Signal Range, V_{ANALOG}	I_S = 10mA, V_{IN} = 0.8V or 4V		-15	-	15	-15	-	15	V

Electrical Specifications V+ = +15V, V- = -15V, GND = 0V, T_A = +25°C **(Continued)**

PARAMETER	TEST CONDITION		DG300A - DG303AA MIN	DG300A - DG303AA (NOTE 6) TYP	DG300A - DG303AA MAX	DG300A - DG303AB/C MIN	DG300A - DG303AB/C (NOTE 6) TYP	DG300A - DG303AB/C MAX	UNITS
Drain-Source ON Resistance, $R_{DS(ON)}$	V_{IN} = 0.8V or V_{IN} = 4.0V	I_S = -10mA, V_D = 10V	-	30	50	-	30	50	Ω
		I_S = 10mA, V_D = -10V	-	30	50	-	30	50	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 0.8V or V_{IN} = 4.0V	V_S = 14V, V_D = -14V	-	0.1	1	-	0.1	5	nA
		V_S = -14V, V_D = 14V	-1	-0.1	-	-5	-0.1	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$	V_{IN} = 0.8V or V_{IN} = 4.0V	V_S = -14V, V_D = 14V	-	0.1	1	-	0.1	5	nA
		V_S = 14V, V_D = -14V	-1	-0.1	-	-5	-0.1	-	nA
Drain ON Leakage Current, $I_{D(ON)}$	V_{IN} = 0.8V or V_{IN} = 4.0V	V_D = V_S = 14V	-	0.1	1	-	0.1	5	nA
		V_D = V_S = -14V	-2	-0.1	-	-5	-0.1	-	nA
POWER SUPPLIES									
Positive Supply Current, I+	V_{IN} = 4V (One Input) (All Others = 0)		-	0.23	0.5	-	0.23	0.5	mA
Negative Supply Current, I-			-10	-0.001	-	-10	-0.001	-	µA
Positive Supply Current, I+	V_{IN} = 0.8V (All Inputs)		-	0.001	10	-	0.001	10	µA
Negative Supply Current, I-			-10	-0.001	-	-10	-0.001	-	µA

Electrical Specifications V+ = +15V, V- = -15V, GND = 0V, T_A = Over Temperature Range

PARAMETER	TEST CONDITION		DG300A - DG303AA MIN	DG300A - DG303AA (NOTE 6) TYP	DG300A - DG303AA MAX	DG300A - DG303AB/C MIN	DG300A - DG303AB/C (NOTE 6) TYP	DG300A - DG303AB/C MAX	UNITS
INPUT									
Input Current with Voltage High, I_{INH}	V_{IN} = 5.0V		-1	-	-	-	-	-	µA
	V_{IN} = 15.0V		-	-	1	-	-	-	µA
Input Current with Voltage Low, I_{INL}	V_{IN} = 0V		-1	-	-	-	-	-	µA
ANALOG SWITCH									
Analog Signal Range, V_{ANALOG}	I_S = 10mA, V_{IN} = 0.8V or 4V		-15	-	15	-15	-	15	V
Drain-Source ON Resistance, $R_{DS(ON)}$	V_{IN} = 0.8V or V_{IN} = 4.0V	I_S = -10mA, V_D = 10V	-	-	75	-	-	75	Ω
		I_S = 10mA, V_D = -10V	-	-	75	-	-	75	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 0.8V or V_{IN} = 4.0V	V_S = 14V, V_D = -14V	-	-	100	-	-	100	nA
		V_S = -14V, V_D = 14V	-100	-	-	-100	-	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$	V_{IN} = 0.8V or V_{IN} = 4.0V	V_S = -14V, V_D = 14V	-	-	100	-	-	100	nA
		V_S = 14V, V_D = -14V	-100	-	-	-100	-	-	nA
Drain ON Leakage Current, $I_{D(ON)}$	V_{IN} = 0.8V or V_{IN} = 4.0V	V_D = V_S = 14V	-	-	100	-	-	100	nA
		V_D = V_S = -14V	-200	-	-	-200	-	-	nA

Electrical Specifications V+ = +15V, V- = -15V, GND = 0V, T_A = Over Temperature Range **(Continued)**

PARAMETER	TEST CONDITION	DG300A - DG303AA			DG300A - DG303AB/C			UNITS
		MIN	(NOTE 6) TYP	MAX	MIN	(NOTE 6) TYP	MAX	
POWER SUPPLIES								
Positive Supply Current, I+	V_{IN} = 4V (One Input) (All Others = 0)	-	-	1	-	-	-	mA
Negative Supply Current, I-		-100	-	-	-	-	-	µA
Positive Supply Current, I+	V_{IN} = 0.8V (All Inputs)	-	-	100	-	-	-	µA
Negative Supply Current, I-		-100	-	-	-	-	-	µA

NOTES:

1. Signals on V_S, V_D or V_{IN} exceeding V+ or V- will be clamped by internal diodes. Limit diode toward current to maximum current ratings.
2. Device mounted with all leads soldered or welded to PC board.
3. Derate 11mW/°C above +75°C
4. Derate 6.5mW/°C above +25°C.
5. Derate 6mW/°C above +75°C.
6. For design only, not 100% tested.
7. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
8. OFF isolation = 20 log V_S/V_D, where V_S = input to OFF switch, and V_D = output.

Pin Description

PIN	SYMBOL	DESCRIPTION
DG300A		
1	NC	No Connection
2	D_1	Drain (Output) terminal for Switch 1
3	NC	No Connection
4	S_1	Source (Input) terminal for Switch 1
5	NC	No Connection
6	IN_1	Logic Control for Switch 1
7	GND	Ground Terminal (Logic Common)
8	V-	Negative Power Supply Terminal
9	IN_2	Logic Control for Switch 2
10	NC	No Connection
11	NC	No Connection
12	S_2	Source (Input) terminal for Switch 2
13	D_2	Drain (Output) terminal for Switch 2
14	V+	Positive Power Supply Terminal
DG301A		
1	NC	No Connection
2	D_1	Drain (Output) terminal for Switch 1
3	NC	No Connection
4	S_1	Source (Input) terminal for Switch 1
5	IN	Logic Control for Switches
6	GND	Ground Terminal (Logic Common)
7	V-	Negative Power Supply Terminal
8	NC	No Connection
9	NC	No Connection
10	S_2	Source (Input) terminal for Switch 2
11	NC	No Connection
12	D_2	Drain (Output) terminal for Switch 2
13	NC	No Connection
14	V+	Positive Power Supply Terminal
DG302A, DG303A		
1	NC	No Connection
2	S_3	Source (Input) terminal for Switch 3
3	D_3	Drain (Output) terminal for Switch 3
4	D_1	Drain (Output) terminal for Switch 1
5	S_1	Source (Input) terminal for Switch 1
6	IN_1	Logic Control for Switch 1
7	GND	Ground Terminal (Logic Common)
8	V-	Negative Power Supply Terminal
9	IN_2	Logic Control for Switch 2
10	S_2	Source (Input) terminal for Switch 2
11	D_2	Drain (Output) terminal for Switch 2
12	D_4	Drain (Output) terminal for Switch 4
13	S_4	Source (Input) terminal for Switch 4
14	V+	Positive Power Supply Terminal

Test Circuits

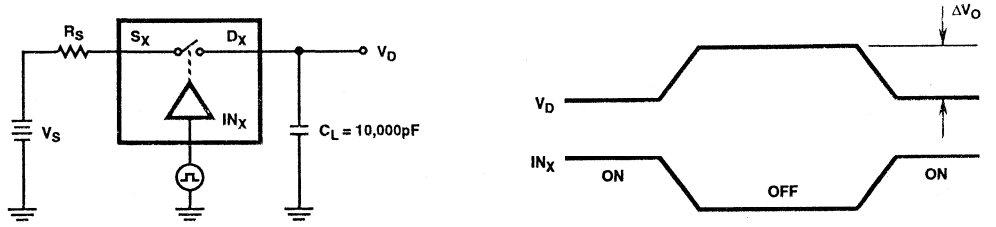


FIGURE 1. CHARGE INJECTION TEST CIRCUIT

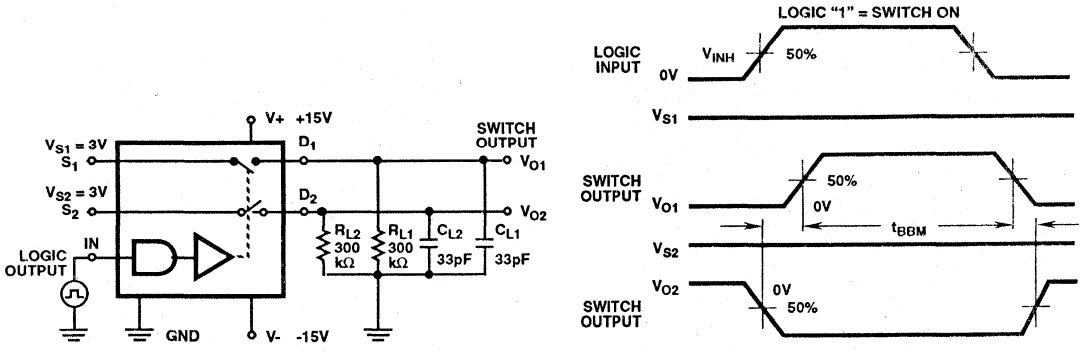


FIGURE 2. BREAK-BEFORE MAKE TEST CIRCUIT (DG301A, DG303A)

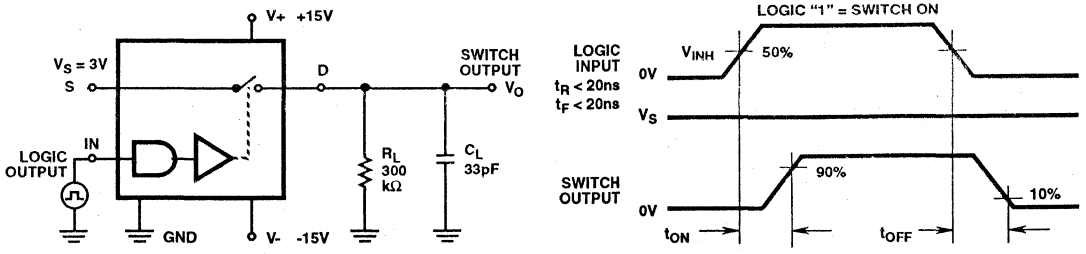


FIGURE 3. t_{ON} and t_{OFF} TEST CIRCUIT

Die Characteristics

DIE DIMENSIONS:
89 x 99 x 12 ± 2mils

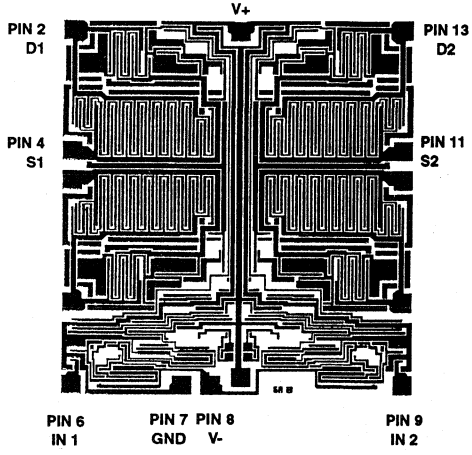
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG Over Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

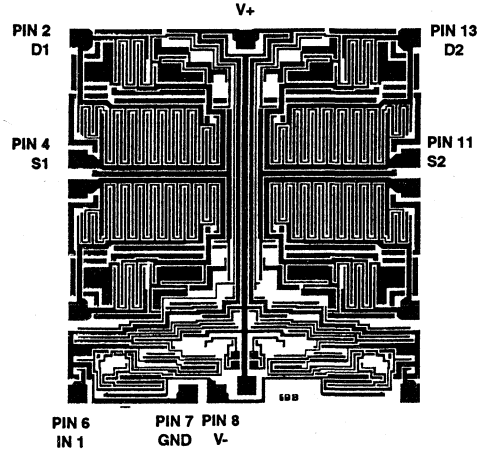
WORST CASE CURRENT DENSITY:
1×10^5 A/cm^2

Metallization Mask Layout

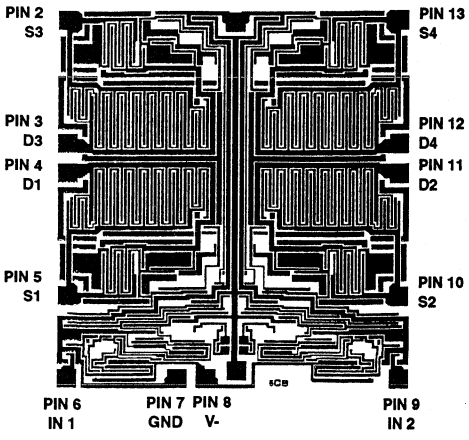
DG300A



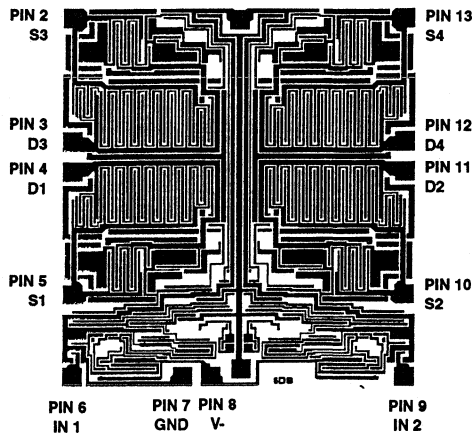
DG301A



DG302A



DG303A



DG308A, DG309

Quad Monolithic SPST CMOS Analog Switches

December 1993

Features

- **Low Power Consumption**
- **CMOS Compatible**
- **±15V Analog Signal Range**
- **Single or Dual Supply Capability**
- **Alternate Source**

Description

The DG308A and DG309 quad monolithic SPST CMOS switches are latch proof and are designed to block signals up to 30V peak-to-peak when OFF. Featuring low ON resistance, low power consumption, and rail-to-rail analog signal range, these switches are ideally suited for high speed switching applications in communications, instrumentation and process control. The DG308A "normally-closed" and DG309 "normally-open" switches have single and dual supply capability. The input thresholds are CMOS compatible.

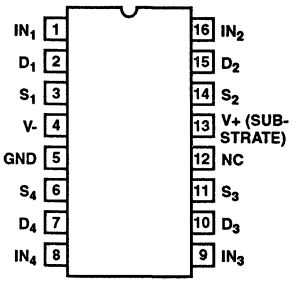
The DG308A and DG309 switches are available over commercial, industrial, and military temperature ranges.

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
DG308AAK	-55°C to +125°C	16 Lead Ceramic DIP
DG308ABK	-25°C to +85°C	16 Lead Ceramic DIP
DG308ACK	0°C to +70°C	16 Lead Ceramic DIP
DG308ACJ	0°C to +70°C	16 Lead Plastic DIP
DG308ACY	0°C to +70°C	16 Lead SOIC (W)
DG308AAK/883B	-55°C to +125°C	16 Lead Ceramic DIP
DG309AK	-55°C to +125°C	16 Lead Ceramic DIP
DG309BK	-25°C to +85°C	16 Lead Ceramic DIP
DG309CK	0°C to +70°C	16 Lead Ceramic DIP
DG309CJ	0°C to +70°C	16 Lead Plastic DIP
DG309CY	0°C to +70°C	16 Lead SOIC (W)
DG309AK/883B	-55°C to +125°C	16 Lead Ceramic DIP

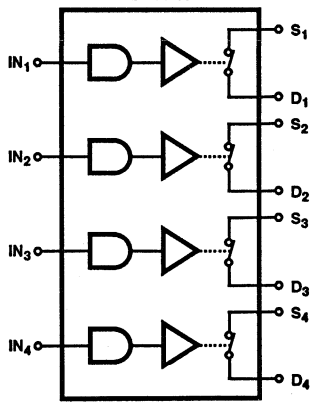
Pinout

DG308A, DG309
(CDIP, PDIP, SOIC)
TOP VIEW

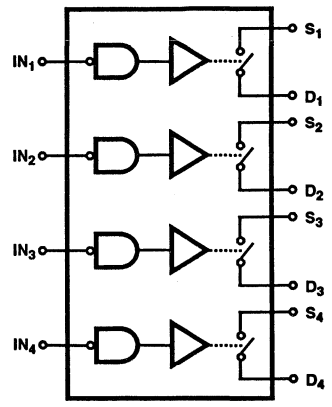


Functional Diagrams

DG308A



DG309



NOTES:
1. Four SPST switches per package.
2. Switches shown for logic "1" input

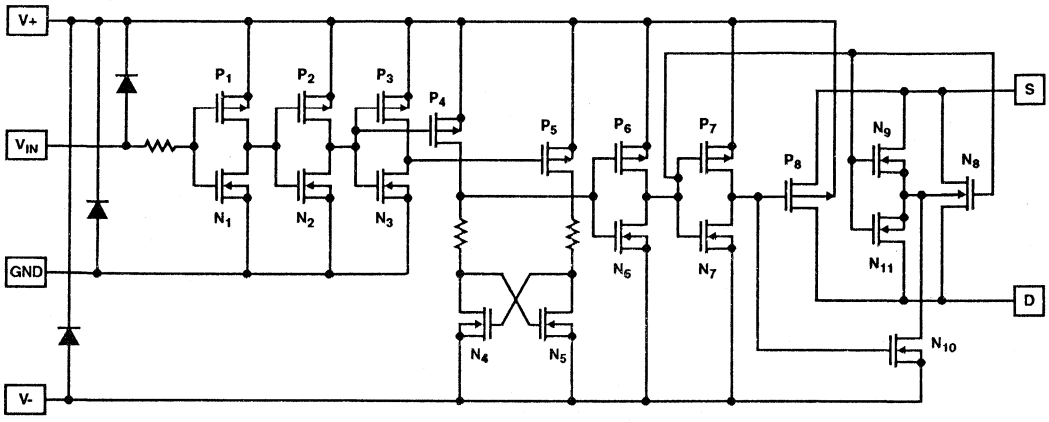
TRUTH TABLE

LOGIC	DG308A	DG309
0	OFF	ON
1	ON	OFF

Logic "0" ≤3.5V, Logic "1" ≥ 11V

Typical Schematic Diagram (One Channel)

DG308A



Absolute Maximum Ratings

V+ to V- 44V
V- to Ground ..... -25V
V_{IN} to Ground (Note 1) ..... (V- -2V), (V+ +2V)
V_S or V_D to V+ (Note 1) ..... +2, (V- -2V)
V_S or V_D to V- (Note 1) ..... -2, (V+ +2V)
Current, any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max) 70mA
Lead Temperature (Soldering 10s) ..... +300°C
Storage Temperature Range
C Suffix ..... -65°C to +125°C
A & B Suffix ..... -65°C to +150°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	80°C/W	24°C/W
Plastic DIP Package	100°C/W	-
SOIC DIP Package	100°C/W	-

Junction Temperature
Plastic DIP Package ..... +150°C
Ceramic DIP Package ..... +175°C
Operating Temperature Range
"A" Suffix ..... -55°C to +125°C
"B" Suffix ..... -25°C to +85°C
"C" Suffix ..... 0°C to +70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications V+ = 15V, V- = -15V, GND = 0V, T_A = +25°C

PARAMETERS	TEST CONDITIONS		DG308AA/DG309A MIN	DG308AA/DG309A (NOTE 2) TYP	DG308AA/DG309A MAX	DG308AB/C, DG309B/C MIN	DG308AB/C, DG309B/C (NOTE 2) TYP	DG308AB/C, DG309B/C MAX	UNITS
DYNAMIC CHARACTERISTICS									
Turn-On Time, t_{ON}	See Figure 1		-	130	200	-	130	200	ns
Turn-Off Time, t_{OFF}	See Figure 1		-	90	150	-	90	150	ns
Charge Injection, Q	C_L = 1µF, R_S = 0, V_S = 0V		-	-10	-	-	-10	-	pC
Source OFF Capacitance, $C_{S(OFF)}$	f = 140kHz	V_S = 0V V_{IN} = 0V (DG308A) V_{IN} = 15V (DG309)	-	11	-	-	11	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$		V_D = 0V V_{IN} = 0V (DG308A) V_{IN} = 15V (DG309)	-	8	-	-	8	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$		$V_S = V_D$ = 0V V_{IN} = 15V (DG308A) V_{IN} = 0V (DG309)	-	27	-	-	27	-	pF
OFF Isolation, OIRR	V_{IN} = 0V (DG308A) V_{IN} = 15V (DG309), R_L = 75Ω, V_S = $2V_{P-P}$, f = 500kHz (Note 4)		-	78	-	-	78	-	dB
INPUT									
Input Current with Voltage High, I_{INH}	V_{IN} = 15V		-	0.001	1	-	0.001	1	µA
Input Current with Voltage Low, I_{INL}	V_{IN} = 0V		-1.0	-0.001	-	-1.0	-0.001	-	µA
SWITCH									
Analog Signal Range, V_{ANALOG}			-15	-	15	-15	-	15	V
Drain Source ON Resistance, $R_{DS(ON)}$	V_{IN} = 11V (DG308A) V_{IN} = 3.5V (DG309)	I_S = -1mA, V_D = +10V	-	60	100	-	60	100	Ω
		I_S = 1mA, V_D = -10V	-	60	100	-	60	100	Ω
Drain ON Leakage Current, $I_{D(ON)}$		$V_D = V_S$ = 14V	-	0.1	1	-	0.1	5	nA
		$V_D = V_S$ = -14V	-2	-0.1	-	-5	-0.1	-	nA
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 3.5V (DG308A) V_{IN} = 11V (DG309)	V_S = 14V, V_D = -14V	-	0.1	1	-	0.1	5	nA
		V_S = -14V, V_D = 14V	-1	-0.1	-	-5	-0.1	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	0.1	1	-	0.1	5	nA
		V_S = 14V, V_D = -14V	-1	-0.1	-	-5	-0.1	-	nA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I+	All Channels ON or OFF V_{IN} = 0V or 15V		-	0.001	10	-	0.001	100	µA
Negative Supply Current, I-			-10	-0.001	-	-100	-0.001	-	µA

Electrical Specifications V+ = 15V, V- = -15V, GND = 0V, T_A = Over Operating Temperature Range

PARAMETERS	TEST CONDITIONS		DG308AA/DG309A MIN	DG308AA/DG309A (NOTE 2) TYP	DG308AA/DG309A MAX	DG308AB/C, DG309B/C MIN	DG308AB/C, DG309B/C (NOTE 2) TYP	DG308AB/C, DG309B/C MAX	UNITS
INPUT									
Input Current with Voltage High, I_{INH}	V_{IN} = 15V		-	-	1	-	-	1	µA
Input Current with Voltage Low, I_{INL}	V_{IN} = 0V		-1	-	-	-1	-	-	µA
SWITCH									
Analog Signal Range, V_{ANALOG}			-15	-	15	-15	-	15	V
Drain Source ON Resistance, $R_{DS(ON)}$	V_{IN} = 11V (DG308A) V_{IN} = 3.5V (DG309)	I_S = -1mA, V_D = 10V	-	-	150	-	-	125	Ω
		I_S = 1mA, V_D = -10V	-	-	150	-	-	125	Ω
Drain ON Leakage Current, $I_{D(ON)}$		V_D = V_S = 14V	-	-	100	-	-	200	nA
		V_D = V_S = -14V	-200	-	-	-200	-	-	nA
Source OFF Leakage Current, $I_{S(OFF)}$	V_{IN} = 3.5V (DG308A) V_{IN} = 11V (DG309)	V_S = 14V, V_D = -14V	-	-	100	-	-	100	nA
		V_S = -14V, V_D = 14V	-100	-	-	-100	-	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$		V_S = -14V, V_D = 14V	-	-	100	-	-	100	nA
		V_S = 14V, V_D = -14V	-100	-	-	-100	-	-	nA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I+	V_{IN} = 0V or 15V		-	-	100	-	-	100	µA
Negative Supply Current, I-			-100	-	-	-100	-	-	µA

NOTES:

1. Signals on V_S, V_D, or V_{IN} exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive is a maximum, is used in this data sheet.
4. OFF isolation = 20log V_D/V_S, where V_S = input to OFF switch, and V_D = output.

Test Circuits

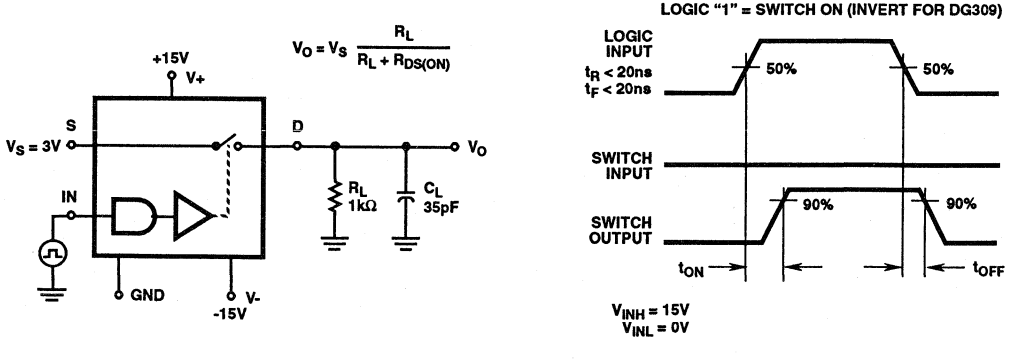


FIGURE 1. t_{ON} AND t_{OFF} SWITCHING TEST

Die Characteristics

DIE DIMENSIONS:
2058µm x 2109µm

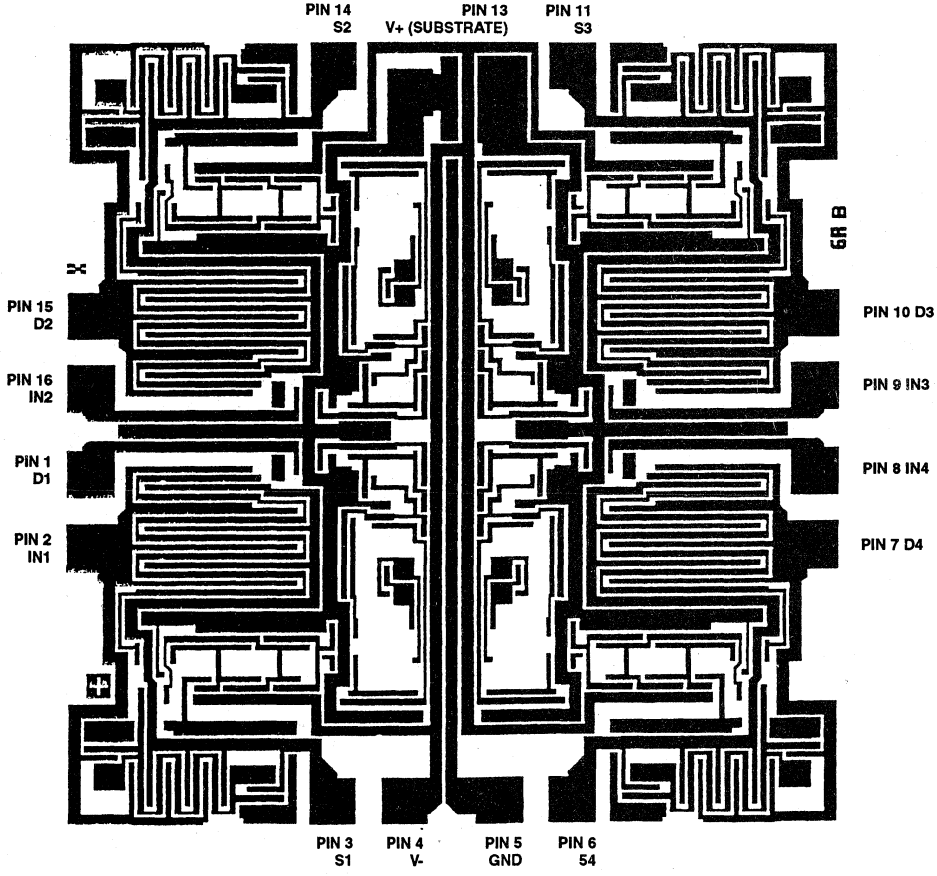
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG Over Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness:8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG308A, DG309



HARRIS SEMICONDUCTOR

DG401, DG403 DG405

Monolithic CMOS Analog Switches

December 1993

Features

- ON-Resistance < 35Ω
- Low Power Consumption (P_D < 35μW)
- Fast Switching Action
  - t_{ON} <150ns
  - t_{OFF} <100ns
- Low Charge Injection
- DG401 Dual SPST; Same Pinout as HI-5041
- DG403 Dual SPDT; DG190, IH5043, IH5151, HI-5051
- DG405 Dual DPST; DG184, HI-5045, IH5145
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG401, DG403 and DG405 monolithic CMOS analog switches have TTL and CMOS compatible digital inputs.

These switches feature low analog ON resistance (< 35Ω) and fast switch time (t_{ON} < 150ns). Low charge injection simplifies sample and hold applications.

The improvements in the DG401/403/405 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±17V.

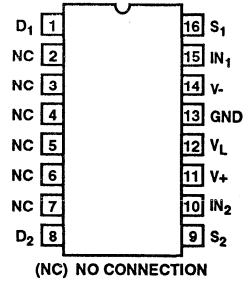
The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±15V analog input range. The three different devices provide the equivalent of two SPST (DG401), two SPDT (DG403) or two DPST (DG405) relay switch contacts with CMOS or TTL level activation. The pinout is similar, permitting a standard layout to be used, choosing the switch function as needed.

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
DG401AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG401DJ	-40°C to +85°C	16 Lead Plastic DIP
DG401DY	-40°C to +85°C	16 Lead SOIC (N)
DG403AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG403DJ	-40°C to +85°C	16 Lead Plastic DIP
DG403DY	-40°C to +85°C	16 Lead SOIC (N)
DG405AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG405DJ	-40°C to +85°C	16 Lead Plastic DIP
DG405DY	-40°C to +85°C	16 Lead SOIC (N)

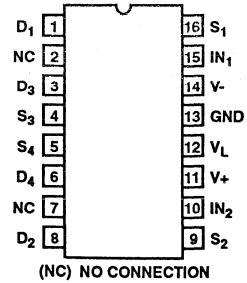
Pinouts

DG401
TOP VIEW



(NC) NO CONNECTION

DG403, DG405
TOP VIEW



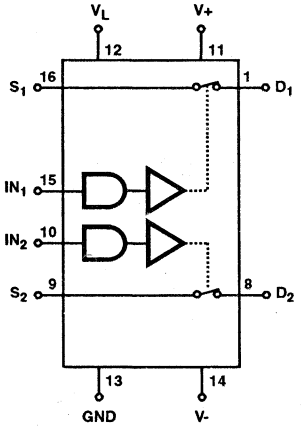
(NC) NO CONNECTION

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

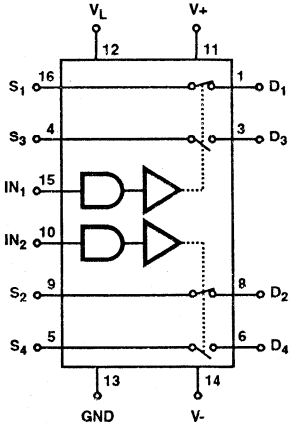
File Number **3284.1**

Functional Diagrams Switches Shown for Logic "1" Input

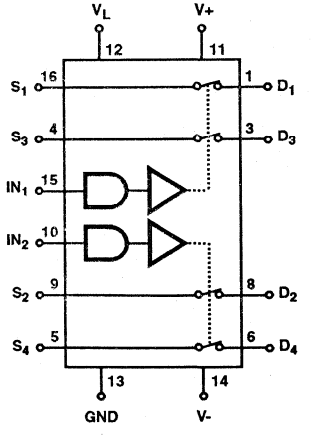
DG401



DG403



DG405



Truth Table

LOGIC	DG401	DG403		DG405
	SWITCH	SWITCH 1, 2	SWITCH 3, 4	SWITCH
0	OFF	OFF	ON	OFF
1	ON	ON	OFF	ON

NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V.

HARRIS SEMICONDUCTOR

DG411, DG412 DG413

Monolithic Quad SPST CMOS Analog Switches

December 1993

Features

- ON-Resistance < 35Ω Max
- Low Power Consumption (P_D < 35μW)
- Fast Switching Action
  - t_{ON} <175ns
  - t_{OFF} <145ns
- Low Charge Injection
- Upgrade from DG211/DG212
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Ordering Information

PART NO.	TEMP. RANGE	PACKAGE
DG411AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG411DJ	-40°C to +85°C	16 Lead Plastic DIP
DG411DY	-40°C to +85°C	16 Lead SOIC (N)
DG412AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG412DJ	-40°C to +85°C	16 Lead Plastic DIP
DG412DY	-40°C to +85°C	16 Lead SOIC (N)
DG413AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG413DJ	-40°C to +85°C	16 Lead Plastic DIP
DG413DY	-40°C to +85°C	16 Lead SOIC (N)

Description

The DG411 series monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole throw (SPST) analog switches, TTL and CMOS compatible digital inputs and a voltage reference for logic thresholds.

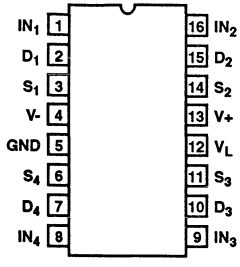
These switches feature lower analog ON resistance (< 35Ω) and faster switch time (t_{ON} < 175ns) compared to the DG211 or DG212. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG411 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 40V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±15V analog input range. The switches in the DG411 and DG412 are identical, differing only in the polarity of the selection logic. Two of the switches in the DG413 (#1 and #4) use the logic of the DG211 and DG411 (i.e. a logic "0" turns the switch ON) and the other two switches use DG212 and DG412 positive logic. This permits independent control of turn-on and turn-off times for SPDT configurations, permitting "break-before-make" or "make-before-break" operation with a minimum of external logic.

Pinout

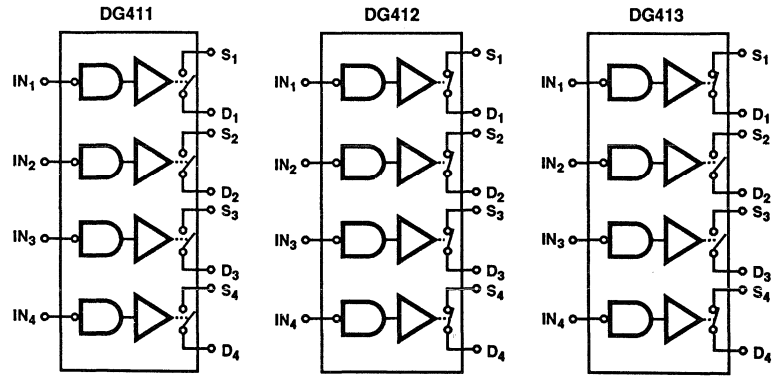
DG411/12/13
(CDIP, PDIP, SOIC)
TOP VIEW



(NC) NO CONNECTION

Functional Diagrams

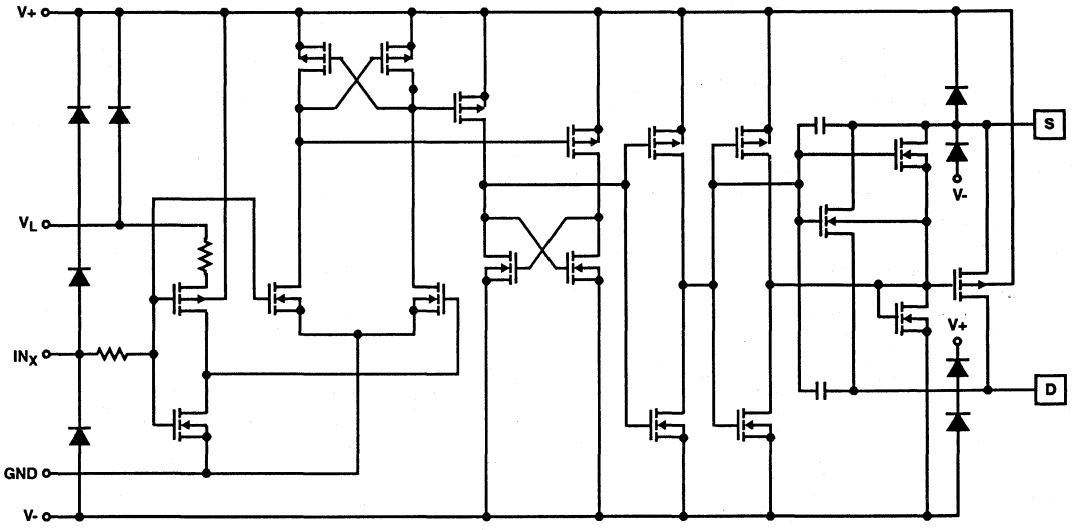
Four SPST Switches per Package Switches Shown for Logic "1" Input



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3282.1**

Typical Schematic Diagram (Typical Channel)



Absolute Maximum Ratings

V+ to V- 44V
GND to V- 25V
V_L ..... (GND -0.3V) to (V+) +0.3V
Digital Inputs, V_S, V_D (Note 1) ..... (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Current, S or D (Pulsed 1ms, 10% Duty Cycle) 100mA
Storage Temperature Range
(D Suffix) ..... -65°C to +125°C

Thermal Information

	θ_{JA}	θ_{JC}
Thermal Resistance (Note 2)		
Ceramic DIP Package	85°C/W	24°C/W
Plastic DIP Package	100°C/W	-
SOIC Package	120°C/W	-

Junction Temperature ..... +170°C
Operating Temperature
(A Suffix) ..... -55°C to +125°C
(D Suffix) ..... -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... ±20V Max
Operating Temperature Range ..... -40°C to +85°C
Input Low Voltage ..... 0.8V Max
Input High Voltage ..... 2.4V Min
Input Rise and Fall Time ..... ≤20ns

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS		(NOTE 4) TEMP	D SUFFIX -40°C TO +85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS							
Turn-ON Time, T_{ON}	R_L = 300Ω, C_L = 35pF, V_S = ±10V, (See Figure 7)		+25°C	-	110	175	ns
			Hot	-	-	220	ns
Turn-OFF Time, T_{OFF}			+25°C	-	100	145	ns
			Hot	-	-	160	ns
Break-Before-Make Time Delay	DG413 Only, R_L = 300Ω, C_L = 35pF		+25°C	-	25	-	ns
Charge Injection, Q	C_L = 10nF, V_G = 0V, R_G = 0Ω		+25°C	-	5	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz		+25°C	-	68	-	dB
Crosstalk (Channel-to-Channel)			+25°C	-	85	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz		+25°C	-	9	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$			+25°C	-	9	-	pF
Channel ON Capacitance, $C_{D(ON)}$ + $C_{S(ON)}$			+25°C	-	35	-	pF
DIGITAL CONTROL							
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V		Full	-0.5	0.005	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V		Full	-0.5	0.005	0.5	µA
ANALOG SWITCH							
Analog Signal Range, V_{ANALOG}	Note 7		Full	-15	-	15	V
Drain-Source ON Resistance, $R_{DS(ON)}$	I_S = -10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V		+25°C	-	25	35	Ω
			Full	-	-	45	Ω
Switch OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V	V_D = -15.5V, V_S = 15.5V	+25°C	-0.25	-0.1	0.25	nA
			Full	-20	-	20	nA
Switch OFF Leakage Current, $I_{D(OFF)}$		V_D = 15.5V, V_S = -15.5V	+25°C	-0.25	-0.1	0.25	nA
			Full	-20	-	20	nA
Channel ON Leakage Current, $I_{D(ON)}$ + $I_{S(ON)}$		V_D = 15.5V, V_S = -15.5V	+25°C	-0.4	-0.1	0.4	nA
			Full	-40	-	40	nA

Electrical Specifications (Unipolar Supplies) Test Conditions: V+ = +12V, V- = 0V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP	D SUFFIX -40°C TO +85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, T_{ON}	R_L = 300Ω, C_L = 35pF, V_S = ±8V, (See Figure 7)	+25°C	-	175	250	ns
		Hot	-	-	315	ns
Turn-OFF Time, T_{OFF}		+25°C	-	95	125	ns
		Hot	-	-	140	ns
Break-Before-Make Time Delay	DG413 Only, R_L = 300Ω, C_L = 35pF	+25°C	-	25	-	ns
Charge Injection, Q	C_L = 10nF, V_G = 6.0V, R_G = 0Ω	+25°C	-	25	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}	Note 7	Full	0	-	12	V
Drain-Source ON Resistance, $R_{DS(ON)}$	I_S = -10mA, V_D = 3.8V, V+ = 10.8V	+25°C	-	40	80	Ω
		Full	-	-	100	Ω
POWER SUPPLY CHARACTERISTICS						
Positive Supply Current, I+	V+ = 13.2V, V- = 0V V_{IN} = 0V or 5V	+25°C	-	0.0001	1	µA
		Hot		-	5	µA
Negative Supply Current, I-		+25°C	-1	-0.0001	-	µA
		Hot	-5	-	-	µA
Logic Supply Current, I_L		+25°C	-	-0.0001	1	µA
		Hot	-	-	5	µA
Ground Current, I_{GND}		+25°C	-1	-0.0001	-	µA
		Hot	-5	-	-	µA

NOTES:

1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. All leads welded or soldered to PC Board.
3. V_{IN} = input voltage to perform proper function.
4. Hot = as determined by the operating temperature suffix.
5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
7. Guaranteed by design, not subject to production test.

Typical Performance Curves

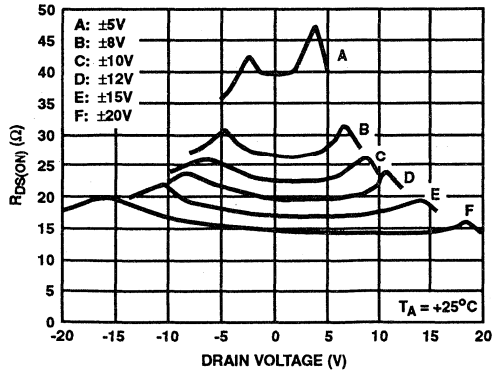


FIGURE 1. ON-RESISTANCE vs V_D AND POWER SUPPLY VOLTAGE

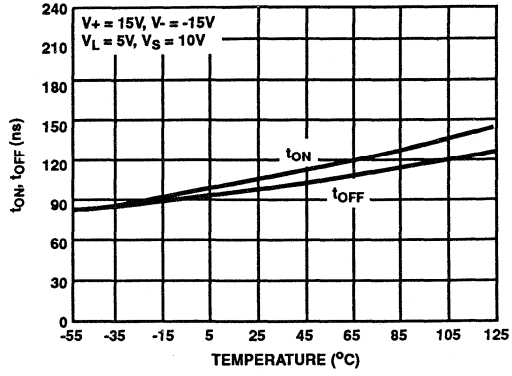


FIGURE 2. SWITCHING TIME vs TEMPERATURE

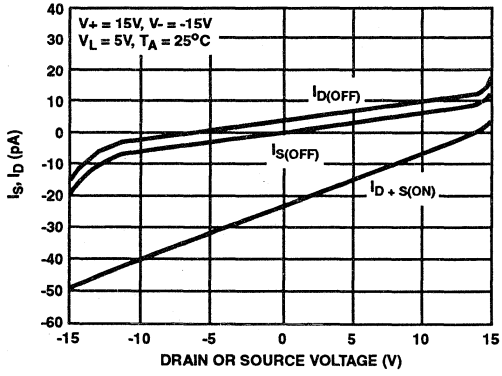


FIGURE 3. LEAKAGE CURRENT vs ANALOG VOLTAGE

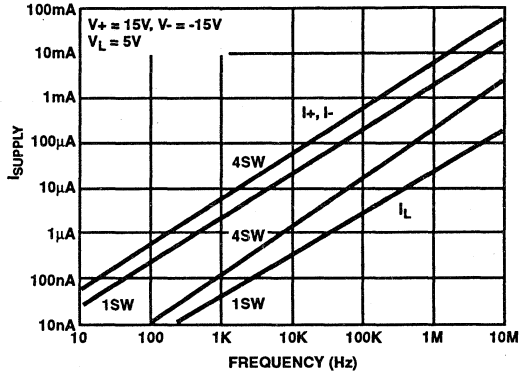


FIGURE 4. SUPPLY CURRENT vs INPUT SWITCHING FREQUENCY

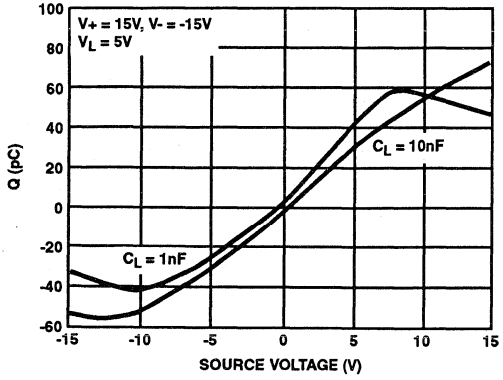


FIGURE 5. CHARGE INJECTION vs ANALOG VOLTAGE (V_D)

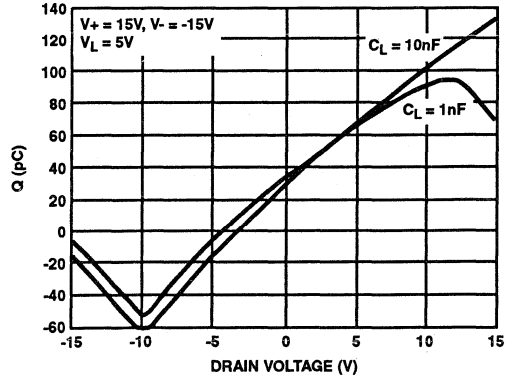


FIGURE 6. CHARGE INJECTION vs ANALOG VOLTAGE (V_S)

Pin Description

PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic control for switch 1
2	D_1	Drain (output) terminal for switch 1
3	S_1	Source (input) terminal for switch 1
4	V-	Negative power supply terminal
5	GND	Ground terminal (Logic Common)
6	S_4	Source (input) terminal for switch 4
7	D_4	Drain (output) terminal for switch 4
8	IN_4	Logic control for switch 4
9	IN_3	Logic control for switch 3
10	D_3	Drain (output) terminal for switch 3
11	S_3	Source (input) terminal for switch 3
12	V_L	Logic reference voltage.
13	V+	Positive power supply terminal (substrate)
14	S_2	Source (input) terminal for switch 2
15	D_2	Drain (output) terminal for switch 2
16	IN_2	Logic control for switch 2

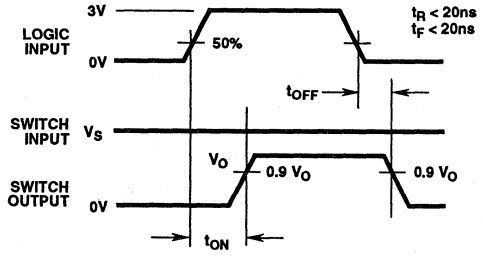
TRUTH TABLE

LOGIC	DG411 SWITCH	DG412 SWITCH	DG413 SWITCH 1, 4	DG413 SWITCH 2, 3
0	ON	OFF	OFF	ON
1	OFF	ON	ON	OFF

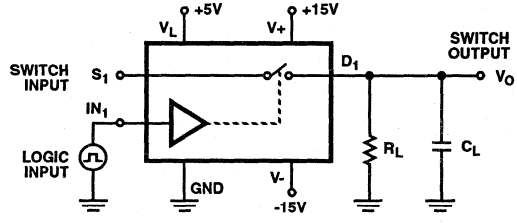
NOTE: Logic "0" ≤0.8V. Logic "1" ≥2.4V.

Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



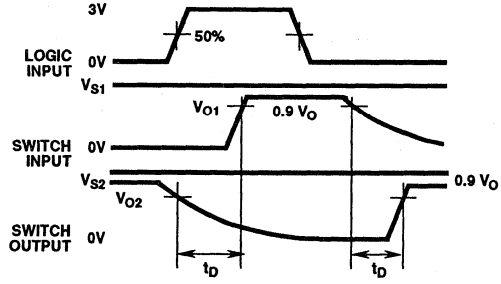
NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

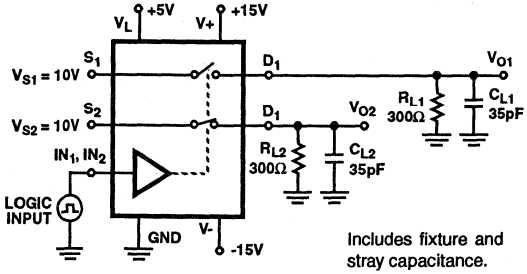


Repeat test for all IN and S.
For load conditions, see Specifications C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + R_{DS(ON)}}$$

FIGURE 7. SWITCHING TIME

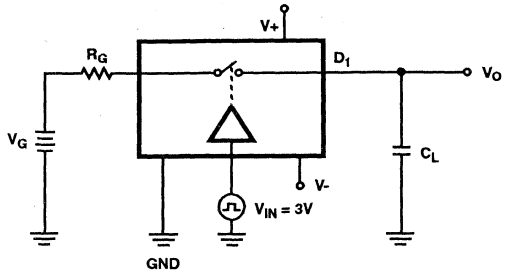


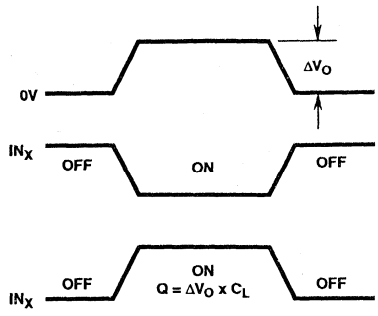


Includes fixture and stray capacitance.

FIGURE 8. BREAK-BEFORE-MAKE

Test Circuits (Continued)





IN_X dependent on switch configuration input polarity determined by sense of switch.

FIGURE 9. CHARGE INJECTION

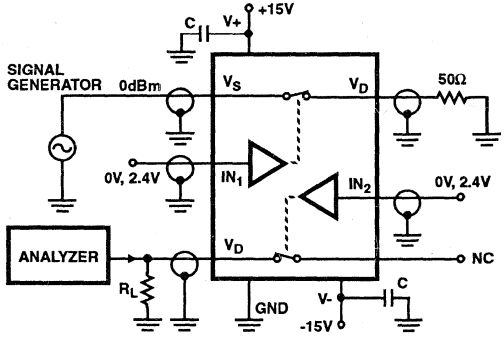


FIGURE 10. CROSSTALK

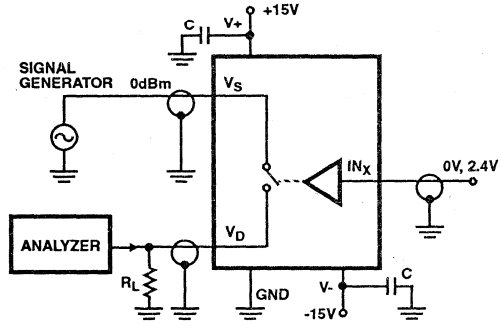


FIGURE 11. OFF ISOLATION

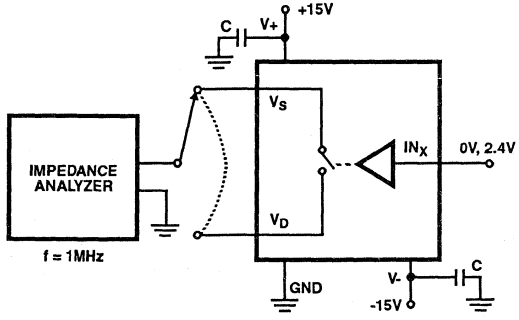


FIGURE 12. SOURCE/DRAIN CAPACITANCES

Typical Applications

Single Supply Operation

The DG411/412/413 can be operated with unipolar supplies from 5V to 44V. These devices are characterized and tested for unipolar supply operation at 12V to facilitate the majority of applications. To function properly 12 volts are tied to Pin 13 and 0 volts are tied to Pin 4.

NOTE: Pin 12 still requires 5V for TTL compatible switching.

Summing Amplifier

When driving a high impedance, high capacitance load such as shown in Figure 9, where the inputs to the summing amplifier have some noise filtering, it is necessary to have shunt switches for rapid discharge of the filter capacitor, thus preventing offsets from occurring at the output.

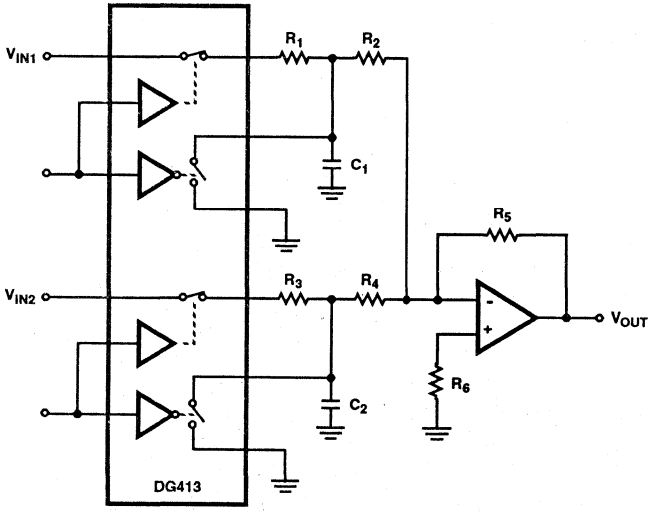


FIGURE 13. SUMMING AMPLIFIER

Die Characteristics

DIE DIMENSIONS:
2760µm x 1780µm x 485 ± 25µm

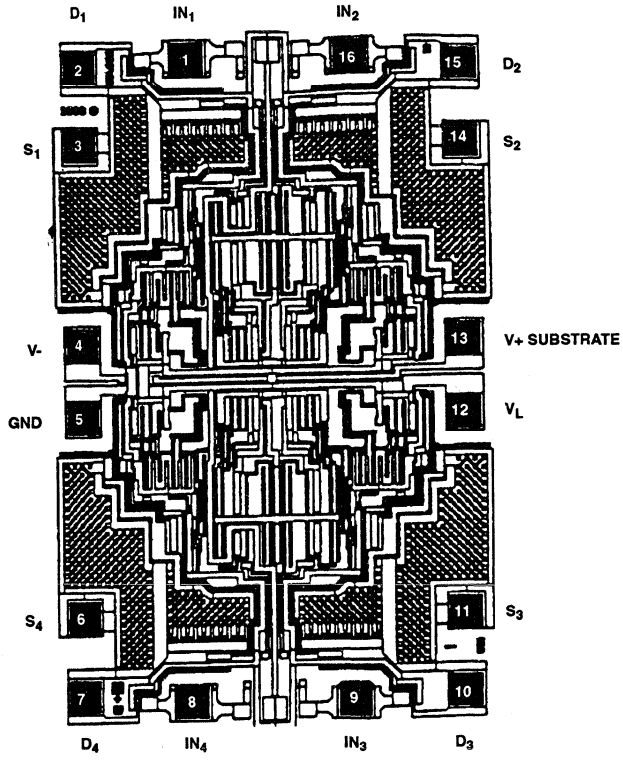
METALLIZATION:
Type: SiAl
Thickness: 12kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
$1.5 \times 10^5 A/cm^2$

Metallization Mask Layout

DG411, DG412, DG413



HARRIS SEMICONDUCTOR

DG441, DG442

Monolithic Quad SPST CMOS Analog Switches

December 1993

Features

- ON-Resistance 85Ω Max
- Low Power Consumption (P_D < 1.6mW)
- Fast Switching Action
  - t_{ON} < 250ns
  - t_{OFF} < 120ns (DG441)
- ESD Protection > ±2000V
- Low Charge Injection
- Upgrade from DG201A/DG202
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG441 and DG442 monolithic CMOS analog switches are drop-in replacements for the popular DG201A and DG202 series devices. They include four independent single pole single throw (SPST) analog switches, TTL and CMOS compatible digital inputs, and a voltage reference for logic thresholds.

These switches feature lower analog ON resistance (<85Ω) and faster switch time (t_{ON} < 250ns) compared to the DG201A and DG202. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG441 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 40V peak-to-peak signals. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

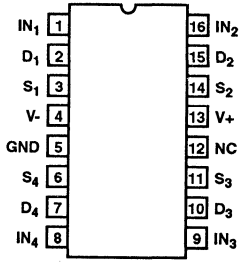
The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range. The switches in the DG441 and DG442 are identical, differing only in the polarity of the selection logic.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG441AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG441DJ	-40°C to +85°C	16 Lead Plastic DIP
DG441DY	-40°C to +85°C	16 Lead SOIC (N)
DG442AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG442DJ	-40°C to +85°C	16 Lead Plastic DIP
DG442DY	-40°C to +85°C	16 Lead SOIC (N)

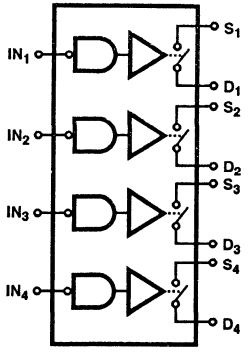
Pinout

DG441, DG442
(PDIP, CDIP, SOIC)
TOP VIEW

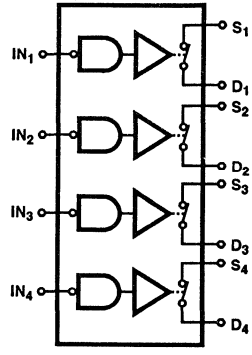


Functional Diagrams

DG441



DG442

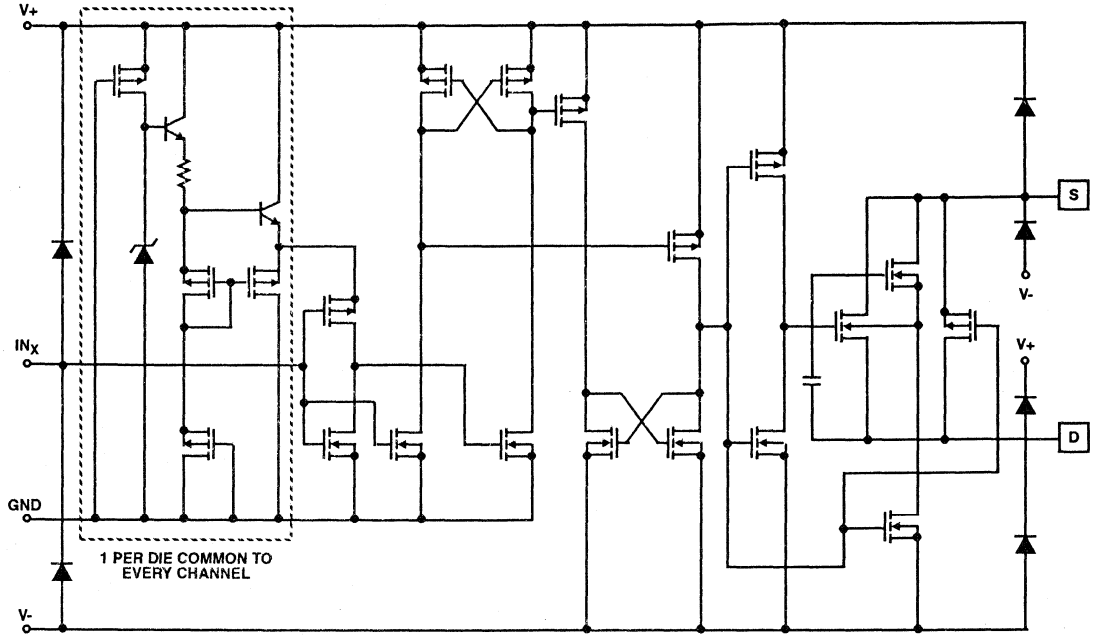


SWITCHES SHOWN FOR LOGIC "1" INPUT

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3281.2**

Schematic Diagram (One Channel)



Absolute Maximum Ratings

V+ to V- ..... +44.0V
GND to V- 25V
Digital Inputs (Note 1) ..... (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current, S or D (Note 1) ..... ±30mA
Peak Current, S or D (Note 1) ..... ±100mA
(Pulsed 1ms, 10% Duty Cycle)
Storage Temperature Range (A Suffix) ..... -65°C to +150°C
(D Suffix) ..... -65°C to +125°C

Thermal Information

Thermal Resistance (Note 3)	θ_{JA}	θ_{JC}
Plastic DIP Package	100°C/W	-
Ceramic DIP Package	85°C/W	24°C/W
SOIC Package	120°C/W	-

Operating Temperature (A Suffix) ..... -55°C to +125°C
(D Suffix) ..... -40°C to +85°C
Junction Temperature (CDIP) ..... +175°C
(PDIP, SOIC) ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... ±20V Max
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0.8V Max
Input High Voltage ..... 2.4V Min
Input Rise and Fall Time 20ns

Electrical Specifications

(Dual Supply) Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, $V_{ANALOG} = V_S$, V_D, Unless Otherwise Specified

PARAMETER	TEST CONDITION	(NOTE 2) TEMP	A SUFFIX -55°C TO +125°C MIN	A SUFFIX -55°C TO +125°C (NOTE 4) TYP	A SUFFIX -55°C TO +125°C MAX	D SUFFIX -40°C TO +85°C MIN	D SUFFIX -40°C TO +85°C (NOTE 4) TYP	D SUFFIX -40°C TO +85°C MAX	UNITS
DYNAMIC CHARACTERISTICS									
Turn-ON Time, T_{ON}	R_1 = 1kΩ, C_L = 35pF, V_S = ±10V, See Figure 18	+25°C	-	150	250	-	150	250	ns
Turn-OFF Time, T_{OFF}		+25°C							
DG441			-	90	120	-	90	120	ns
DG442			-	110	170	-	110	170	ns
Charge Injection, Q	C_L = 1nF, V_S = 0V, V_{GEN} = 0V, R_{GEN} = 0Ω	+25°C	-	-1	-	-	-1	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz	+25°C	-	60	-	-	60	-	dB
Crosstalk (Channel-to-Channel)	R_L = 50Ω, C_L = 5pF, f = 1MHz	+25°C	-	-100	-	-	-100	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz	+25°C	-	4	-	-	4	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	f = 1MHz	+25°C	-	4	-	-	4	-	pF
Channel ON Capacitance, $C_{D(ON)} + C_{S(ON)}$	V_{ANALOG} = 0	+25°C	-	16	-	-	16	-	pF
ANALOG SWITCH									
Analog Signal Range, V_{ANALOG}	Note 4	Full	-15	-	15	-15	-	15	V
Drain-Source ON Resistance, $R_{DS(ON)}$	I_S = 10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V	+25°C	-	50	85	-	50	85	Ω
		Hot	-	-	100	-	-	100	Ω
Switch OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	+25°C	-0.5	0.01	0.5	-0.5	0.01	0.5	nA
		Hot	-20	-	20	-20	-	20	nA
Switch OFF Leakage Current, $I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	+25°C	-0.5	0.01	0.5	-0.5	0.01	0.5	nA
		Hot	-20	-	20	-20	-	20	nA

Electrical Specifications

(Dual Supply) Test Conditions: V+ = +15V, V- = -15V, V_{IN} = 2.4V, 0.8V, V_{ANALOG} = V_S, V_D, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	(NOTE 2) TEMP	A SUFFIX -55°C TO +125°C MIN	A SUFFIX -55°C TO +125°C (NOTE 4) TYP	A SUFFIX -55°C TO +125°C MAX	D SUFFIX -40°C TO +85°C MIN	D SUFFIX -40°C TO +85°C (NOTE 4) TYP	D SUFFIX -40°C TO +85°C MAX	UNITS
ANALOG SWITCH (Continued)									
Channel ON Leakage Current, $I_{D(ON)} + I_{S(ON)}$	V+ = 16.5V, V- = -16.5V, $V_S = V_D = \pm 15.5V$	+25°C	-0.5	0.08	0.5	-0.5	0.08	0.5	nA
		Hot	-40	-	40	-40	-	40	nA
DIGITAL CONTROL									
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-0.5	-0.00001	0.5	-0.5	-0.00001	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-0.5	0.00001	0.5	-0.5	0.00001	0.5	µA
POWER SUPPLIES									
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	Full	-	15	100	-	15	100	µA
Negative Supply Current, I-		+25°C	-1	-0.0001	-	-1	-0.0001	-	µA
		Full	-5	-	-	-5	-	-	µA
Ground Current, I_{GND}		Full	-100	-15	-	-100	-15	-	µA

Electrical Specifications

(Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_{IN} = 2.4V, 0.8V, Unless Otherwise Specified

PARAMETER	TEST CONDITION	(NOTE 2) TEMP	A SUFFIX -55°C TO +125°C MIN	A SUFFIX -55°C TO +125°C (NOTE 4) TYP	A SUFFIX -55°C TO +125°C MAX	D SUFFIX -40°C TO +85°C MIN	D SUFFIX -40°C TO +85°C (NOTE 4) TYP	D SUFFIX -40°C TO +85°C MAX	UNITS
DYNAMIC CHARACTERISTICS									
Turn-ON Time, T_{ON}	R_L = 1KΩ, C_L = 35pF, See Test Circuit, V_S = 8V	+25°C	-	300	400	-	300	400	ns
Turn-OFF Time, T_{OFF}		+25°C	-	60	200	-	60	200	ns
Charge Injection, Q	C_L = 1nF, V_{GEN} = 6V, R_{GEN} = 0Ω	+25°C	-	2	-	-	2	-	pC
ANALOG SWITCH									
Analog Signal Range, V_{ANALOG}	Note 4	Full	0	-	12	0	-	12	V
Drain-Source ON-Resistance, $R_{DS(ON)}$	I_S = 10mA, V_D = 3V, 8V V+ = 10.8V	+25°C	-	100	160	-	100	160	Ω
		Full	-	-	200	-	-	200	Ω
POWER SUPPLIES									
Positive Supply Current, I+	V+ = 13.2V, V- = 0V, V_{IN} = 0V or 5V	Full	-	15	100	-	15	100	µA
Negative Supply Current, I-		+25°C	-1	-0.0001	-	-1	-0.0001	-	µA
		Full	-100	-0.0001	-	-100	-0.0001	-	µA
Ground Current, I_{GND}		Full	-100	-15	-	-100	-15	-	µA

NOTES:

1. All leads soldered to PC Board.
2. Room: +25°C. Cold: A suffix -55°C, D suffix -40°C. Hot: A suffix +125°C, D suffix +85°C
3. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor production tested.

Typical Performance Curves

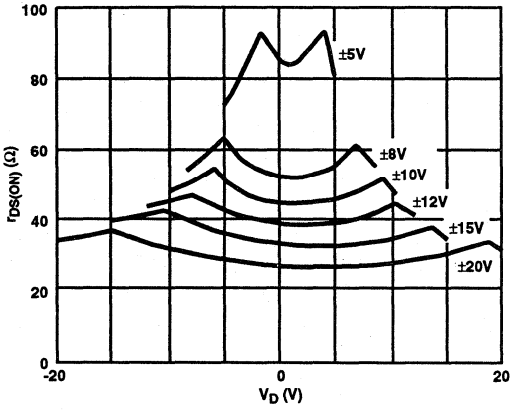


FIGURE 1. $R_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

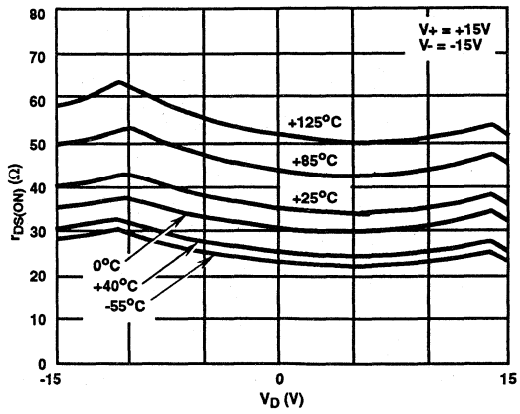


FIGURE 2. $R_{DS(ON)}$ vs V_D AND TEMPERATURE

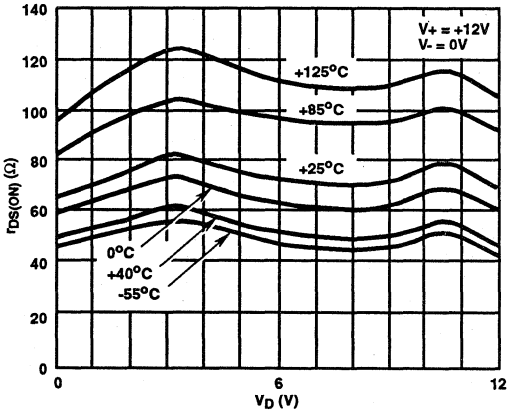


FIGURE 3. $R_{DS(ON)}$ vs V_D AND TEMPERATURE (SINGLE 12V SUPPLY)

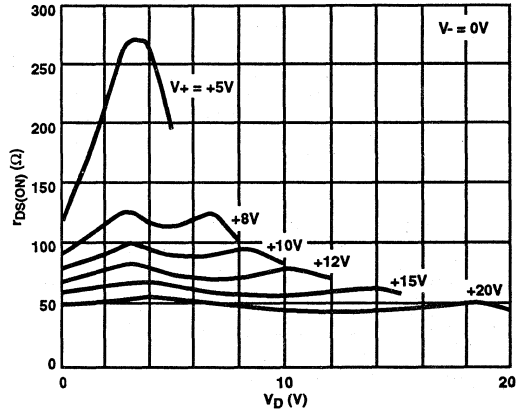


FIGURE 4. $R_{DS(ON)}$ vs V_D AND UNIPOLAR POWER SUPPLY VOLTAGE

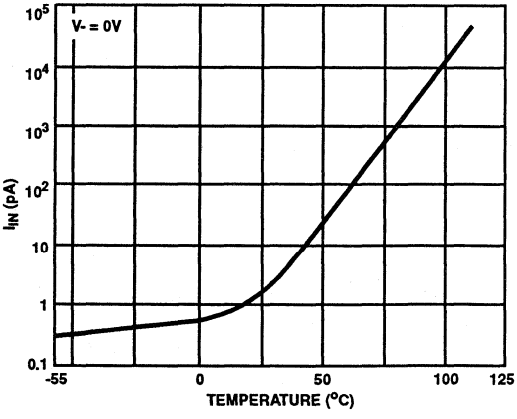


FIGURE 5. INPUT CURRENT vs TEMPERATURE

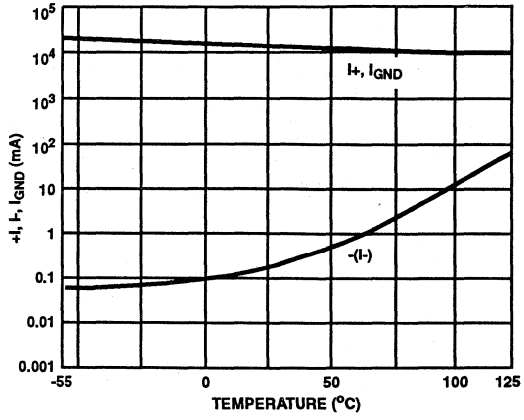


FIGURE 6. SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

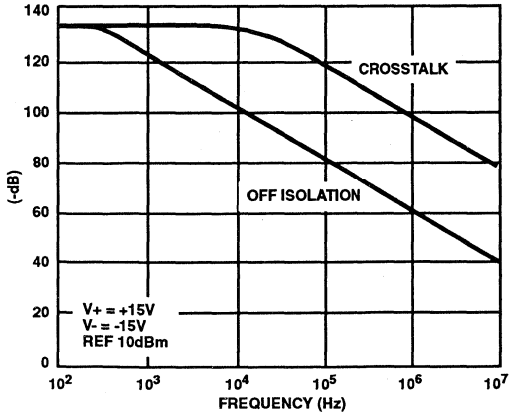


FIGURE 7. CROSSTALK AND OFF ISOLATION vs FREQUENCY

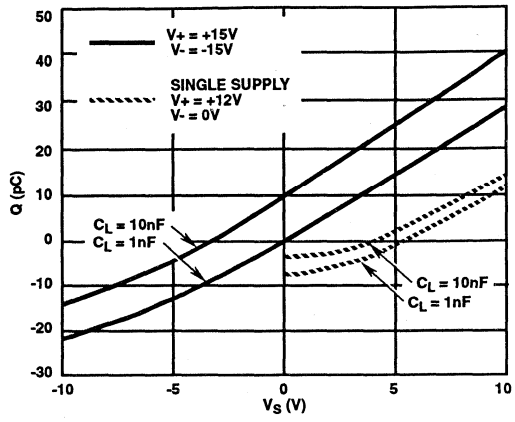


FIGURE 8. CHARGE INJECTION vs SOURCE VOLTAGE

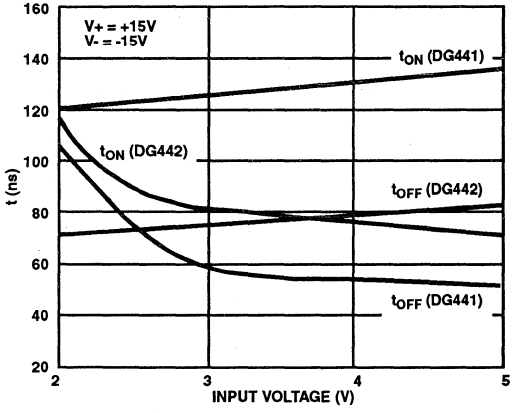


FIGURE 9. SWITCHING TIMES vs INPUT VOLTAGE

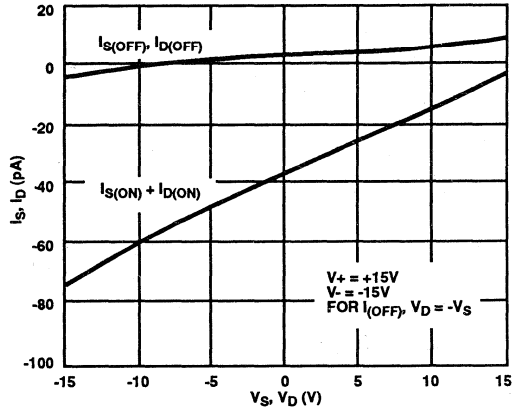


FIGURE 10. SOURCE/DRAIN LEAKAGE CURRENTS

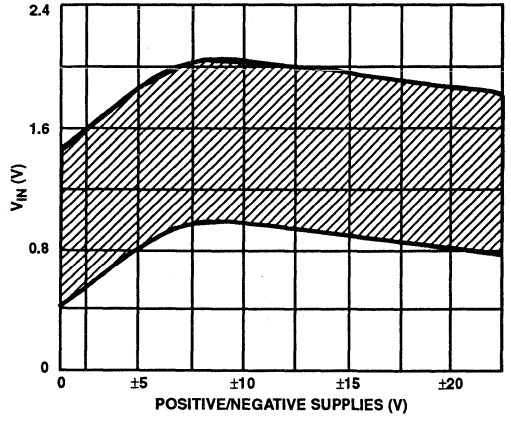


FIGURE 11. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

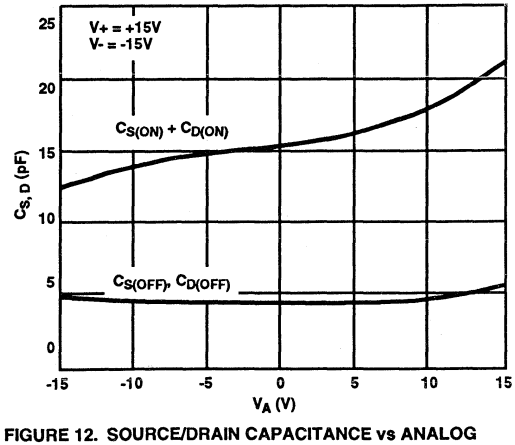


FIGURE 12. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

Typical Performance Curves (Continued)

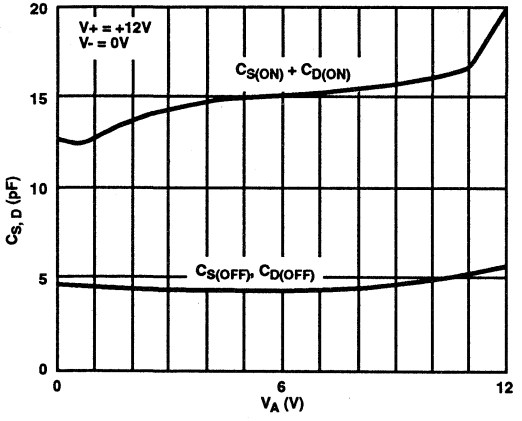


FIGURE 13. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

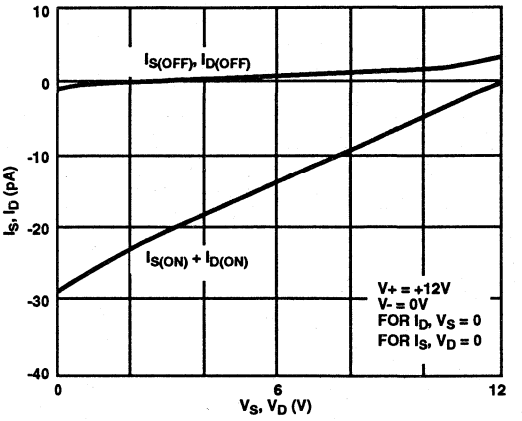


FIGURE 14. SOURCE/DRAIN LEAKAGE CURRENTS (SINGLE 12V SUPPLY)

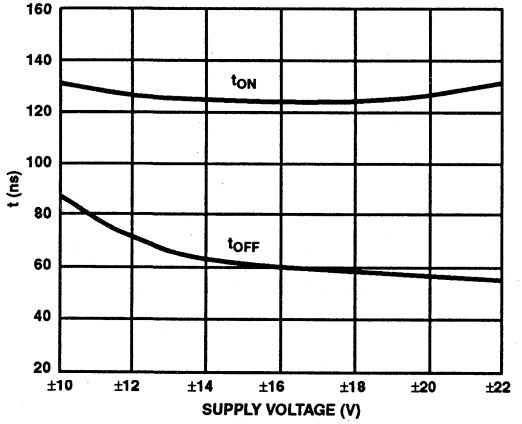


FIGURE 15. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG441)

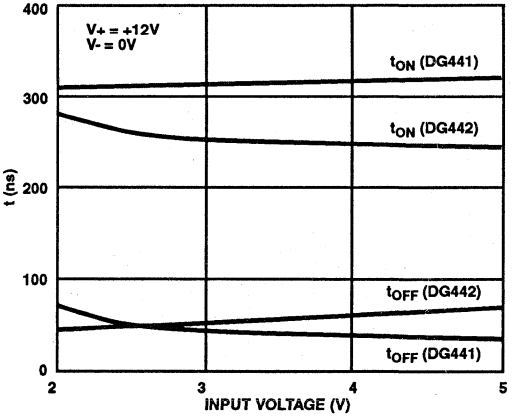


FIGURE 16. SWITCHING TIMES vs INPUT VOLTAGE

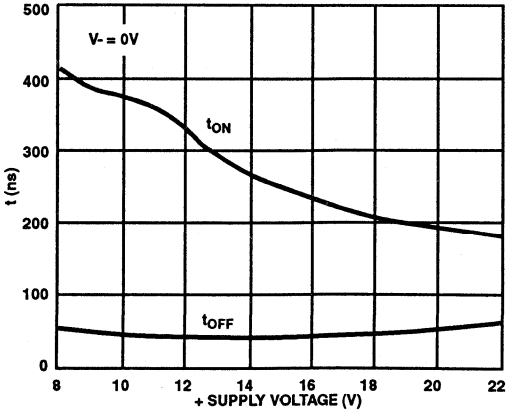


FIGURE 17. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG441)

Pin Description

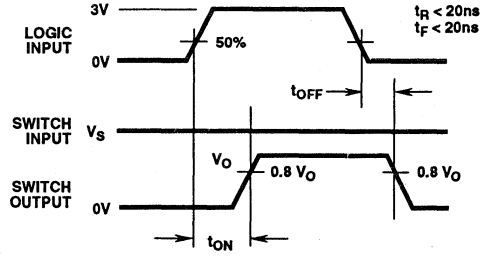
PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic control for switch 1
2	D_1	Drain (output) terminal for switch 1
3	S_1	Source (input) terminal for switch 1
4	V-	Negative power supply terminal
5	GND	Ground terminal (Logic Common)
6	S_4	Source (input) terminal for switch 4
7	D_4	Drain (output) terminal for switch 4
8	IN_4	Logic control for switch 4
9	IN_3	Logic control for switch 3
10	D_3	Drain (output) terminal for switch 3
11	S_3	Source (input) terminal for switch 3
12	NC	No internal connection
13	V+	Positive power supply terminal (substrate)
14	S_2	Source (input) terminal for switch 2
15	D_2	Drain (output) terminal for switch 2
16	IN_2	Logic control for switch 2

TRUTH TABLE

LOGIC	V_{IN}	DG441	DG442
0	≤0.8V	ON	OFF
1	≥2.4V	OFF	ON

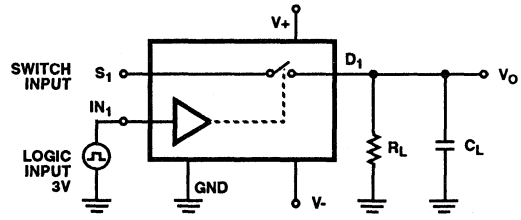
Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 18A.



Repeat test for Channels 2, 3 and 4.
For load conditions, see Specifications C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 18B.

FIGURE 18. SWITCHING TIME

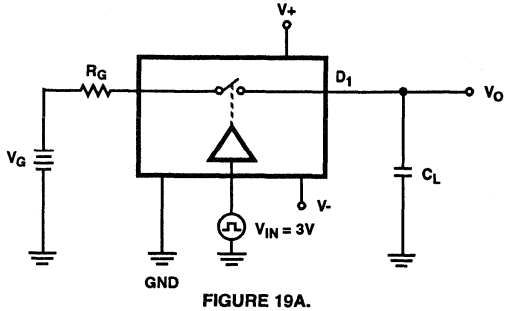


FIGURE 19A.

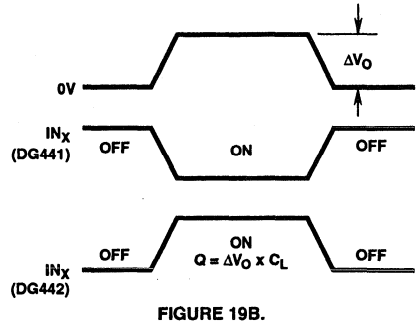


FIGURE 19B.

FIGURE 19. CHARGE INJECTION

Test Circuits (Continued)

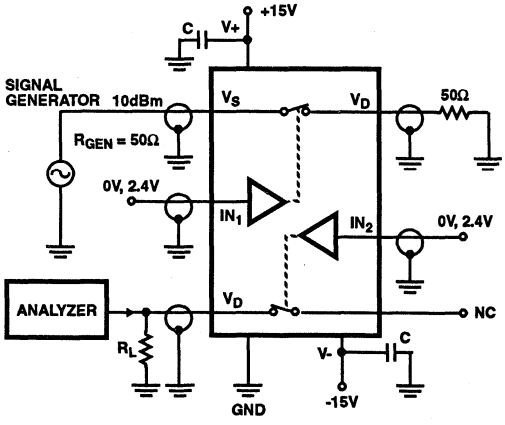


FIGURE 20. CROSSTALK

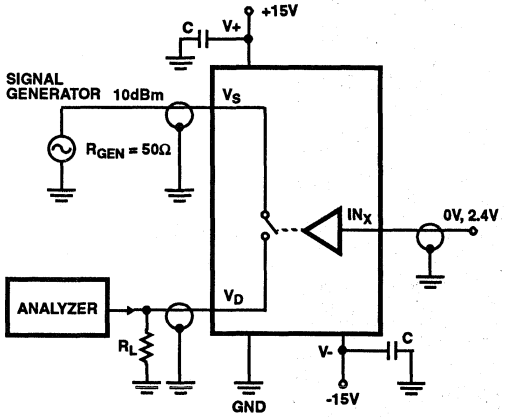


FIGURE 21. OFF ISOLATION

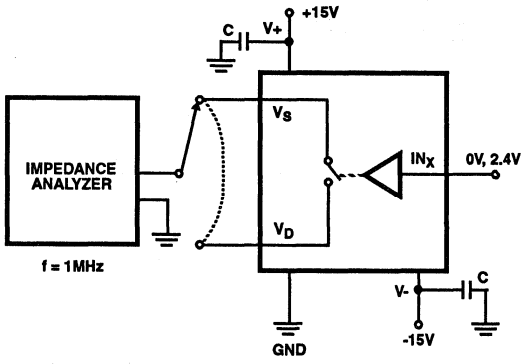
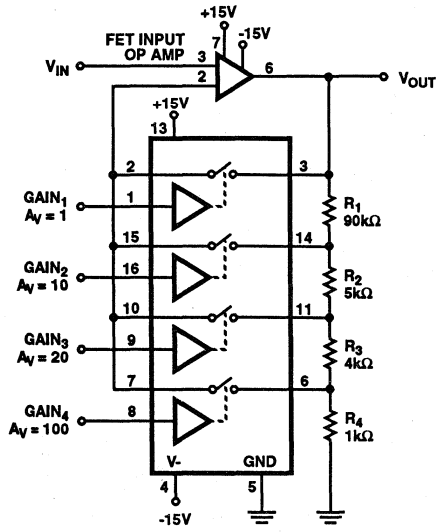


FIGURE 22. SOURCE/DRAIN CAPACITANCES

Applications

GAIN ERROR IS DETERMINED ONLY BY THE RESISTOR TOLERANCE. OP AMP OFFSET AND CMRR WILL LIMIT ACCURACY OF CIRCUIT



$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

WITH SW_4 CLOSED

FIGURE 23. PRECISION WEIGHTED RESISTOR PROGRAMMABLE GAIN AMPLIFIER

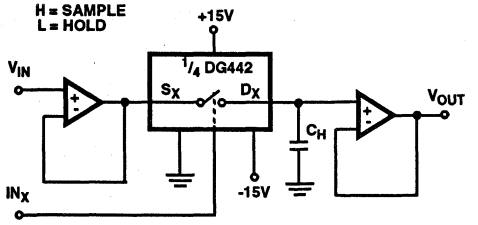


FIGURE 24. OPEN LOOP SAMPLE AND HOLD

Die Characteristics

DIE DIMENSIONS:
2160µm x 1760µm x 485 ± 25µm

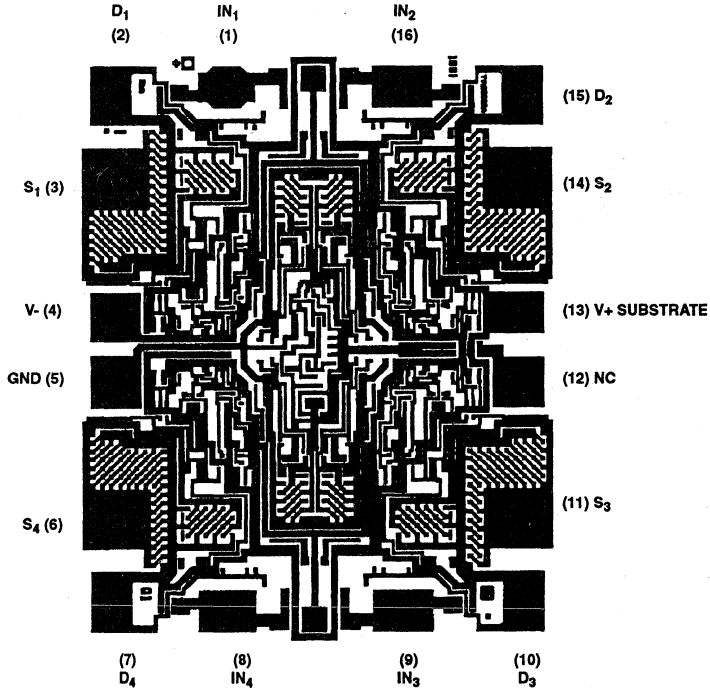
METALLIZATION:
Type: CuAl
Thickness: 12kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
9.1 x 10^4A/cm^2

Metallization Mask Layout

DG441, DG442



HARRIS SEMICONDUCTOR

DG444, DG445

Monolithic Quad SPST CMOS Analog Switches

December 1993

Features

- ON-Resistance 85Ω Max
- Low Power Consumption (P_D < 35mW)
- Fast Switching Action
  - t_{ON} < 250ns
  - t_{OFF} < 120ns (DG444)
- ESD Protection > ±2000V
- Low Charge Injection
- Upgrade from DG211/DG212
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Audio Switching
- Battery Operated Systems
- Data Acquisition
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Automatic Test Equipment

Description

The DG444 and DG445 monolithic CMOS analog switches are drop-in replacements for the popular DG211 and DG212 series devices. They include four independent single pole single throw (SPST) analog switches, TTL and CMOS compatible digital inputs and a voltage reference for logic thresholds.

These switches feature lower analog ON resistance (<85Ω) and faster switch time (t_{ON} < 250ns) compared to the DG211 and DG212. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG444 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling ±20V signals when operating with ±20V power supplies.

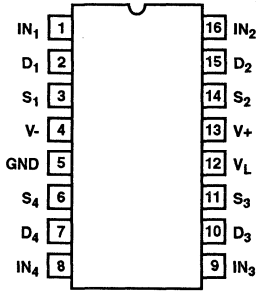
The four switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range. The switches in the DG444 and DG445 are identical, differing only in the polarity of the selection logic.

Ordering Information

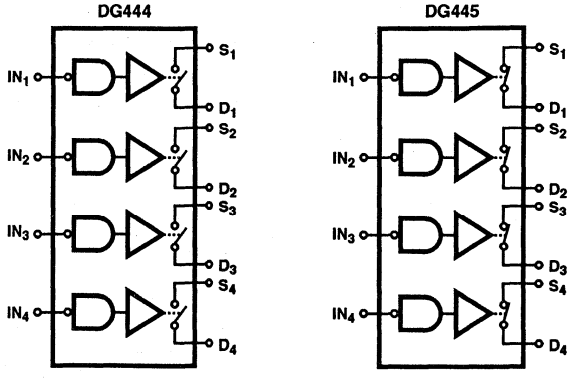
PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG444DJ	-40°C to +85°C	16 Lead Plastic DIP
DG444DY	-40°C to +85°C	16 Lead SOIC (N)
DG445DJ	-40°C to +85°C	16 Lead Plastic DIP
DG445DY	-40°C to +85°C	16 Lead SOIC (N)

Pinout

DG444, DG445
(PDIP, SOIC)
TOP VIEW



Functional Diagrams



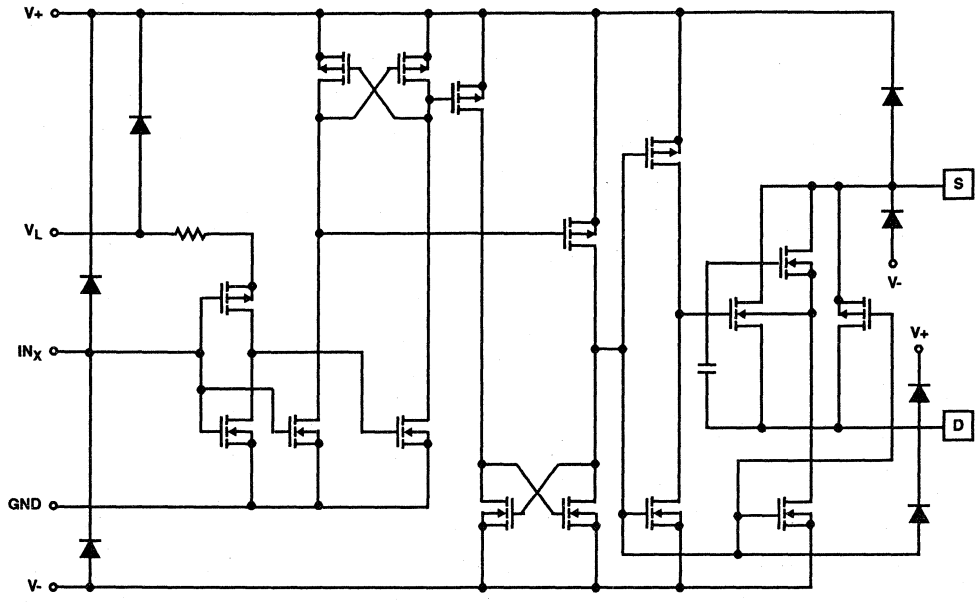
SWITCHES SHOWN FOR LOGIC "1" INPUT

9 SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3586.1

Typical Schematic Diagram (One Channel)



Absolute Maximum Ratings

V+ to V- 44V
GND to V- 25V
V_L ..... (GND - 0.3V) to (V+) + 0.3V
Digital Inputs, V_S, V_D (Note 1) ..... (V-) -2V to (V+) + 2V or 30mA, Whichever Occurs First
Continuous Current (Any Terminal) 30mA
Current, S or D (Pulsed 1ms, 10% Duty Cycle) 100mA
Storage Temperature Range (D Suffix) ..... -65°C to +150°C

Thermal Information

Thermal Resistance (Note 3) θ_{JA}
Plastic DIP Package ..... 100°C/W
SOIC Package ..... 120°C/W
Operating Temperature (D Suffix) ..... -40°C to +85°C
Junction Temperature (PDIP, SOIC) ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... ±20V Max
Operating Temperature Range ..... -55°C to +125°C
Input Low Voltage ..... 0.8V Max
Input High Voltage ..... 2.4V Min
Input Rise and Fall Time ..... ≤20ns

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP	D SUFFIX -40°C TO +85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, T_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = ±10V, (See Figure 18)	+25°C	-	150	250	ns
Turn-OFF Time, T_{OFF}						
DG444		+25°C	-	90	120	ns
DG445		+25°C	-	110	170	ns
Charge Injection, Q	C_L = 1nF, V_S = 0V, V_{GEN} = 0V, R_{GEN} = 0Ω	+25°C	-	-1	-	pC
OFF Isolation	R_L = 50Ω, C_L = 5pF, f = 1MHz	+25°C	-	60	-	dB
Crosstalk (Channel-to-Channel)	Any Other Channel Switches R_L = 50Ω, C_L = 5pF, f = 1MHz	+25°C	-	100	-	dB
Source OFF Capacitance, $C_{S(OFF)}$	f = 1MHz	+25°C	-	4	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	f = 1MHz	+25°C	-	4	-	pF
Channel ON Capacitance, $C_{D(ON)}$ + $C_{S(ON)}$	V_{ANALOG} = 0	+25°C	-	16	-	pF
DIGITAL CONTROL						
Input Current V_{IN} Low, I_{IL}	V_{IN} Under Test = 0.8V, All Others = 2.4V	Full	-0.5	-0.00001	0.5	µA
Input Current V_{IN} High, I_{IH}	V_{IN} Under Test = 2.4V, All Others = 0.8V	Full	-0.5	0.00001	0.5	µA
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}		Full	-15	-	15	V
Drain-Source ON Resistance, $R_{DS(ON)}$	I_S = -10mA, V_D = ±8.5V, V+ = 13.5V, V- = -13.5V	+25°C	-	50	85	Ω
		Full	-	-	100	Ω
Switch OFF Leakage Current, $I_{S(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	+25°C	-0.5	0.01	0.5	nA
		Hot	-20	-	20	nA
Switch OFF Leakage Current, $I_{D(OFF)}$	V+ = 16.5V, V- = -16.5V, V_D = ±15.5V, V_S = ∓15.5V	+25°C	-0.5	0.01	0.5	nA
		Hot	-20	-	20	nA
Channel ON Leakage Current, $I_{D(ON)}$ + $I_{S(ON)}$	V+ = 16.5V, V- = -16.5V V_S = V_D = ±15.5V	+25°C	-0.5	0.08	0.5	nA
		Hot	-40	-	40	nA

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP	D SUFFIX -40°C TO +85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 16.5V, V- = -16.5V, V_{IN} = 0V or 5V	+25°C	-	0.001	1	µA
		Hot	-	-	5	µA
Negative Supply Current, I-		+25°C	-1	-0.0001	-	µA
		Hot	-5	-	-	µA
Logic Supply Current, I_L		+25°C	-	0.001	1	µA
		Hot	-	-	5	µA
Ground Current, I_{GND}		+25°C	-1	-0.001	-	µA
		Hot	-5	-	-	µA

Electrical Specifications (Unipolar Supplies) Test Conditions: V+ = +12V, V- = 0V, V_L = 5V, V_{IN} = 2.4V, 0.8V (Note 3), Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 4) TEMP	D SUFFIX -40°C TO +85°C (NOTE 5) MIN	(NOTE 6) TYP	(NOTE 5) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, T_{ON}	R_L = 1kΩ, C_L = 35pF, V_S = 8V, (See Figure 18)	+25°C	-	300	400	ns
Turn-OFF Time, T_{OFF}		+25°C	-	60	200	ns
Charge Injection, Q	C_L = 1nF, V+ = 12V, V_{GEN} = 6V, R_{GEN} = 0Ω	+25°C	-	2	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}	(Note 5)	Full	0	-	12	V
Drain-Source ON Resistance, $R_{DS(ON)}$	I_S = -10mA, V_D = 3V, 8V V+ = 10.8V, V_L = 5.25V	+25°C	-	100	160	Ω
		Full	-	-	200	Ω
POWER SUPPLIES						
Positive Supply Current, I+	V+ = 13.2V, V_{IN} = 0V or 5V	+25°C	-	0.001	1	µA
		Full	-	-	5	µA
Negative Supply Current, I-	V_{IN} = 0V or 5V	+25°C	-1	-0.0001	-	µA
		Full	-5	-	-	µA
Logic Supply Current, I_L	V_L = 5.25V, V_{IN} = 0V or 5V	+25°C	-	0.001	1	µA
		Full	-	-	5	µA
Ground Current, I_{GND}	V_{IN} = 0V or 5V	+25°C	-1	-0.001	-	µA
		Full	-5	-	-	µA

NOTES:

1. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. All leads welded or soldered to PC Board.
3. V_{IN} = input voltage to perform proper function.
4. Hot = as determined by the operating temperature suffix.
5. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
7. Guaranteed by design, not subject to production test.

Typical Performance Curves

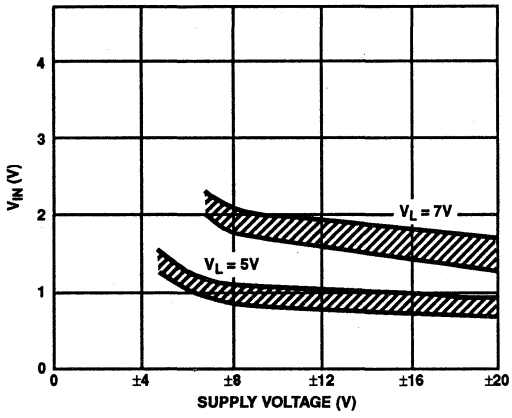


FIGURE 1. SWITCHING THRESHOLD vs SUPPLY VOLTAGE

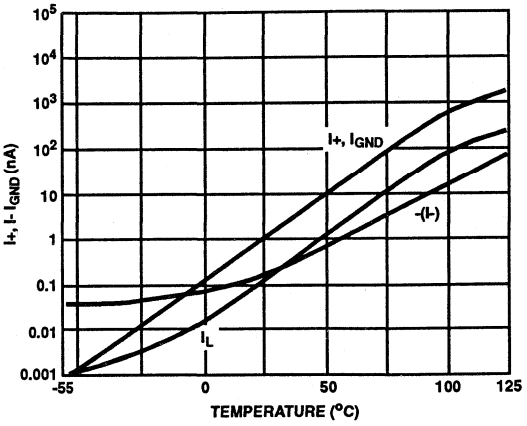


FIGURE 2. SUPPLY CURRENT vs TEMPERATURE

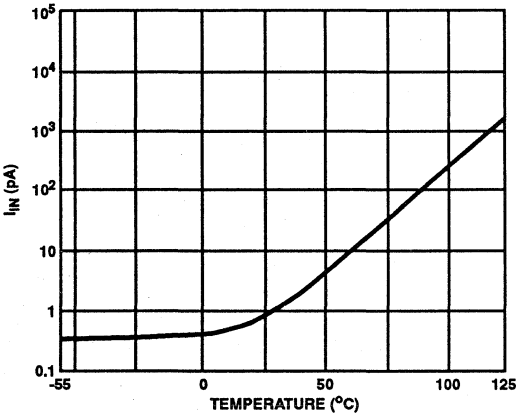


FIGURE 3. INPUT CURRENT vs TEMPERATURE

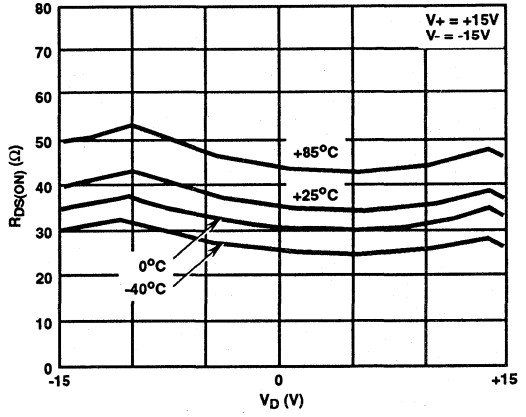


FIGURE 4. $R_{DS(ON)}$ vs V_D AND TEMPERATURE

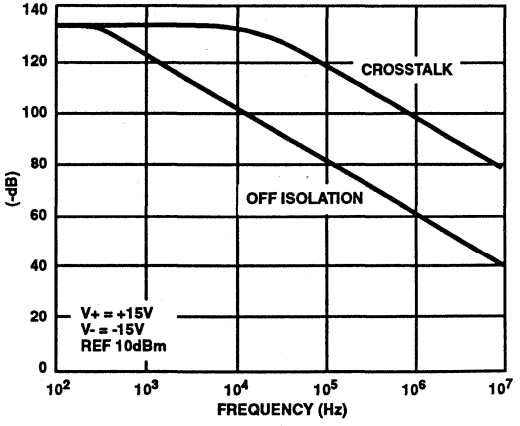


FIGURE 5. CROSSTALK AND OFF ISOLATION vs FREQUENCY

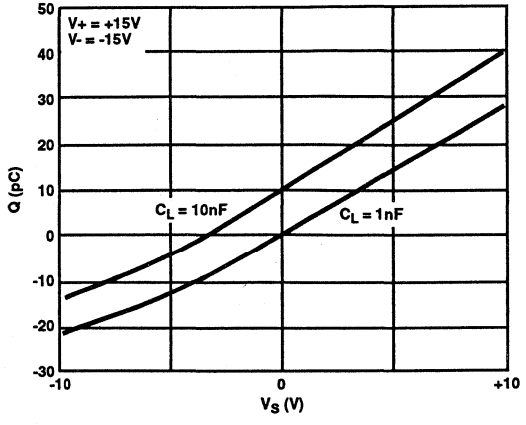


FIGURE 6. CHARGE INJECTION vs SOURCE VOLTAGE

Typical Performance Curves (Continued)

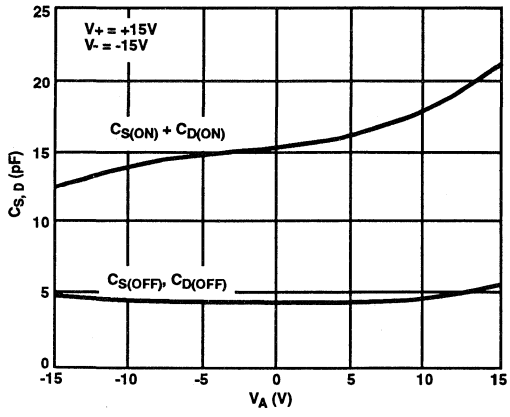


FIGURE 7. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

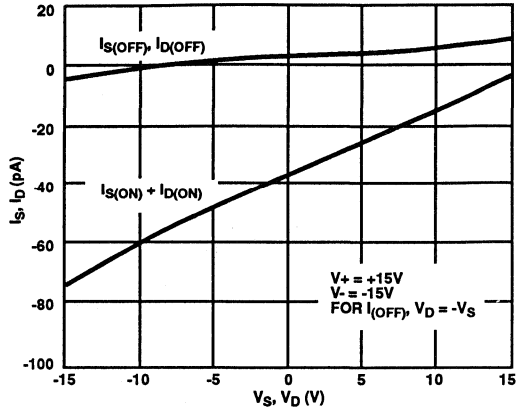


FIGURE 8. SOURCE/DRAIN LEAKAGE CURRENTS

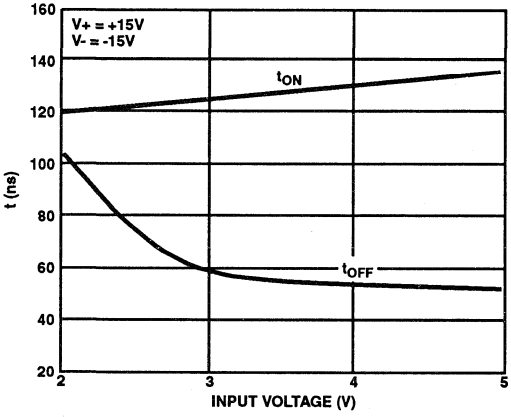


FIGURE 9. SWITCHING TIME vs INPUT VOLTAGE

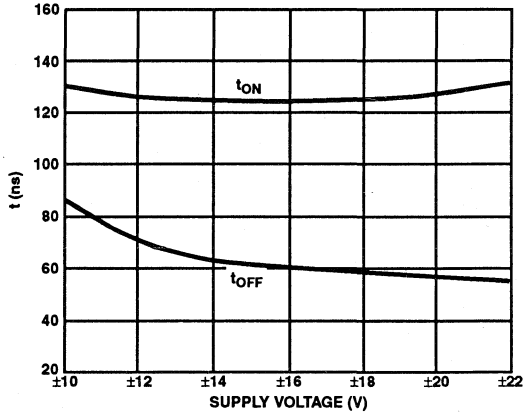


FIGURE 10. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG444)

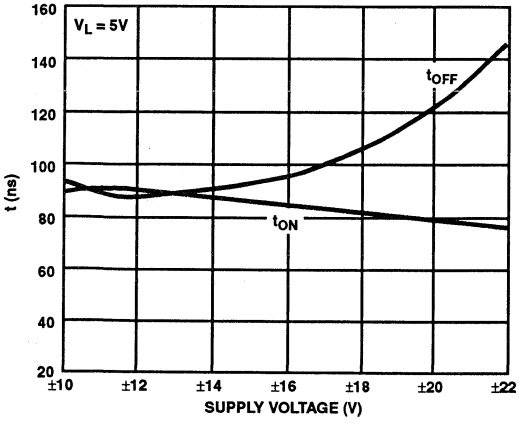


FIGURE 11. SWITCHING TIME vs POWER SUPPLY VOLTAGE (DG445)

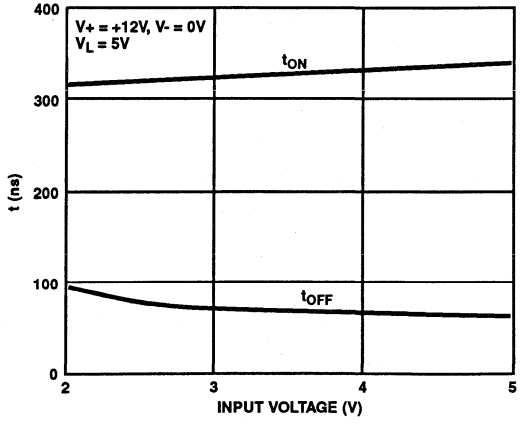


FIGURE 12. SWITCHING TIME vs INPUT VOLTAGE (DG444)

Typical Performance Curves (Continued)

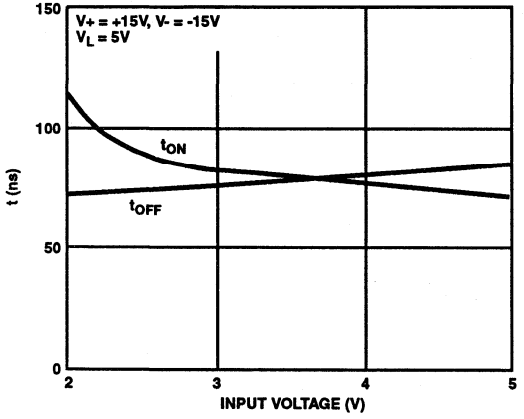


FIGURE 13. SWITCHING TIME vs INPUT VOLTAGE (DG445)

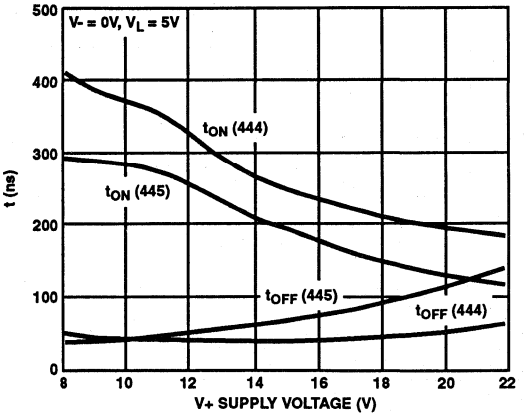


FIGURE 14. SWITCHING TIMES vs POWER SUPPLY VOLTAGE

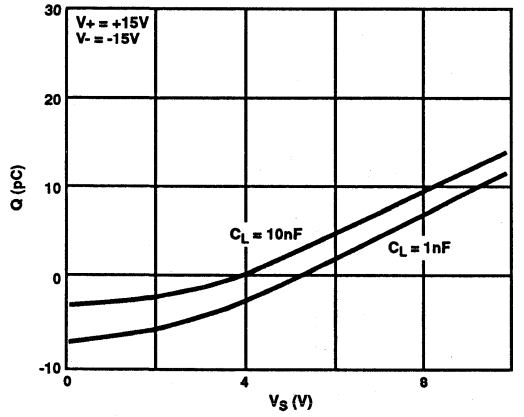


FIGURE 15. CHARGE INJECTION vs SOURCE VOLTAGE (SINGLE 12V SUPPLY)

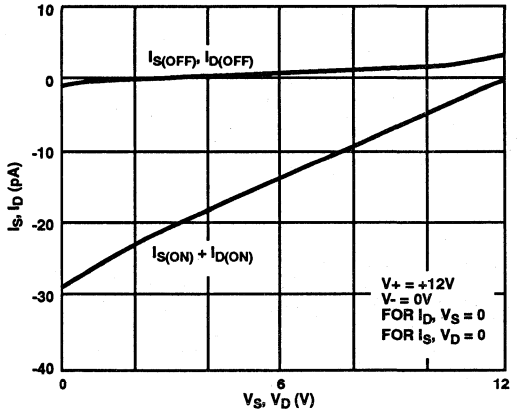


FIGURE 16. SOURCE/DRAIN LEAKAGE CURRENTS (SINGLE 12V SUPPLY)

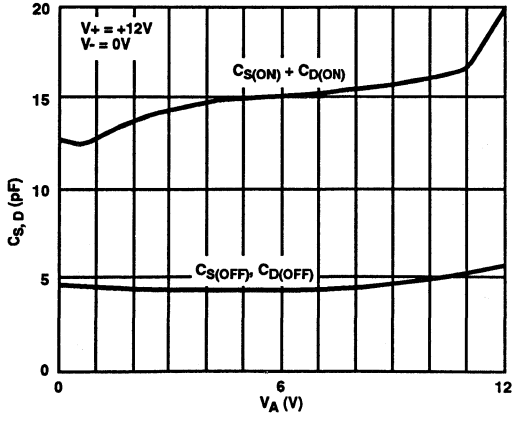


FIGURE 17. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

Pin Description

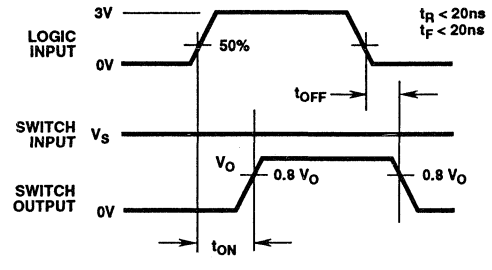
PIN	SYMBOL	DESCRIPTION
1	IN_1	Logic control for switch 1
2	D_1	Drain (output) terminal for switch 1
3	S_1	Source (input) terminal for switch 1
4	V-	Negative power supply terminal
5	GND	Ground terminal (Logic Common)
6	S_4	Source (input) terminal for switch 4
7	D_4	Drain (output) terminal for switch 4
8	IN_4	Logic control for switch 4
9	IN_3	Logic control for switch 3
10	D_3	Drain (output) terminal for switch 3
11	S_3	Source (input) terminal for switch 3
12	V_L	Logic reference voltage.
13	V+	Positive power supply terminal (substrate)
14	S_2	Source (input) terminal for switch 2
15	D_2	Drain (output) terminal for switch 2
16	IN_2	Logic control for switch 2

TRUTH TABLE

LOGIC	V_{IN}	DG444	DG445
0	≤0.8V	ON	OFF
1	≥2.4V	OFF	ON

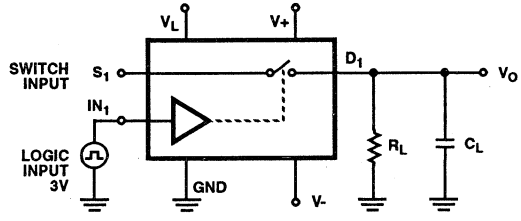
Test Circuits

V_O is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.



NOTE: Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 18A.



Repeat test for Channels 2, 3 and 4.
For load conditions, see Specifications C_L (includes fixture and stray capacitance)

$$V_O = V_S \frac{R_L}{R_L + r_{DS(ON)}}$$

FIGURE 18B.

FIGURE 18. SWITCHING TIME

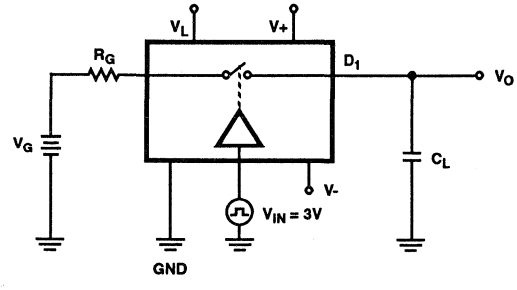


FIGURE 19A.

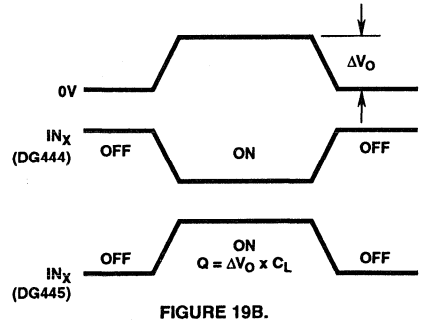


FIGURE 19B.

FIGURE 19. CHARGE INJECTION

Test Circuits (Continued)

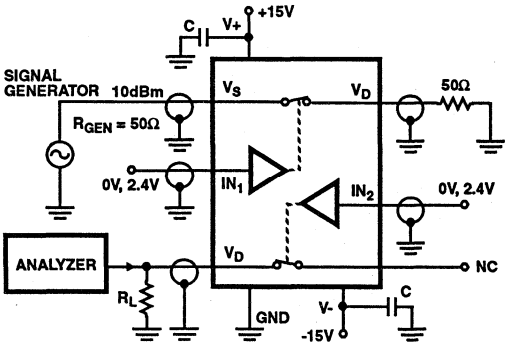


FIGURE 20. CROSSTALK

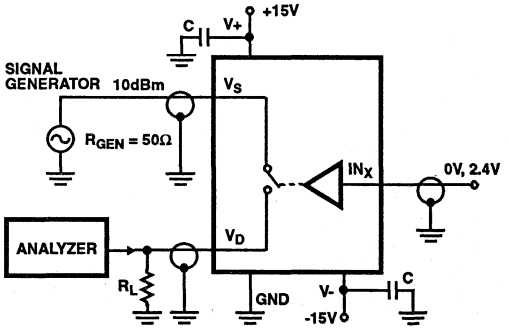


FIGURE 21. OFF ISOLATION

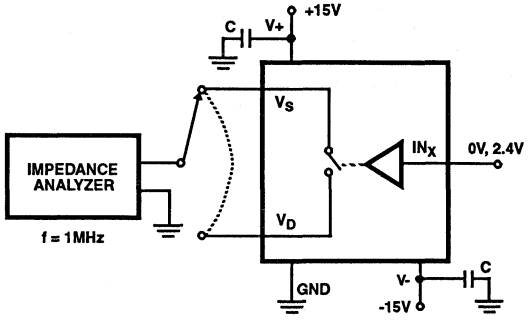
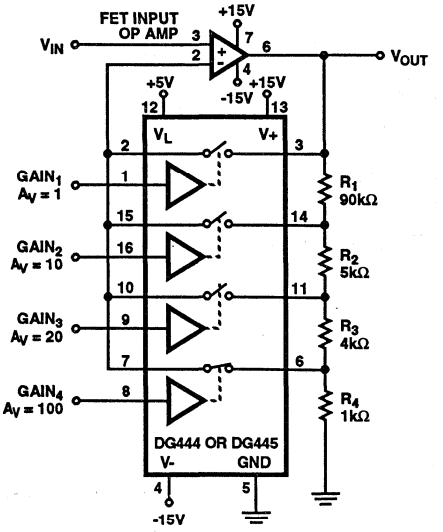


FIGURE 22. SOURCE/DRAIN CAPACITANCES

Typical Applications



GAIN ERROR IS DETERMINED ONLY BY THE RESISTOR TOLERANCE, OP AMP OFFSET AND CMRR WILL LIMIT ACCURACY OR CIRCUIT

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1 + R_2 + R_3 + R_4}{R_4} = 100$$

WITH SW_4 CLOSED

FIGURE 23. PRECISION WEIGHTED RESISTOR PROGRAMMABLE GAIN AMPLIFIER

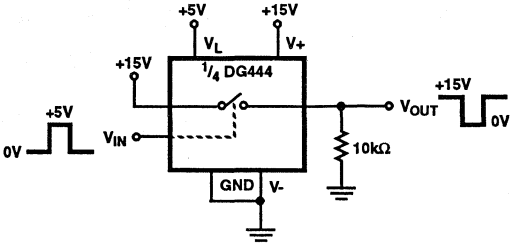


FIGURE 24. LEVEL SHIFTER

Die Characteristics

DIE DIMENSIONS:
2160µm x 1760µm x 485 ± 25µm

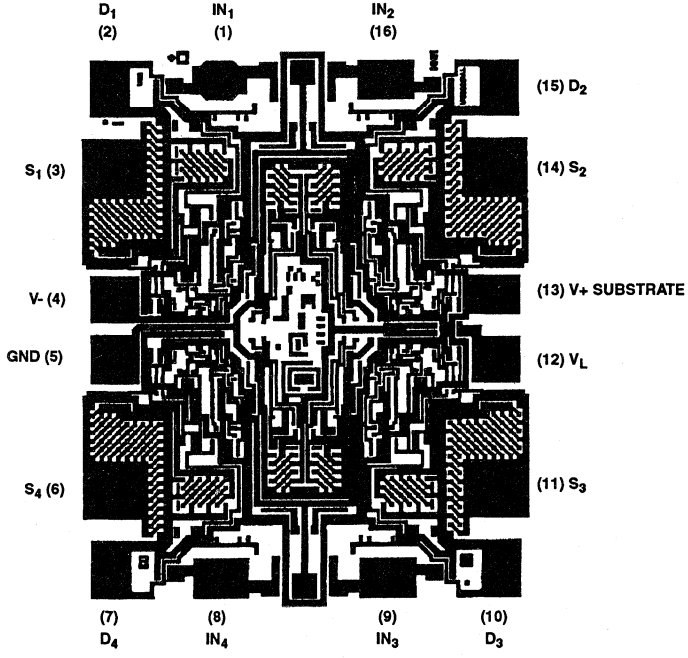
METALLIZATION:
Type: CuAl
Thickness: 12kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
$9.1 \times 10^4 A/cm^2$

Metallization Mask Layout

DG444, DG445



HARRIS SEMICONDUCTOR

HI-200, HI-201

December 1993

Dual/Quad SPST CMOS Analog Switches

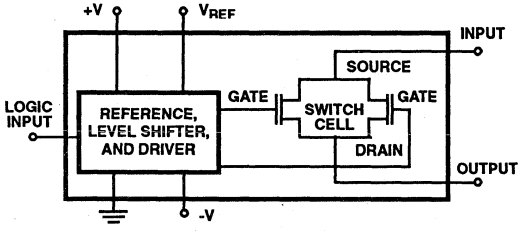
Features

- Analog Voltage Range ..... ±15V
- Analog Current Range..... 80mA
- Turn-On Time 240ns
- Low R_{ON} 55Ω
- Low Power Dissipation 15mW
- TTL/CMOS Compatible

Applications

- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks

Functional Diagram



Description

HI-200/HI-201 are monolithic devices comprising independently selectable SPST switches which feature fast switching speeds (HI-200 240ns, and HI-201 185ns) combined with low power dissipation (15mW at +25°C). Each switch provides low "ON" resistance operation for input signal voltage up to the supply rails and for signal current up to 80mA. Rugged DI construction eliminates latch-up and substrate SCR failure modes.

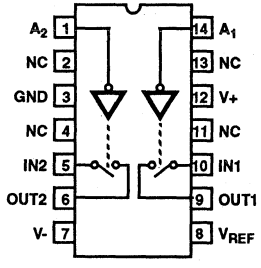
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200/HI-201 are ideal components for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters, and operational amplifier gain switching networks.

HI-200 is a dual SPST CMOS analog switch available in DIP and (TO-99) metal cans and is pin compatible with other available "200 series" switches. For Mil-Std-883 compliant parts, request the HI-200/883 data sheet.

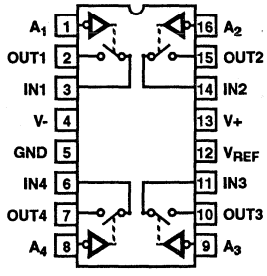
HI-201 is a quad SPST CMOS analog switch available in DIP and SOIC package and pin compatible with other available "200 series" switches. For Mil-Std-883 compliant parts, request the HI-201/883 data sheet.

Pinouts

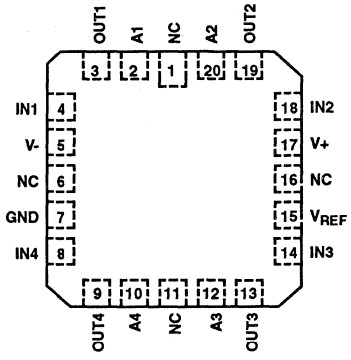
HI-200 (CDIP, PDIP, SOIC)
TOP VIEW



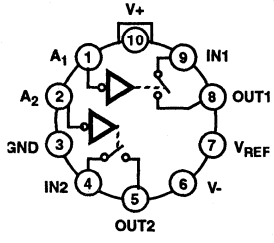
HI-201 (CDIP, PDIP, SOIC)
TOP VIEW



HI-201 (20 PIN PLCC, CLCC)
TOP VIEW



HI-200 (CAN)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

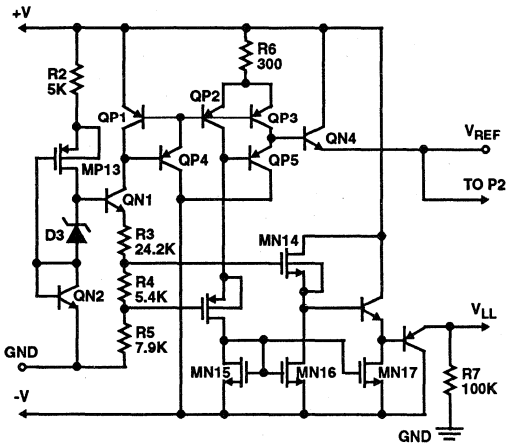
File Number 3121

Ordering Information

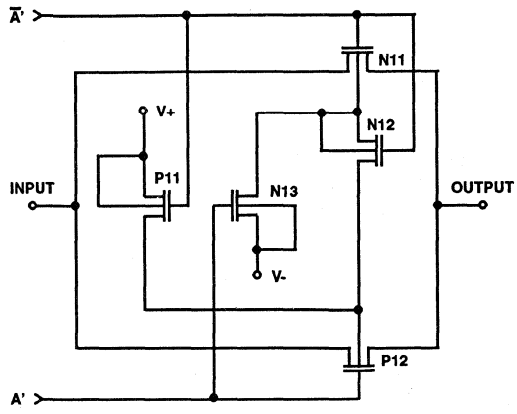
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI2-0200-5	0°C to +75°C	10 Pin Metal Can
HI1-0200-5	0°C to +75°C	14 Lead Ceramic DIP
HI2-0200-4	-25°C to +85°C	10 Pin Metal Can
HI3-0200-5	0°C to +75°C	14 Lead Plastic DIP
HI2-0200-7	0°C to +75°C +96 Hr. Burn-In	10 Pin Metal Can
HI1-0200-7	0°C to +75°C +96 Hr. Burn-In	14 Lead Ceramic DIP
HI1-0200-2	-55°C to +125°C	14 Lead Ceramic DIP
HI1-0200-4	-25°C to +85°C	14 Lead Ceramic DIP
HI2-0200-2	-55°C to +125°C	10 Pin Metal Can
HI1-0201-7	0°C to +75°C +96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-0201-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-0201-4	-25°C to +85°C	16 Lead Ceramic DIP
HI4P0201-5	0°C to +75°C	20 Lead PLCC
HI9P0201-5	0°C to +75°C	16 Lead SOIC (W)
HI9P0201-9	-40°C to +85°C	16 Lead SOIC (W)
HI1-0201-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-0201-5	0°C to +75°C	16 Lead Plastic DIP
HI9P0200-5	0°C to +75°C	14 Lead SOIC (N)
HI9P0200-9	-40°C to +85°C	14 Lead SOIC (N)
HI1-0200/883	-55°C to +125°C	14 Lead Ceramic DIP
HI2-0200/883	-55°C to +125°C	10 Pin Metal Can
HI1-0201/883	-55°C to +125°C	16 Lead Ceramic DIP
HI4-0201/883	-55°C to +125°C	20 Lead CLCC

Schematic Diagrams

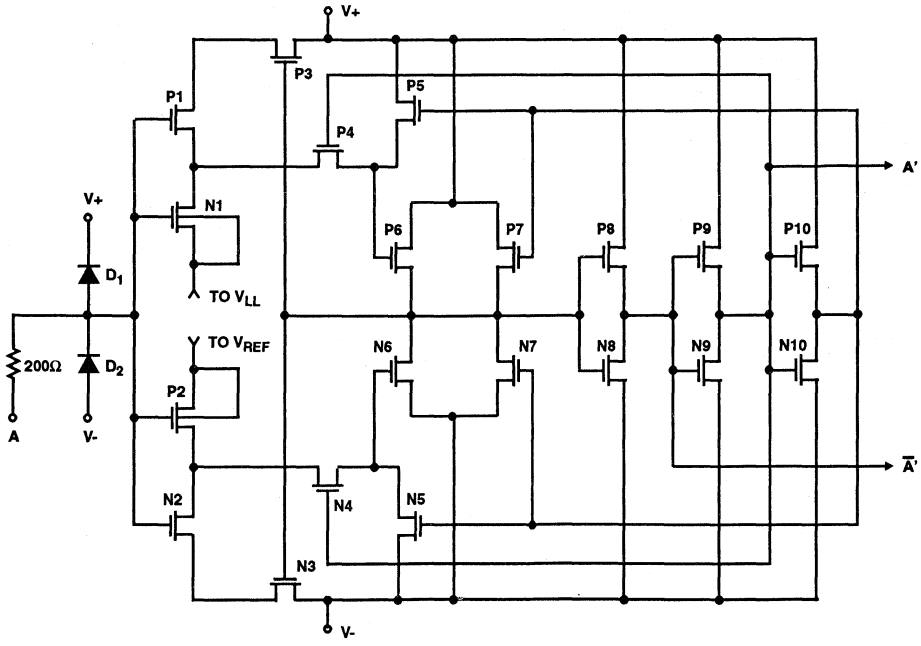
TTL/CMOS REFERENCE CIRCUIT V_{REF} CELL



SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

Supply Voltage ..... 44V (±22)
V_{REF} to Ground ..... +20V, -5V
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage (One Switch) ..... $+V_{SUPPLY}$ +2.0V
$-V_{SUPPLY}$ -2.0V
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	80°C/W	24°C/W
PLCC Package	80°C/W	-
Plastic DIP Package	100°C/W	-
Plastic SOP Package (14 Lead)	120°C/W	-
Plastic SOP Package (16 Lead)	100°C/W	-
Metal Can Package	136°C/W	65°C/W

Operating Temperature Range
HI-200-2, HI-201-2 ..... -55°C to +125°C
HI-200-4, HI-201-4 ..... -25°C to +85°C
HI-200-5, HI-201-5 ..... 0°C to +75°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. HI-200-4 has Same Specifications as HI-200-5 Over -20°C to +85°C Temperature Range

PARAMETER	TEST CONDITIONS	TEMP	HI-200-2, HI-201-2 -55°C TO +125°C			HI-200-5, HI201-5 0°C TO +75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Break-Before-Make Delay, t_{OPEN}	(Note 3)								
HI-200		+25°C	-	60	-	-	60	-	ns
HI-201		+25°C	-	30	-	-	30	-	ns
Switch On Time, t_{ON}									
HI-200		+25°C	-	240	500	-	240	-	ns
HI-201		+25°C	-	185	500	-	185	-	ns
		Full	-	1000	-	-	1000	-	ns
Switch Off Time, t_{OFF}									
HI-200		+25°C	-	330	500	-	500	-	ns
HI-201		+25°C	-	220	500	-	220	-	ns
		Full	-	1000	-	-	1000	-	ns
"Off Isolation"	(Note 4)								
HI-200		+25°C	-	70	-	-	70	-	dB
HI-201		+25°C	-	80	-	-	80	-	dB
Input Switch Capacitance, $C_{S(OFF)}$		+25°C	-	5.5	-	-	5.5	-	pF
Output Switch Capacitance, $C_{D(OFF)}$		+25°C	-	5.5	-	-	5.5	-	pF
Output Switch Capacitance, $C_{D(ON)}$		+25°C	-	11	-	-	11	-	pF
Digital Input Capacitance, C_A		+25°C	-	5	-	-	5	-	pF
Drain-to-Source Capacitance, $C_{D-S(OFF)}$		+25°C	-	0.5	-	-	0.5	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL}		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH}		Full	2.4	-	-	2.4	-	-	V
Input Leakage Current (High or Low), I_A	(Note 2)	Full	-	-	1.0	-	-	1.0	µA

Electrical Specifications Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. HI-200-4 has Same Specifications as HI-200-5 Over -20°C to +85°C Temperature Range **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP	HI-200-2, HI-201-2 -55°C TO +125°C			HI-200-5, HI201-5 0°C TO +75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range, V_S		Full	-15	-	+15	-15	-	+15	V
On Resistance, R_{ON}	(Note 1)	+25°C	-	55	70	-	55	80	Ω
		Full	-	80	100	-	72	100	Ω
Off Input Leakage Current, $I_{S(OFF)}$	(Note 6)	+25°C	-	1	5	-	1	50	nA
HI-200		Full	-	100	500	-	10	500	nA
Off Output Leakage Current, $I_{D(OFF)}$	(Note 6)	+25°C	-	1	5	-	1	50	nA
HI-200		Full	-	100	500	-	10	500	nA
On Leakage Current, $I_{D(ON)}$	(Note 6)	+25°C	-	1	5	-	1	50	nA
HI-200		Full	-	100	500	-	10	500	nA
$I_{S(OFF)}$		+25°C	-	2	5	-	2	50	nA
HI-201		Full	-	-	500	-	-	250	nA
$I_{D(OFF)}$		+25°C	-	2	5	-	2	50	nA
HI-201		Full	-	35	500	-	35	250	nA
$I_{D(ON)}$		+25°C	-	2	5	-	2	50	nA
HI-201		Full	-	-	500	-	-	250	nA
POWER REQUIREMENTS (Note 5)									
Power Dissipation, P_D		+25°C	-	15	-	-	15	-	mW
		Full	-	-	60	-	-	60	mW
Current, I+		+25°C	-	0.5	-	-	0.5	-	mA
		Full	-	-	2.0	-	-	2.0	mA
Current, I-		+25°C	-	0.5	-	-	0.5	-	mA
		Full	-	-	2.0	-	-	2.0	mA

NOTES:

1. V_{OUT} = ± 10V, I_{OUT} = 1mA.
2. Digital Inputs are MOS gates: typical leakage is < 1nA.
3. V_{AH} = 4.0V.
4. V_A = 5V, R_L = 1kΩ, C_L = 10pF, V_S = $3V_{RMS}$, f = 100kHz.
5. V_A = +3V or V_A = 0V for Both Switches.
6. Refer to Leakage Current Measurements (Figure 4).

Performance Curves and Test Circuits T_A = +25°C, V_{SUPPLY} = 15V, V_{AH} = 2.4V, V_{AL} = 0.8V and V_{REF} = Open

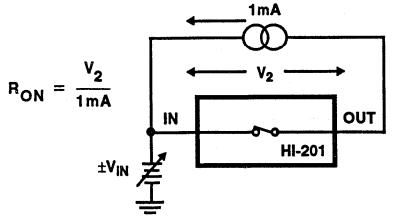


FIGURE 1. ON RESISTANCE vs ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE

Performance Curves and Test Circuits

T_A = +25°C, V_{SUPPLY} = 15V, V_{AH} = 2.4V, V_{AL} = 0.8V and V_{REF} = Open (Continued)

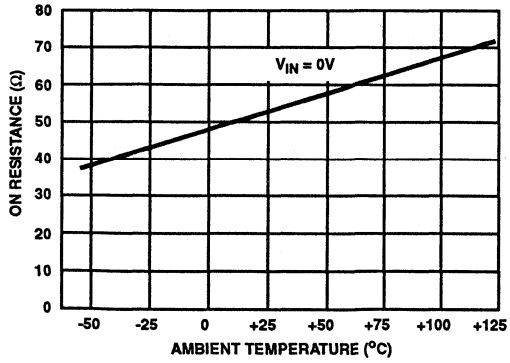


FIGURE 2. ON RESISTANCE vs TEMPERATURE

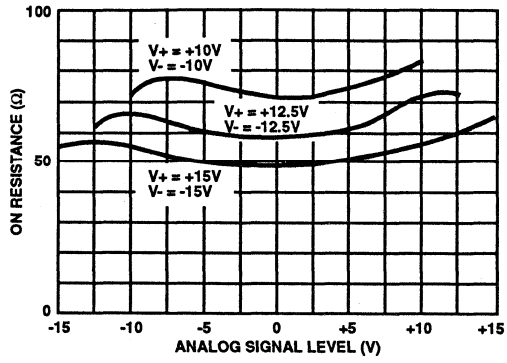


FIGURE 3. HI-201 ON RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

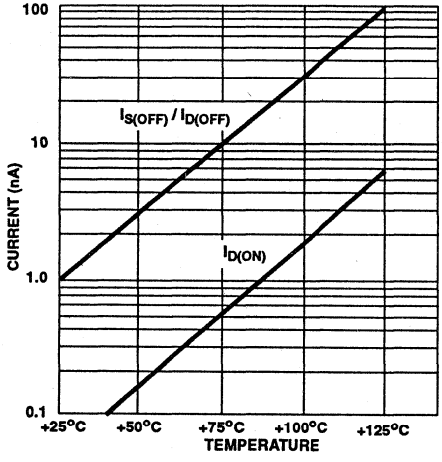


FIGURE 4A. HI-201 SWITCH LEAKAGE CURRENT vs TEMPERATURE

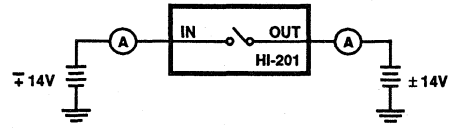


FIGURE 4B. OFF LEAKAGE CURRENT vs TEMPERATURE

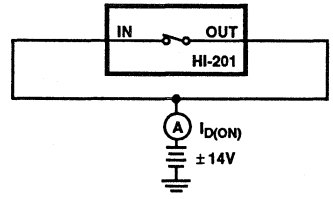


FIGURE 4C. ON LEAKAGE CURRENT vs TEMPERATURE

FIGURE 4.

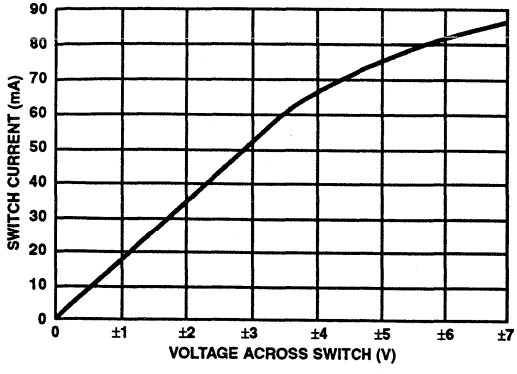


FIGURE 5A.

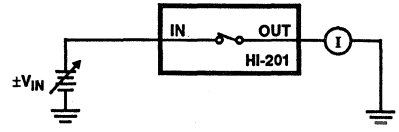


FIGURE 5B.

FIGURE 5. SWITCH CURRENT vs VOLTAGE

Switching Waveforms

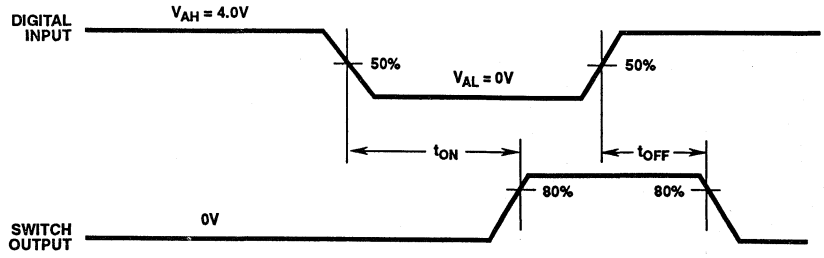
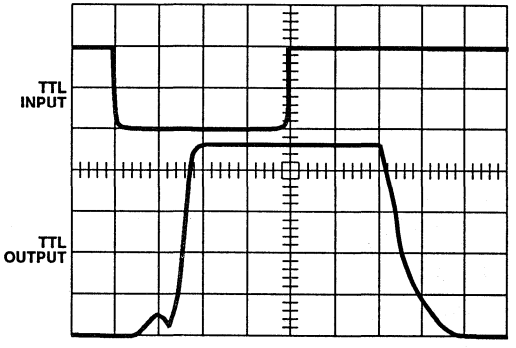


FIGURE 6. LOGIC "0" = SWITCH ON

t_{ON}, t_{OFF} (TTL INPUT), V_{IN} = +4.0V
Vertical: 2V/Div
Horizontal: 100ns/Div.



t_{ON}, t_{OFF} (TTL INPUT), V_{IN} = +15.0V
Vertical: 5V/Div
Horizontal: 100ns/Div.

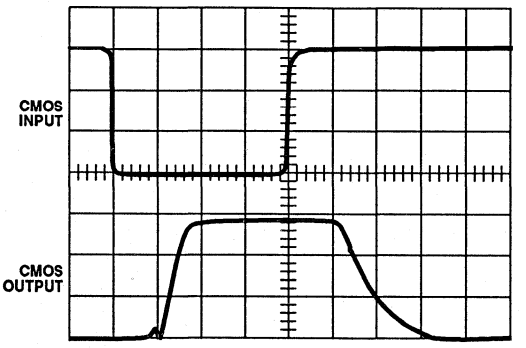


FIGURE 7. TTL INPUT

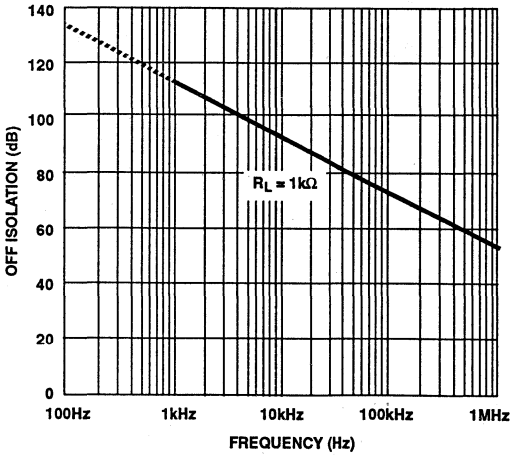


FIGURE 8. OFF ISOLATION vs FREQUENCY

For more information see Application Notes 520, 521, 531, 532 and 557.

Die Characteristics

DIE DIMENSIONS:
54 x 79 x 19 mils

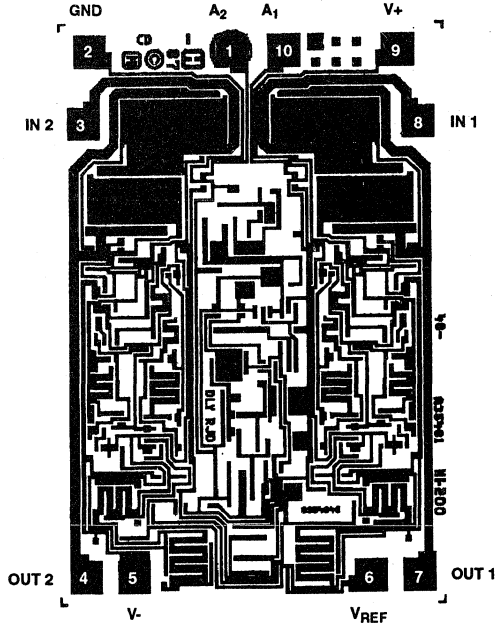
METALLIZATION:
Type: CuAL
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Nitride Thickness: 3.5kÅ ± 1kÅ
Silox Thickness: 12kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
2×10^5 A/cm^2 at 25mA

Metallization Mask Layout

HI-200



Die Characteristics

DIE DIMENSIONS:
81 x 85 x 19 mils

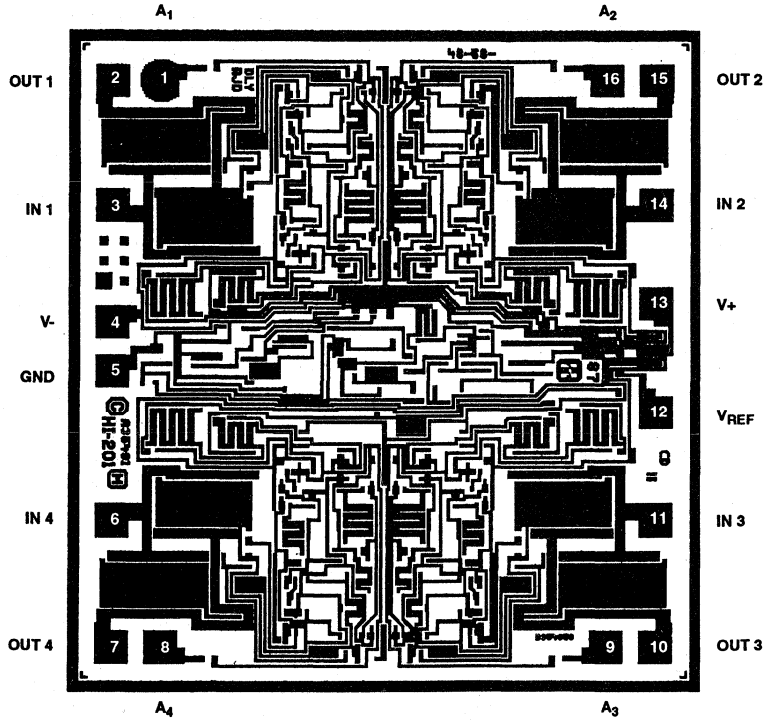
METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride over Silox
Nitride Thickness: 3.5kÅ ± 1kÅ
Silox Thickness: 12kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
2×10^5 A/cm^2 at 25mA

Metallization Mask Layout

HI-201



HARRIS SEMICONDUCTOR

HI-201HS

High Speed Quad SPST CMOS Analog Switch

December 1993

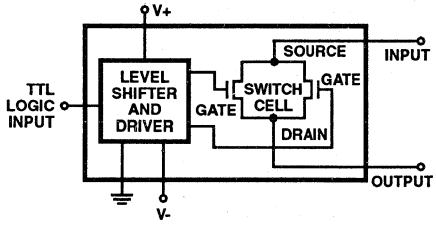
Features

- Fast Switching Times, t_{ON} = 30ns, t_{OFF} = 40ns
- Low "ON" Resistance of 30Ω
- Pin Compatible with Standard HI-201
- Wide Analog Voltage Range (±15V Supplies) of ±15V
- Low Charge Injection (±15V Supplies) 10pC
- TTL Compatible
- Symmetrical Switching Analog Current Range of 80mA

Applications

- High Speed Multiplexing
- High Frequency Analog Switching
- Sample and Hold Circuits
- Digital Filters
- Operational Amplifier Gain Switching Networks
- Integrator Reset Circuits

Functional Diagram



LOGIC	SWITCH
0	ON
1	OFF

Description

The HI-201HS is a monolithic CMOS Analog Switch featuring very fast switching speeds and low ON resistance. The integrated circuit consists of four independently selectable SPST switches and is pin compatible with the industry standard HI-201 switch.

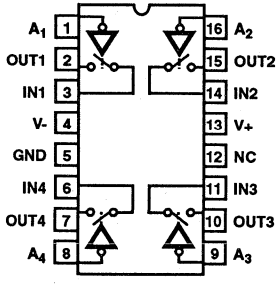
Fabricated using silicon-gate technology and the Harris Dielectric Isolation process, this TTL compatible device offers improved performance over previously available CMOS analog switches. Featuring maximum switching times of 50ns, low ON resistance of 50Ω maximum, and a wide analog signal range, the HI-201HS is designed for any application where improved switching performance, particularly switching speed, is required. (A more detailed discussion on the design and application of the HI-201HS can be found in Application Note 543.)

Ordering Information

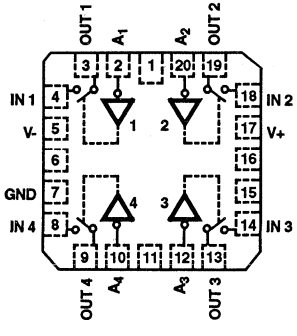
PART NUMBER	TEMP. RANGE	PACKAGE
HI1-0201HS-5	0°C to +75°C	16 Lead Ceramic DIP
HI3-0201HS-4	-25°C to +85°C	16 Lead Plastic DIP
HI1-0201HS-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0201HS-4	-25°C to +85°C	16 Lead Ceramic DIP
HI4P0201HS-5	0°C to +75°C	20 Lead PLCC
HI3-0201HS-5	0°C to +75°C	16 Lead Plastic DIP
HI1-0201HS-7	0°C to +75°C	16 Lead Ceramic DIP
HI4-0201HS/883	-55°C to +125°C	20 Lead LCC
HI9P0201HS-5	0°C to +75°C	16 Lead SOIC (W)
HI9P0201HS-9	-40°C to +85°C	16 Lead SOIC (W)
HI1-0201HS/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0201HS -8	-55°C to +125°C	16 Lead Ceramic DIP

Pinouts

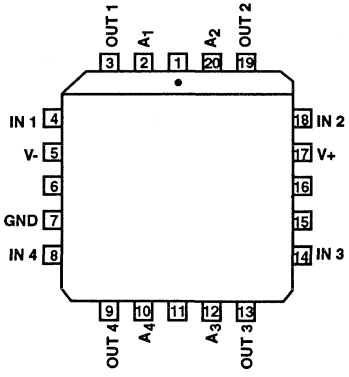
HI-201HS (CDIP, PDIP, SOIC)
TOP VIEW



HI201HS (LCC)
TOP VIEW



HI201HS (PLCC)
TOP VIEW

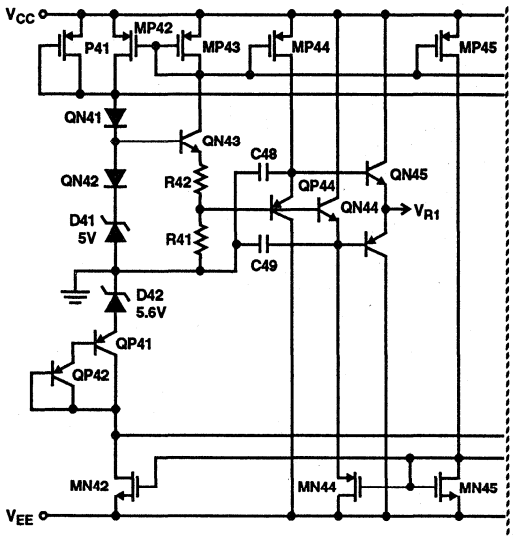


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

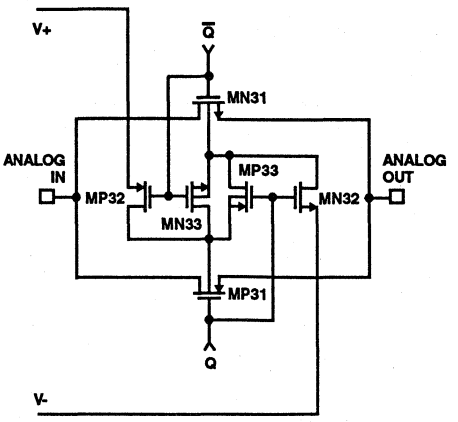
File Number **3123**

Schematic Diagrams

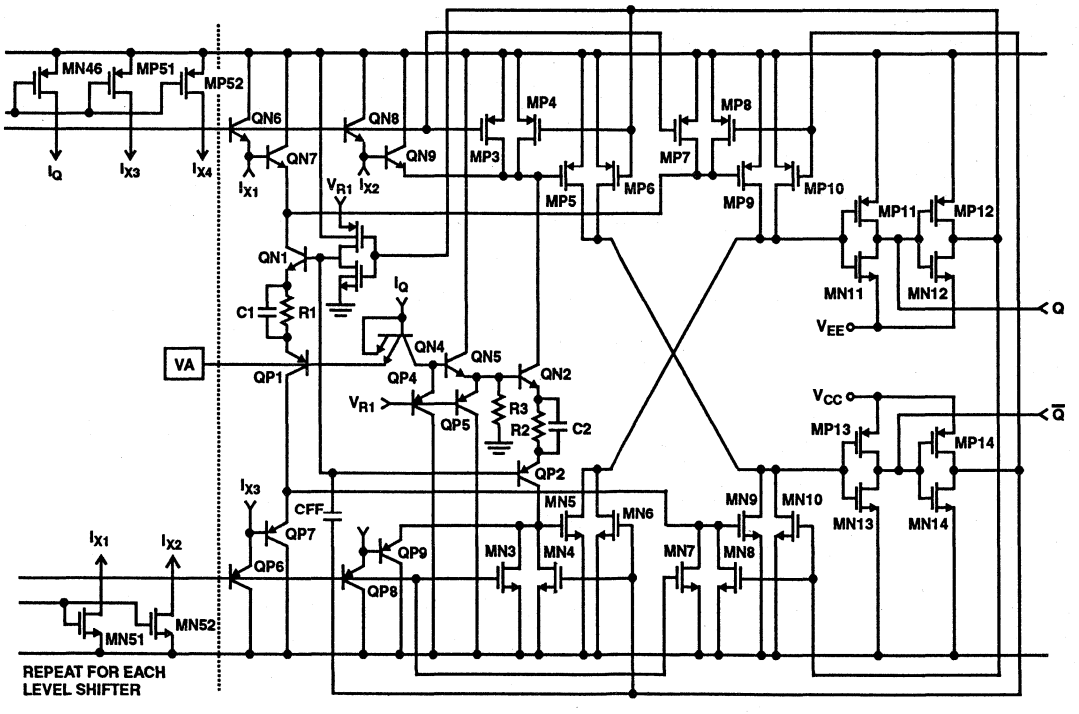
TTL/CMOS REFERENCE CIRCUIT



SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



9 SWITCHES

Absolute Maximum Ratings

Supply Voltage (Between Pins 4 and 13) 36V
Digital Input Voltage (Pins 1, 8, 9, 16) ..... (V+) +4V, (V-) -4V
Analog Input Voltage (One Switch) ..... (V+) +2.0V
Pins 2, 3, 6, 7, 10, 11, 14, 15 ..... (V-) -2.0V
Peak Current (S or D)
(Pulse at 1ms, 10% Duty Cycle Max.) 50mA
Continuous Current Any Terminal (Except S or D) 25mA
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP	80°C/W	24°C/W
Plastic DIP	100°C/W	-
PLCC	80°C/W	-
SOIC	100°C/W	-

Operating Temperature
HI-201HS-2,-8 ..... -55°C to +125°C
HI-201HS-4 ..... -25°C to +85°C
HI-201HS-5,-7 ..... 0°C to +75°C
HI-201HS-9 ..... -40°C to +85°C
Junction Temperature
Ceramic Package ..... +175°C
Plastic Package ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, GND = 0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP	HI-201HS-2/-8			HI-201HS-5/-4/-9/-7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
t_{ON}, Switch On Time	(Note 3)	+25°C	-	30	50	-	30	50	ns
t_{OFF1}, Switch Off Time	(Note 3)	+25°C	-	40	50	-	40	50	ns
t_{OFF2}, Switch Off Time	(Note 3)	+25°C	-	150	-	-	150	-	ns
Output Settling Time 0.1%		+25°C	-	180	-	-	180	-	ns
"Off Isolation"	(Note 4)	+25°C	-	72	-	-	72	-	dB
Crosstalk	(Note 5)	+25°C	-	86	-	-	86	-	dB
Charge Injection	(Note 6)	+25°C	-	10	-	-	10	-	pC
$C_{S(OFF)}$, Input Switch Capacitance		+25°C	-	10	-	-	10	-	pF
$C_{D(OFF)}$, Output Switch Capacitance		+25°C	-	10	-	-	10	-	pF
$C_{D(ON)}$, Output Switch Capacitance		+25°C	-	30	-	-	30	-	pF
C_A, Digital Input Capacitance		+25°C	-	18	-	-	18	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance		+25°C	-	0.5	-	-	0.5	-	pF
DIGITAL INPUT CHARACTERISTICS									
V_{AL}, Input Low Threshold		Full	-	-	0.8	-	-	0.8	V
V_{AH}, Input High Threshold		+25°C	2.0	-	-	2.0	-	-	V
		Full	2.4	-	-	2.4	-	-	V
I_{AL}, Input Leakage Current (Low)		+25°C	-	-200	-	-	-200	-	µA
		Full	-	-	-500	-	-	-500	µA
I_{AH}, Input Leakage Current (High)	V_{AH} = 4.0V	+25°C	-	20	-	-	20	-	µA
		Full	-	-	+40	-	-	+40	µA
ANALOG SWITCH CHARACTERISTICS									
V_S, Analog Signal Range		Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance	(Note 2)	+25°C	-	30	50	-	30	50	Ω
		Full	-	-	75	-	-	75	Ω
R_{ON} Match		+25°C	-	3	-	-	3	-	%

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, GND = 0V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP	HI-201HS-2/-8			HI-201HS-5/-4/-9/-7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{S(OFF)}$, Off Input Leakage Current		+25°C	-	0.3	10	-	0.3	10	nA
		Full	-	-	100	-	-	50	nA
$I_{D(OFF)}$, Off Output Leakage Current		+25°C	-	0.3	10	-	0.3	10	nA
		Full	-	-	100	-	-	50	nA
$I_{D(ON)}$, On Leakage Current		+25°C	-	0.1	10	-	0.1	10	nA
		Full	-	-	100	-	-	50	nA
POWER SUPPLY CHARACTERISTICS (Note 7)									
P_D, Power Dissipation		+25°C	-	120	-	-	120	-	mW
		Full	-	-	240	-	-	240	mW
I+, Current (Pin 13)		+25°C	-	4.5	-	-	4.5	-	mA
		Full	-	-	10.0	-	-	10.0	mA
I-, Current (Pin 4)		+25°C	-	3.5	-	-	3.5	-	mA
		Full	-	-	6	-	-	6	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. $V_{OUT} = \pm 10V$, $I_{OUT} = 1mA$.
3. $R_L = 1k\Omega$, $C_L = 35pF$, $V_{IN} = +10V$, $V_A = +3V$. (See Switching Waveforms).
4. $V_A = 3V$, $R_L = 1k\Omega$, $C_L = 10pF$, $V_{IN} = 3V_{RMS}$, f = 100kHz.
5. $V_A = 3V$, $R_L = 1k\Omega$, $V_{IN} = 3V_{RMS}$, f = 100kHz.
6. $C_L = 1000pF$, $V_{IN} = 0V$, $R_{IN} = 0V$, $\Delta Q = C_L \times \Delta V_O$.
7. $V_A = 3V$ or $V_A = 0$ for all switches.

Switching Waveforms

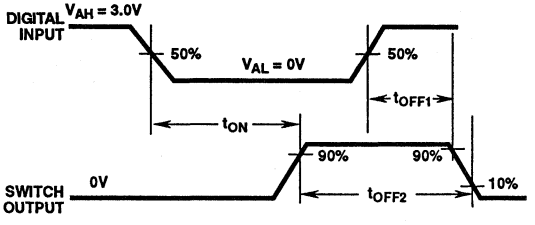
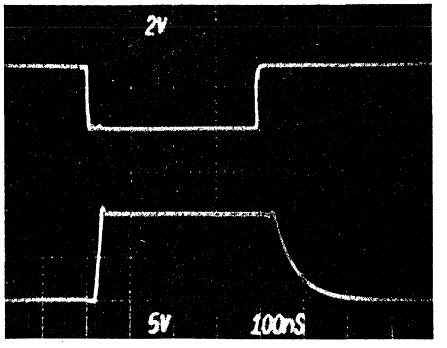


FIGURE 1A.



TOP: TTL Input (2V/Div.) BOTTOM: Output (5V/Div.)
HORIZONTAL: 100ns/Div.

FIGURE 1B.

FIGURE 1. SWITCH t_{ON} AND t_{OFF} TIMES

Typical Performance Curves

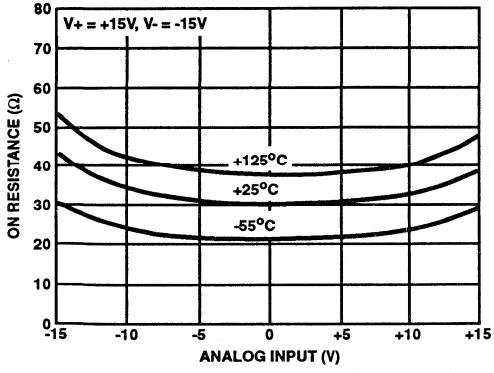


FIGURE 2. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL AND TEMPERATURE

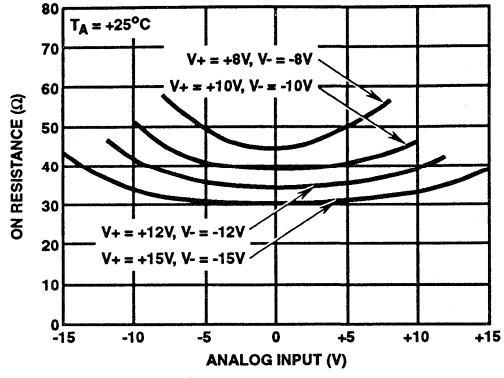


FIGURE 3. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

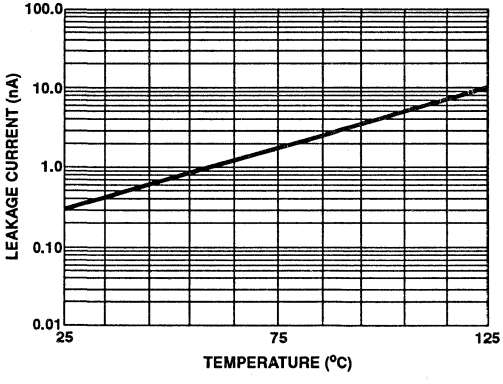


FIGURE 4. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE†

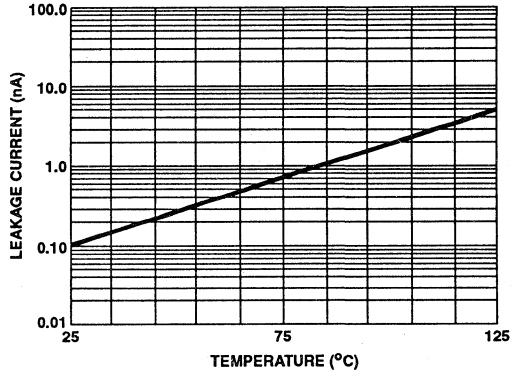


FIGURE 5. $I_{D(ON)}$ vs TEMPERATURE†

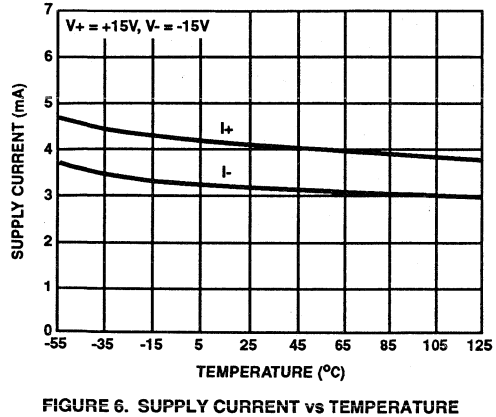


FIGURE 6. SUPPLY CURRENT vs TEMPERATURE

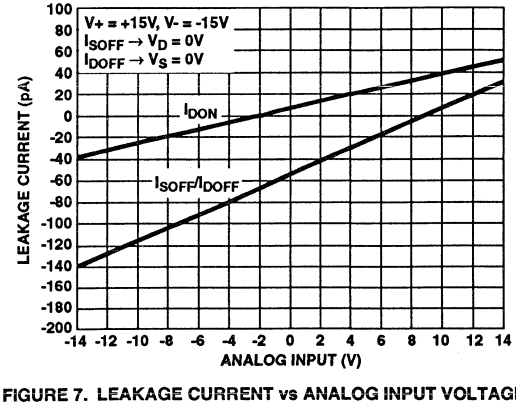


FIGURE 7. LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE

† Theoretically, leakage current will continue to decrease below +25°C. But due to environmental conditions, leakage measurements below this temperature are not representative of actual switch performance.

Typical Performance Curves (Continued)

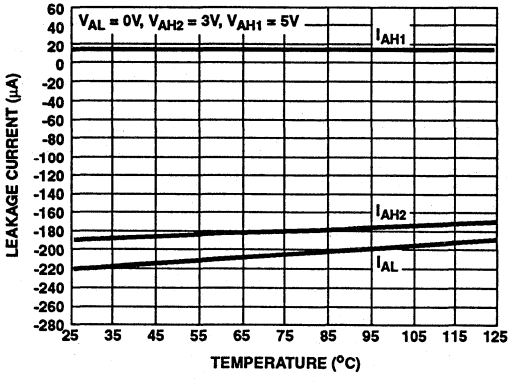


FIGURE 8. DIGITAL INPUT LEAKAGE CURRENT vs TEMPERATURE†

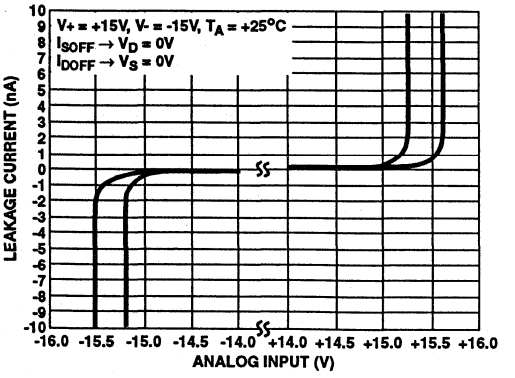


FIGURE 9. LEAKAGE CURRENT vs ANALOG INPUT VOLTAGE

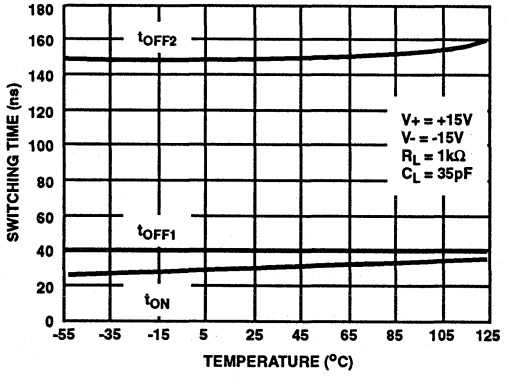


FIGURE 10. SWITCHING TIME vs TEMPERATURE

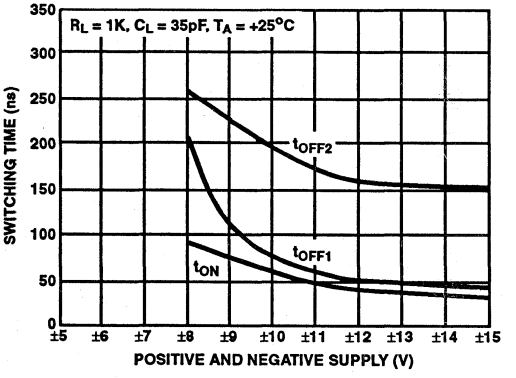


FIGURE 11. SWITCHING TIME vs POSITIVE AND NEGATIVE SUPPLY VOLTAGE

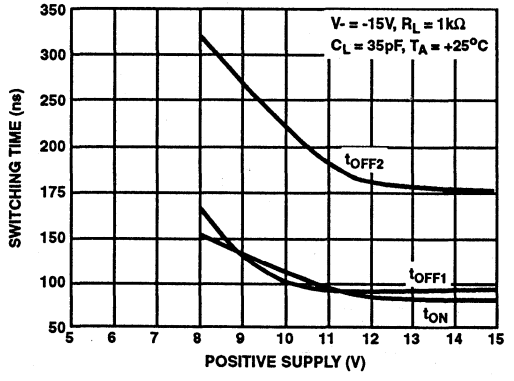


FIGURE 12. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE

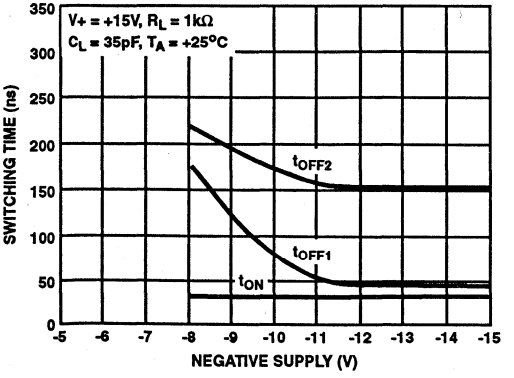


FIGURE 13. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE

† Theoretically, leakage current will continue to decrease below +25°C. But due to environmental conditions, leakage measurements below this temperature are not representative of actual switch performance.

Typical Performance Curves (Continued)

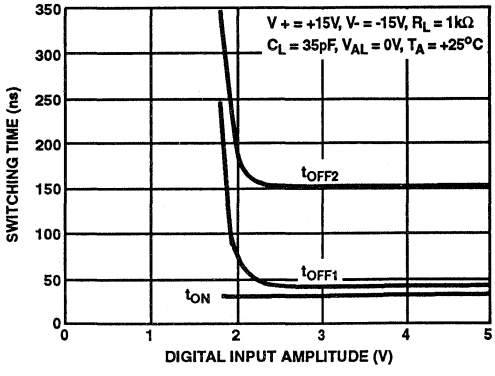


FIGURE 14. SWITCHING TIME vs INPUT LOGIC AMPLITUDE

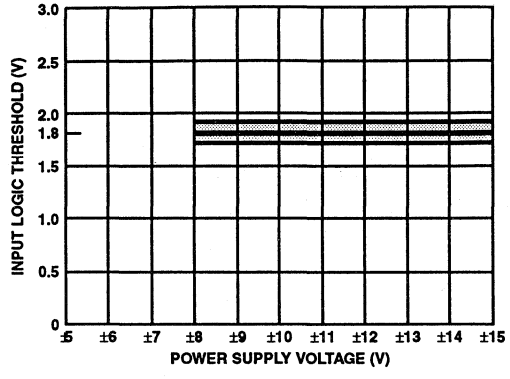


FIGURE 15. INPUT SWITCHING THRESHOLD vs POSITIVE AND NEGATIVE SUPPLY VOLTAGES

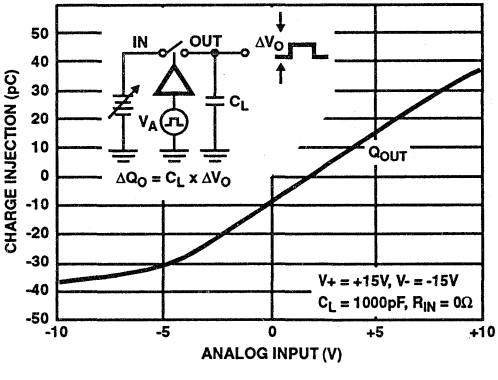


FIGURE 16. CHARGE INJECTION vs ANALOG INPUT

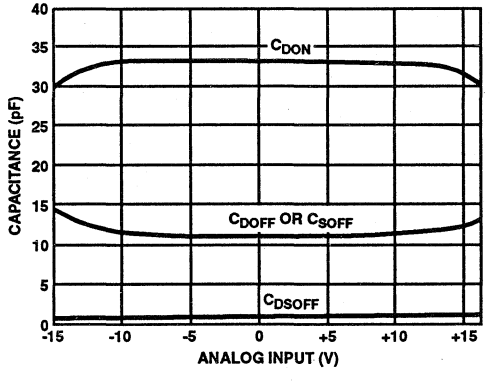


FIGURE 17. CAPACITANCE vs ANALOG INPUT

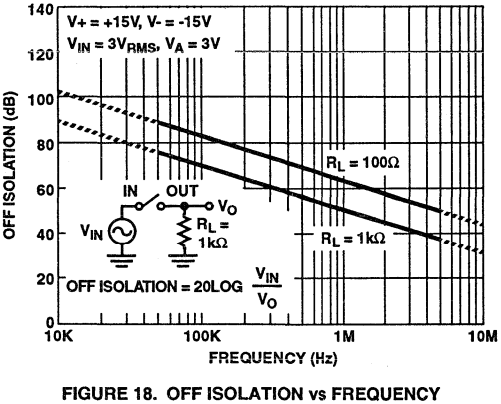


FIGURE 18. OFF ISOLATION vs FREQUENCY

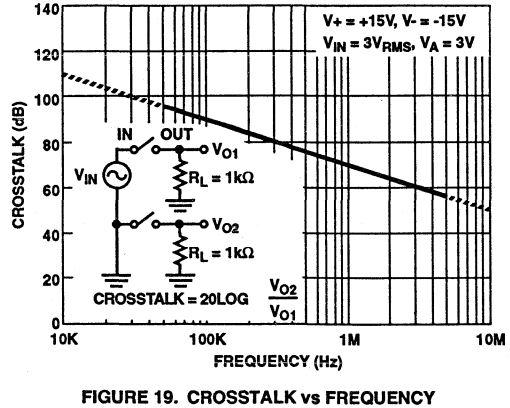


FIGURE 19. CROSSTALK vs FREQUENCY

Test Circuit

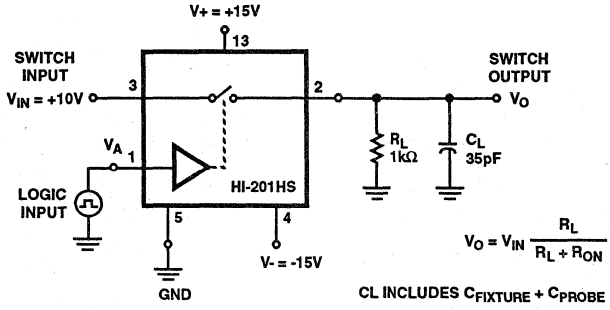


FIGURE 20. SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF1}, t_{OFF2})

Switching Characteristics

Typical delay, t_{ON}, t_{OFF}, settling time and switching transients in this circuit. If R_L or C_L is increased, there will be corresponding increases in rise and/or fall RC times..

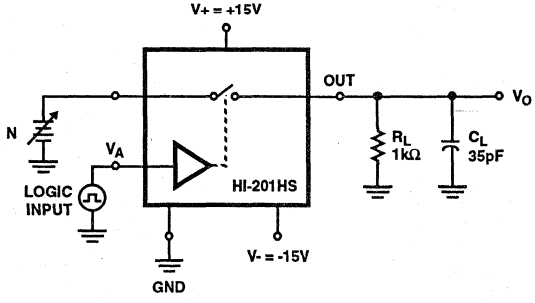


FIGURE 21A.

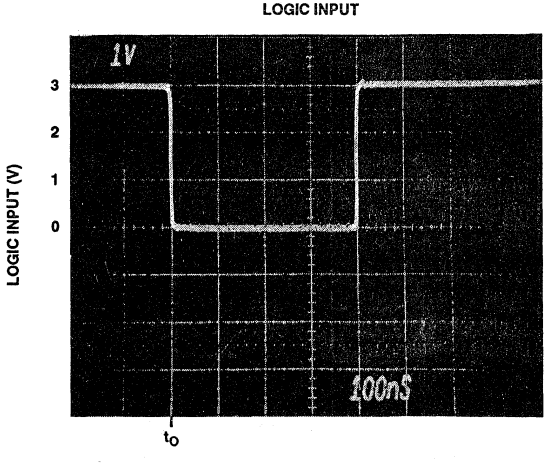
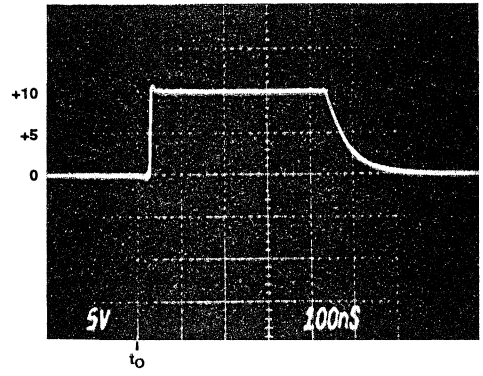


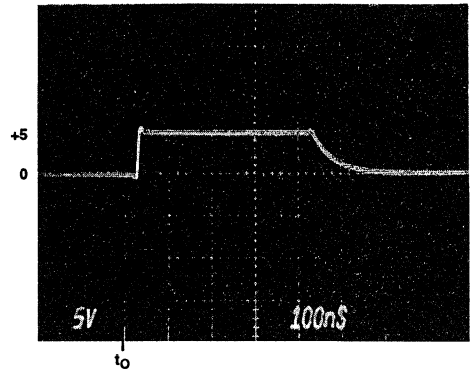
FIGURE 21B.

FIGURE 21. SWITCHING CHARACTERISTICS vs INPUT VOLTAGE

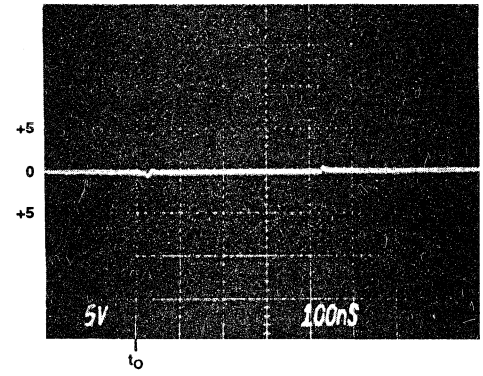
Switching Characteristics (Continued)



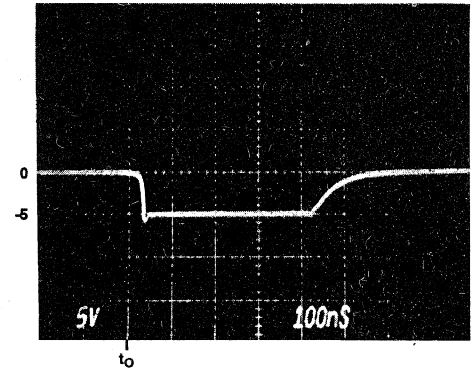
22A. V_{IN} = +10V



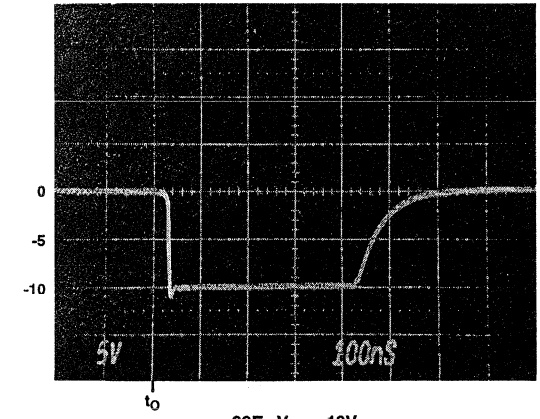
22B. V_{IN} = +5V



22C. V_{IN} = 0V



22D. V_{IN} = -5V



22E. V_{IN} = -10V

FIGURE 22. V_O - OUTPUT SWITCHING WAVEFORMS

Application Information

Logic Compatibility

The HI-201HS is TTL compatible. Its logic inputs (Pins 1, 8, 9, 16) are designed to react to digital inputs which exceed a fixed, internally generated TTL switching threshold. The HI-201HS can also be driven with CMOS logic (0V-15V), although the switch performance with CMOS logic will be inferior to that with TTL logic (0V-5V).

The logic input design of the HI-201HS is largely responsible for its fast switching speed. It is a design which features a unique input stage consisting of complementary vertical PNP and NPN bipolar transistors. This design differs from that of the standard HI-201 product where the logic inputs are MOS transistors.

Although the new logic design enhances the switching speed performance, it also increases the logic input leakage currents. Therefore, the HI-201HS will exhibit larger digital input leakage currents in comparison to the standard HI-201 product.

Charge Injection

Charge injection is the charge transferred, through the internal gate-to-channel capacitances, from the digital logic input to the analog output. To optimize charge injection performance for the HI-201HS, it is advisable to provide a TTL logic input with fast rise and fall times.

If the power supplies are reduced from ±15V, charge injection will become increasingly dependent upon the digital input frequency. Increased logic input frequency will result in larger output error due to charge injection.

Power Supply Considerations

The electrical characteristics specified in this data sheet are guaranteed for power supplies $\pm V_S = \pm 15V$. Power supply voltages less than ±15V will result in reduced switch performance. The following information is intended as a design aid only.

POWER SUPPLY VOLTAGES	SWITCH PERFORMANCE
$\pm 12 < \pm V_S \pm 15V$	Minimal Variation
$\pm V_S < \pm 12V$	Parametric variation becomes increasingly large (increased ON resistance, longer switching times).
$\pm V_S < \pm 10V$	Not Recommended.
$\pm V_S > \pm 16V$	Not Recommended.

Single Supply

The switch operation of the HI-201HS is dependent upon an internally generated switching threshold voltage optimized for ±15V power supplies. The HI-201HS does not provide the necessary internal switching threshold in a single supply system. Therefore, if single supply operation is required, the HI-300 series of switches is recommended. The HI-300 series will remain operational to a minimum +5V single supply.

Switch performance will degrade as power supply voltage is reduced from optimum levels (±15V). So it is recommended that a single supply design be thoroughly evaluated to ensure that the switch will meet the requirements of the application.

For Further Information See Application Notes 520, 521, 531, 532, 543 and 557.

Die Characteristics

DIE DIMENSIONS:
2440µm x 2860µm x 485µm ± 25µm

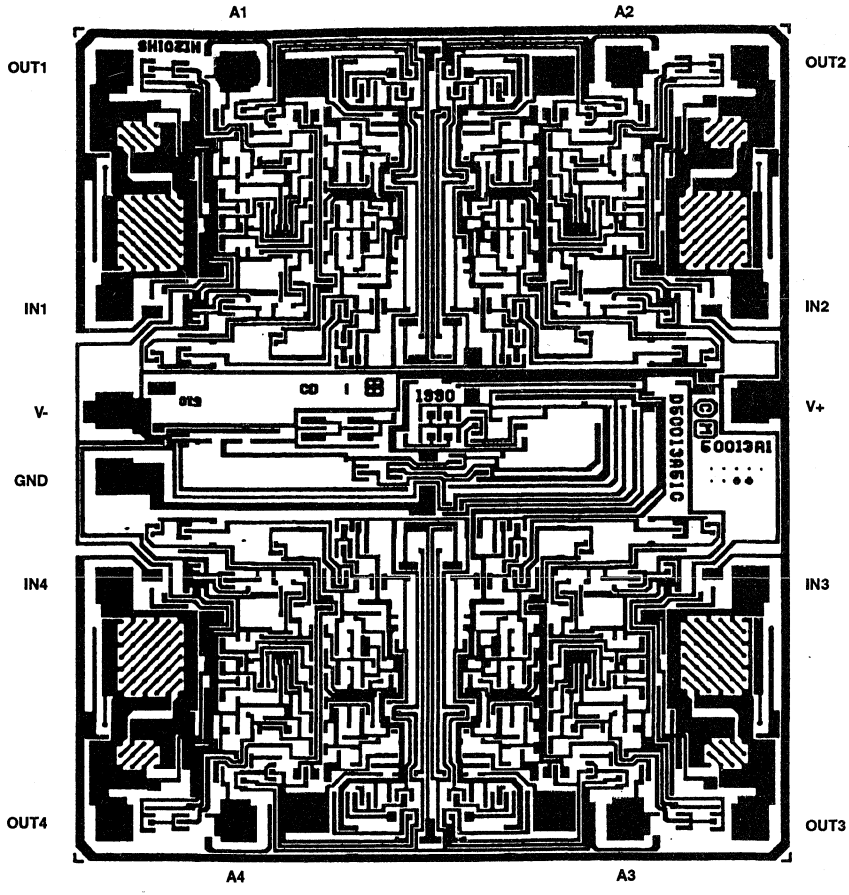
METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ± 1kÅ
Silox Thickness: 12kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$9.5 \times 10^4 A/cm^2$

Metallization Mask Layout

HI-201HS



HI-300 thru HI-307

December 1993

CMOS Analog Switches

Features

- Analog Signal Range (±15V Supplies) ±15V
- Low Leakage (Typical at +25°C) 40pA
- Low Leakage (Typical at +125°C) 1nA
- Low On Resistance (Typical at +25°C) 35Ω
- Break-Before-Make Delay (Typical) 60ns
- Charge Injection 30pC
- TTL, CMOS Compatible
- Symmetrical Switch Elements
- Low Operating Power 1.0mW (Typical for HI-300 - 303)

Applications

- Sample and Hold (i.e. Low Leakage Switching)
- Op Amp Gain Switching (i.e. Low On Resistance)
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Description

The HI-300 thru HI-307 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These switches feature break-before-make switching, (HI-301, HI-303, HI-305 and HI-307 only), low and nearly constant ON resistance over the full analog signal range, and low power dissipation, (a few mW for the HI-300 thru HI-303, a few hundred mW for the HI-304 thru HI-307).

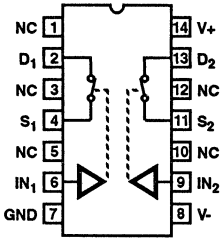
The HI-300 thru HI-303 are TTL compatible and have a logic "0" condition with an input less than 0.8V and a logic "1" condition with an input greater than 4.0V. The HI-304 thru HI-307 switches are CMOS compatible and have a low state with an input less than 3.5V and a high state with an input greater than 11V. (See pinouts for switch conditions with a logic "1" input.)

All the devices are available in a 14 lead Epoxy or Ceramic DIP. The HI-300, HI-301, HI-304 and HI-305 are also available in a 10 pin Metal Can. Each of the switch types are available in either the -55°C to +125°C or 0°C to +75°C operating ranges.

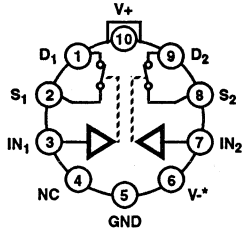
Pinouts (Switch States are for a Logic "1" Input)

DUAL SPST HI-300 AND HI-304
TOP VIEWS

(CDIP, PDIP, SOIC)



(METAL CAN)

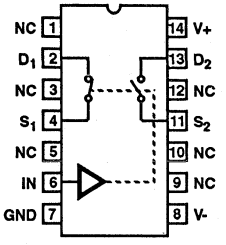


LOGIC	SWITCH
0	OFF
1	ON

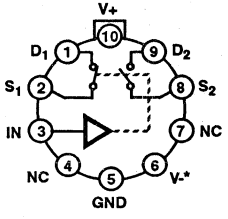
* The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

SPST HI-301 AND HI-305
TOP VIEWS

(CDIP, PDIP, SOIC)



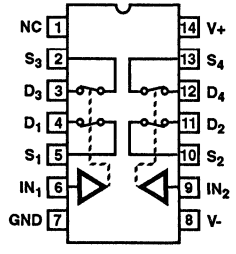
(METAL CAN)



LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

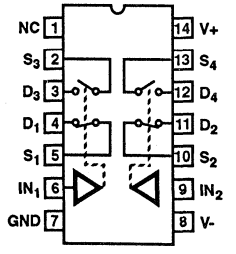
* The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-302 AND HI-306 (PDIP, CDIP, SOIC)
TOP VIEW



LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT HI-303 AND HI-307 (PDIP, CDIP, SOIC)
TOP VIEW



LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

9 SWITCHES

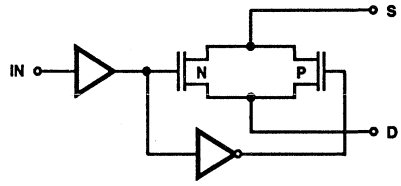
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0300-2	-55°C to +125°C	14 Lead Ceramic DIP
HI1-0300-5	0°C to +75°C	14 Lead Ceramic DIP
HI2-0300-2	-55°C to +125°C	10 Pin TO-5 Can
HI2-0300-5	0°C to +75°C	10 Pin TO-5 Can
HI3-0300-5	0°C to +75°C	14 Lead Plastic DIP
HI9P0300-5	0°C to +75°C	14 Lead SOIC
HI9P0300-9	-40°C to +85°C	14 Lead SOIC
HI1-0301-2	-55°C to +125°C	14 Lead Ceramic DIP
HI1-0301-5	0°C to +75°C	14 Lead Ceramic DIP
HI2-0301-2	-55°C to +125°C	10 Pin TO-5 Can
HI2-0301-5	0°C to +75°C	10 Pin TO-5 Can
HI3-0301-5	0°C to +75°C	14 Lead Plastic DIP
HI9P0301-5	0°C to +75°C	14 Lead SOIC
HI9P0301-9	-40°C to +85°C	14 Lead SOIC
HI1-0302-2	-55°C to +125°C	14 Lead Ceramic DIP
HI1-0302-5	0°C to +75°C	14 Lead Ceramic DIP
HI3-0302-5	0°C to +75°C	14 Lead Plastic DIP
HI9P0302-5	0°C to +75°C	14 Lead SOIC
HI9P0302-9	-40°C to +85°C	14 Lead SOIC
HI1-0303-2	-55°C to +125°C	14 Lead Ceramic DIP
HI1-0303-5	0°C to +75°C	14 Lead Ceramic DIP
HI3-0303-5	0°C to +75°C	14 Lead Plastic DIP
HI9P0303-5	0°C to +75°C	14 Lead SOIC
HI9P0303-9	-40°C to +85°C	14 Lead SOIC

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0304-2	-55°C to +125°C	14 Lead Ceramic DIP
HI1-0304-5	0°C to +75°C	14 Lead Ceramic DIP
HI2-0304-2	-55°C to +125°C	10 Pin TO-5 Can
HI2-0304-5	0°C to +75°C	10 Pin TO-5 Can
HI3-0304-5	0°C to +75°C	14 Lead Plastic DIP
HI9P0304-5	0°C to +75°C	14 Lead SOIC
HI9P0304-9	-40°C to +85°C	14 Lead SOIC
HI1-0305-2	-55°C to +125°C	14 Lead Ceramic DIP
HI1-0305-5	0°C to +75°C	14 Lead Ceramic DIP
HI2-0305-2	-55°C to +125°C	10 Pin TO-5 Can
HI2-0305-5	0°C to +75°C	10 Pin TO-5 Can
HI3-0305-5	0°C to +75°C	14 Lead Plastic DIP
HI9P0305-5	0°C to +75°C	14 Lead SOIC
HI9P0305-9	-40°C to +85°C	14 Lead SOIC
HI1-0306-2	-55°C to +125°C	14 Lead Ceramic DIP
HI1-0306-5	0°C to +75°C	14 Lead Ceramic DIP
HI3-0306-5	0°C to +75°C	14 Lead Plastic DIP
HI9P0306-5	0°C to +75°C	14 Lead SOIC
HI9P0306-9	-40°C to +85°C	14 Lead SOIC
HI1-0307-2	-55°C to +125°C	14 Lead Ceramic DIP
HI1-0307-5	0°C to +75°C	14 Lead Ceramic DIP
HI3-0307-5	0°C to +75°C	14 Lead Plastic DIP
HI19P307-5	0°C to +75°C	14 Lead SOIC
HI9P0307-9	-40°C to +85°C	14 Lead SOIC

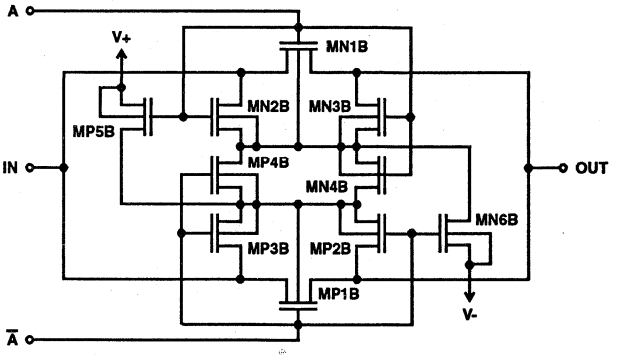
Functional Block Diagram

TYPICAL SWITCH HI-300 SERIES

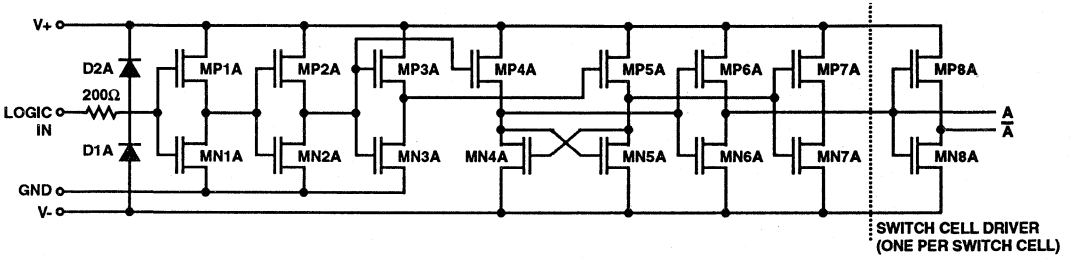


Schematic Diagrams

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

Voltage Between Supplies ..... 44V (±22V)
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage ..... $+V_{SUPPLY}$ +1.5V
$-V_{SUPPLY}$ -1.5V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
Typical Derating Factor ..... 1.5mA/MHz Increase in ICCOP
ESD Classification ..... Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
14 Lead Ceramic DIP	95°C/W	24°C/W
14 Lead Plastic DIP	100°C/W	-
14 Lead SOIC	120°C/W	-
10 Pin TO-100 Metal Can	136°C/W	65°C/W

Maximum Power Dissipation
Ceramic DIP 588mW
Plastic DIP 526mW
Metal Can 435mW
Derate 6.9mW/0°C above T_A = +70°C
Operating Temperature Range
HI-3XX-2 ..... -55°C to +125°C
HI-3XX-5 ..... 0°C to +75°C
Junction Temperature
Ceramic DIP, TO-Can ..... +175°C
Plastic DIP, SOIC ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V; V_{IN} = Logic Input. HI-300-303: V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V. HI-304-307: V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V, Unless Otherwise Specified.

PARAMETERS	TEMP	-55°C TO +125°C			0°C TO +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS								
Break-Before-Make Delay, t_{OPEN} (Note 15)	+25°C	-	60	-	-	60	-	ns
Switch On Time, t_{ON} (Note 13)	+25°C	-	210	300	-	210	300	ns
Switch Off Time, t_{OFF} (Note 13)	+25°C	-	160	250	-	160	250	ns
Switch Off Time, t_{ON} (Note 14)	+25°C	-	160	250	-	160	250	ns
Switch Off Time, t_{OFF} (Note 14)	+25°C	-	100	150	-	100	150	ns
"Off Isolation" (Note 6)	+25°C	-	60	-	-	60	-	dB
Charge Injection (Note 7)	+25°C	-	3	-	-	3	-	mV
Input Switch Capacitance, $C_{S(OFF)}$	+25°C	-	16	-	-	16	-	pF
Output Switch Capacitance, $C_{D(OFF)}$	+25°C	-	14	-	-	14	-	pF
Output Switch Capacitance, $C_{D(ON)}$	+25°C	-	35	-	-	35	-	pF
(High) Digital Input Capacitance, C_{IN}	+25°C	-	5	-	-	5	-	pF
(Low) Digital Input Capacitance, C_{IN}	+25°C	-	5	-	-	5	-	pF
DIGITAL INPUT CHARACTERISTICS								
Input Low Level, V_{INL} (Note 13)	Full	-	-	0.8	-	-	0.8	V
Input High Level, V_{INH} (Note 13)	Full	4	-	-	4	-	-	V
Input Low Level, V_{INL} (Note 14)	Full	-	-	3.5	-	-	3.5	V
Input High Level, V_{INH} (Note 14)	Full	11	-	-	11	-	-	V
Input Leakage Current (Low), I_{INL} (Note 5)	Full	-	-	1	-	-	1	µA
Input Leakage Current (High), I_{INH} (Note 5)	Full	-	-	1	-	-	1	µA
ANALOG SWITCH CHARACTERISTICS								
Analog Signal Range	Full	-15	-	+15	-15	-	+15	V
On Resistance, R_{ON} (Note 2)	+25°C	-	35	50	-	35	50	Ω
	Full	-	40	75	-	40	75	Ω
Off Input Leakage Current, $I_{S(OFF)}$ (Note 3)	+25°C	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA

Electrical Specifications Supplies = +15V, -15V; V_{IN} = Logic Input. HI-300-303: V_{IN} - for Logic "1" = 4V, for Logic "0" = 0.8V. HI-304-307: V_{IN} - for Logic "1" = 11V, for Logic "0" = 3.5V, Unless Otherwise Specified. **(Continued)**

PARAMETERS	TEMP	-55°C TO +125°C			0°C TO +75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Off Output Leakage Current, $I_{D(OFF)}$ (Note 3)	+25°C	-	0.04	1	-	0.04	5	nA
	Full	-	1	100	-	0.2	100	nA
On Leakage Current, $I_{D(ON)}$ (Note 4)	+25°C	-	0.03	1	-	0.03	5	nA
	Full	-	0.5	100	-	0.2	100	nA
POWER SUPPLY CHARACTERISTICS								
Current, I+ (Notes 8, 13)	+25°C	-	0.09	0.5	-	0.09	0.5	mA
	Full	-	-	1	-	-	1	mA
Current, I- (Notes 8, 13)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I+ (Notes 9, 13)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I- (Notes 9, 13)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I+ (Notes 10, 14)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I- (Notes 10, 14)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I+ (Notes 11, 14)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA
Current, I- (Notes 11, 14)	+25°C	-	0.01	10	-	0.01	100	µA
	Full	-	-	100	-	-	-	µA

NOTES:

1. As with all semiconductors, stresses listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Specifications" are the only conditions recommended for satisfactory operation.
2. $V_S = \pm 10V$, $I_{OUT} = \mp 10mA$. On resistance derived from the voltage measured across the switch under the above conditions.
3. $V_S = \pm 14V$, $V_D = \mp 14V$.
4. $V_S = V_D = \pm 14V$.
5. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
6. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1K.
7. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. (HI-300 - 303) Switches are symmetrical; S and D may be interchanged. Logic Drive = 15V (HI-304 - 307).
8. V_{IN} = 4V (one input) (all other inputs = 0V).
9. V_{IN} = 0.8V (all inputs).
10. V_{IN} = 15V (all inputs).
11. V_{IN} = 0V (all inputs).
12. To drive from DTL/TTL circuits, pullup resistors to +5V supply are recommended.
13. HI-300 thru HI-303 only.
14. HI-304 thru HI-307 only.
15. HI-301, HI-303, HI-305, HI-307 only.

Typical Performance Curves

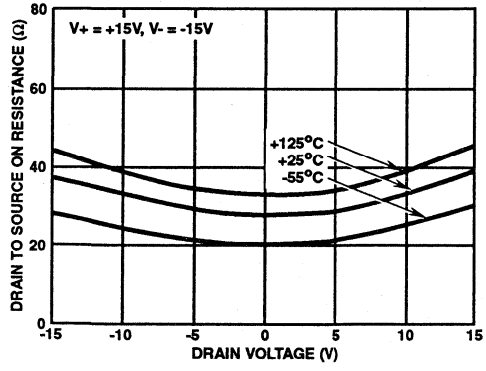


FIGURE 1. $R_{DS(ON)}$ vs V_D AND TEMPERATURE

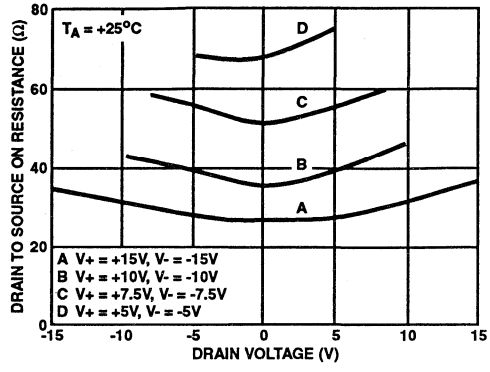


FIGURE 2. $R_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

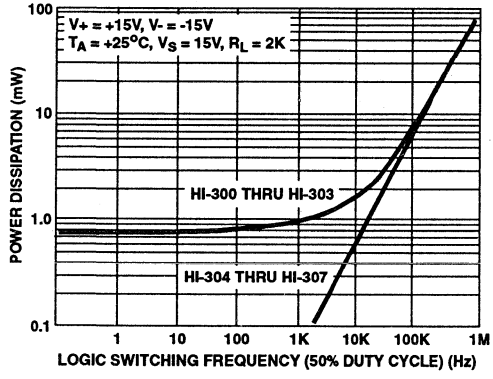


FIGURE 3. DEVICE POWER DISSIPATION vs SWITCHING FREQUENCY SINGLE LOGIC INPUT

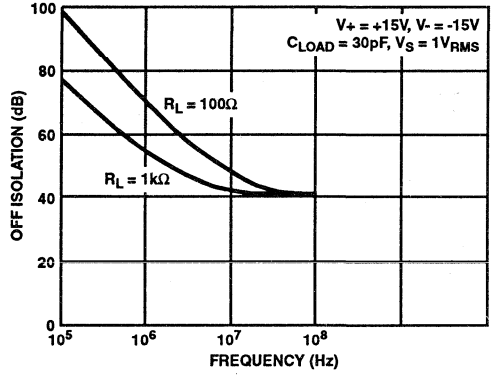


FIGURE 4. OFF ISOLATION vs FREQUENCY

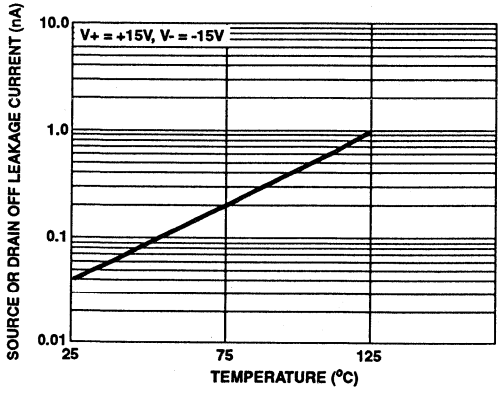


FIGURE 5. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE†

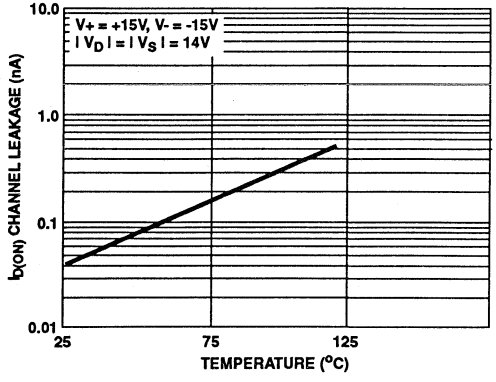
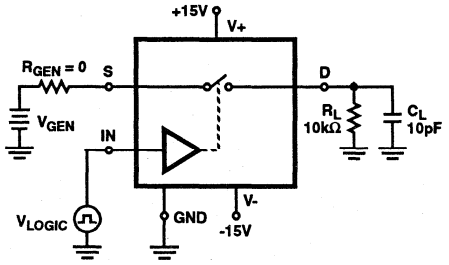


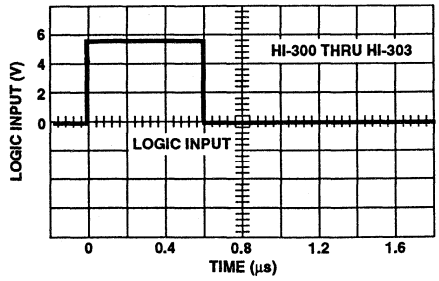
FIGURE 6. $I_{D(ON)}$ vs TEMPERATURE†

† The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

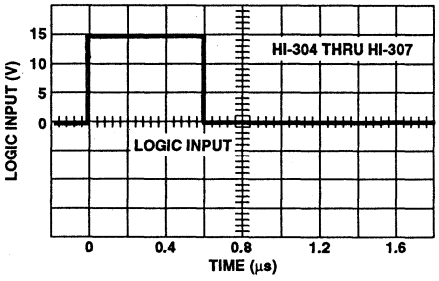
Typical Performance Curves (Continued)



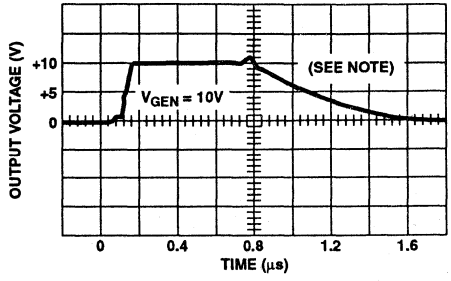
7A. TEST CIRCUIT



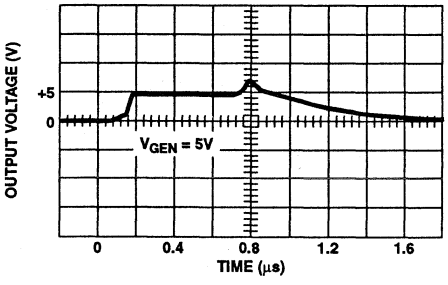
7B. $V_{IN(LOGIC)}$ vs TIME



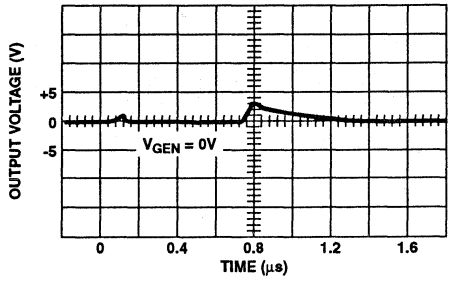
7C. $V_{IN(LOGIC)}$ vs TIME



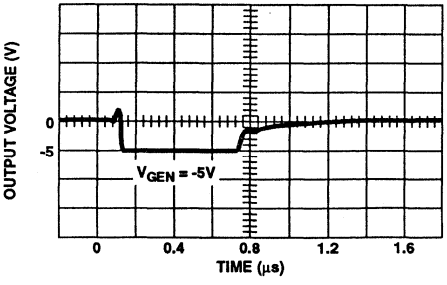
7D. V_{OUT} vs TIME



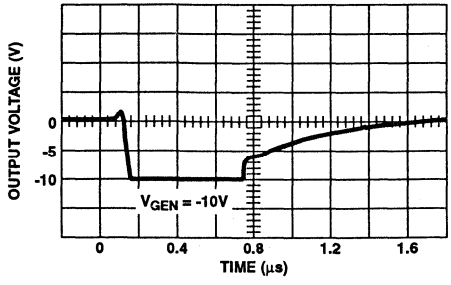
7E. V_{OUT} vs TIME



7F. V_{OUT} vs TIME



7G. V_{OUT} vs TIME



7H. V_{OUT} vs TIME

NOTE: If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

FIGURE 7. TYPICAL DELAY, RISE, FALL, SETTLING TIMES AND SWITCHING TRANSIENTS

Typical Performance Curves (Continued)

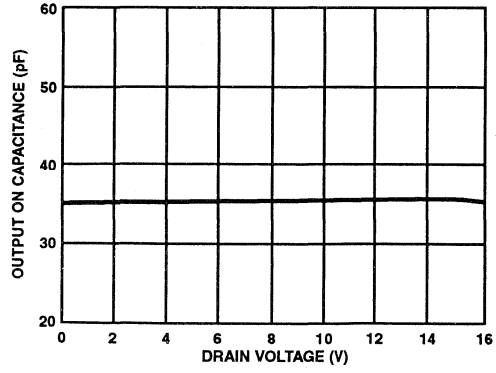


FIGURE 8. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE

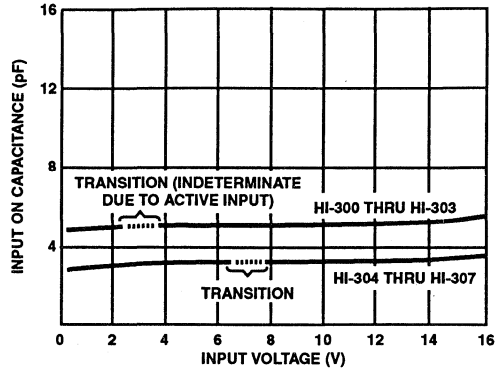


FIGURE 9. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE

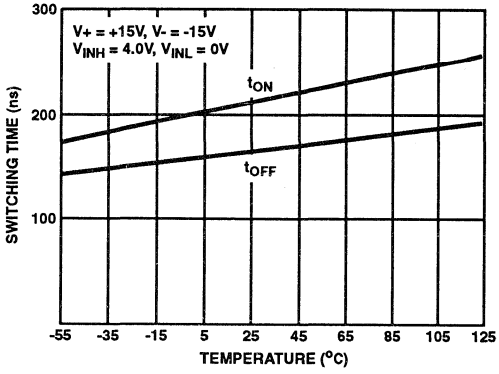


FIGURE 10. SWITCHING TIME vs TEMPERATURE, HI-300 THRU HI-303

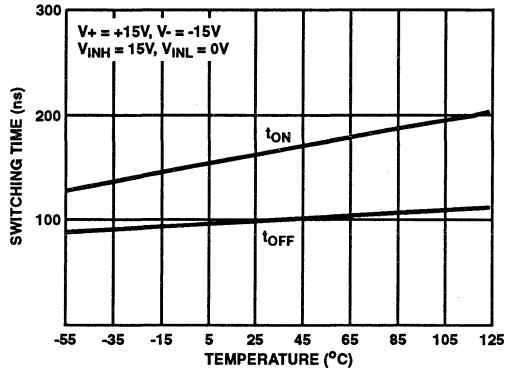


FIGURE 11. SWITCHING TIME vs TEMPERATURE, HI-304 THRU HI-307

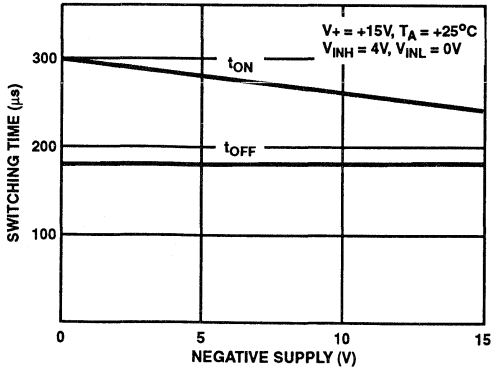


FIGURE 12. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE, HI-300 THRU HI-303

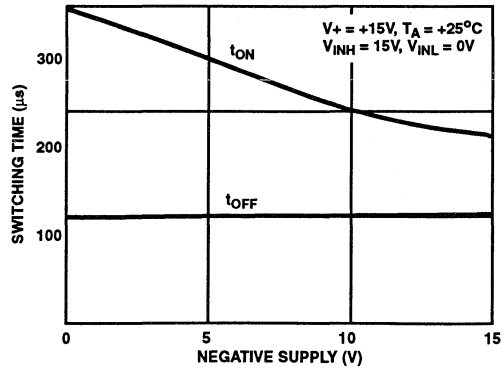


FIGURE 13. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE, HI-304 THRU HI-307

Typical Performance Curves (Continued)

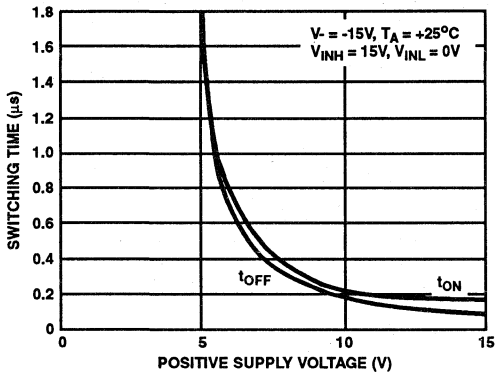


FIGURE 14. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE, HI-304 THRU HI-307

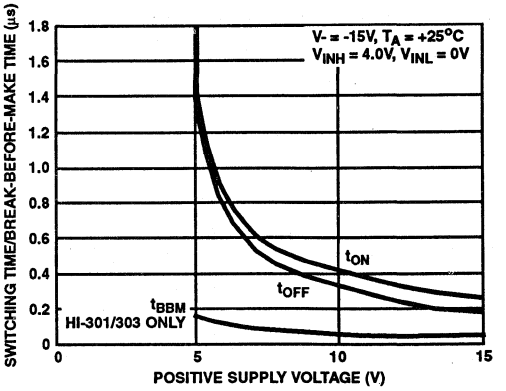


FIGURE 15. SWITCHING TIME AND BREAK-BEFORE-MAKE TIME vs POSITIVE SUPPLY VOLTAGE, HI-300 THRU HI-303

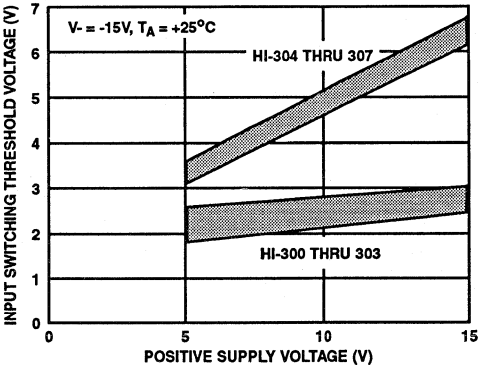
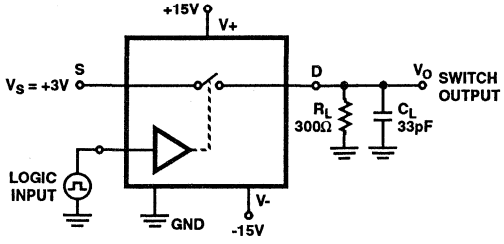


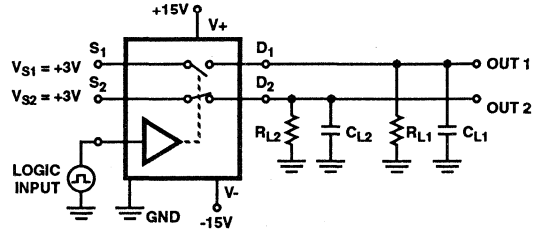
FIGURE 16. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE, HI-300 THRU HI-307

Test Circuits

SWITCH TYPE	V_{INH}
HI-300 thru HI-303	4V
HI-304 thru HI-307	15V

SWITCH TYPE	V_{INH}
HI-301, HI-303	5V
HI-305, HI-307	15V





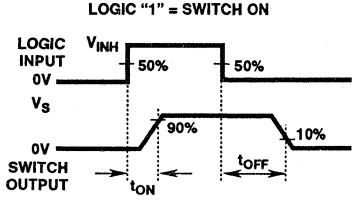


FIGURE 17. SWITCHING TEST CIRCUIT (t_{ON}, t_{OFF})

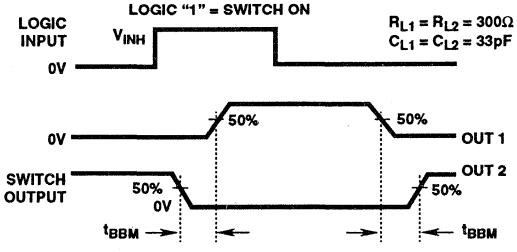


FIGURE 18. BREAK-BEFORE-MAKE TEST CIRCUIT (t_{BBM})

HI-381 thru HI-390

December 1993

CMOS Analog Switches

Features

- Analog Signal Range (±15V Supplies) ±15V
- Low Leakage 40pA
- Low On Resistance 35Ω
- Break-Before-Make Delay 60ns
- Charge Injection 30pC
- TTL Compatible
- Symmetrical Switch Elements
- Low Operating Power 1.0mW

Applications

- Sample and Hold (i.e. Low Leakage Switching)
- Op Amp Gain Switching (i.e. Low On Resistance)
- Portable, Battery Operated Circuits
- Low Level Switching Circuits
- Dual or Single Supply Systems

Description

The HI-381 thru HI-390 series of switches are monolithic devices fabricated using CMOS technology and the Harris dielectric isolation process. These devices are TTL compatible and are available in four switching configurations. (See device pinout for particular switching function with a logic "1" input.)

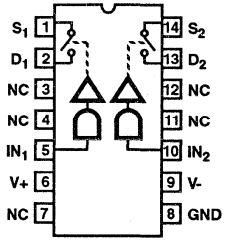
These switches feature low leakage and supply currents, low and nearly constant ON resistance over the analog signal range, break-before-make switching and low power dissipation.

The HI-381 and HI-387 switches are available in a 14 lead Plastic, Ceramic DIP, or 10 pin Metal Can. The HI-384 and HI-390 are available in a 16 lead Plastic or Ceramic DIP. Each of the indivual switch types are available in the -55°C to +125°C, -40°C to +85°C, or 0°C to +75°C operating ranges.

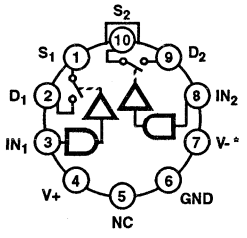
Pinouts (Switch States are for a Logic "1" Input)

DUAL SPST HI-381
TOP VIEWS

(CDIP, PDIP, SOIC)



(METAL CAN)

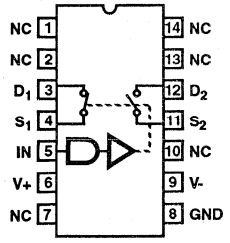


LOGIC	SWITCH
0	OFF
1	ON

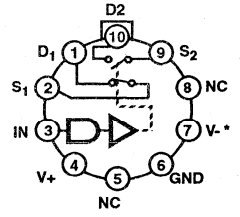
* The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

SPDT HI-387
TOP VIEWS

(CDIP, PDIP, SOIC)



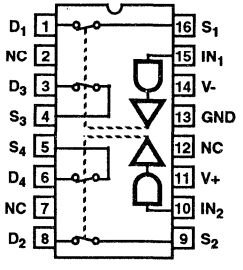
(METAL CAN)



LOGIC	SW1	SW2
0	OFF	ON
1	ON	OFF

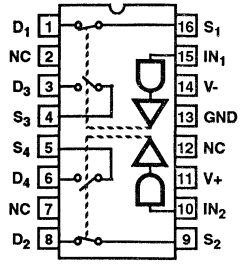
* The substrate and case are internally tied to V-. (The case should not be used as the V- connection, however.)

DUAL DPST HI-384 (CDIP, PDIP, SOIC)
TOP VIEW



LOGIC	SW 1 - 4
0	OFF
1	ON

DUAL SPDT HI-390 (CDIP, PDIP, SOIC)
TOP VIEW



LOGIC	SW1 SW2	SW3 SW4
0	OFF	ON
1	ON	OFF

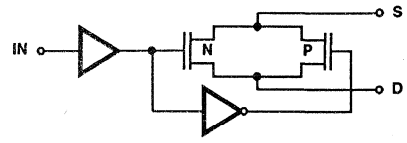
File Number 3126

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0381-2	-55°C to +125°C	14 Lead Ceramic DIP
HI1-0381-5	0°C to +75°C	14 Lead Ceramic DIP
HI1-0381/883	-55°C to +125°C	14 Lead Ceramic DIP
HI2-0381-2	-55°C to +125°C	10 Pin TO-5 Metal Can
HI2-0381-5	0°C to +75°C	10 Pin TO-5 Metal Can
HI2-0381/883	-55°C to +125°C	10 Pin TO-5 Metal Can
HI1-0384-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0384-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-0384/883	-55°C to +125°C	16 Lead Ceramic DIP
HI9P0384-5	0°C to +75°C	16 Lead Plastic SOIC (W)
HI1-0387-2	-55°C to +125°C	14 Lead Ceramic DIP
HI1-0387-5	0°C to +75°C	14 Lead Ceramic DIP
HI2-0387-2	-55°C to +125°C	10 Pin TO-5 Metal Can
HI2-0387-5	0°C to +75°C	10 Pin TO-5 Metal Can
HI9P0387-5	0°C to +75°C	14 Lead Plastic SOIC
HI1-0390-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0390-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-0390/883	-55°C to +125°C	16 Lead Ceramic DIP
HI9P0390-5	0°C to +75°C	16 Lead Plastic SOIC (W)
HI3-0381-5	0°C to +75°C	14 Lead Plastic DIP
HI9P0381-5	0°C to +75°C	14 Lead Plastic SOIC
HI9P0381-9	-40°C to +85°C	14 Lead Plastic SOIC
HI1-0387/883	-55°C to +125°C	14 Lead Ceramic DIP
HI2-0387/883	-55°C to +125°C	10 Pin TO-5 Metal Can
HI3-0387-5	0°C to +75°C	14 Lead Plastic DIP
HI9P0387-9	-40°C to +85°C	14 Lead Plastic SOIC
HI3-0390-5	0°C to +75°C	16 Lead Plastic DIP
HI3-0390-9	-40°C to +85°C	16 Lead SOIC (W)
HI3-0384-5	0°C to +75°C	16 Lead Plastic DIP
HI3-0384-9	-40°C to +85°C	16 Lead SOIC (W)

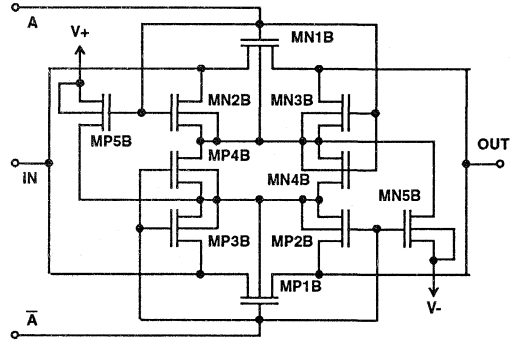
Functional Block Diagram

TYPICAL SWITCH 3XX SERIES

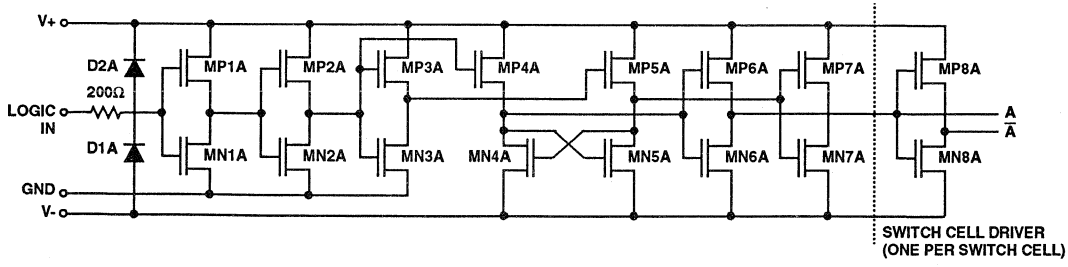


Schematic Diagrams

SWITCH CELL



DIGITAL INPUT BUFFER AND LEVEL SHIFTER



Absolute Maximum Ratings

Voltage Between Supplies ..... 44V (±22V)
Digital Input Voltage ..... $+V_{SUPPLY}$ +4V
$-V_{SUPPLY}$ -4V
Analog Input Voltage ..... $+V_{SUPPLY}$ +1.5V
$-V_{SUPPLY}$ -1.5V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s)..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package, 14 Lead.....	95°C/W	24°C/W
Ceramic DIP Package, 16 Lead.....	80°C/W	24°C/W
Plastic DIP Package, 14 Lead.....	100°C/W	-
Plastic DIP Package, 16 Lead.....	100°C/W	-
Plastic SOIC Package, 14 Lead	120°C/W	-
Plastic SOIC Package, 16 Lead	100°C/W	-
Metal Can Package	136°C/W	65°C/W

Junction Temperature
Ceramic DIP ..... +175°C
Plastic DIP..... +150°C
Plastic SOIC ..... +150°C
Metal Can ..... +175°C
Operating Temperature Range
HI-3XX-2 ..... -55°C to +125°C
HI-3XX-5 ..... 0°C to +75°C
HI-3XX-9 ..... -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V; V_{IN} = Logic Input. VIN for Logic "1" = 4V, for Logic "0" = 0.8V, Unless Otherwise Specified.

PARAMETERS	TEST CONDITIONS	TEMP	HI-3XX-2			HI-3XX-5-9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Break-Before-Make Delay, t_{OPEN} (HI-387/HI-390 Only)		+25°C	-	60	-	-	60	-	ns
Switch On Time, t_{ON}		+25°C	-	210	300	-	210	300	ns
Switch Off Time, t_{OFF}		+25°C	-	160	250	-	160	250	ns
"Off Isolation"	(Note 5)	+25°C	-	60	-	-	60	-	dB
Charge Injection	(Note 6)	+25°C	-	3	-	-	3	-	mV
Input Switch Capacitance, $C_{S(OFF)}$		+25°C	-	16	-	-	16	-	pF
Output Switch Capacitance, $C_{D(OFF)}$		+25°C	-	14	-	-	14	-	pF
Output Switch Capacitance, $C_{D(ON)}$		+25°C	-	35	-	-	35	-	pF
Digital Input Capacitance (High), C_{IN}		+25°C	-	5	-	-	5	-	pF
Digital Input Capacitance (Low), C_{IN}		+25°C	-	5	-	-	5	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Level, V_{INL}		Full	-	-	0.8	-	-	0.8	V
Input High Level, V_{INH}		Full	4	-	-	4	-	-	V
Input Leakage Current (Low), I_{INL}	(Note 4)	Full	-	-	1	-	-	1	µA
Input Leakage Current (High), I_{INH}	(Note 4)	Full	-	-	1	-	-	1	µA
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range		Full	-15	-	+15	-15	-	+15	V
On Resistance, R_{ON}	(Note 1)	+25°C	-	35	50	-	35	50	Ω
		Full	-	40	75	-	45	75	Ω
Off Input Leakage Current, $I_{S(OFF)}$	(Note 2)	+25°C	-	0.04	1	-	0.04	5	nA
		Full	-	1	100	-	0.2	100	nA
Off Output Leakage Current, $I_{D(OFF)}$	(Note 2)	+25°C	-	0.04	1	-	0.04	5	nA
		Full	-	1	100	-	0.2	100	nA
On Input Leakage Current, $I_{S(ON)}$	(Note 3)	+25°C	-	0.03	1	-	0.03	5	nA
		Full	-	0.5	100	-	0.2	100	nA

Electrical Specifications Supplies = +15V, -15V; V_{IN} = Logic Input. VIN for Logic "1" = 4V, for Logic "0" = 0.8V, Unless Otherwise Specified. **(Continued)**

PARAMETERS	TEST CONDITIONS	TEMP	HI-3XX-2			HI-3XX-5-9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS									
Current, I+	(Note 7)	+25°C	-	0.09	0.5	-	0.09	0.5	mA
		Full	-	-	1	-	-	1	mA
Current, I-	(Note 7)	+25°C	-	0.01	10	-	0.01	100	µA
		Full	-	-	100	-	-	-	µA
Current, I+	(Note 8)	+25°C	-	0.01	10	-	0.01	100	µA
		Full	-	-	100	-	-	-	µA
Current, I-	(Note 8)	+25°C	-	0.01	10	-	0.01	100	µA
		Full	-	-	100	-	-	-	µA

NOTES:

1. $V_S = \pm 10V$, $I_{OUT} = \mp 10mA$. On resistance derived from the voltage measured across the switch under the above conditions.
2. $V_S = \pm 14V$, $V_D = \mp 14V$.
3. $V_S = V_D = \pm 14V$.
4. The digital inputs are diode protected MOS gates and typical leakages of 1nA or less can be expected.
5. $V_S = 1V_{RMS}$, f = 500kHz, C_L = 15pF, R_L = 1K, $C_L = C_{FIXTURE} + C_{PROBE}$ "off isolation" = $20_{Log}\ V_S/V_D$.
6. V_S = 0V, C_L = 10,000pF, Logic Drive = 5V pulse. Switches are symmetrical; S and D may be interchanged.
7. V_{IN} = 4V (one input) (all other inputs = 0V).
8. V_{IN} = 0.8V (all inputs).

Typical Performance Curves

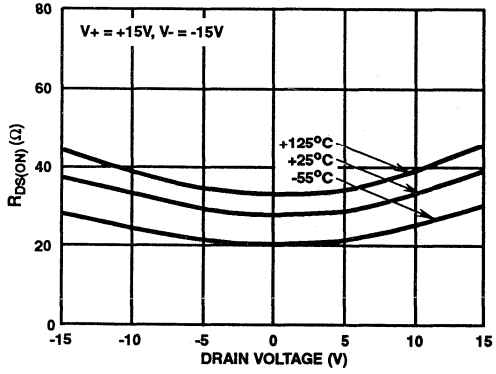


FIGURE 1. $R_{DS(ON)}$ vs V_D AND TEMPERATURE

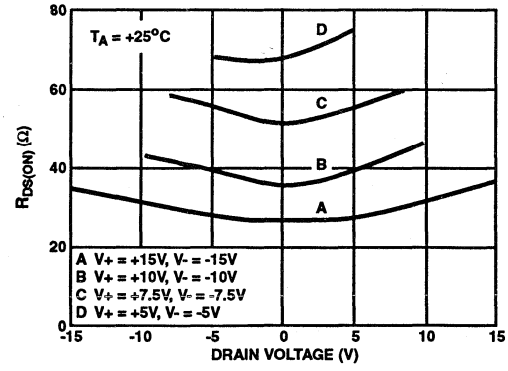


FIGURE 2. $R_{DS(ON)}$ vs V_D AND POWER SUPPLY VOLTAGE

Typical Performance Curves (Continued)

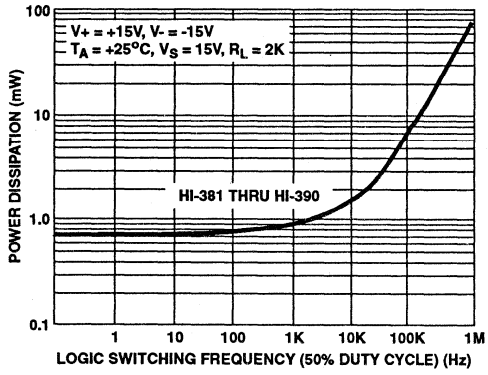


FIGURE 3. DEVICE POWER DISSIPATION vs SWITCHING FREQUENCY (SINGLE LOGIC INPUT)

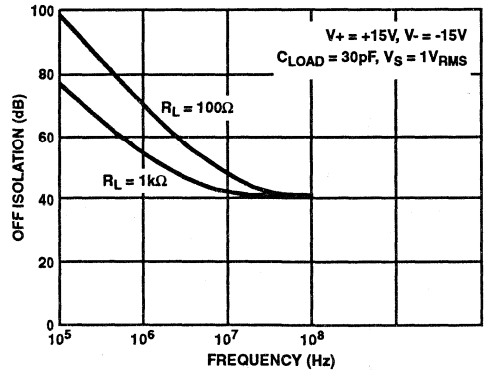


FIGURE 4. OFF ISOLATION vs FREQUENCY

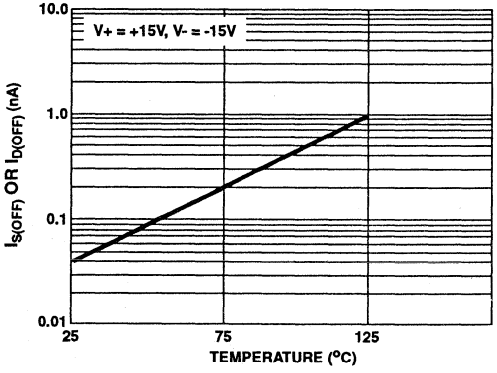


FIGURE 5. $I_{S(OFF)}$ OR $I_{D(OFF)}$ vs TEMPERATURE*

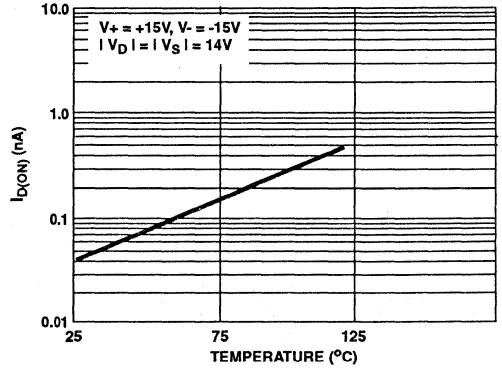


FIGURE 6. $I_{D(ON)}$ vs TEMPERATURE*

* The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

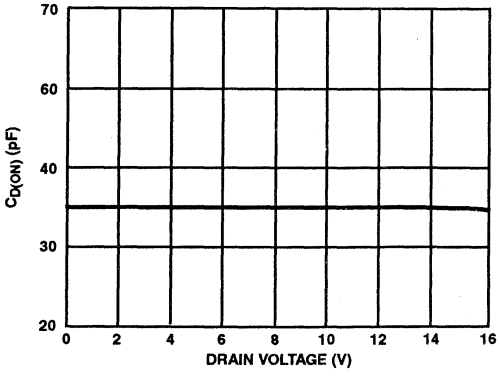


FIGURE 7. OUTPUT ON CAPACITANCE vs DRAIN VOLTAGE

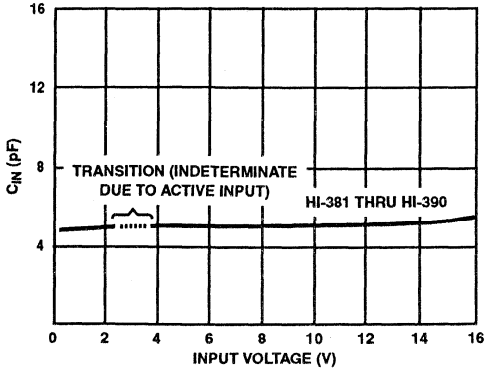
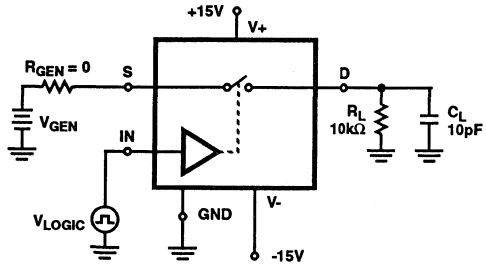
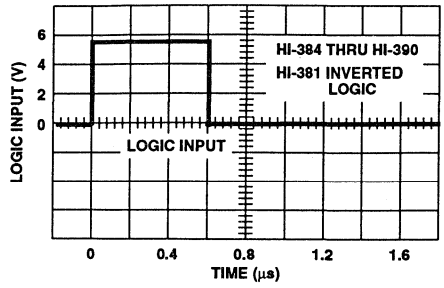


FIGURE 8. DIGITAL INPUT CAPACITANCE vs INPUT VOLTAGE

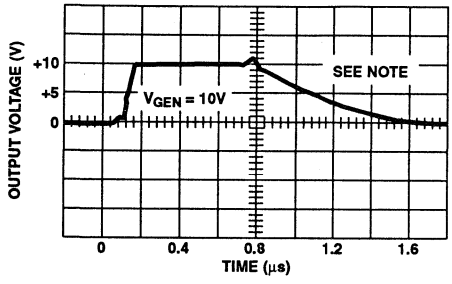
Typical Performance Curves (Continued)



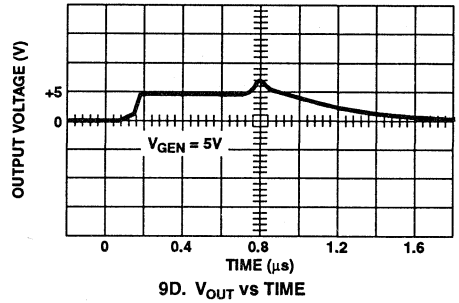
9A. TEST CIRCUIT



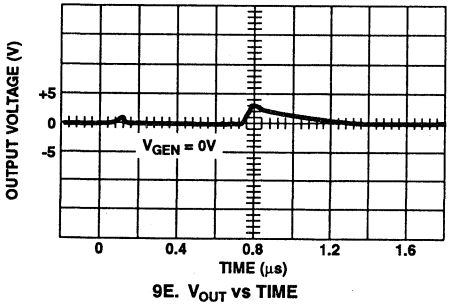
9B. V_{IN} LOGIC vs TIME



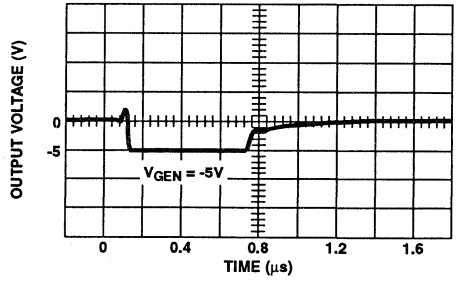
9C. V_{OUT} vs TIME



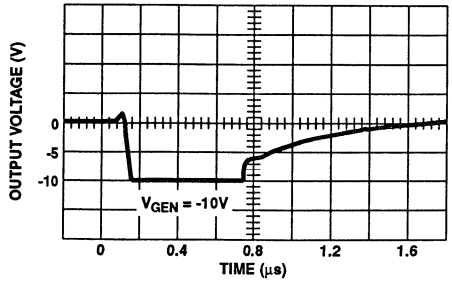
9D. V_{OUT} vs TIME



9E. V_{OUT} vs TIME



9F. V_{OUT} vs TIME



9G. V_{OUT} vs TIME

NOTE: If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

FIGURE 9. TYPICAL DELAY, RISE, FALL, SETTLING TIMES AND SWITCHING TRANSIENTS

Typical Performance Curves (Continued)

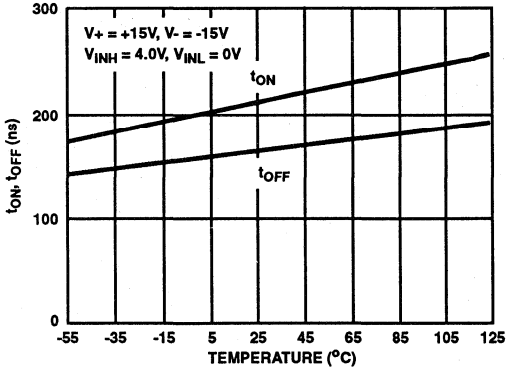


FIGURE 10. SWITCHING TIME vs TEMPERATURE, HI-381 THRU HI-390

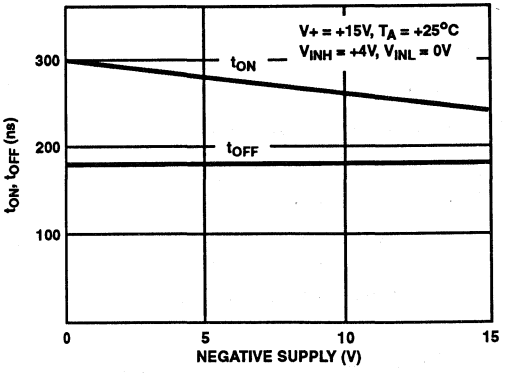


FIGURE 11. SWITCHING TIME vs NEGATIVE SUPPLY VOLTAGE, HI-381 THRU HI-390

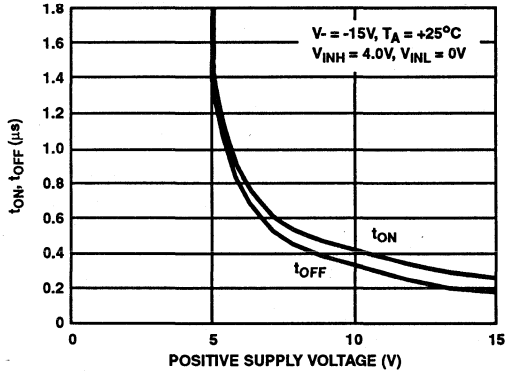


FIGURE 12. SWITCHING TIME vs POSITIVE SUPPLY VOLTAGE, HI-381 THRU HI-390

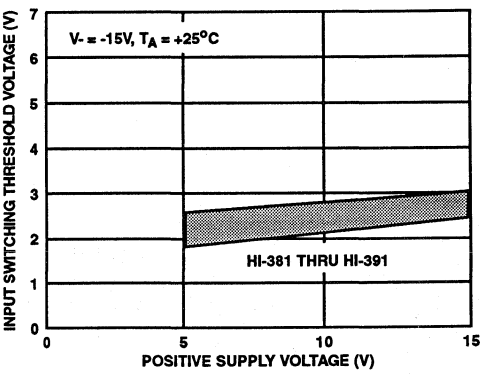


FIGURE 13. INPUT SWITCHING THRESHOLD vs POSITIVE SUPPLY VOLTAGE, HI-381 THRU HI-390

HARRIS SEMICONDUCTOR

HI-5040 thru HI-5051, HI-5046A and HI-5047A

December 1993

CMOS Analog Switches

Features

- ±15V Wide Analog Signal Range
- Low "ON" Resistance 25Ω (Typical)
- High Current Capability 80mA (Typical)
- Break-Before-Make Switching
  - Turn-On Time 370ns (Typical)
  - Turn-Off Time 280ns (Typical)
- No Latch-Up
- Input MOS Gates are Protected from Electrostatic Discharge
- DTL, TTL, CMOS, PMOS Compatible

Applications

- High Frequency Switching
- Sample and Hold
- Digital Filters
- Operational Amplifier Gain Switching

Description

This family of CMOS analog switches offers low resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25Ω for HI-5048 through HI-5051 and HI-5046A and HI-5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at +25°C). This family of switches also features very low power operation (1.5mW at +25°C).

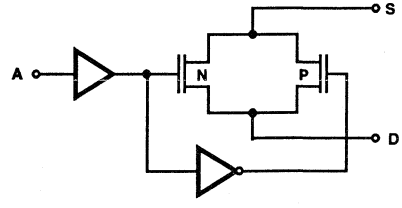
There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional Description). All devices are available in 16 lead DIP packages. The HI-5040 and HI-5050 switches can directly replace IH-5040 series devices except IH5048, and are functionally compatible with the DG180 and DG190 family. Each switch type is available in the -55°C to +125°C and 0°C to +75°C performance grades.

Functional Description

PART NUMBER	TYPE	R_{ON}
HI-5040	SPST	50Ω
HI-5041	Dual SPST	50Ω
HI-5042	SPDT	50Ω
HI-5043	Dual SPDT	50Ω
HI-5044	DPST	50Ω
HI-5045	Dual DPST	50Ω
HI-5046	DPDT	50Ω
HI-5046A	DPDT	25Ω
HI-5047	4PST	50Ω
HI-5047A	4PST	25Ω
HI-5048	Dual SPST	25Ω
HI-5049	Dual DPST	25Ω
HI-5050	SPDT	25Ω
HI-5051	Dual SPDT	25Ω

Functional Block Diagram

TYPICAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3127**

Ordering Information

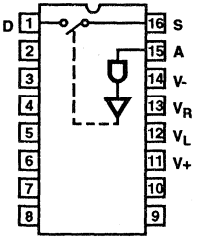
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-5040-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI3-5040-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5040-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5040-5	0°C to +75°C	16 Lead Ceramic DIP
HI3-5041-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5041-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5041-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5041-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI3-5042-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5042-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5042-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5042-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5043-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5043-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-5043-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5043-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5044-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5044-5	0°C to +75°C	16 Lead Ceramic DIP
HI3-5044-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5044-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5045-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5045-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5045-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-5045-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5046-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5046-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5046-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI3-5046-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5046A-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI3-5046A-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5046A-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5046A-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5047-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5047-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5047-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-5047-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5047A-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5047A-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-5047A-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5047A-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-5048-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5048-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI3-5048-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5048-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5049-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5049-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-5049-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5049-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5050-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5050-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-5050-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5050-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI1-5051-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-5051-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5051-7	0°C to +75°C + 96 Hr. Burn-In	16 Lead Ceramic DIP
HI4P5051-5	0°C to +75°C	20 Lead PLCC
HI3-5051-5	0°C to +75°C	16 Lead Plastic DIP
HI1-5040/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5041/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5042/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5043/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5044/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5045/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5046/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5046A/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5047/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5047A/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-504[illegible]/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-50[illegible]/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5050/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-5051/883	-55°C to +125°C	16 Lead Ceramic DIP
HI4-5043/883	-55°C to +125°C	20 Lead CLCC
HI4-5045/883	-55°C to +125°C	16 Lead Ceramic DIP
HI4-5051/883	-55°C to +125°C	16 Lead Ceramic DIP
HI9P5043-5	0°C to +75°C	16 SOIC (N)
HI9P5045-5	0°C to +75°C	16 SOIC (N)
HI9P5049-5	0°C to +75°C	16 SOIC (N)
HI9P5051-5	0°C to +75°C	16 SOIC (N)
HI9P5043-9	-40°C to +85°C	16 SOIC (N)
HI9P5045-9	-40°C to +85°C	16 SOIC (N)
HI9P5049-9	-40°C to +85°C	16 SOIC (N)
HI9P5051-9	-40°C to +85°C	16 SOIC (N)

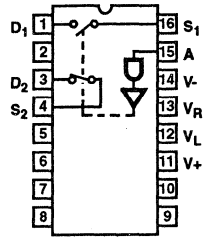
Pin Configurations Switch States are Logic "0" Input

SINGLE CONTROL

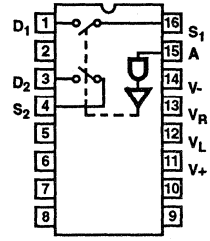
SPST
HI-5040 (50Ω)



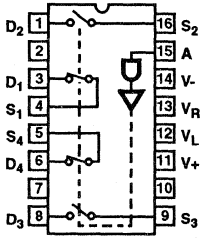
SPDT
HI-5042 (50Ω), HI-5050 (25Ω)



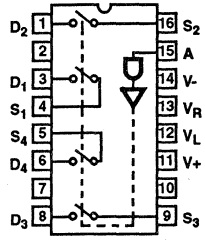
DPST
HI-5044 (50Ω)



DPDT
HI-5046 (50Ω), HI-5046A (25Ω)

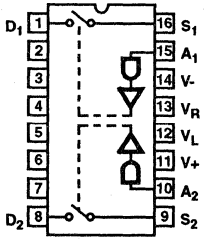


4PST
HI-5047 (50Ω), HI-5047A (25Ω)

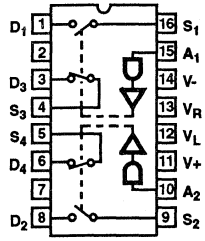


DUAL CONTROL

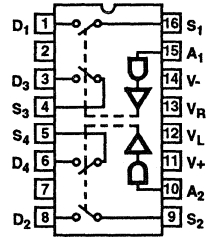
DUAL SPST
HI-5041 (50Ω)



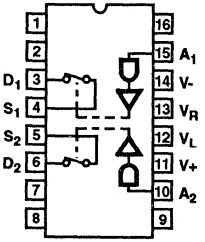
DUAL SPDT
HI-5043 (50Ω), HI-5051 (25Ω)



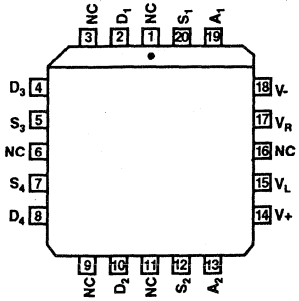
DUAL DPST
HI-5045 (50Ω), HI-5049 (25Ω)



DUAL SPST
HI-5048 (25Ω)



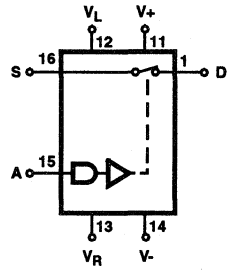
DUAL SPDT
HI-5043 (50Ω), HI-5051 (25Ω)



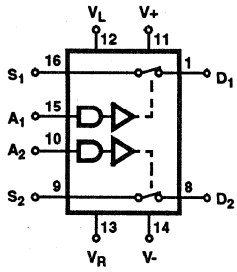
NOTE: Unused pins may be internally connected. Ground all unused pins.

Switch Functions Switch States are Logic "1" Input

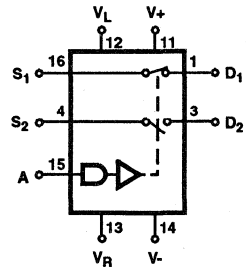
SPST
HI-5040 (50Ω)



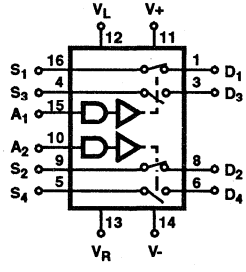
DUAL SPST
HI-5041 (50Ω)



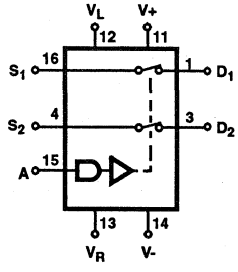
SPDT
HI-5042 (50Ω)



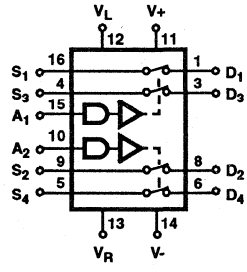
DUAL SPDT
HI-5043 (50Ω)



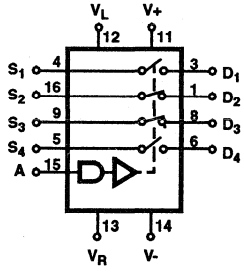
DPST
HI-5044 (50Ω)



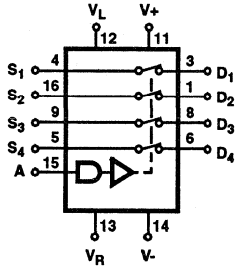
DUAL DPST
HI-5045 (50Ω)



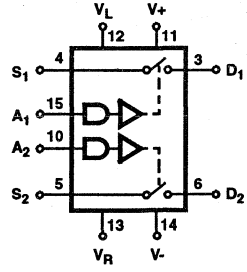
DPDT
HI-5046 (50Ω), HI-5046A (25Ω)



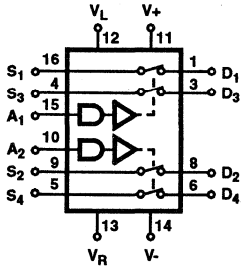
4PST
HI-5047 (50Ω), HI-5047A (25Ω)



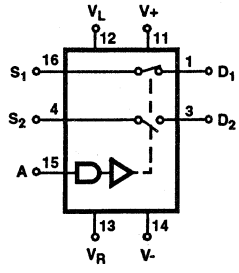
DUAL SPST
HI-5048 (25Ω)



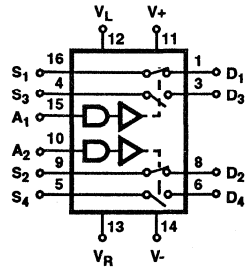
DUAL DPST
HI-5049 (25Ω)



SPDT
HI-5050 (25Ω)



DUAL SPDT
HI-5051 (25Ω)



Absolute Maximum Ratings

Supply Voltage (V+, V-) 36V
V_R to Ground ..... V+, V-
Digital and Analog Input Voltage ..... $+V_{SUPPLY}$ +4V, $-V_{SUPPLY}$ -4V
Analog Current (S to D) Continuous..... 30mA
Analog Current (S to D) Peak..... 80mA
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10s)..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	80°C/W	24°C/W
SOIC Package	120°C/W	-
Plastic DIP Package	100°C/W	-
PLCC Package	80°C/W	-
CLCC Package	75°C/W	20°C/W

Junction Temperature
Plactic Packages ..... +150°C
Ceramic Packages ..... +175°C
Operating Temperature Range
HI-50XX-2 ..... -55°C to +125°C
HI-50XX-5, -7..... 0°C to +75°C
HI-50XX-9 ..... -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, V_L = +5V, Unless Otherwise Specified. For Test Conditions, Consult Performance Characteristics, Unused Pins are Grounded.

PARAMETER	TEST CONDITIONS	TEMP	-55°C To +125°C			0°C To +75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
t_{ON}, Switch On Time	(Note 4)	+25°C	-	370	500	-	370	500	ns
t_{OFF}, Switch Off Time	(Note 4)	+25°C	-	280	500	-	280	500	ns
Charge Injection	(Note 2)	+25°C	-	5	20	-	5	-	mV
"Off Isolation"	(Note 3)	+25°C	75	80	-	-	80	-	dB
"Crosstalk"	(Note 3)	+25°C	80	88	-	-	88	-	dB
$C_{S(OFF)}$, Input Switch Capacitance		+25°C	-	11	-	-	11	-	pF
$C_{D(OFF)}$, Output Switch Capacitance		+25°C	-	11	-	-	11	-	pF
$C_{D(ON)}$, Output Switch Capacitance		+25°C	-	22	-	-	22	-	pF
C_A, Digital Input Capacitance		+25°C	-	5	-	-	5	-	pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance		+25°C	-	0.5	-	-	0.5	-	pF
DIGITAL INPUT CHARACTERISTICS									
V_{AL}, Input Low Threshold		Full	-	-	0.8	-	-	0.8	V
V_{AH}, Input High Threshold		Full	2.4	-	-	2.4	-	-	V
I_A, Input Leakage Current (High or Low)		Full	-	0.01	1.0	-	0.01	1.0	µA
ANALOG SWITCH CHARACTERISTICS									
Analog Signal Range		Full	-15	-	+15	-15	-	+15	V
R_{ON}, On Resistance	(Note 1A)	+25°C	-	50	75	-	50	75	Ω
		Full	-	-	150	-	-	150	Ω
R_{ON}, On Resistance	(Note 1B)	+25°C	-	25	45	-	25	45	Ω
		Full	-	-	50	-	-	50	Ω
R_{ON}, Channel-to-Channel Match	(Note 1A)	+25°C	-	2	10	-	2	10	Ω
R_{ON}, Channel-to-Channel Match	(Note 1B)	+25°C	-	1	5	-	1	5	Ω
$I_{S(OFF)} = I_{D(OFF)}$, Off Input or Output Leakage Current		+25°C	-	0.8	2	-	0.8	2	nA
		Full	-	100	200	-	100	200	nA

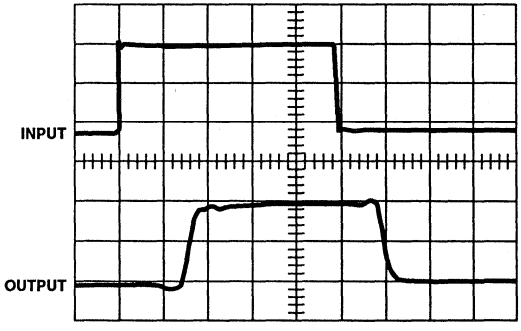
Electrical Specifications Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 2.4V, V_{AL} (Logic Level Low) = +0.8V, V_L = +5V, Unless Otherwise Specified. For Test Conditions, Consult Performance Characteristics, Unused Pins are Grounded. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP	-55°C To +125°C			0°C To +75°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
$I_{D(ON)}$, On Leakage Current		+25°C	-	0.01	2	-	0.01	2	nA
		Full	-	2	200	-	2	200	nA
POWER REQUIREMENTS									
P_D, Quiescent Power Dissipation		+25°C	-	1.5	-	-	1.5	-	mW
I+, I-, I_L, I_R		+25°C	-	-	0.2	-	-	0.3	mA
I+, +15V Quiescent Current	(Note 4)	Full	-	-	0.3	-	-	0.5	mA
I-, -15V Quiescent Current	(Note 4)	Full	-	-	0.3	-	-	0.5	mA
I_L, +5V Quiescent Current	(Note 4)	Full	-	-	0.3	-	-	0.5	mA
I_R, Ground Quiescent Current	(Note 4)	Full	-	-	0.3	-	-	0.5	mA

NOTES:

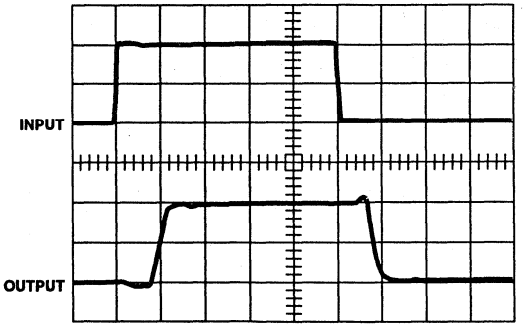
1. V_{OUT} = ±10V, I_{OUT} = ∓1mA
   A). For HI-5040 thru HI-5047
   B). For HI-5048 thru HI-5051, HI-5046A/5047A.
2. V_{IN} = 0V, C_L = 10,000pF.
3. R_L = 100Ω, f = 100kHz, V_{IN} = 2.0V_{P-P}, C_L = 5pF.
4. V_{AL} = 0V, V_{AH} = 5V.

Switching Waveforms



Top: TTL Input (1V/Div.)
V_{AH} = 5V, V_{AL} = 0V
Bottom: Output (2V/Div.)
Horizontal: 200ns/Div.

FIGURE 1.



Top: CMOS Input (5V/Div.)
V_{AH} = 10V, V_{AL} = 0V
Bottom: Output (5V/Div.)
Horizontal: 200ns/Div.

FIGURE 2.

Typical Performance Curves and Test Circuits

T_A = +25°C, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3.0V and V_{AL} = 0.8V, Unless Otherwise Specified

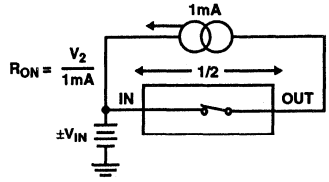


FIGURE 3. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL, SUPPLY VOLTAGE AND TEMPERATURE

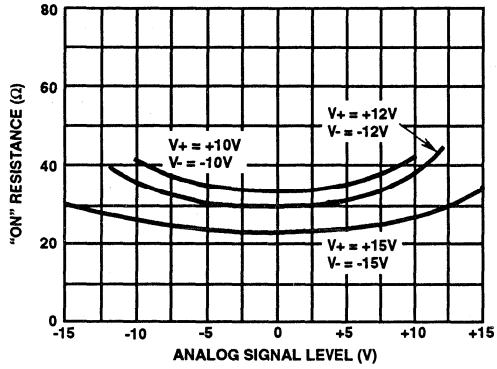


FIGURE 4. "ON" RESISTANCE vs ANALOG SIGNAL LEVEL AND POWER SUPPLY VOLTAGE

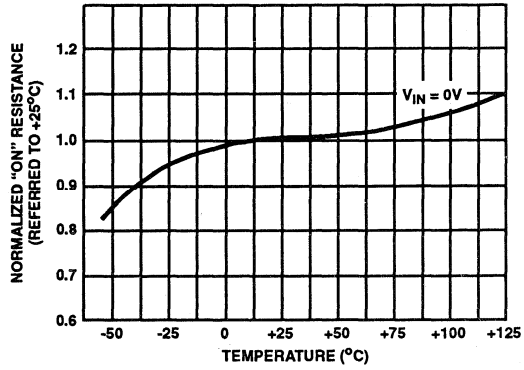
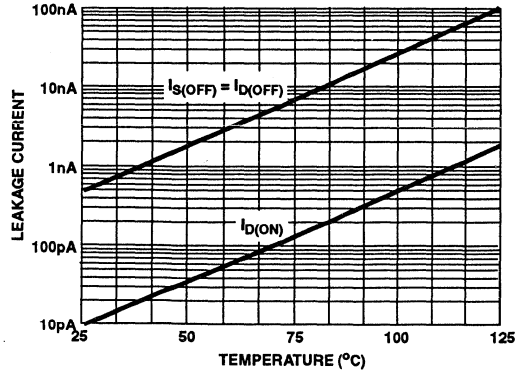
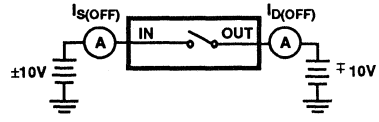


FIGURE 5. NORMALIZED "ON" RESISTANCE vs TEMPERATURE



OFF LEAKAGE CURRENT vs TEMPERATURE



ON LEAKAGE CURRENT vs TEMPERATURE

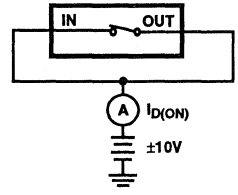
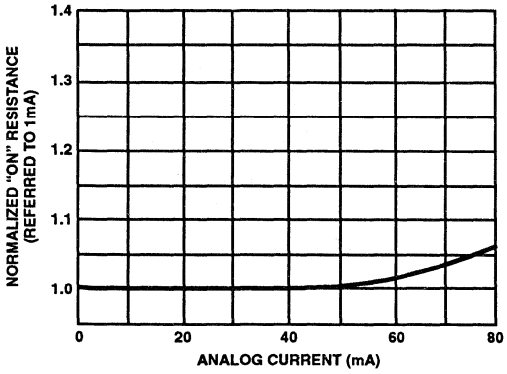


FIGURE 6. ON/OFF LEAKAGE CURRENT vs TEMPERATURE

Typical Performance Curves and Test Circuits

T_A = +25°C, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3.0V and V_{AL} = 0.8V, Unless Otherwise Specified **(Continued)**



"ON" RESISTANCE vs ANALOG CURRENT

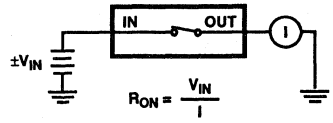
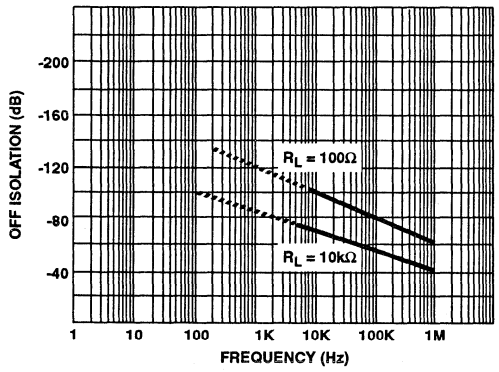


FIGURE 7. NORMALIZED "ON" RESISTANCE vs ANALOG CURRENT



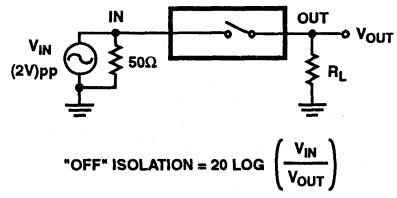
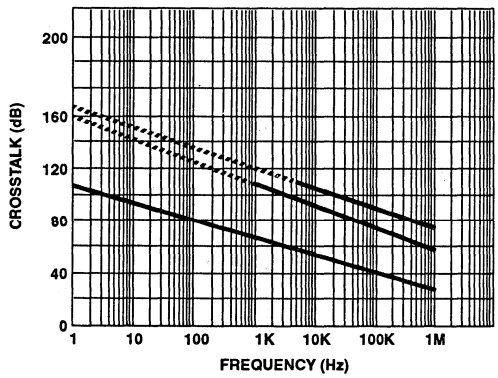


FIGURE 8. "OFF" ISOLATION vs FREQUENCY



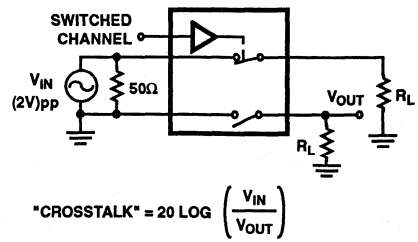
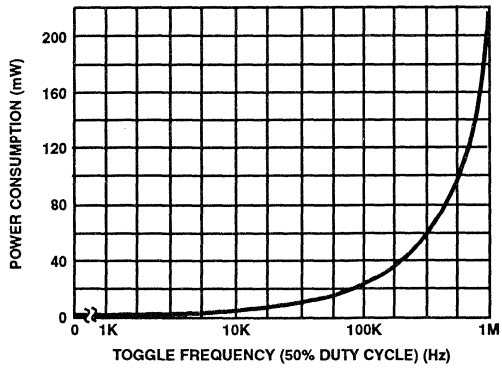


FIGURE 9. CROSSTALK vs FREQUENCY

Typical Performance Curves and Test Circuits

T_A = +25°C, V+ = +15V, V- = -15V, V_L = +5V, V_R = 0V, V_{AH} = 3.0V and V_{AL} = 0.8V, Unless Otherwise Specified **(Continued)**



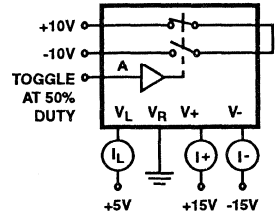


FIGURE 10. POWER CONSUMPTION vs FREQUENCY

Switching Characteristics

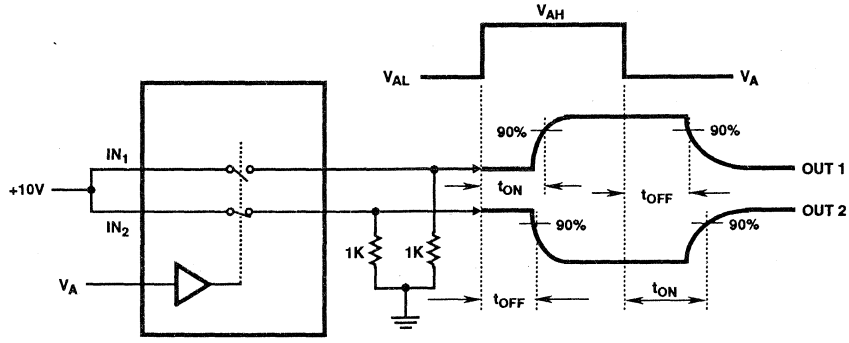


FIGURE 11. ON/OFF SWITCH TIME vs LOGIC LEVEL

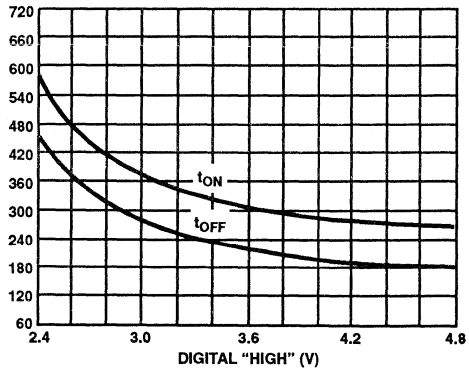


FIGURE 12. SWITCHING TIMES FOR POSITIVE DIGITAL TRANSITION

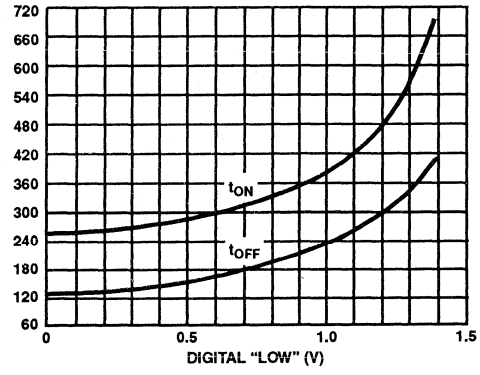


FIGURE 13. SWITCHING TIMES FOR NEGATIVE DIGITAL TRANSITION

Switching Characteristics (Continued)

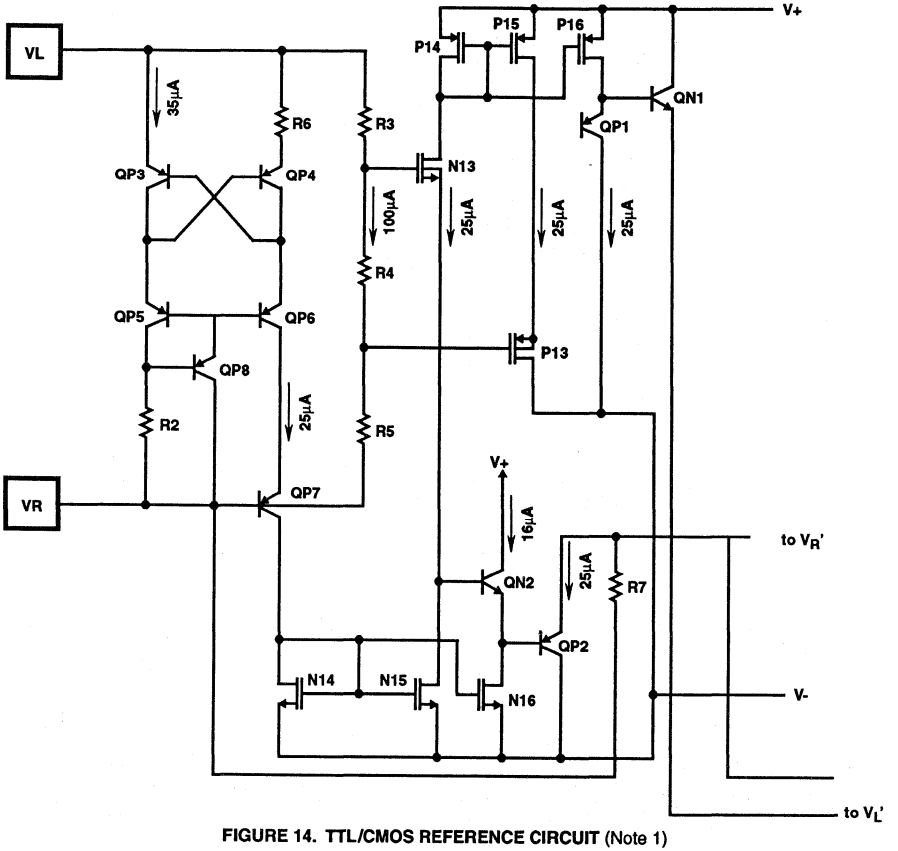


FIGURE 14. TTL/CMOS REFERENCE CIRCUIT (Note 1)

NOTE:

1. Connect V+ to V_L for minimizing power consumption when driving from CMOS circuits.

Switching Characteristics (Continued)

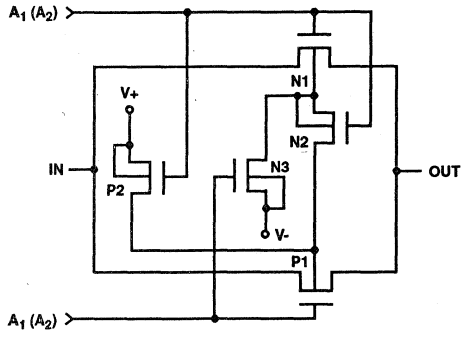
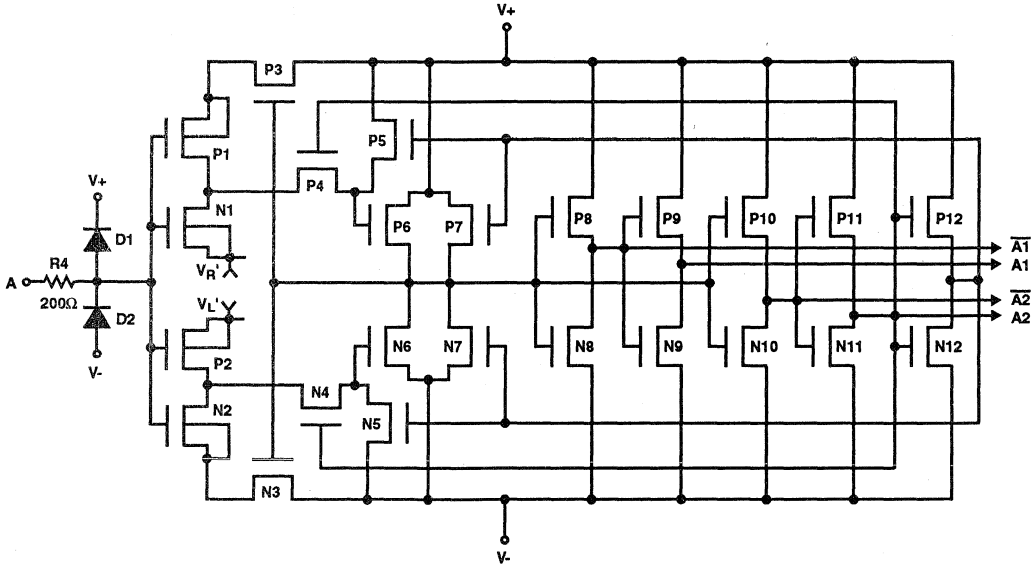


FIGURE 15. SWITCH CELL



NOTES:

1. All n-channel bodies to V-, all p-channel bodies to V+ except as shown.
2. For further information refer to Application Notes 520, 521, 531, 532 and 557.

FIGURE 16. DIGITAL INPUT BUFFER AND LEVEL SHIFTER

HARRIS SEMICONDUCTOR

IH5043

December 1993

Dual SPDT CMOS Analog Switch

Features

- See HI504X and IH514X for Other Functions
- Dual SPDT
- Switches Greater than $20V_{PP}$ Signals with ±15V Supplies
- Quiescent Current Less than 1mA
- Break-Before-Make Switching t_{OFF} 200ns, t_{ON} 300ns Typical
- TTL, DTL, CMOS, PMOS Compatible

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5043MJE	-55°C to +125°C	16 Lead Ceramic DIP
IH5043CJE	0°C to +70°C	16 Lead Ceramic DIP
IH5043CPE	0°C to +70°C	16 Lead Plastic DIP
IH5043CY	0°C to +70°C	16 Lead SOIC (W)
IH5043MJE/883B	-55°C to +125°C	16 Lead Ceramic DIP

Description

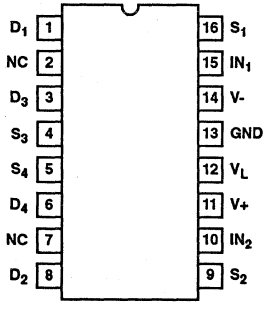
The IH5043 analog switch uses an improved, high voltage CMOS monolithic technology. These devices provide ease of use and performance advantages not previously available from solid state switches.

Key performance advantage is TTL compatibility and ultra low power operation. The quiescent current requirement is less than 1mA. Also, the IH5043 guarantees Break-Before-Make switching, accomplished by extending the t_{ON} time (300ns Typ.), so that it exceeds t_{OFF} time (200ns Typ.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is eliminated.

The IH5043 is a pin-for-pin, improved performance replacement for other analog switches.

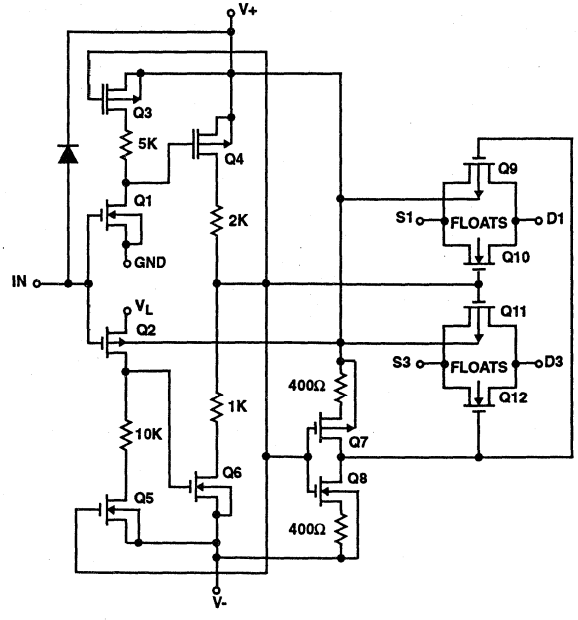
Pinout

IH5043
(CDIP, PDIP, SOIC)
TOP VIEW



Functional Block Diagram

FUNCTIONAL DRIVER, TYPICAL DRIVER, GATE ($^1/_2$ AS SHOWN)



9 SWITCHES

File Number 3130

Absolute Maximum Ratings

V+ to V- ..... <36V
V+ to V_D ..... <30V
V_D to V- ..... <30V
V_D to V_S ..... <±22V
V_L to V- ..... <33V
V_L to V_{IN} ..... <30V
V_L to GND ..... <20V
V_{IN} to GND ..... <20V
Continuous Current (S-D) 30mA
Peak Current (S-D) 70mA
(Pulsed at 1ms, 10% duty cycle Max)
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	80°C/W	24°C/W
Plastic DIP Package	100°C/W	-
SOIC Package	100°C/W	-

Operating Temperature
M Suffix ..... -55°C to +125°C
C Suffix ..... 0°C to +70°C
Junction Temperature
Plastic Packages ..... +150°C
Ceramic Package ..... +175°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

+25°C, V+ = +15V, V- = -15V, V_L = +5V

PER CHANNEL PARAMETERS	TEST CONDITIONS	MILITARY			COMMERCIAL			UNIT
		-55°C	+25°C	+125°C	0°C	+25°C	+70°C	
Input Logic Current, $I_{IN(ON)}$	V_{IN} = 2.4V	±1	±1	10	±1	±1	10	µA
Input Logic Current, $I_{IN(OFF)}$	V_{IN} = 0.8V	±1	±1	10	±1	±1	10	µA
Drain Source On Resistance, $R_{DS(ON)}$	I_S = 10mA, V_{ANALOG} = -10V to +10V	75	75	150	80	80	130	Ω
Channel to Channel $R_{DS(ON)}$ Match, $\Delta R_{DS(ON)}$		-	25 (Typ)	-	-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}		-	±11 (Typ)	-	-	±10 (Typ)	-	V
Switch OFF Leakage Current, $I_{D(OFF)}/I_{S(OFF)}$	V_{ANALOG} = -10V to +10V	-	±1	100	-	±5	100	nA
Switch On Leakage Current, $I_{D(ON)}+I_{S(ON)}$	$V_D = V_S$ = -10V to +10V	-	±2	200	-	±10	100	nA
Switch "ON" Time, t_{ON}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V, see Figure 7	-	1000	-	-	1000	-	ns
Switch "OFF" Time, t_{OFF}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V, see Figure 7	-	500	-	-	500	-	ns
Charge Injection, $Q_{(INJ)}$	See Figure 8	-	15 (Typ)	-	-	20 (Typ)	-	mV
Minimum Off Isolation Rejection Ratio, OIRR	f = 1MHz, R_L = 100Ω, $C_L \leq$ 5pF, See Figure 4	-	54 (Typ)	-	-	50 (Typ)	-	dB
V+ Power Supply Quiescent Current, I_{+Q}		±1	±1	10	10	10	100	µA
V- Power Supply Quiescent Current, I_{-Q}	V+ = +15V, V- = -15V, V_L = +5V	±1	±1	10	10	10	100	µA
+5V Supply Quiescent Current, I_{-LQ}		±1	±1	10	10	10	100	µA
Ground Supply Quiescent Current, I_{GND}		±1	1	10	10	10	100	µA
Minimum Channel to Channel Cross Coupling Rejection Ratio, CCRR	One Channel Off; Any Other Channel Switches as per Figure 3	-	54 (Typ)	-	-	50 (Typ)	-	dB

NOTE:

1. Typical values are for design aid only, not guaranteed and not subject to production testing.

Typical Performance Curves (Per Channel)

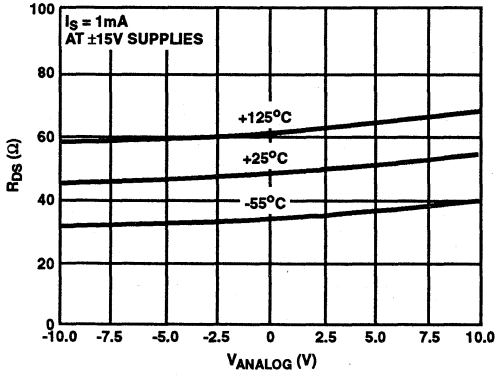


FIGURE 1. $R_{DS(ON)}$ vs V_{ANALOG}

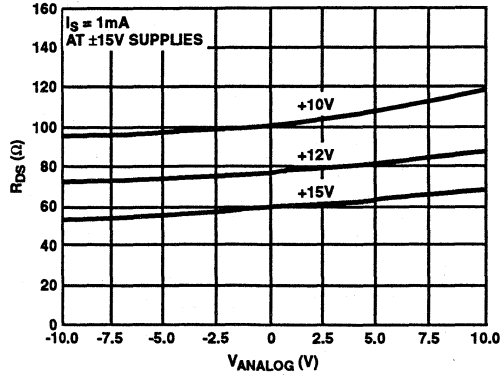
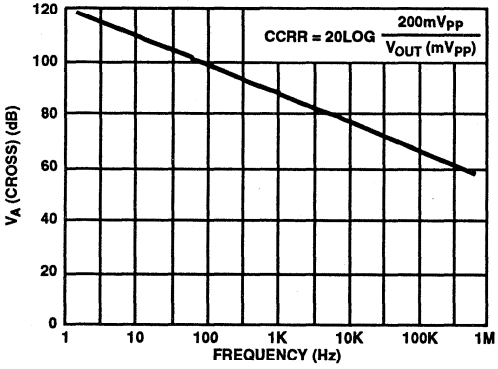


FIGURE 2. $R_{DS(ON)}$ vs POWER SUPPLY VOLTAGE



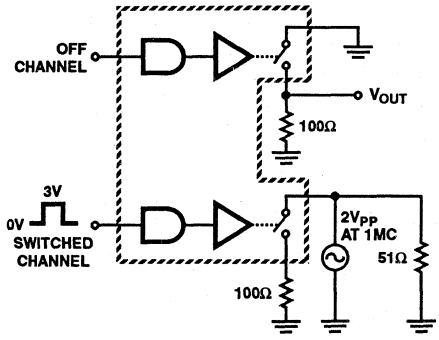
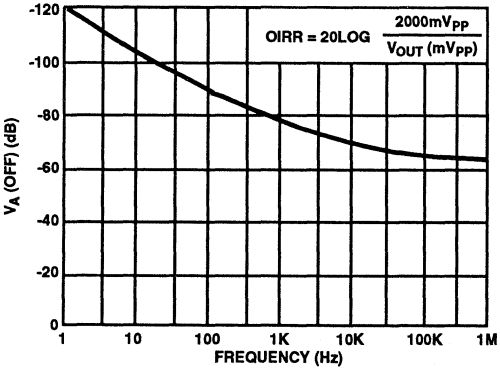


FIGURE 3.



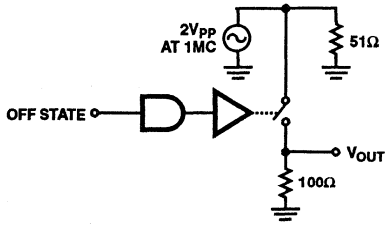


FIGURE 4.

Typical Performance Curves (Per Channel) (Continued)

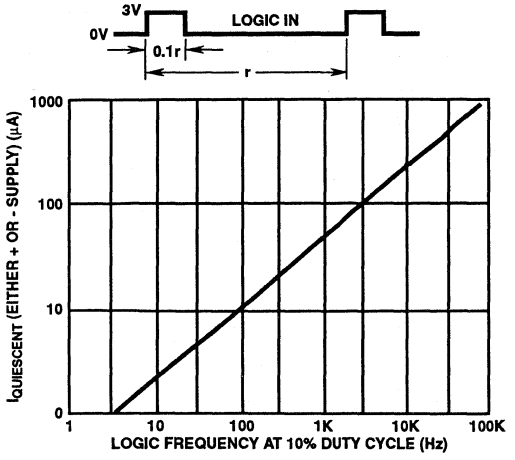


FIGURE 5. POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

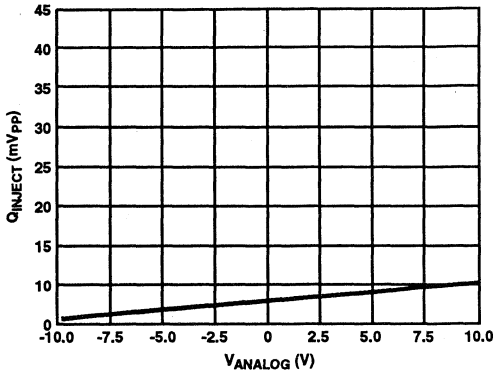


FIGURE 6. CHARGE INJECTION vs V_{ANALOG} (SEE FIGURE 8)

Test Circuits

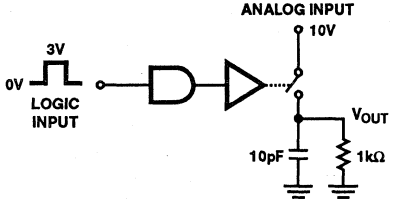


FIGURE 7.

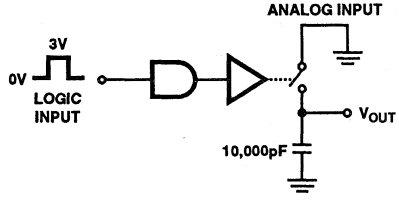
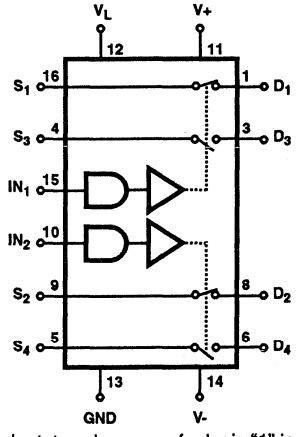


FIGURE 8.



Switch states shown are for logic "1" input.

FIGURE 9. SWITCHING STATE DIAGRAM

Typical Applications

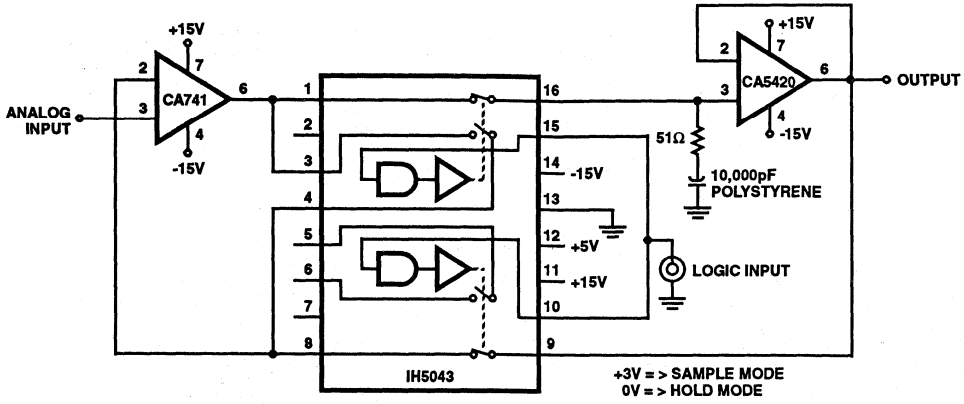


FIGURE 10. IMPROVED SAMPLE AND HOLD

EXAMPLE: If $-V_{ANALOG} = -10V_{DC}$ and $+V_{ANALOG} = +10V_{DC}$ then Ladder Legs are switched between $\pm 10V_{DC}$, depending upon state of Logic Strobe.

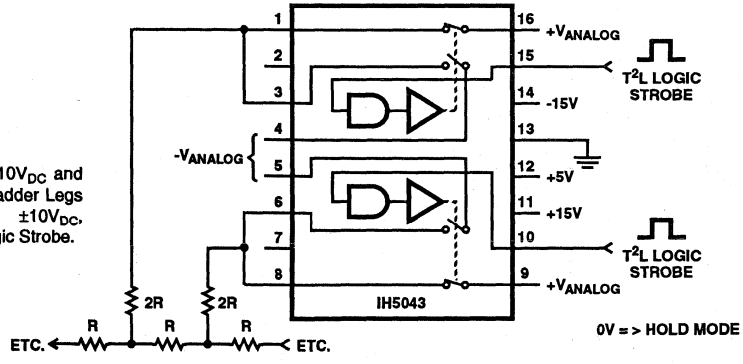
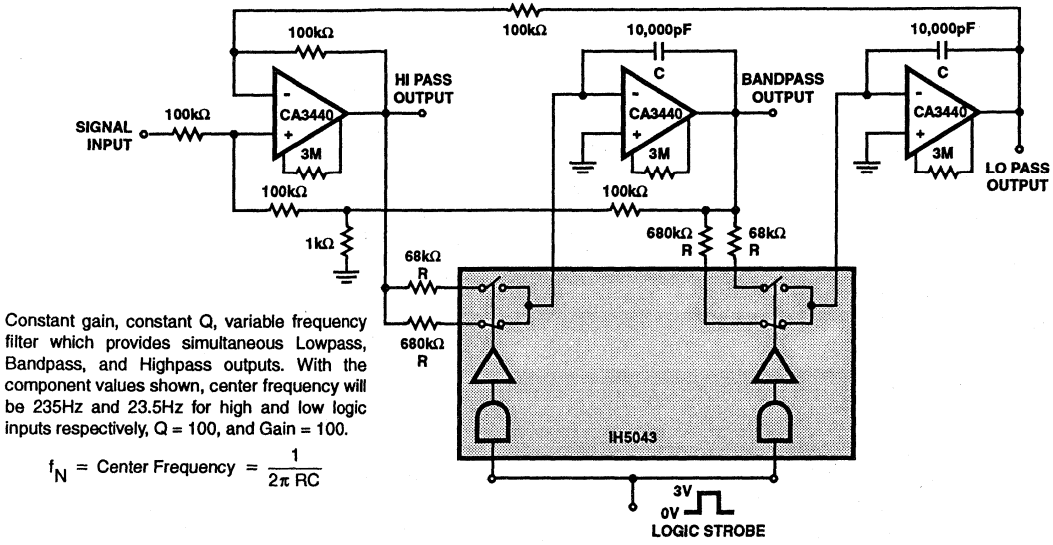


FIGURE 11. USING THE CMOS SWITCH TO DRIVE AN R/2R LADDER NETWORK (2 LEGS)

Typical Applications (Continued)



Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_N = \text{Center Frequency} = \frac{1}{2\pi RC}$$

FIGURE 12. DIGITALLY TUNED LOW POWER ACTIVE FILTER

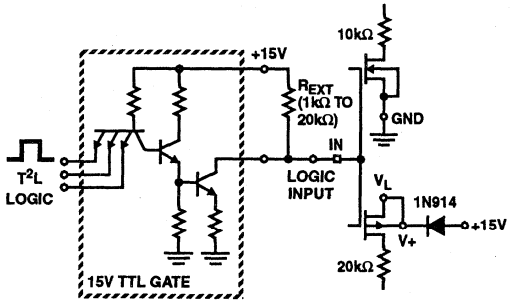


FIGURE 13. INTERFACING WITH TTL OPEN COLLECTOR LOGIC (TYP EXAMPLE FOR +15V CASE SHOWN)

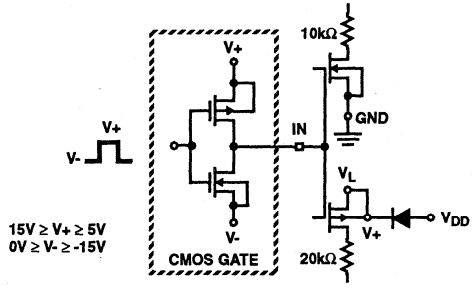


FIGURE 14. INTERFACING WITH CMOS LOGIC

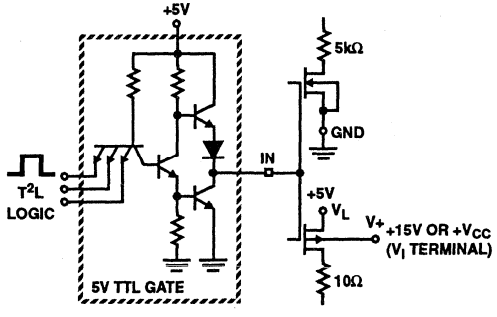


FIGURE 15. TTL LOGIC INTERFACE

Die Characteristics

DIE DIMENSIONS:
1778µm x 1905µm

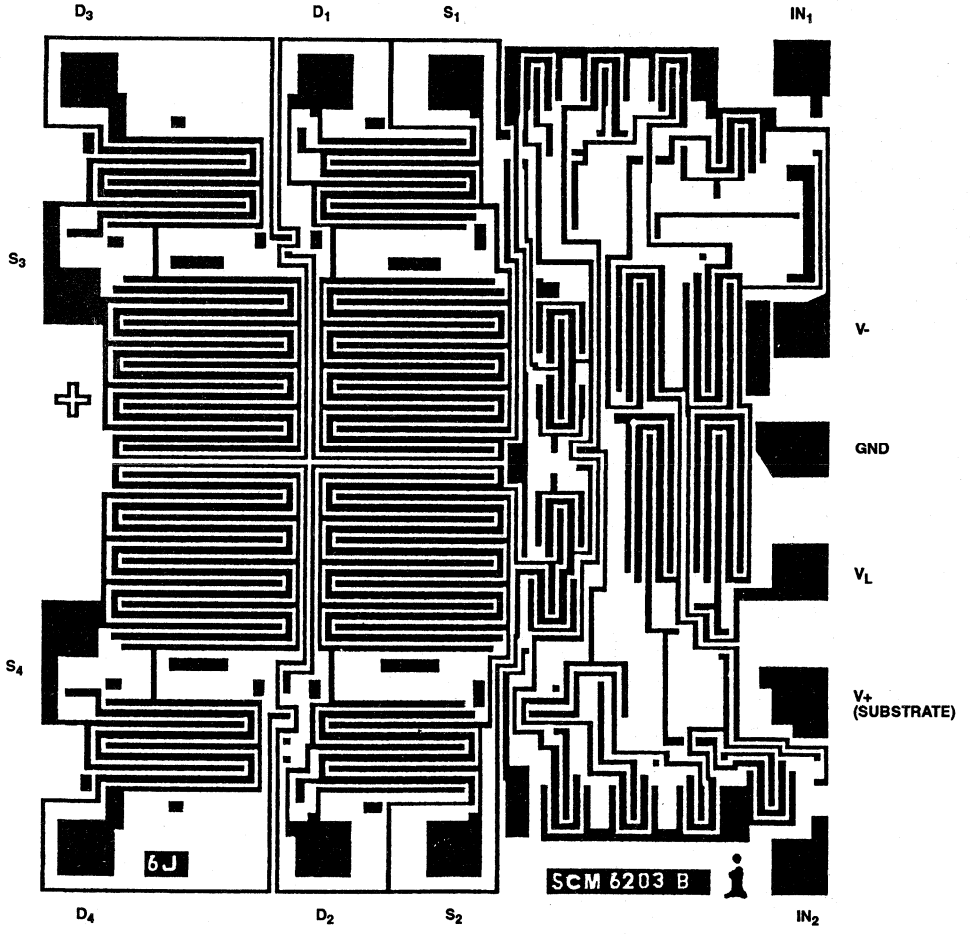
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

IH5043



HARRIS SEMICONDUCTOR

IH5052, IH5053

December 1993

Quad CMOS Analog Switch

Features

- Switches Greater Than 20Vpp Signals with ±15V Supplies
- Quiescent Current Less Than 10μA
- Break-Before-Make Switching t_{OFF} = 500ns, t_{ON} = 1000ns Typical
- TTL, CMOS Compatible
- IH5052 4 Normally Closed Switches
- IH5053 4 Normally Open Switches
- Low $R_{DS(ON)}$ 80Ω Typical

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5052CDE	-0°C to +70°C	16 Lead Ceramic DIP
IH5052MDE	-55°C to +125°C	16 Lead Ceramic DIP
IH5053CDE	-0°C to +70°C	16 Lead Ceramic DIP
IH5053MDE	-55°C to +125°C	16 Lead Ceramic DIP

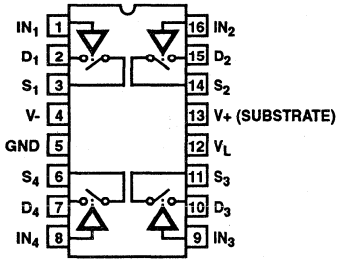
Description

The IH5052, IH5053 analog switches use an improved, high voltage CMOS technology, which provides performance advantages not previously available from solid state switches. Key performance advantages are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 10μA.

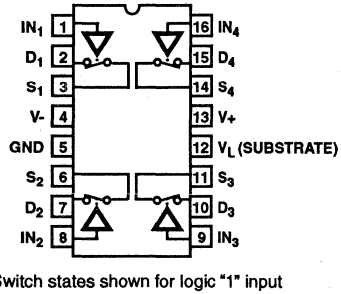
The IH5052, IH5053 also guarantees Break-Before-Make switching. This is accomplished by extending the t_{ON} time (1000ns) such that it exceeds t_{OFF} time (500ns). This insures that an ON channel will be turned OFF before an OFF channel can turn ON, and eliminates the need for external logic required to avoid channel to channel shorting during switching. With a logic "0" (0.8V or less) at its control inputs, the IH5052 switches are closed, while the IH5053 switches are closed with a logic "1" (2.4V or more) at its control inputs.

Pinouts

IH5052 (CDIP)
TOP VIEW

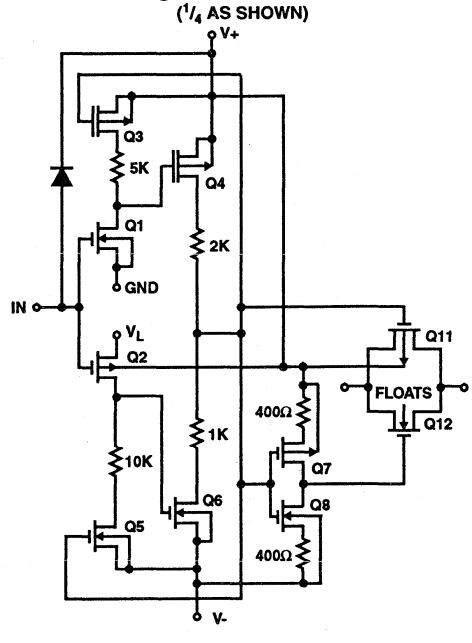


IH5053 (CDIP)
TOP VIEW



Switch states shown for logic "1" input

Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3131

Absolute Maximum Ratings

V+ to V- ..... <36V
V+ to V_D ..... <30V
V_D to V- ..... <30V
V_D to V_S ..... <±22V
V_L to V- ..... <33V
V_L to V_{IN} ..... <30V
V_L to GND ..... <20V
V_{IN} to GND ..... <20V
Continuous Current (S-D) 30mA
Peak Current (S-D) 70mA
(Pulsed at 1ms, 10% duty cycle Max)
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Operating Temperature
M Suffix ..... -55°C to +125°C
C Suffix ..... 0°C to +70°C
Junction Temperature ..... +175°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C, V+ = +15V, V- = -15V, V_L = +5V

PER CHANNEL PARAMETERS	TEST CONDITIONS	M SUFFIX			C SUFFIX			UNITS
		-55°C	+25°C	+125°C	0°C	+ 25°C	+ 70°C	
Input Logic Current, $I_{IN(ON)}$	V_{IN} = 2.4V (IH5053) = 0.8V (IH5052)	10	±1	10	-	±10	-	µA
Input Logic Current, $I_{IN(OFF)}$	V_{IN} = 0.8V (IH5053) = 2.4V (IH5052)	10	±1	10	-	±10	-	µA
Drain Source On Resistance, $R_{DS(ON)}$	I_S = 10mA, V_{ANALOG} = -10V to +10V	75	75	100	80	80	100	Ω
Channel to Channel, $R_{DS(ON)}$ Match	(Note 1)	-	25 (Typ)	-	-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}	(Note 1)	-	±11 (Typ)	-	-	±10 (Typ)	-	V
Switch OFF Leakage Current, $I_{D(OFF)}$, $I_{S(OFF)}$	V_{ANALOG} = -10V to +10V	-	±1	100	-	±5	100	nA
Switch On Leakage Current, $I_{D(ON)} + I_{S(ON)}$	$V_D = V_S$ = -10V to +10V	-	±2	200	-	±10	100	nA
Switch "ON" Time, t_{ON}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V See Figure 7	-	500	-	-	1000	-	ns
Switch "OFF" Time, T_{OFF}	R_L = 1kΩ, V_{ANALOG} = -10V to +10V See Figure 7	-	250	-	-	500	-	ns
Charge Injection, Q(INJ)	See Figure 8 (Note 1)	-	15 (Typ)	-	-	20 (Typ)	-	mV
Minimum Off Isolation Rejection Ratio OIRR	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF See Figure 4 (Note 1)	-	54 (Typ)	-	-	50 (Typ)	-	dB
+ Power Supply Quiescent Current, I+	V+ = +15V, V- = -15V, V_L = +5V	10	10	100	10	10	100	µA
- Power Supply Quiescent Current, I-	V+ = +15V, V- = -15V, V_L = +5V	10	10	100	10	10	100	µA
+5V Supply Quiescent Current, I_{VL}	V+ = +15V, V- = -15V, V_L = +5V	10	10	100	10	10	100	µA
Minimum Channel to Channel Cross Coupling Rejection Ratio, CCRR	One Channel Off	-	54 (Typ)	-	-	50 (Typ)	-	dB

NOTE:

1. Typical values are for Design Aid only, not guaranteed nor production tested.

Typical Performance Curves

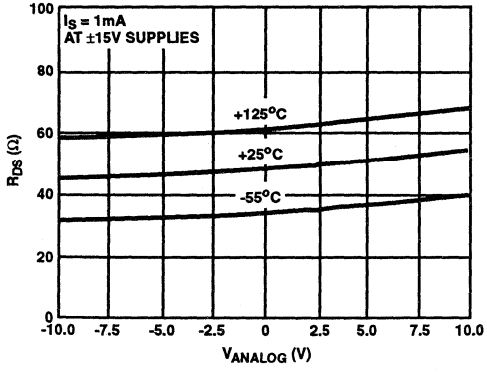


FIGURE 1. $R_{DS(ON)}$ vs V_{ANALOG}

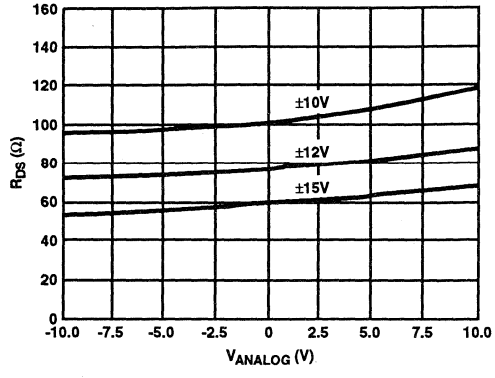


FIGURE 2. $R_{DS(ON)}$ vs POWER SUPPLY VOLTAGE

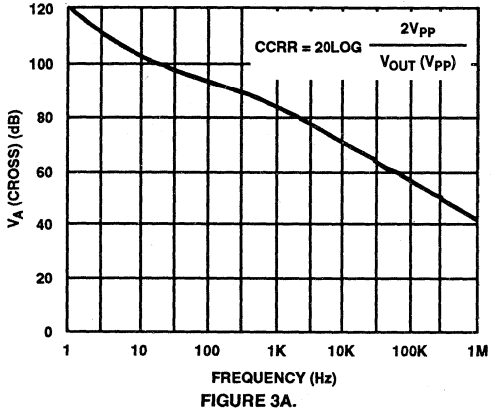


FIGURE 3A.

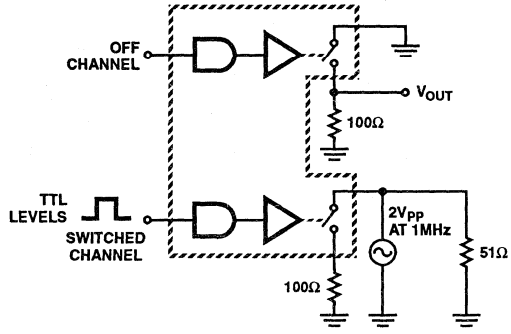


FIGURE 3B.

FIGURE 3. CROSS COUPLING REJECTION vs FREQUENCY

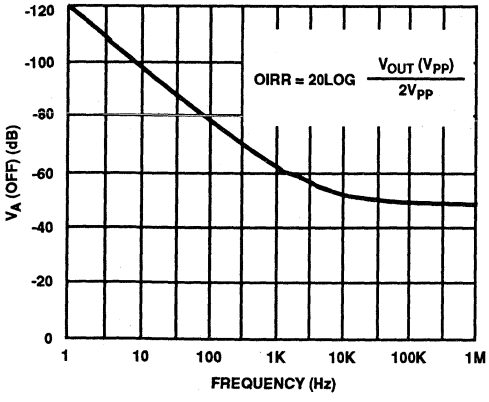


FIGURE 4A.

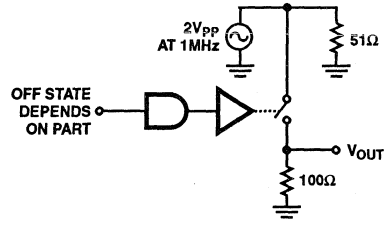


FIGURE 4B.

FIGURE 4. OFF ISOLATION vs FREQUENCY

Typical Performance Curves (Continued)

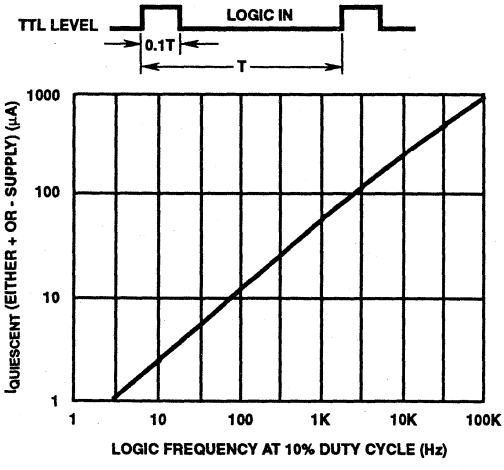


FIGURE 5. POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

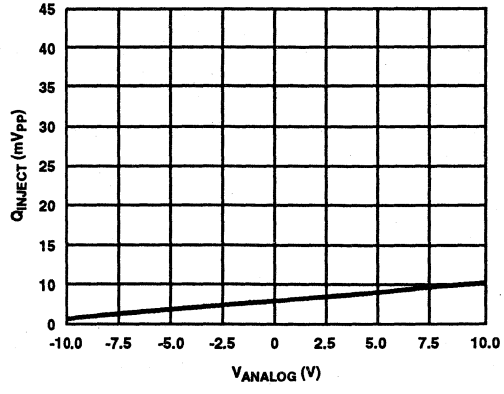


FIGURE 6. CHARGE INJECTION vs V_{ANALOG} (SEE FIGURE 8) C_L = 10,000pF

Test Circuits

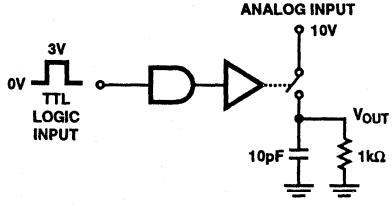


FIGURE 7.

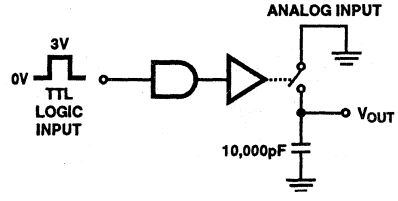


FIGURE 8.

Typical Applications

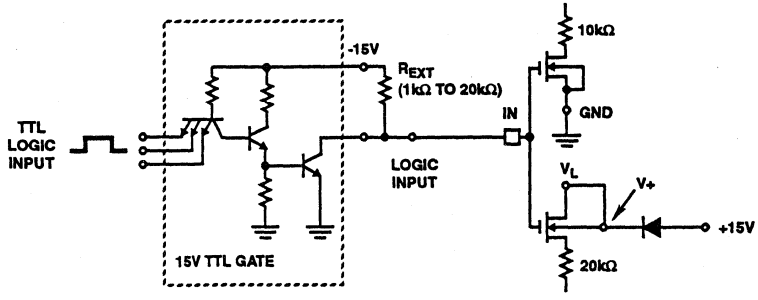


FIGURE 9. +15V OPEN COLLECTOR TTL INTERFACE TO IH5052/IH5053

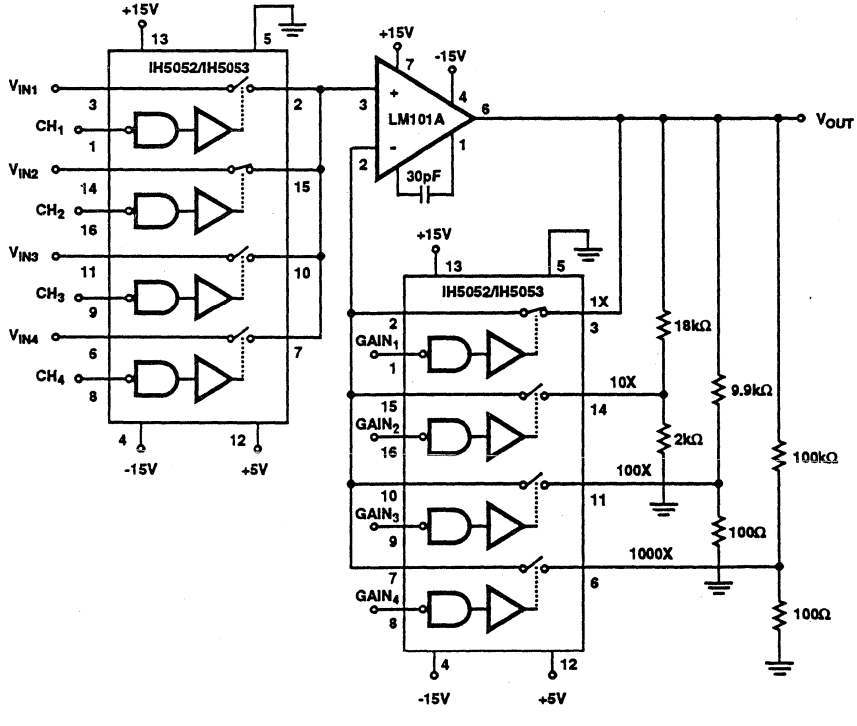


FIGURE 10. ACTIVE LOW PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY

Typical Applications

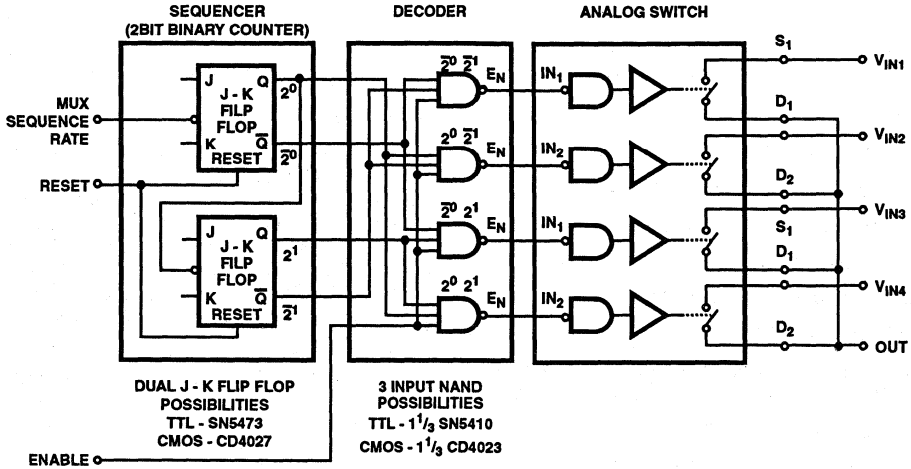


FIGURE 11. 4 - CHANNEL SEQUENCING MUX

TRUTH TABLE (IH5052)

ENABLE	MUX SEQUENCE RATE	SEQUENCER OUTPUT		SWITCH STATES (- DENOTES OFF)			
		2^0	2^1	SW1	SW2	SW3	SW4
0	0	0	0	-	-	-	-
1	0	0	0	ON	-	-	-
1	1 Pulse	1	0	-	ON	-	-
1	2 Pulses	0	1	-	-	-	-
1	3 Pulses	1	1	-	-	-	ON
1	4 Pulses	0	0	ON	-	-	-

A Latching DPDT Switch

The latch feature insures positive switching action in response to non-repetitive or erratic commands. The A_1 and A_2 inputs are normally low. A HIGH input to A_2 turns S_1 and S_2 ON, a HIGH to A_1 turns S_3 and S_4 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.

TRUTH TABLE (IH5052)

COMMAND		STATE OF SWITCHES AFTER COMMAND	
A_2	A_1	S_3 and S_4	S_1 and S_2
0	0	Same	Same
0	1	On	Off
1	0	Off	On
1	1	INDETERMINATE	

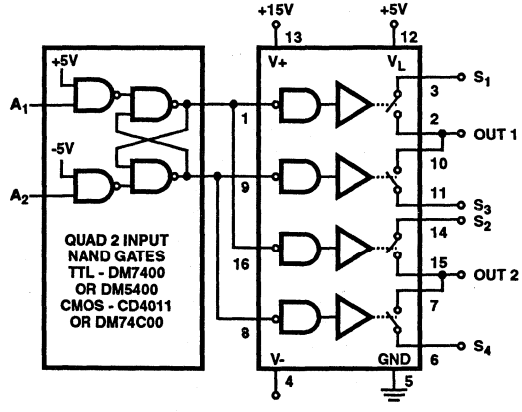


FIGURE 12. A LATCHING DPDT

HARRIS SEMICONDUCTOR IH5140 thru IH5145

High-Level CMOS Analog Switch

December 1993

Features

- Super Fast Break-Before-Make Switching
- t_{ON} 80ns Typ, t_{OFF} 50ns Typ (SPST Switches)
- Power Supply Currents Less Than 1μA
- OFF Leakages Less Than 100pA at +25°C Typical
- Non-Latching with Supply Turn-Off
- Single Monolithic CMOS Chip
- Plug-In Replacements for IH5040 Family and Part of the DG180 Family to Upgrade Speed and Leakage
- Greater Than 1MHz Toggle Rate
- Switches Greater Than 20Vp-p Signals with ±15V Supplies
- TTL, CMOS Direct Compatibility
- Internal Diode in Series with V+ for Fault Protection

Description

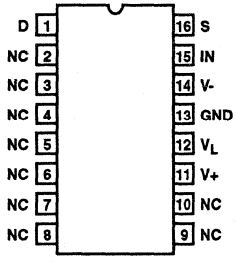
The IH5140 Family of CMOS switches utilizes Harris' latch-free junction isolated processing to build the fastest switches currently available. These switches can be toggled at a rate of greater than 1MHz with fast t_{ON} times (80ns typical) and faster t_{OFF} times (50ns typical), guaranteeing break before make switching. This family of switches combines the speed of the hybrid FET DG180 family with the reliability and low power consumption of a monolithic CMOS construction.

Very low quiescent power is dissipated in either the ON or the OFF state of the switch. Maximum power supply current is 10μA (at +25°C) from any supply and typical quiescent currents are in the 10nA which makes these devices ideal for portable equipment and military applications.

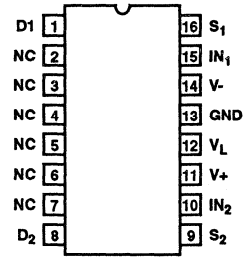
The IH5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic. It is pin compatible with Harris' IH5040 family and part of the DG180/DG190 family as shown in the switching state diagrams.

Pinouts

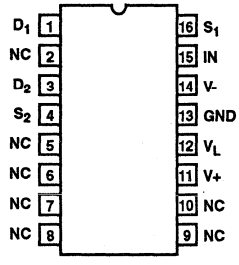
IH5140
(PDIP, CDIP)
TOP VIEW



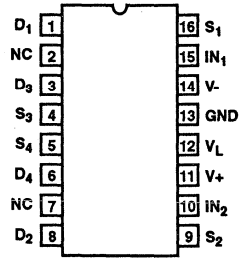
IH5141
(PDIP, CDIP)
TOP VIEW



IH5142
(PDIP, CDIP)
TOP VIEW



IH5143
(PDIP, CDIP)
TOP VIEW

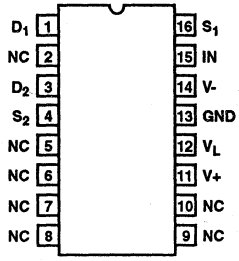


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

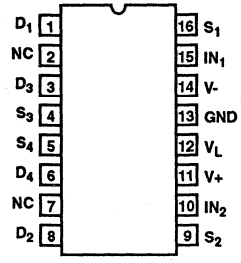
File Number **3132**

Pinouts (Continued)

IH5144
(PDIP, CDIP)
TOP VIEW



IH5145
(PDIP, CDIP)
TOP VIEW



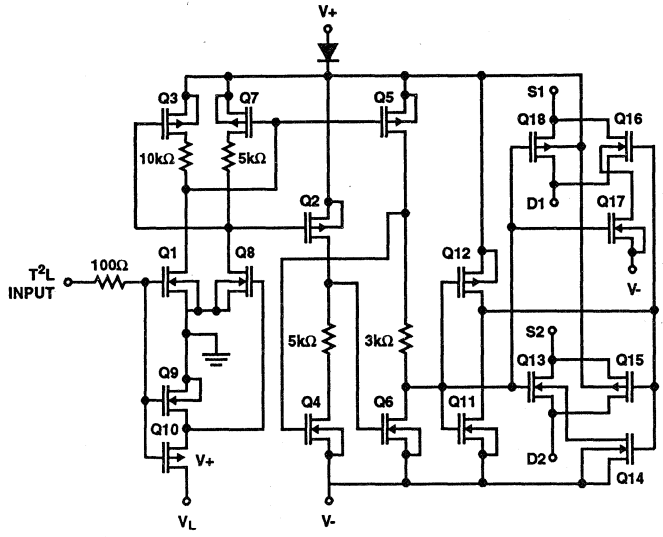
Ordering Information

PART NUMBER	FUNCTION	TEMPERATURE RANGE	PACKAGE
IH5140MJE	SPST	-55°C to +125°C	16 Lead Ceramic DIP
IH5140CJE	SPST	0°C to +70°C	16 Lead Ceramic DIP
IH5140CPE	SPST	0°C to +70°C	16 Lead Plastic DIP
IH5141MJE	Dual SPST	-55°C to +125°C	16 Lead Ceramic DIP
IH5141CJE	Dual SPST	0°C to +70°C	16 Lead Ceramic DIP
IH5141CPE	Dual SPST	0°C to +70°C	16 Lead Plastic DIP
IH5142MJE	SPDT	-55°C to +125°C	16 Lead Ceramic DIP
IH5142CJE	SPDT	0°C to +70°C	16 Lead Ceramic DIP
IH5142CPE	SPDT	0°C to +70°C	16 Lead Plastic DIP
IH5143MJE	Dual SPDT	-55°C to +125°C	16 Lead Ceramic DIP
IH5143CJE	Dual SPDT	0°C to +70°C	16 Lead Ceramic DIP
IH5143CPE	Dual SPDT	0°C to +70°C	16 Lead Plastic DIP
IH5144MJE	DPST	-55°C to +125°C	16 Lead Ceramic DIP
IH5144CJE	DPST	0°C to +70°C	16 Lead Ceramic DIP
IH5144CPE	DPST	0°C to +70°C	16 Lead Plastic DIP
IH5145MJE	Dual DPST	-55°C to +125°C	16 Lead Ceramic DIP
IH5145CJE	Dual DPST	0°C to +70°C	16 Lead Ceramic DIP
IH5145CPE	Dual DPST	0°C to +70°C	16 Lead Plastic DIP
IH5140MJE/883B	SPST	-55°C to +125°C	16 Lead Ceramic DIP
IH5141MJE/883B	Dual SPST	-55°C to +125°C	16 Lead Ceramic DIP
IH5142MJE/883B	SPDT	-55°C to +125°C	16 Lead Ceramic DIP
IH5143MJE/883B	Dual SPDT	-55°C to +125°C	16 Lead Ceramic DIP
IH5144MJE/883B	DPST	-55°C to +125°C	16 Lead Ceramic DIP
IH5145MJE/883B	Dual DPST	-55°C to +125°C	16 Lead Ceramic DIP

NOTES:

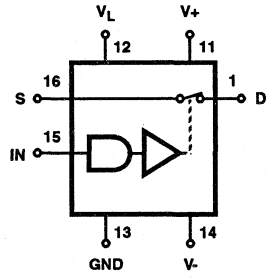
1. For MIL-STD-883 compliant parts, request the /883 datasheet on the above products.

Functional Block Diagram

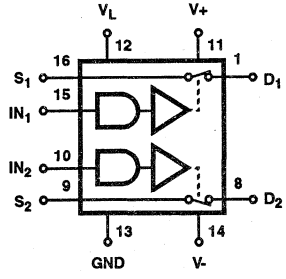


TYPICAL DRIVER/GATE - IH5142

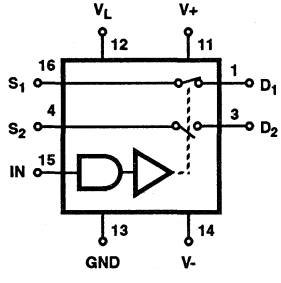
Switching State Diagrams



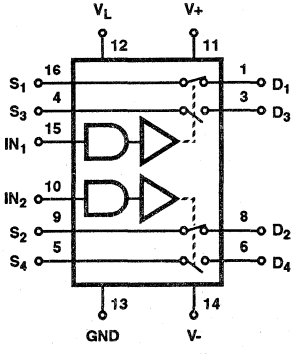
DIP (JE, PE)
SPST IH5140



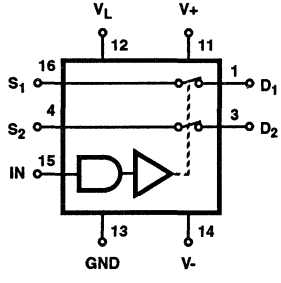
DIP (JE, PE)
DUAL SPST IH5141



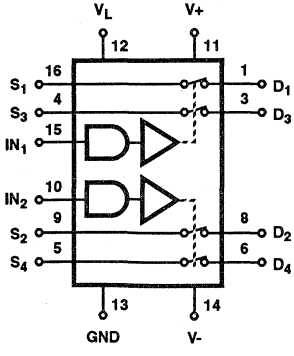
DIP(JE, PE)
SPDT IH5142



DIP (JE, PE)
DUAL SPDT IH5143



DIP (JE, PE)
DPST IH5144



DIP (JE, PE)
DUAL DPST IH5145

Absolute Maximum Ratings

V+ to V- ..... <36V
V+ to V_D ..... <30V
V_D to V- ..... <30V
V_D to V_S ..... <±22V
V_L to V- ..... <33V
V_L to V_{IN} ..... <30V
V_L to GND ..... <20V
V_{IN} to GND ..... <20V
Current (Any Terminal) 30mA
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	80°C/W	24°C/W
Plastic DIP Package	100°C/W	-

Operating Temperature
M ..... -55°C to +125°C
C ..... 0°C to +70°C
Junction Temperature
Ceramic DIP Package ..... +175°C
Plastic DIP Package ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications +25°C, V+ = +15V, V- = -15V, V_L = +5V

PER CHANNEL PARAMETERS	TEST CONDITIONS	MILITARY			COMMERCIAL			UNITS
		-55°C	+25°C	+125°C	0°C	+25°C	+70°C	
LOGIC INPUT								
Input Logic Current, I_{INH}	V_{IN} = 2.4V, Note 1	±1	±1	10	–	±10	10	µA
Input Logic Current, I_{INL}	V_{IN} = 0.8V, Note 1	±1	±1	10	–	±10	10	µA
SWITCH								
Drain Source On Resistance, $R_{DS(ON)}$	I_S = -10mA, V_{ANALOG} = -10V to +10V	50	50	75	75	75	100	Ω
Channel to Channel $R_{DS(ON)}$ Match, $\Delta R_{DS(ON)}$		-	25 (Typ)	-	-	30 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}		-	±11 (Typ)	-	-	±10 (Typ)	-	V
Switch OFF Leakage Current, $I_{D(OFF)}$+$I_{S(OFF)}$	V_D = +10V, V_S = -10V	-	±0.5	100	-	±5	100	nA
	V_D = -10V, V_S = +10V	-	±0.5	100	-	±5	100	nA
Switch On Leakage Current, $I_{D(ON)}$+$I_{S(ON)}$	V_D = V_S = -10V to +10V	-	±1	200	-	±2	200	nA
Minimum Channel to Channel Cross Coupling Rejection Ratio, CCRR	One Channel Off; Any Other Channel Switches, See Performance Characteristics	-	54 (Typ)	-	-	50 (Typ)	-	dB
Switch "ON" Time, t_{ON}	See switching time specifications and timing diagrams							
Switch "OFF" Time, t_{OFF}	See switching time specifications and timing diagrams							
Charge Injection, $Q_{(INJ)}$	See Performance Characteristics	-	10 (Typ)	-	-	15 (Typ)	-	pC
Minimum Off Isolation Rejection Ratio, OIRR	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF, See Performance Characteristics	-	54 (Typ)	-	-	50 (Typ)	-	dB
SUPPLY								
+ Power Supply Quiescent Current, I+	V+ = +15V, V- = -15V, V_L = +5V, See Performance Characteristics	1.0	1.0	10	10	10	100	µA
- Power Supply Quiescent Current, I-		1.0	1.0	10	10	10	100	µA
+5V Supply Quiescent Current, I_L		1.0	1.0	10	10	10	100	µA
Ground Supply Quiescent Current, I_{GND}		1.0	1.0	10	10	10	100	µA

NOTE:

1. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the minimum range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.

Switching Time Specifications (t_{ON}, t_{OFF} are Maximum Specifications and t_{ON} - t_{OFF} is Minimum Specification)

PART NUMBER	SPECIFICATIONS	TEST CONDITIONS	MILITARY			COMMERCIAL			UNITS
			-55°C	+25°C	+125°C	0°C	+25°C	+70°C	
IH5140, IH5141	Switch "ON" Time, t_{ON}	Figure 8, Note 2	-	100	-	-	150	-	ns
	Switch "OFF" Time, t_{OFF}		-	75	-	-	125	-	ns
	Break-Before-Make, t_{ON} - t_{OFF}		-	10	-	-	5	-	ns
	Switch "ON" Time, t_{ON}	Figure 7	-	150	-	-	175	-	ns
	Switch "OFF" Time, t_{OFF}		-	125	-	-	150	-	ns
IH5142, IH5143	Switch "ON" Time, t_{ON}	Figure 8, Note 2	-	175	-	-	250	-	ns
	Switch "OFF" Time, t_{OFF}		-	125	-	-	150	-	ns
	Break-Before-Make, t_{ON} - t_{OFF}		-	10	-	-	5	-	ns
	Switch "ON" Time, t_{ON}	Figure 7	-	200	-	-	300	-	ns
	Switch "OFF" Time, t_{OFF}		-	125	-	-	150	-	ns
	Switch "ON" Time, t_{ON}	Figure 2, Note 2	-	175	-	-	250	-	ns
	Switch "OFF" Time, t_{OFF}		-	125	-	-	150	-	ns
	Break-Before-Make, t_{ON} - t_{OFF}		-	10	-	-	5	-	ns
	Switch "ON" Time, t_{ON}	Figure 3, Note 2	-	200	-	-	300	-	ns
	Switch "OFF" Time, t_{OFF}		-	125	-	-	150	-	ns
	Break-Before-Make, t_{ON} - t_{OFF}		-	10	-	-	5	-	ns
IH5144, IH5145	Switch "ON" Time, t_{ON}	Figure 8, Note 2	-	175	-	-	250	-	ns
	Switch "OFF" Time, t_{OFF}		-	125	-	-	150	-	ns
	Break-Before-Make, t_{ON} - t_{OFF}		-	10	-	-	5	-	ns
	Switch "ON" Time, t_{ON}	Figure 7	-	200	-	-	300	-	ns
	Switch "OFF" Time, t_{OFF}		-	125	-	-	150	-	ns

NOTES:

1. Switching times are measured at 90% points.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.

Typical Performance Curves

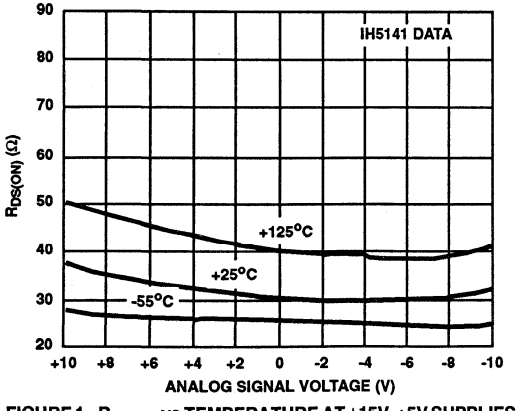


FIGURE 1. $R_{DS(ON)}$ vs TEMPERATURE AT ±15V, +5V SUPPLIES

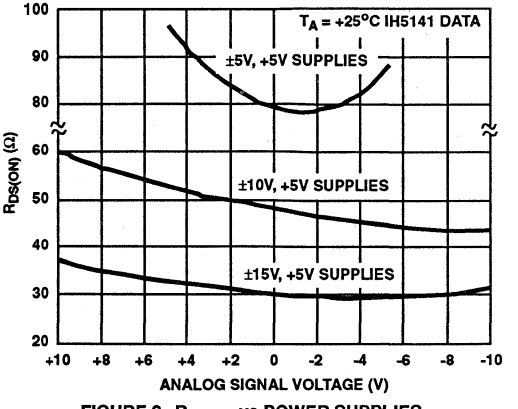
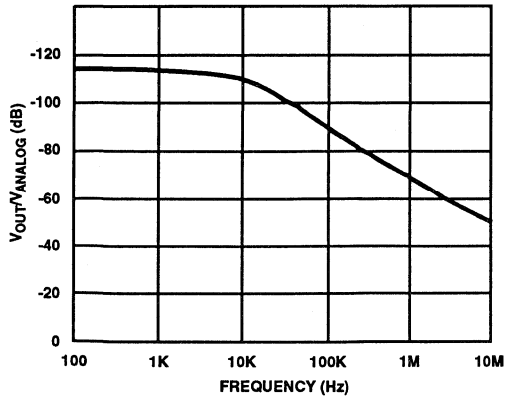
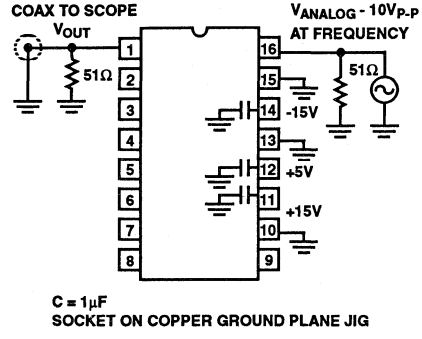


FIGURE 2. $R_{DS(ON)}$ vs POWER SUPPLIES

Typical Performance Curves (Continued)

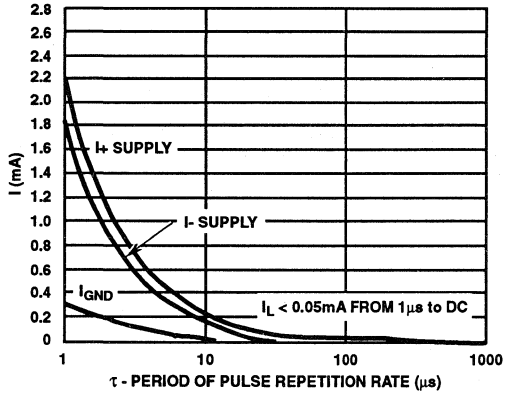


3A.

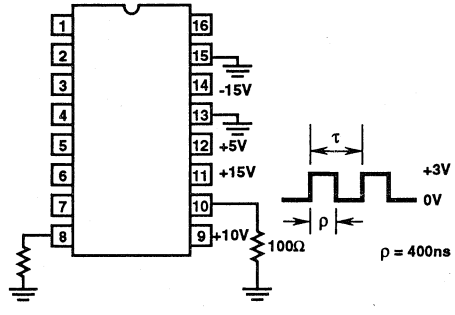


3B.

FIGURE 3. "OFF" ISOLATION vs FREQUENCY

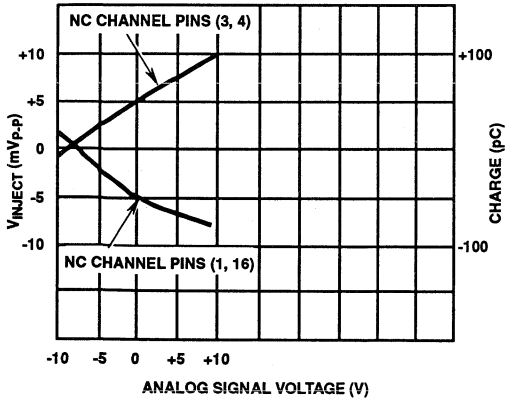


4A.

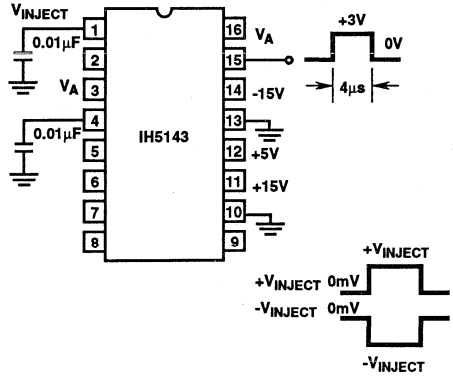


4B.

FIGURE 4. POWER SUPPLY CURRENTS vs LOGIC STROBE RATE



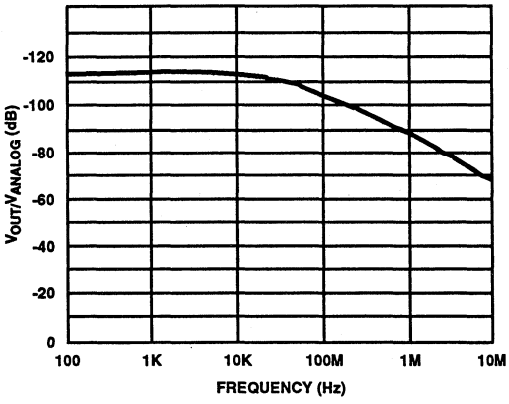
5A.

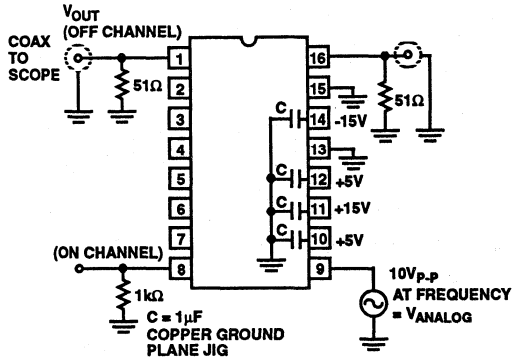


5B.

FIGURE 5. CHARGE INJECTION vs ANALOG SIGNAL

Typical Performance Curves (Continued)





6A. 6B.

FIGURE 6. CHANNEL TO CHANNEL CROSS COUPLING REJECTION vs FREQUENCY

Test Circuits

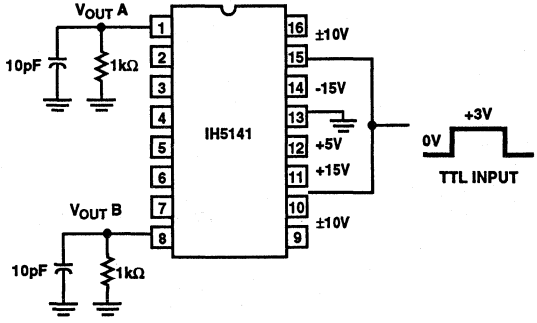
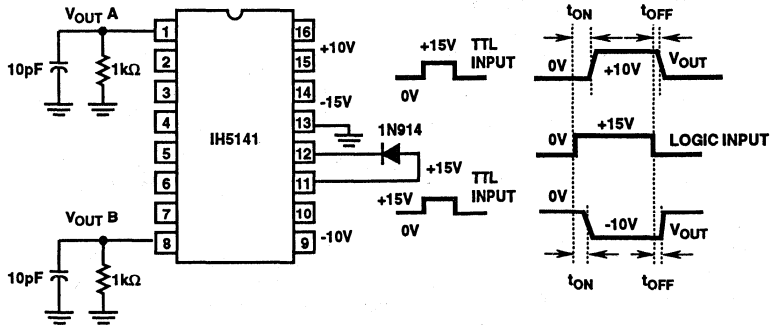


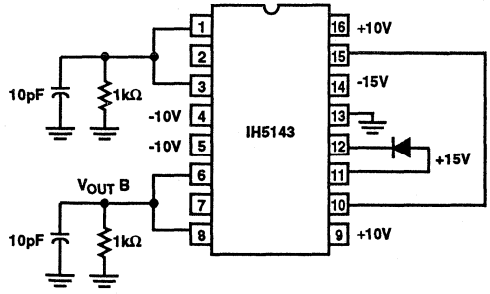
FIGURE 7. IH5141 t_{ON} AND t_{OFF} (3V DIGITAL INPUT)



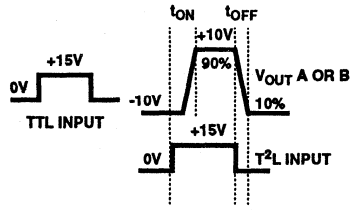
NOTE: SWITCHING TIMES ARE MEASURED AT 90% POINTS

FIGURE 8. IH5141 t_{ON} AND t_{OFF} (15V DIGITAL INPUT)

Test Circuits (Continued)



9A.



9B.

FIGURE 9. IH5143 t_{ON} AND t_{OFF} (15V DIGITAL INPUT)

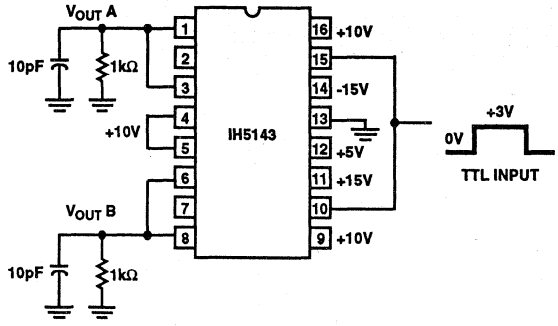


FIGURE 10. IH5143 t_{ON} AND t_{OFF} (3V DIGITAL INPUT)

Typical Applications

To maximize switching speed on the IH5140 family, TTL open collector logic (15V with a 1kΩ or less collector resistor) should be used. This configuration will result in (SPST) t_{ON} and t_{OFF} times of 80ns and 50ns, for signals between -10V and +10V. The SPDT and DPST switches are approximately 30ns slower in both t_{ON} and t_{OFF} with the same drive configuration. 15V CMOS logic levels can be used (0V to +15V), but propagation delays in the CMOS logic will slow down the switching (typical 50ns → 100ns delays).

When driving the IH5140 Family from either +5V TTL or CMOS logic, switching times run 20ns slower than if they were driven from +15V logic levels. Thus t_{ON} is about 105ns, and t_{OFF} 75ns for SPST switches, and 135ns and 105ns (t_{ON}, t_{OFF}) for SPDT or DPST switches. The low level drive can be made as fast as the high level drive if ±5V strobe levels are used instead of the usual 0V → +3.0V drive. Pin 13 is taken to -5V instead of the usual GND and strobe input is taken from +5V to -5V levels as shown in Figure 11.

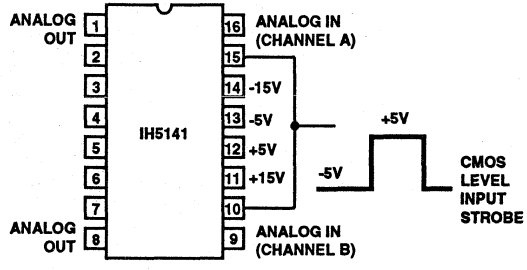


FIGURE 11.

The typical channel of the IH5140 family consists of both P and N-channel MOSFETs. The N-channel MOSFET uses a "Body Puller" FET to drive the body to -15V (±15V supplies) to get good breakdown voltages when the switch is in the off state (see Figure 12). This "Body Puller" FET also allows the N-channel body to electrically float when the switch is in the

on state producing a fairly constant $R_{DS(ON)}$ with different signal voltages. While this "Body Puller" FET improves switch performance, it can cause a problem when analog input signals are present (negative signals only) and power supplies are off. This fault condition is shown in Figure 13.

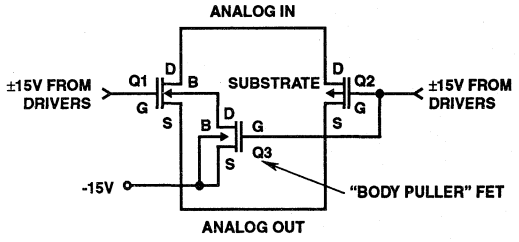


FIGURE 12.

Current will flow from -10V analog voltage through the drain to body junction of Q1, then through the drain to body junction of Q3 to GND. This means that there is 10V across two forward-biased silicon diodes and current will go to whatever value the input signal source is capable of supplying. If the analog input signal is derived from the same supplies as the switch this fault condition cannot occur. Turning off the supplies would turn off the analog signal at the same time.

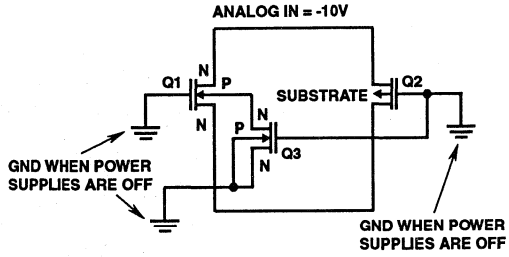


FIGURE 13.

This fault situation can also be eliminated by placing a diode in series with the negative supply line (pin 14) as shown in Figure 14. Now when the power supplies are off and a negative input signal is present this diode is reverse biased and no current can flow.

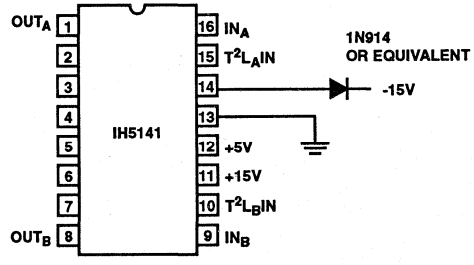
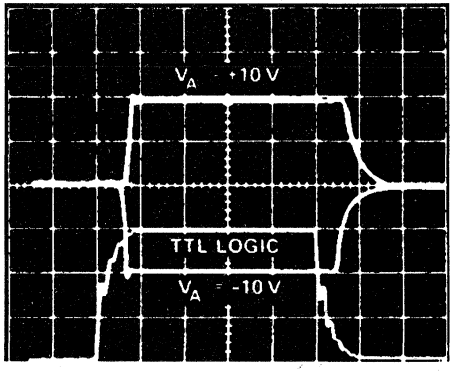
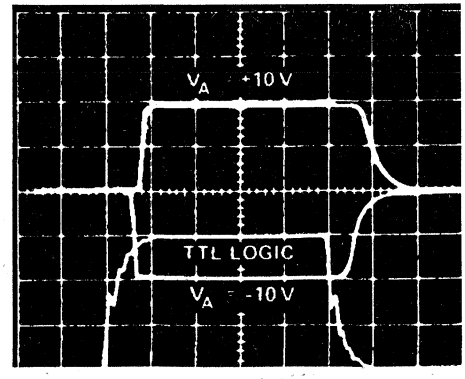


FIGURE 14.

Typical Switching Waveforms (Scale: Vertical = 5V/DIV., Horizontal = 100ns/DIV.)

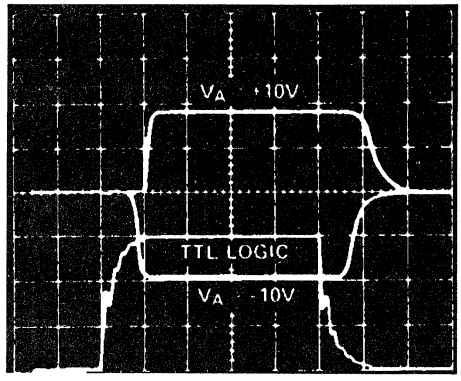


15A. -55°C



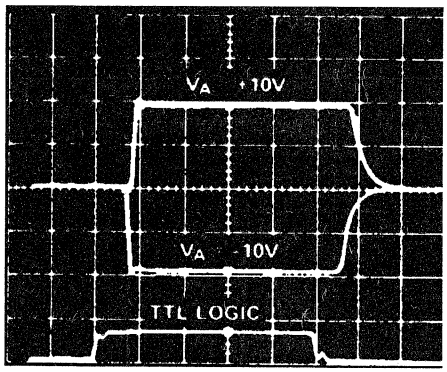
15B. +25°C

Typical Switching Waveforms (Scale: Vertical = 5V/DIV., Horizontal = 100ns/DIV.) (Continued)

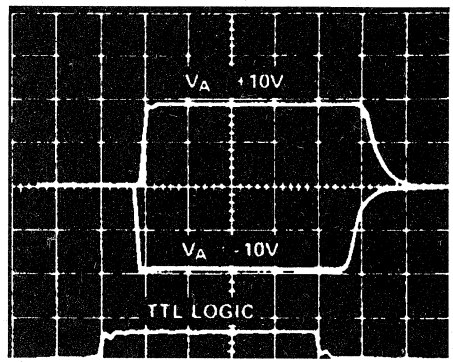


15C. +125°C

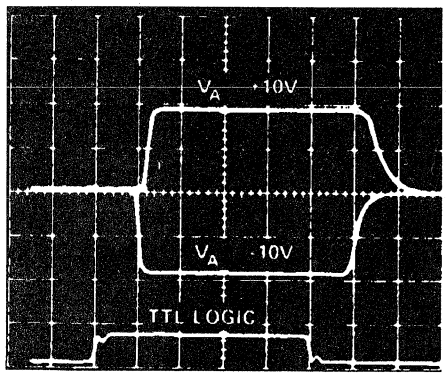
FIGURE 15. TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 12)



16A. -55°C



16B. +25°C



16C. +125°C

FIGURE 16. TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 13)

Typical Switching Waveforms (Scale: Vertical = 5V/DIV., Horizontal = 100ns/DIV.) (Continued)

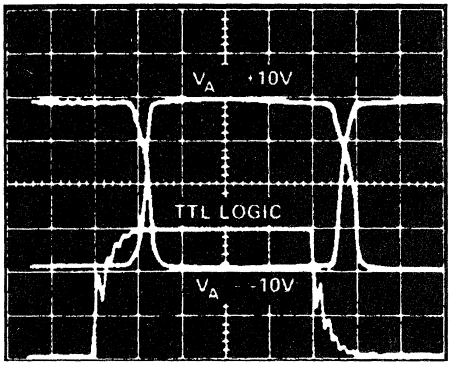


FIGURE 17. +25°C TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 14)

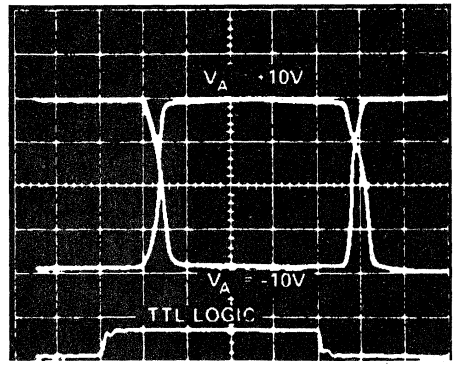


FIGURE 18. +25°C TTL OPEN COLLECTOR LOGIC DRIVE
(Corresponds to Figure 19)

Typical Applications

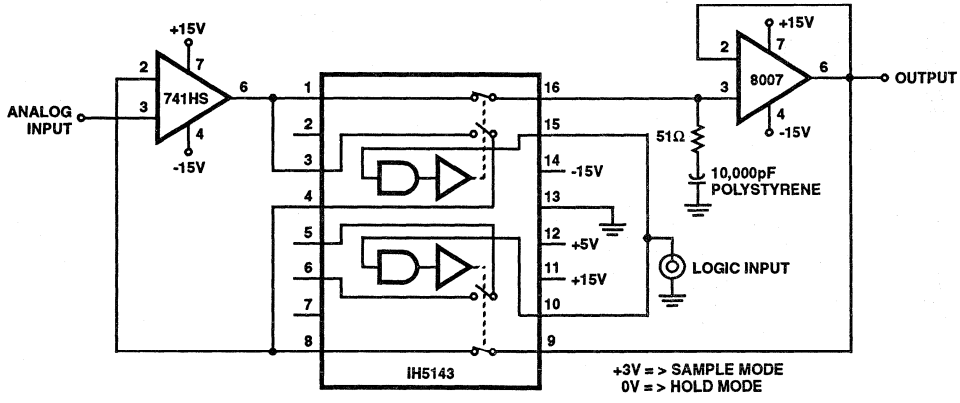


FIGURE 19. IMPROVED SAMPLE AND HOLD USING IH5143

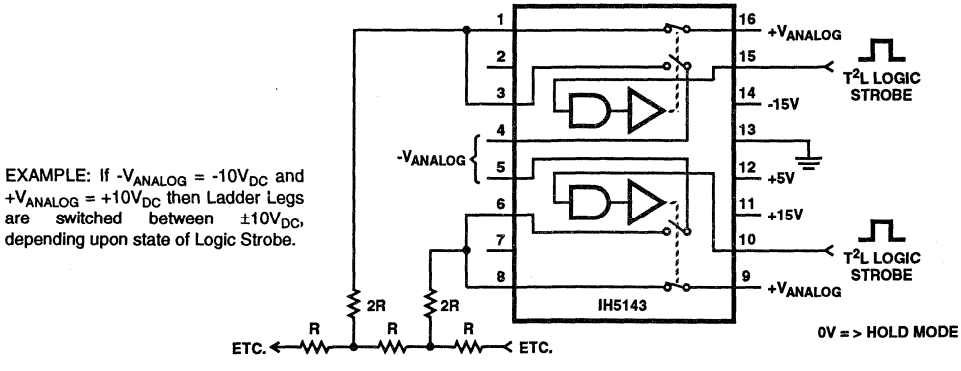
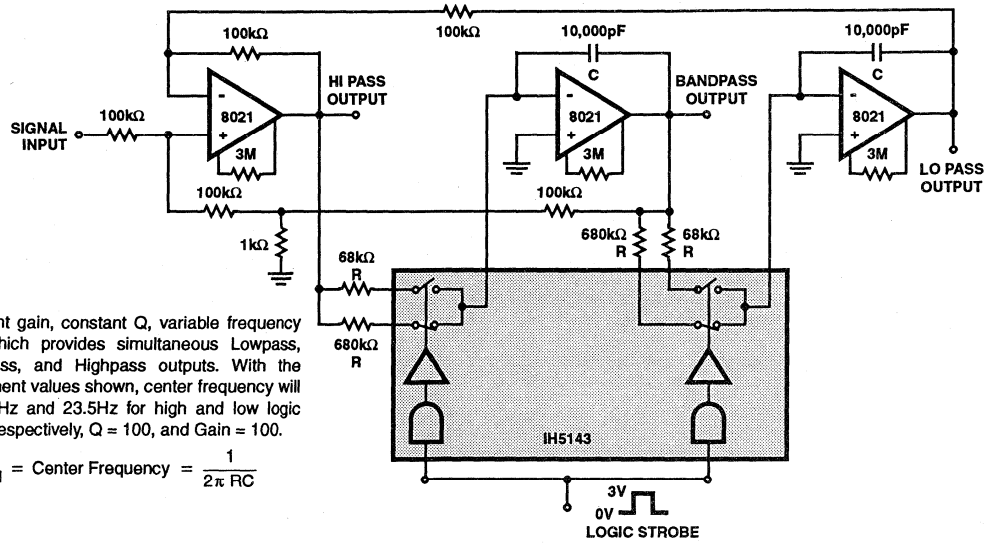


FIGURE 20. USING THE CMOS SWITCH TO DRIVE AN R/2R LADDER NETWORK (2 LEGS)

Typical Applications (Continued)



Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_N = \text{Center Frequency} = \frac{1}{2\pi RC}$$

FIGURE 21. DIGITALLY TUNED LOW POWER ACTIVE FILTER

HARRIS SEMICONDUCTOR

IH5151

December 1993

Dual SPDT CMOS Analog Switch

Features

- Low $R_{DS(ON)}$ of 25Ω
- Switches Greater than $20V_{P-P}$ Signals with ±15V Supplies
- Quiescent Current Less than 100μA
- Break-Before-Make Switching t_{OFF} 120ns Typ., t_{ON} 200ns Typical
- TTL, CMOS Compatible
- Complete Monolithic Construction
- ±5V to ±15V Supply Range

Description

The IH5151 solid state analog switch is designed using an improved, high voltage CMOS technology.

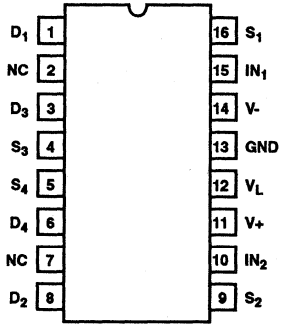
Key performance advantages in the IH5151 are TTL compatibility and ultra low power operation. $R_{DS(ON)}$ switch resistance is typically in the 14Ω to 18Ω area, for signals in the -10V to +10V range. Quiescent current is less than 10μA. The IH5151 also guarantees Break-Before-Make switching which is logically accomplished by extending the t_{ON} time (200ns typ.) such that it exceeds t_{OFF} time (120ns typ.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. The need for external logic required to avoid channel to channel shorting during switching is thus eliminated.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5151CPE	0°C to +70°C	16 Lead Plastic DIP
IH5151CJE	0°C to +70°C	16 Lead Ceramic DIP
IH5151MJE	-55°C to +125°C	16 Lead Ceramic DIP
IH5151MJE/883B	-55°C to +125°C	16 Lead Ceramic DIP

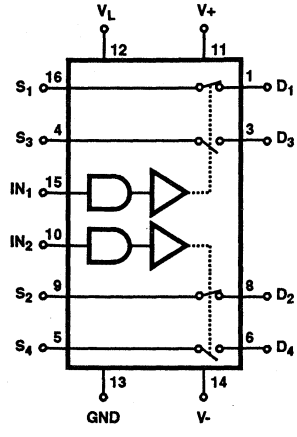
Pinout

IH5151
(CDIP, PDIP)
TOP VIEW



Switching State Diagram

SWITCH STATE SHOWN FOR LOGIC "1" INPUT.



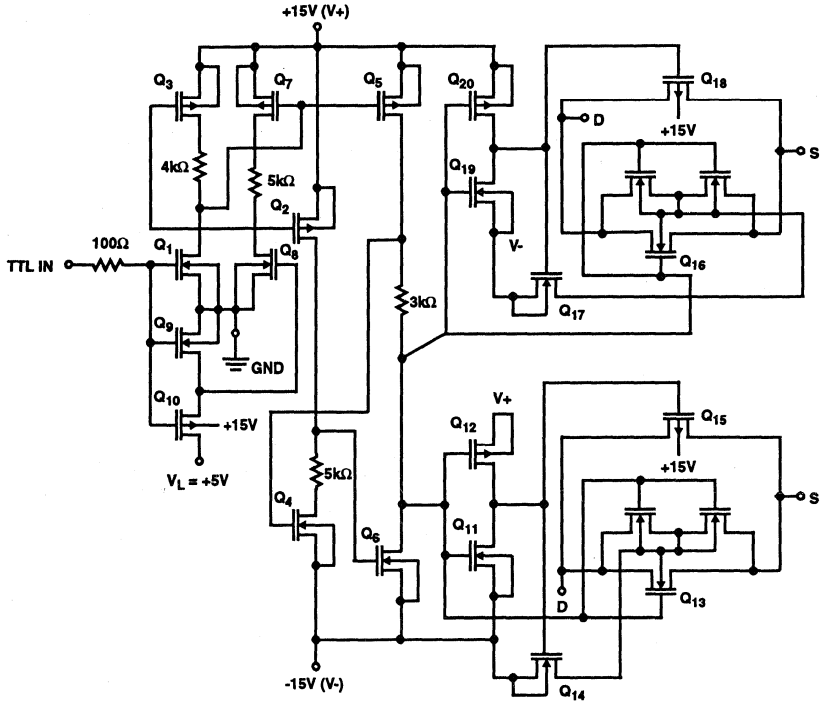
9 SWITCHES

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3133

Functional Block Diagram

ONE SET OF SWITCHES SHOWN



Absolute Maximum Ratings

V+ to V- ..... <36V
V_D to V- ..... <30V
V_D to V_S ..... <±22V
V_L to V- ..... <33V
V_L to V_{IN} ..... <30V
V_L ..... <20V
V_{IN} ..... <20V
Current (Any Terminal) 50mA
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	77°C/W	23°C/W
Plastic DIP Package	100°C/W	-

Operating Temperature
C Suffix ..... 0°C to +70°C
M Suffix ..... -55°C to +125°C
Junction Temperature
Ceramic DIP Package ..... +175°C
Plastic DIP Package ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications T_A = +25°C, V+ = +15V, V- = -15V, V_L = +5V

PER CHANNEL PARAMETERS	TEST CONDITIONS	MILITARY			COMMERCIAL			UNITS
		-55°C	+25°C	+125°C	0°C	+25°C	+70°C	
LOGIC INPUTS								
Input Logic Current, $I_{IN(ON)}$	V_{IN} = 2.4V (Note 1)	±1	±1	±10	–	±1	±10	µA
Input Logic Current, $I_{IN(OFF)}$	V_{IN} = 0.8V (Note 1)	±1	±1	±10	–	±1	±10	µA
SWITCH								
Drain Source On Resistance, $R_{DS(ON)}$	V_D = ±10V, I_S = -10mA	25	25	50	-	30	-	Ω
Channel to Channel $R_{DS(ON)}$ Match, $\Delta R_{DS(ON)}$	(Note 2)	-	10 (Typ)	-	-	15 (Typ)	-	Ω
Minimum Analog Signal Handling Capability, V_{ANALOG}	(Note 2)	-	±14 (Typ)	-	-	±14 (Typ)	-	V
Switch OFF Leakage Current, $I_{D(OFF)}$, $I_{S(OFF)}$	V_{ANALOG} = -10V to +10V	-	±1.0	100	-	±2.0	100	nA
Switch On Leakage Current, $I_{D(ON)}+I_{S(ON)}$	$V_D = V_S$ = -10V to +10V	-	±1.0	100	-	±2.0	100	nA
Charge Injection, $Q_{(INJ)}$	(Figure 5, Note 2)	-	10 (Typ)	-	-	10 (Typ)	-	mV
Minimum Off Isolation Rejection Ratio, OIRR	f = 1MHz, R_L = 100Ω, C_L ≤ 5pF (Figure 3, Note 2)	-	54 (Typ)	-	-	50 (Typ)	-	dB
Switch "On" Time, t_{ON}	R_L = 1kΩ, V_{ANALOG} = -10V (Note 3)	-	-	500	-	-	500	ns
Switch "Off" Time, t_{OFF}	T_O +10V; (Figure 6, Note 3)	-	-	250	-	-	250	ns
POWER SUPPLY CHARACTERISTICS								
+ Power Supply Quiescent Current, I+	V+ = +15V, V- = -15V, V_L = +5V, V_R = 0	10	10	100	-	10	-	µA
- Power Supply Quiescent Current, I-		10	10	100	-	10	-	µA
+5V Supply Quiescent Current, I_L		10	10	100	-	10	-	µA
Ground Supply Quiescent Current, I_{GND}		10	10	100	-	10	-	µA
Minimum Channel to Channel Cross Coupling Rejection Ratio, CCRR	(Figure 2, Note 2)	-	54 (Typ)	-	-	50 (Typ)	-	dB

NOTE:

1. Some channels are turned on by high (1) logic inputs and other channels are turned on by low (0) inputs; however 0.8V to 2.4V describes the minimum range for switching properly. Refer to logic diagrams to find logical value of logic input required to produce ON or OFF state.
2. Typical values are for design aid only, not guaranteed or production tested.
3. For IH5151 devices, channels which are off for logic input ≥ 2.4V (Pins 3 and 4, 5 and 6) have slower t_{ON} time, than channels on Pins 1, 16 and 8, 9. This is done so switch will maintain break-before-make action when connected in DT configuration, i.e. Pin 1 connected in Pin 3.

Typical Performance Curves Per Channel

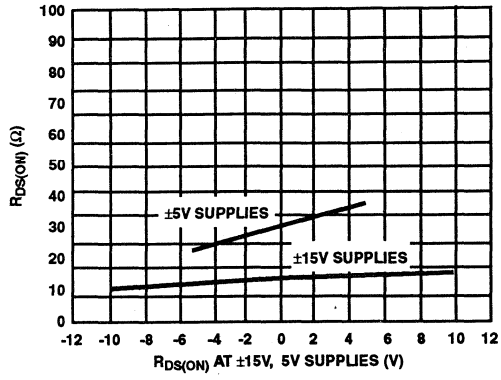


FIGURE 1. $R_{DS(ON)}$ vs ANALOG INPUT VOLTAGE

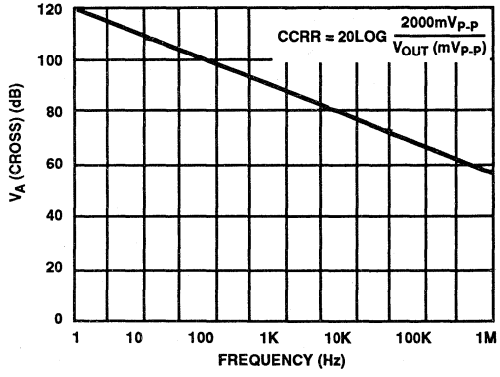


FIGURE 2A.

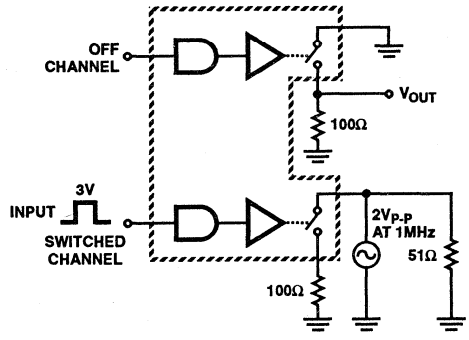


FIGURE 2B.

FIGURE 2. CROSS COUPLING REJECTION vs FREQUENCY

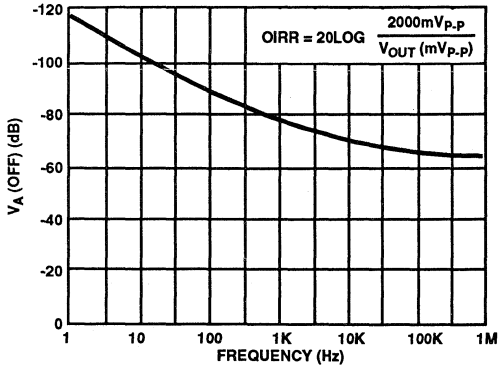


FIGURE 3A.

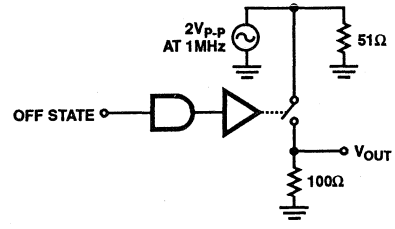


FIGURE 3B.

FIGURE 3. OFF ISOLATION vs FREQUENCY

Typical Performance Curves Per Channel (Continued)

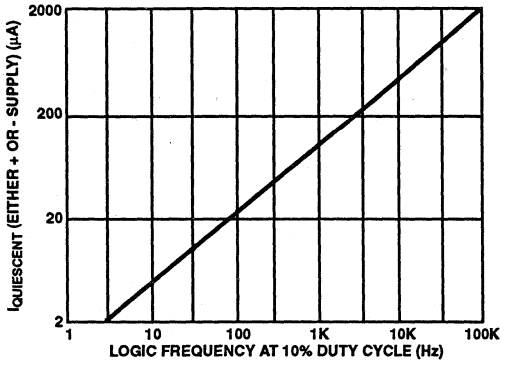


FIGURE 4A.

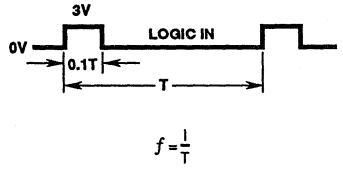


FIGURE 4B.

FIGURE 4. POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

Test Circuits

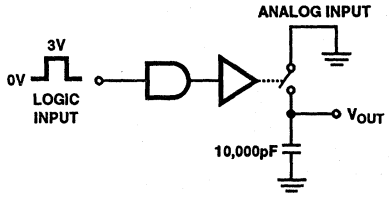


FIGURE 5. CHARGE INJECTION TEST CIRCUIT

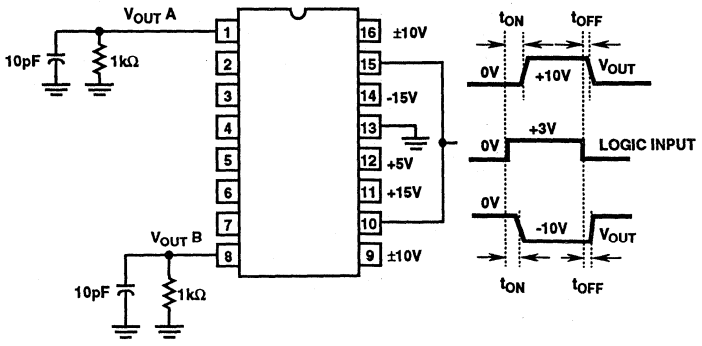


FIGURE 6. SWITCHING TIME TEST CIRCUIT

Typical Applications

Nulling Out Charge Injection

Charge injection (Qinj. on spec. sheet) is caused by gate to drain, or gate to source capacitance of the output switch MOSFETs. The gates of these MOSFETs typically swing from -15V to +15V as a rapidly changing pulse; thus this $30V_{P-P}$ pulse is coupled through gate capacitance to output load capacitance, and the output "step" is a voltage divider from this combination. For example:

$$Qinject\ (V_{PP}) \cong \frac{C_{GATE}}{C_{LOAD}} \times 30V\ step.$$

i.e.

C_{GATE} = 1.5pF, C_{LOAD} = 100pF, then

$$Qinject\ (V_{PP}) = \frac{1.5pF}{100pF} \times 30V\ step = 45mV_{PP}$$

Thus if you are using a switch in a Sample & Hold application with C_{SAMPLE} = 1000pF, a $45mV_{P-P}$ "Sample to Hold error step" will occur.

To null this error step out to zero the circuit in Figure 7 can be used.

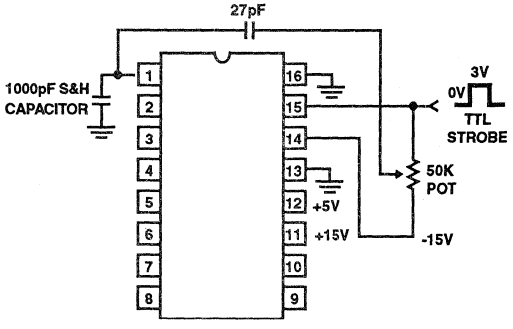


FIGURE 7. ADJUSTABLE CHARGE INJECTION COMPENSATION CIRCUIT

The circuit in Figure 7 nulls out charge injection effects on switch pins 1 and 16; a similar circuit would be required on switch pins 8 and 9.

Simply adjust the pot until V_{OUT} = $0mV_{P-P}$ pulse, with V_{ANALOG} = 0V.

If you do not desire to do any adjusting, but wish the least amount of charge injection possible, then the circuit in Figure 8 should be used.

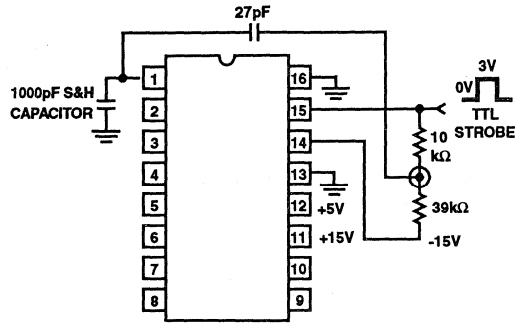


FIGURE 8. NO-ADJUST CHARGE INJECTION COMPENSATION CIRCUIT

This configuration will produce a typical charge injection of V_{OUT} $\pm 10mV_{P-P}$ into the 1000pF S & H capacitor shown.

Fault Condition Protection

If your system has analog voltage levels which are independent of the ±15V (Power Supplies), and these analog levels can be present when supplies are shut off, you should add fault protection diodes as shown in Figure 9.

If the analog input levels are below ±15V, the pn junctions of Q13 & Q15 are reversed biased. However if the ±15V supplies are shut off and analog levels are still present, the configuration becomes as shown in Figure 10.

The need for the diodes in this circumstance is shown in Figure 11. If ANALOG INPUT is greater than 1V, then the pn junction of Q15 is forward biased and excessive current will be drawn. The addition of IN914 diodes prevents the fault currents from destroying the switch. A similar event would occur if ANALOG INPUT was less than or equal to -1V, wherein Q13 would become forward biased. The IN914 diodes form a "back to back" diode arrangement with Q13 and Q15 bodies.

This structure provides a degree of overvoltage protection when supplies are on normally, and analog input level exceeds supplies.

This circuit will switch up to about ±8V ANALOG overvoltages. Beyond this drain(N) to body(P) breakdown VOLTAGE of Q13 limits overvoltage protection.

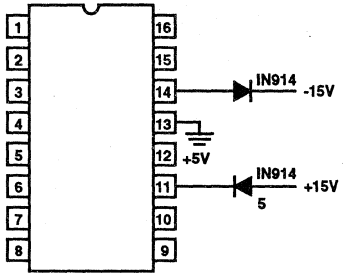


FIGURE 9. ADDING DIODES PROTECTS SWITCH

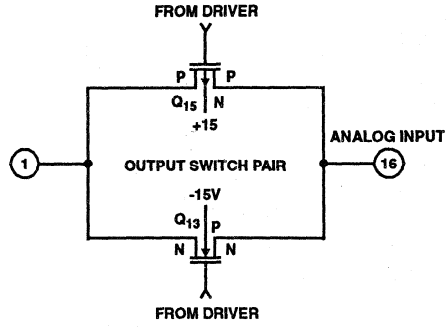


FIGURE 10. SWITCH WITHOUT PROTECTION DIODES

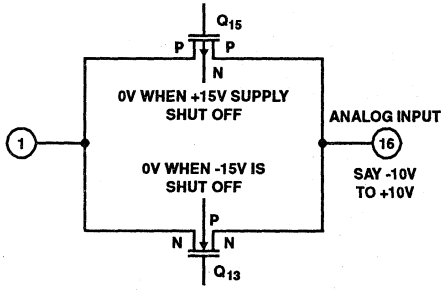


FIGURE 11. FAULT CONDITION WITHOUT PROTECTION DIODES

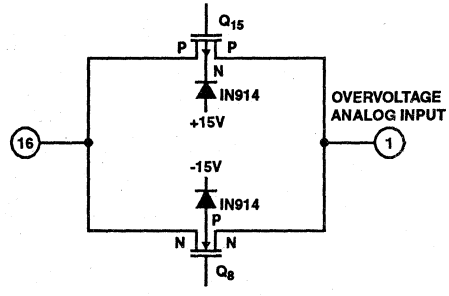


FIGURE 12. FAULT CONDITION WITH PROTECTION DIODES

Die Characteristics

DIE DIMENSIONS:
2515µm x 3074µm

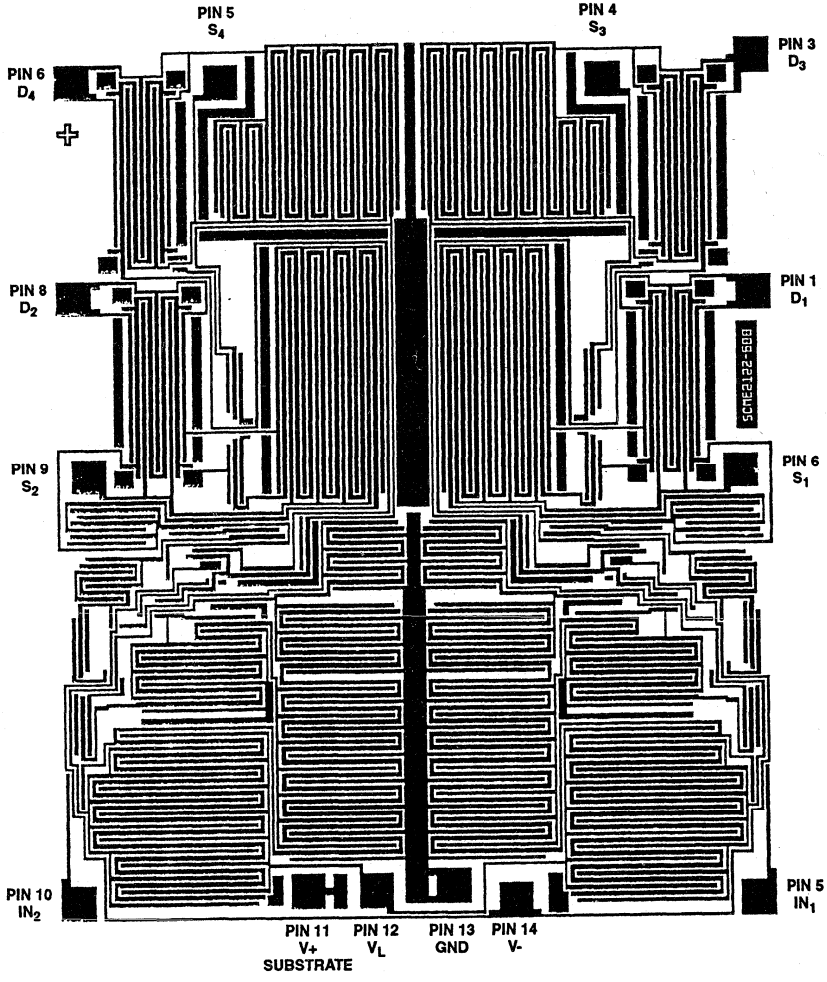
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG Over Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

IH5151



HARRIS SEMICONDUCTOR

IH5341, IH5352

Dual SPST, Quad SPST CMOS RF/Video Switches

December 1993

Features

- $R_{DS(ON)} < 75\Omega$
- Switch Attenuation Varies Less Than 3dB From DC to 100MHz
- "OFF" Isolation > 70dB Typical at 10MHz
- Cross Coupling Isolation > 60dB at 10MHz
- Compatible With TTL, CMOS Logic
- Wide Operating Power Supply Range
- Power Supply Current < 1μA
- "Break-Before-Make" Switching
- Fast Switching (80ns/150ns Typ)

Applications

- Video Switch
- Communications Equipment
- Disk Drives
- Instrumentation
- CATV

Description

The IH5341 (IH5352) is a dual (quad) SPST, CMOS monolithic switch which uses a "Series/Shunt" ("T" switch) configuration to obtain high "OFF" isolation while maintaining good frequency response in the "ON" condition.

Construction of remote and portable video equipment with extended battery life is facilitated by the extremely low current requirements. Switching speeds are typically t_{ON} = 150ns and t_{OFF} = 80ns. "Break-Before-Make" switching is guaranteed.

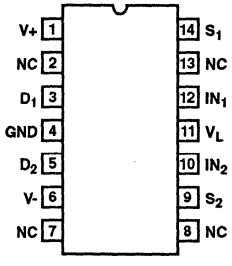
Switch "ON" resistance is typically 40Ω - 50Ω with ±15V power supplies, increasing to typically 175Ω for ±5V supplies.

Ordering Information

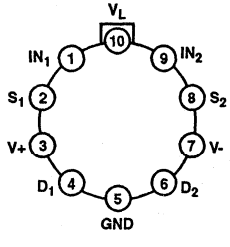
PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH5341CPD	0°C to +70°C	14 Lead Plastic DIP
IH5341ITW	-25°C to +85°C	10 Pin TO-100 Can
IH5341MTW	-55°C to +125°C	10 Pin TO-100 Can
IH5341MTW/883B	-55°C to +125°C	10 Pin TO-100 Can
IH5352CPE	0°C to +70°C	16 Lead Plastic DIP
IH5352IJE	-25°C to +85°C	16 Lead Ceramic DIP
IH5352MJE	-55°C to +125°C	16 Lead Ceramic DIP
IH5352MJE/883B	-55°C to +125°C	16 Lead Ceramic DIP
IH5352CBP	0°C to +70°C	20 Lead SOIC
IH5352IBP	-25°C to +85°C	20 Lead SOIC

Pinouts

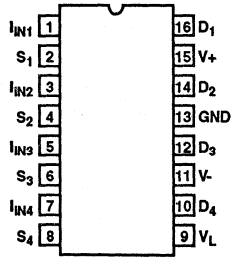
IH5341 (PDIP) TOP VIEW



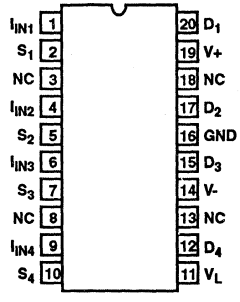
IH5341 (TO-100 CAN) TOP VIEW



IH5352 (CDIP, PDIP) TOP VIEW



IH5352 (SOIC) TOP VIEW

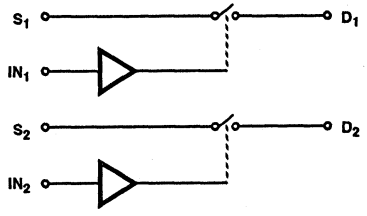


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

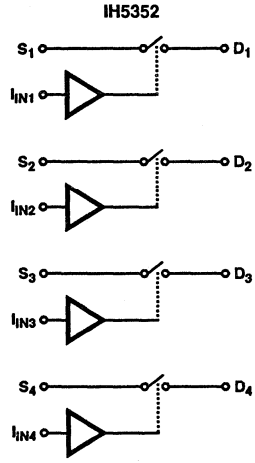
File Number 3134

Functional Block Diagrams

IH5341

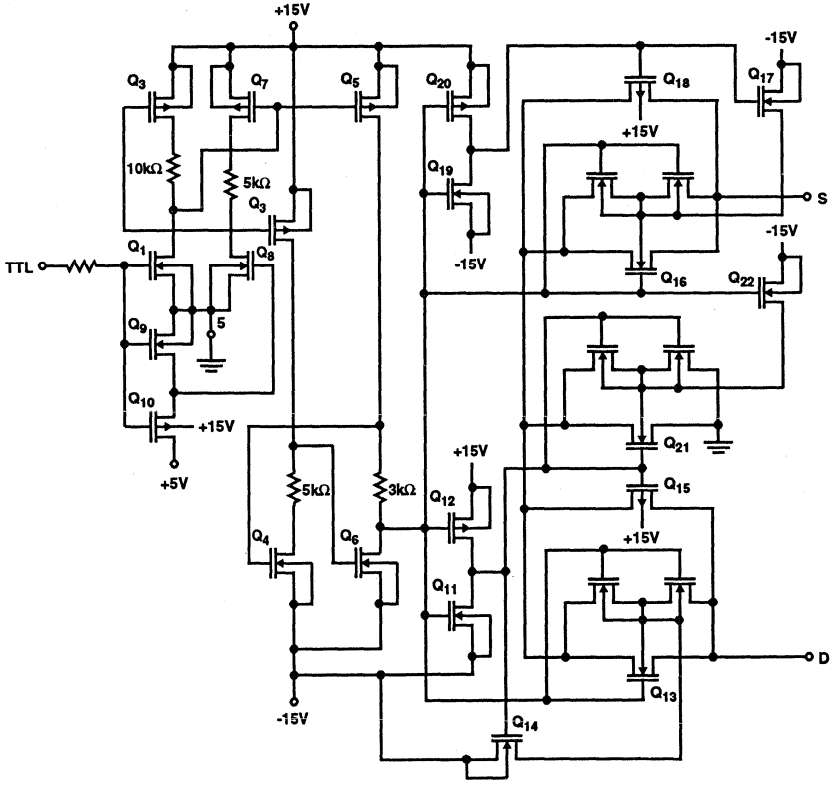


IH5352



Switches are open for a logic "0" control input, and closed for a logic "1" control input.

Schematic Diagram ($^1/_2$ IH5341, $^1/_4$ IH5352)



Absolute Maximum Ratings

V+ to Ground ..... +18V
V- to Ground ..... -18V
V_L to Ground ..... V+ to V-
Logic Control Voltage ..... V+ to V-
Analog Input Voltage ..... V+ to V-
Current (Any Terminal) 50mA
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	70°C/W	19°C/W
TO-100 Can Package	136°C/W	65°C/W
SOIC Package	120°C/W	-
Plastic DIP Package	100°C/W	-

Operating Temperature
(M Version) ..... -55°C to +125°C
(I Version) ..... -25°C to +85°C
(C Version) ..... 0°C to +70°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

$V+ = +15V$, $V_L = +5V$, $V- = -15V$, $T_A = +25°C$ Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS		(NOTE 1) TYP	M GRADE DEVICE -55°C	M GRADE DEVICE +25°C	M GRADE DEVICE +125°C	I/C GRADE DEVICE -25°C/ 0°C	I/C GRADE DEVICE +25°C	I/C GRADE DEVICE +85°C/ +70°C	UNITS
DC CHARACTERISTICS										
Supply Voltage Ranges (Note 3)										
Positive Supply, V+			5 to 15	-	-	-	-	-	-	V
Logic Supply, V_L			5 to 15	-	-	-	-	-	-	V
Negative Supply, V-			-5 to -15	-	-	-	-	-	-	V
Switch "ON" Resistance, $R_{DS(ON)}$	$V_D = \pm5V$, $I_S = 10mA$, $V_{IN} \geq 2.4V$ (Note 4)		50	75	75	100	75	75	100	Ω
	$V_D = \pm10V$, $I_S = 10mA$, $V_{IN} \geq 2.4V$ (Note 4)		100	125	125	cd175	150	150	175	Ω
Switch "ON" Resistance, $R_{DS(ON)}$	$V+ = V_L = +5V$, $V_{IN} = 3V$, $V- = -5V$, $V_D = \pm3V$, $I_S = 10mA$		175	250	250	350	300	300	350	Ω
On Resistance Match Between Channels, $\Delta R_{DS(ON)}$	$I_S = 10mA$, $V_D = \pm5V$		5	-	-	-	-	-	-	Ω
Logic "1" Input Voltage, V_{IH}			>2.4	-	-	-	-	-	-	V
Logic "0" Input Voltage, V_{IL}			<0.8	-	-	-	-	-	-	V
Switch "OFF" Leakage, $I_{D(OFF)}$ or $I_{S(OFF)}$	$V_{S/D} = \pm5V$ or $\pm14V$, $V_{IN} \leq 0.8V$ (Notes 2 and 4)	IH5341	-	-	±0.5	50	-	±1	100	nA
		IH5352	-	-	±1	50	-	±2	100	nA
Switch "ON" Leakage, $I_{D(ON)} + I_{S(ON)}$	$V_{S/D} = \pm5V$, $V_{IN} \geq 2.4V$	IH5341	-	-	±1	50	-	±2	100	nA
	$V_{S/D} = \pm14V$, $V_{IN} \geq 2.4V$		-	-	±1	100	-	±2	100	nA
	$V_{S/D} = \pm5V$ or $\pm14V$, $V_{IN} \leq 0.8V$	IH5352	-	-	±1	100	-	±2	100	nA
Input Logic Current, I_{IN}	$V_{IN} > 2.4V$ or $< 0V$		0.1	±1	±1	10	±1	±1	10	mA
Positive Supply Quiescent Current, I+	$V_{IN} = 0V$ or $+5V$		0.1	1	1	10	1	1	10	mA
Negative Supply Quiescent Current, I-	$V_{IN} = 0V$ or $+5V$		0.1	1	1	10	1	1	10	µA
Logic Supply Quiescent Current, I_L	$V_{IN} = 0V$ or $+5V$		0.1	1	1	10	1	1	10	µA

Electrical Specifications V+ = +15V, V_L = +5V, V- = -15V, T_A = +25°C Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 1) TYP	M GRADE DEVICE -55°C	M GRADE DEVICE +25°C	M GRADE DEVICE +125°C	I/C GRADE DEVICE -25°C/ 0°C	I/C GRADE DEVICE +25°C	I/C GRADE DEVICE +85°C/ +70°C	UNITS
AC CHARACTERISTICS									
Switch "ON" Time, t_{ON}		-	-	150	300	-	-	-	ns
Switch "OFF" Time, t_{OFF}		-	-	80	150	-	-	-	ns
"OFF" Isolation Rejection Ratio, OIRR		-	-	70	-	-	-	-	dB
Cross Coupling Rejection Ratio, CCRR		-	-	60	-	-	-	-	dB
Switch Attenuation 3dB Frequency, f_{3dB}		-	-	100	-	-	-	-	MHz

NOTES:

1. Typical values are not tested in production. They are given as a design aid only.
2. Positive and negative voltages applied to opposite sides of switch, in both directions successively.
3. These are the operating voltages at which the other parameters are tested, and are not directly tested.
4. The logic inputs are either greater than or equal to 2.4V or less than or equal to 0.8V, as required, for this test.

Typical Performance Curves

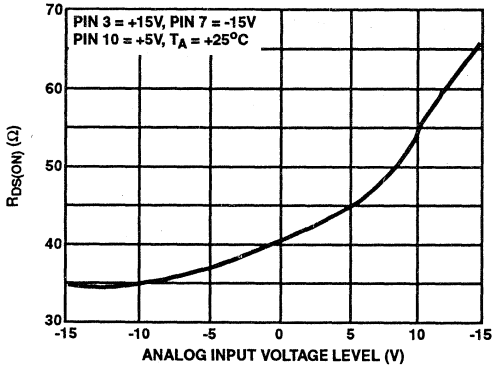


FIGURE 1. $R_{DS(ON)}$ vs ANALOG INPUT VOLTAGE WITH ±15V POWER SUPPLIES

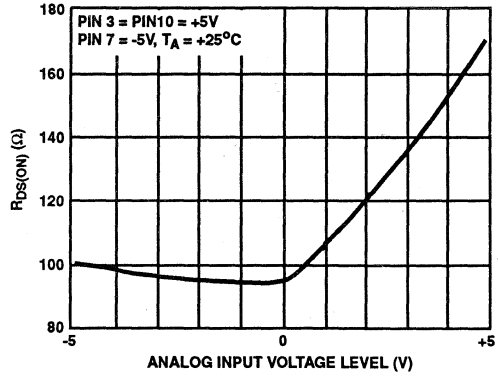


FIGURE 2. $R_{DS(ON)}$ vs ANALOG INPUT LEVEL WITH ±5V POWER SUPPLIES

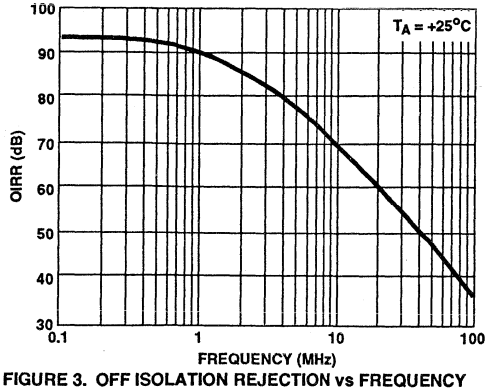


FIGURE 3. OFF ISOLATION REJECTION vs FREQUENCY (SEE FIGURE 8)

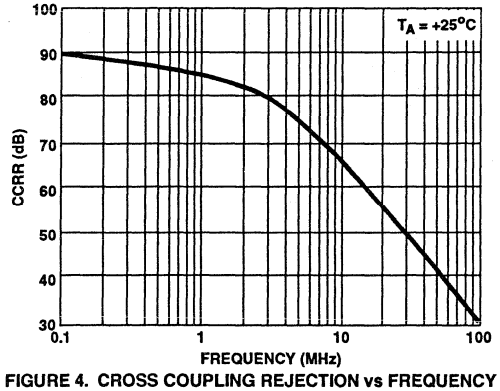


FIGURE 4. CROSS COUPLING REJECTION vs FREQUENCY (SEE FIGURE 9)

Typical Performance Curves (Continued)

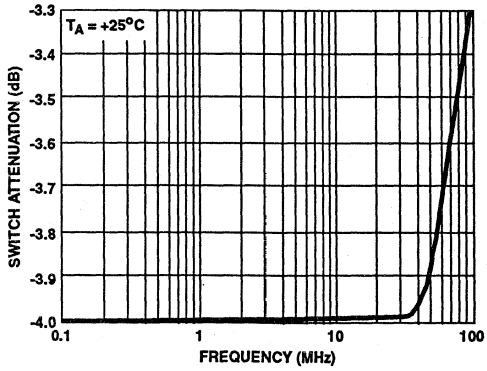
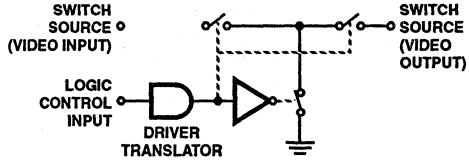


FIGURE 5. TYPICAL SWITCH ATTENUATION vs FREQUENCY (R_L = 75Ω, SEE FIGURE 10)

Detailed Description

Figure 6 shows the internal circuit of one channel of the IH5352. This is identical to the IH5341 "T-Switch" configuration. Here, a shunt switch is closed, and the two series switches are open when the video switch channel is open or off. This provides much better isolation between the input and output terminals than a simple series switch does, especially at high frequencies. The result is excellent off-isolation in the Video and RF frequency ranges when compared to conventional analog switches.

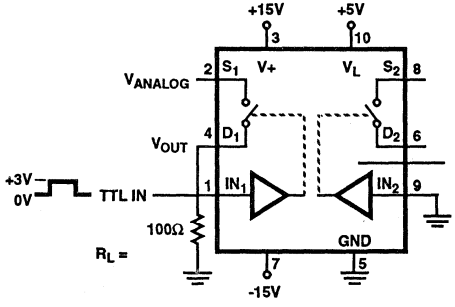
The control input level shifting circuitry is very similar to that of the IH5140 series of Analog Switches, and gives very high speed, guaranteed "Break-Before-Make" action, low static power consumption and TTL compatibility.



NOTE: 1 channel of 4 shown.

FIGURE 6. INTERNAL SWITCH CONFIGURATION

Test Circuits



NOTE: Only one channel shown. Other acts identically.

FIGURE 7A. SWITCHING TIME TEST CIRCUIT

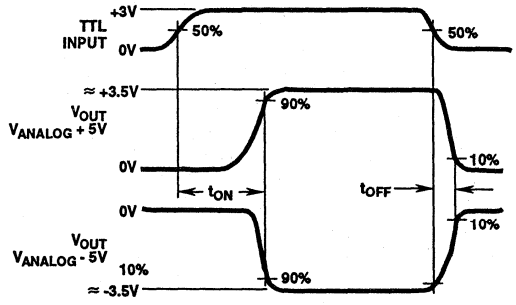
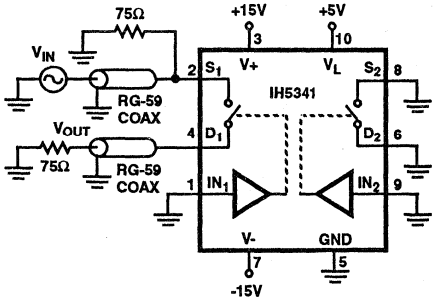


FIGURE 7B. SWITCHING TIME WAVEFORMS

FIGURE 7.

Test Circuits (Continued)

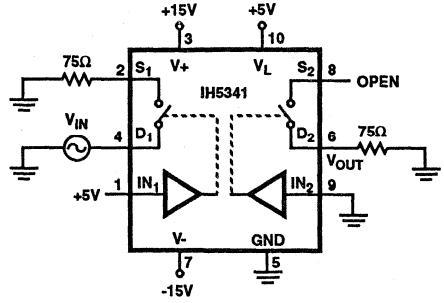


V_{IN} = ±5V (10V_{P-P}) at f = 10MHz

$$OIRR = 20\log\frac{V_{IN}}{V_{OUT}}$$

NOTE: Only one channel shown. Other acts identically.

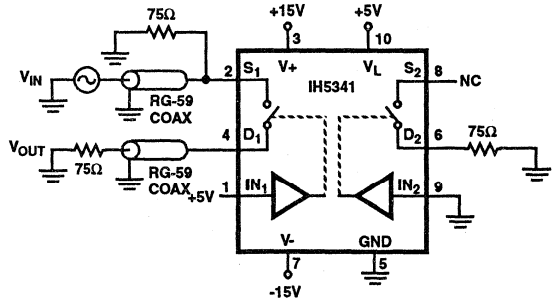
FIGURE 8. OFF ISOLATION TEST CIRCUIT



V_{IN} = 225mV_{RMS} at f = 10MHz

$$CCRR = 20\log\frac{V_{IN}}{V_{OUT}}$$

FIGURE 9. OFF ISOLATION TEST CIRCUIT



$$ATTN: = 20\log\frac{R_L}{R_{DS(ON)} + R_L}$$

Nominally, at DC, this ratio is equal to -4dB. When the attenuation reaches -1dB, the frequency at which this occurs is f_{3dB}

NOTE: Only one channel shown. Other acts identically.

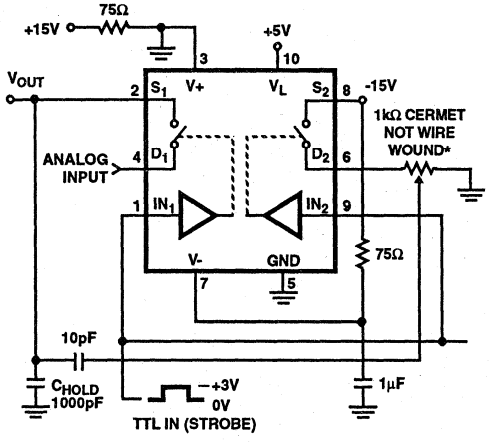
FIGURE 10. SWITCH ATTENUATION vs FREQUENCY

Typical Applications

Charge Compensation Techniques

Charge injection results from the signals out of the level translation circuit being coupled through the gate-channel and gate-source/drain capacitances to the switch inputs and outputs. This feedthrough is particularly troublesome in Sample-and-Hold or Track-and-Hold applications, as it causes a Sample (Track) to Hold offset. The IH5341 devices have a typical injected charge of 30pC-50pC (corresponding to 30mV-50mV in a 1000pF capacitor), at $V_{S/D}$ of about 0V.

This Sample (Track) to Hold offset can be compensated by bringing in a signal equal in magnitude but of the opposite polarity. The circuit of Figure 11 accomplishes this charge injection compensation by using one side of the device as a S & H (T & H) switch, and the other side as a generator of a compensating signal. The 1kΩ potentiometer allows the user to adjust the net injected charge to exactly zero for any analog voltage in the -5V to +5V range.



* Adjust pot for 0mV$_{P-P}$ steip at V_{OUT} with no analog (AC) signal present.

FIGURE 11. CHARGE INJECTION COMPENSATION

Since individual parts are very consistent in their charge injection, it is possible to replace the potentiometer with a pair of fixed resistors, and achieve less than 5mV error for all devices without adjustment.

An alternative arrangement, using a standard TTL inverter to generate the required inversion, is shown in Figure 12. The capacitor needs to be increased, and becomes the only method of adjustment. A fixed value of 22pF is good for analog values referred to ground, while 35pF is optimum for AC coupled signals referred to -5V as shown in the figure. The choice of -5V is based on the virtual disappearance at this analog level of the transient component of switching charge injection. This combination will lead to a virtually "glitch-free" switch.

Overvoltage Protection

If sustained operation with no supplies but with analog signals applied is possible, it is recommended that diodes (such as 1N914) be inserted in series with the supply lines to the IH5341. Such conditions can occur if these signals come from a separate power supply or another location, for example. The diodes will be reverse biased under this type of operation, preventing heavy currents from flowing from the analog source through the IH5341.

The same method of protection will provide over 25V o vervoltage protection on the analog inputs when the supplies are present. The schematic for this connection is shown in Figure 13.

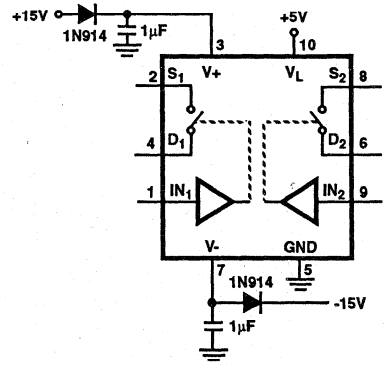


FIGURE 13. OVERVOLTAGE PROTECTION

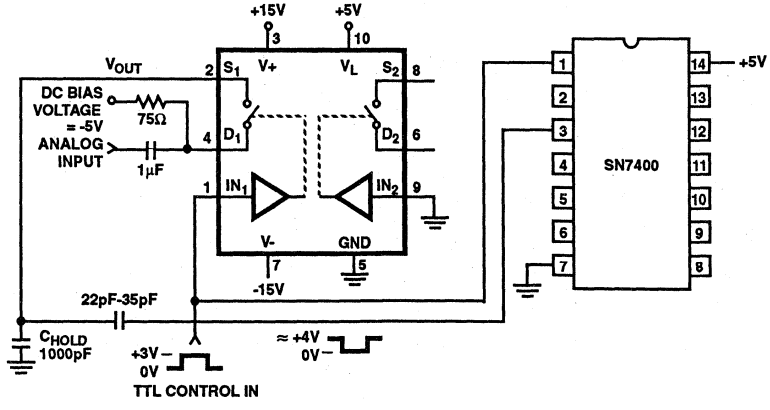


FIGURE 12. ALTERNATIVE COMPENSATION CIRCUIT

Die Characteristics

DIE DIMENSIONS:
2388µm x 2515µm

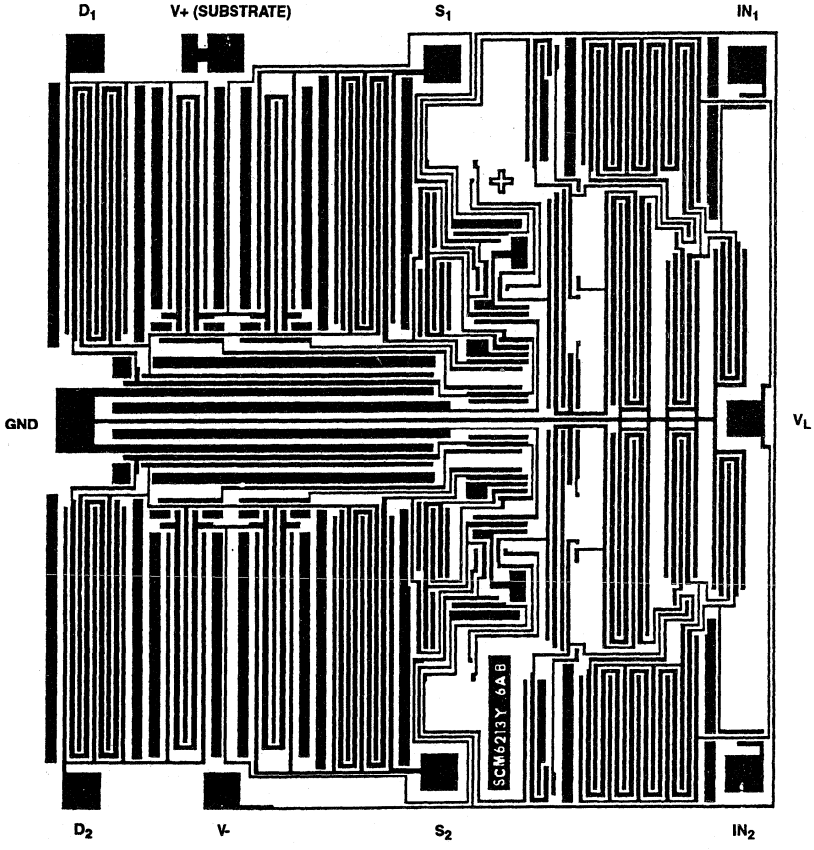
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

IH5341



Die Characteristics

DIE DIMENSIONS:
2617µm x 5233µm

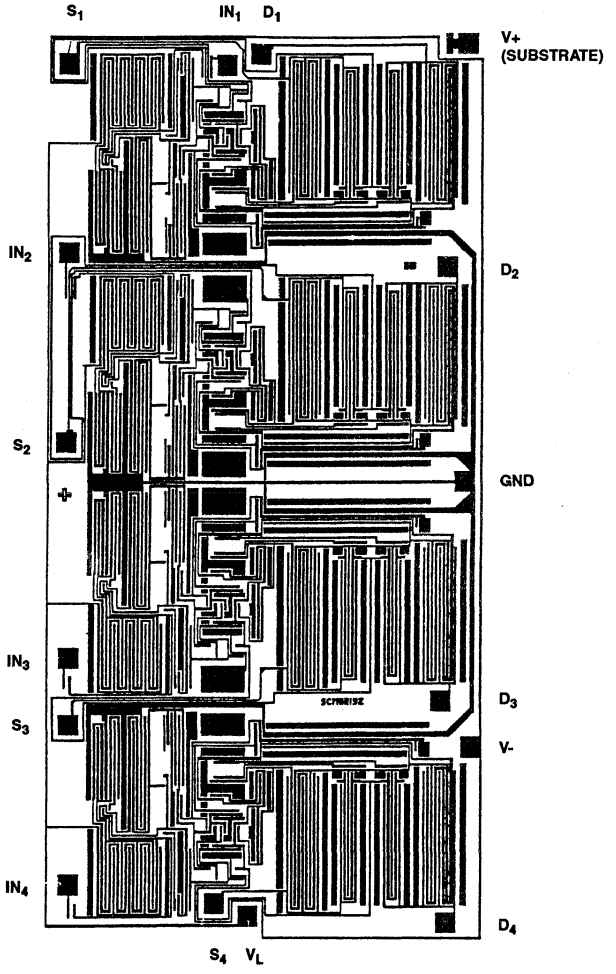
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1 x 10^4 A/cm^2

Metallization Mask Layout

IH5352



DATA ACQUISITION 10

MULTIPLEXERS

NOTE: Bold Type Designates a New Product from Harris.

TABLE 1. SINGLE 1 x 8 (FIGURES 1, 2)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	FEATURES
DG408	DJ, DY	DG408AK/883	40	2.4	0.8	44V CMOS-JI		115	105	Low $R_{DS(ON)}$
DG458	DJ, DY	DG458AK/883	1200	2.4	0.8	44V CMOS-JI	0.03	200	250	Fault Protected
DG508A	AK, BK, BY, CJ, CK, CY	DG508AAK/883B	450	2.4	0.8	44V CMOS-DI	0.3	250	250	
DG528	AK, BK, BY, CJ, CK, CY	DG528AK/883B	450	2.4	0.8	44V CMOS-JI	0.015	1,000	400	Microprocessor Compatible
HI1-0508	-2, -4, -5, -7, -8, -9	HI1-0508/883	400	2.4	0.8	44V CMOS-DI	0.3	250	250	
HI3-0508	-5									
HI4P0508	-5									
HI9P0508	-5, -9									
		HI4-0508/883								
HI1-0508A	-2, -5, -7, -8		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Overvoltage Protection. See Table 8 (Note 5)
HI3-0508A	-5									
HI1-0518	-2, -5, -8, -9		750	2.4	0.8	33V CMOS-DI	0.015	120	140	Programmable 1 of 8, Differential 2 of 4, Figure 2, See Table 8, (Note 5)
HI3-0518	-5, -9									
HI4-0518	-8									
HI4P0518	-5, -9									
HI9P0518	-5, -9									
HI1-0548	-2, -4, -5	HI1-0548/883	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Overvoltage Protection. 7% $R_{DS(ON)}$ Matching. See Table 8 (Note 5)
HI3-0548	-5, -9									
HI4P0548	-5									
HI9P0548	-5, -9									
		HI4-0548/883								
HI1-1818A	-2, -5, -7	HI1-1818A/883	400	4.0	0.4	40V CMOS-DI	0.1	300	300	
HI3-1818A	-5									
HI4P1818A	-5									

TABLE 2. SINGLE 1 x 16 (FIGURE 3)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	FEATURES
DG406	DJ, DY	DG406AK/883	50	2.4	0.8	44V CMOS-JI	0.01	150	70	Low $R_{DS(ON)}$, Low Leakage
DG506A	AK, BK, BY, CJ, CK, CY	DG506AAK/883B	450	2.4	0.8	44V CMOS-DI	0.3	250	250	
DG526	AK, BK, BY, CJ, CK, CY	DG526AK/883B	400	2.4	0.8	44V CMOS-JI	0.2	700	400	Microprocessor Compatible
HI1-0506	-2, -4, -5, -7, -8, -9	HI1-0506/883	400	2.4	0.8	44V CMOS-DI	0.3	250	250	
HI3-0506	-5									
HI4P0506	-5									
HI9P0506	-5, -9									
		HI4-0506/883								
HI1-0506A	-2, -5, -7, -8		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Overvoltage Protection. See Table 8 (Note 5)
HI3-0506A	-5									
HI1-0516	-2, -5, -8	HI1-0516/883	750	2.4	0.8	33V CMOS-DI	0.03	120	140	Programmable, 1 of 16, Differential 2 of 8. See Table 8 (Note 5)
HI3-0516	-5									
HI4-0516	-8	HI4-0516/883								
HI4P0516	-5									
HI9P0516	-5, -9									
HI1-0546	-2, -4, -5, -7	HI1-0546/883	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Overvoltage Protection. See Table 8 (Note 5) 7% $R_{DS(ON)}$ Matching
HI3-0546	-5, -9									
HI4P0546	-5									
HI9P0546	-5, -9									
		HI4-0546/883								

TABLE 3. DUAL 1 x 4 (FIGURE 4)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	FEATURES
DG409	DJ, DY	DG409AK/883	40	2.4	0.8	44V CMOS-JI		115	105	Low $R_{DS(ON)}$
DG459	DJ, DY	DG459AK/883	1200	2.4	0.8	44V CMOS-JI	0.03	200	250	Fault Protected
DG509A	AK, BK, BY, CJ, CK, CY	DG509AAK/883B	400	2.4	0.8	44V CMOS-JI	0.3	250	250	
DG529	AK, BK, BY, CK, CY	DG529K/883B	450	2.4	0.8	44V CMOS-JI	0.008	1000	400	Microprocessor Compatible
HI1-0509	-2, -4, -5, -7, -8, -9	HI1-0509/883	400	2.4	0.8	44V CMOS-DI	0.3	250	250	
HI3-0509	-5									
HI4P0509	-5									
HI9P0509	-5, -9									
		HI4-0509/883								
HI1-0509A	-2, -5, -7, -8		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Overvoltage Protection, See Table 8 (Note 5)
HI3-0509A	-5									
HI1-0518	-2, -5, -8, -9		750	2.4	0.8	33V CMOS-DI	0.015	120	140	Programmable 1 of 8, Differential 2 of 4, (Figure 2), See Table 7
HI3-0518	-5, -9									
HI4-0518	-8									
HI4P0518	-5, -9									
HI9P0518	-5, -9									
HI1-0539	-2, -4, -5, -8		850	4.0	0.8	33V CMOS-DI	0.001	250	160	Low Level Signals, 3% Max $R_{DS(ON)}$ Matching
HI3-0539	-5									
HI4P0539	-5									

TABLE 3. DUAL 1 x 4 (FIGURE 4) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	FEATURES
HI1-0549	-2, -4, -5	HI1-0549/883	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	70V Active Overvoltage Protection, 7% $R_{DS(ON)}$ Matching, See Table 8 (Note 5)
HI3-0549	-5, -9									
HI4P0549	-5									
HI9P0549	-5, -9									
		HI4-0549/883								
HI1-1828A	-2, -5, -7	HI1-1828/883	400	4.0	0.4	40V CMOS-DI	125 Max	300	300	
HI3-1828A	-5									
HI4P1828A	-5, -8									
		HI4-1828A/883								

TABLE 4. DUAL 1 x 8 (FIGURE 5)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	FEATURES
DG407	DJ, DY	DG407AK/883	50	2.4	0.8	44V CMOS-JI	0.01	150	70	Low $R_{DS(ON)}$, Low Leakage
DG507A	AK, BK, BY, CJ, CK, CY	DG507AAK/883B	450	2.4	0.8	44V CMOS-JI	0.03	250	250	
DG527	AK, BK, BY, CJ, CK, CY	DG527AK/883B	400	2.4	0.8	44V CMOS-JI	0.2	700	400	Microprocessor Compatible
HI1-0507	-2, -4, -5, -7, -8, -9	HI1-0507/883	400	2.4	0.8	44V CMOS-DI	0.3	250	250	
HI3-0507	-5									
HI4P0507	-5									
HI9P0507	-5, -9									
		HI4-0507/883								
HI1-0507A	-2, -5, -7, -8		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Overvoltage Protection, See Table 8 (Note 5)
HI3-0507A	-5									

TABLE 4. DUAL 1 x 8 (FIGURE 5) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	FEATURES
HI1-0516	-2, -5, -8	HI1-0516/883	750	2.4	0.8	33V CMOS-DI	0.03	120	140	Programmable, 1 of 16, Differential 2 of 8, See Table 8
HI3-0516	-5									
HI4-0516	-8	HI4-0516/883								
HI4P0516	-5									
HI9P0516	-5, -9									
HI1-0547	-2, -4, -5, -9	HI1-0547/883	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	Active Overvoltage Protection, 7% $R_{DS(ON)}$ Matching, See Table 8 (Note 5)
HI3-0547	-5, -9									
HI4P0547	-5									
HI9P0547	-5, -9									
		HI4-0547/883								

TABLE 5. LATCHABLE MULTIPLEXERS, µPROCESSOR COMPATIBLE, SELECT LATCHES

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	FEATURES
DG526	AK, BK, CJ, CK	DG526AK/883B	400	2.4	0.8	44V CMOS-JI	0.2	700	400	1 of 16 Channels, Microprocessor Compatible
DG527	AK, BK, CJ, CK	DG527AK/883B	400	2.4	0.8	44V CMOS-JI	0.2	700	400	Differential 1 if 8 Channel, Microprocessor Compatible
DG528	AK, BK, CJ, CK	DG528AK/883B	450	2.4	0.8	44V CMOS-JI	0.015	1,000	400	1 of 8 Channels, Microprocessor Compatible
DG529	AK, BK, CJ, CK	DG529AK/883B	450	2.4	0.8	44V CMOS-JI	0.008	1,000	400	Dual 1 of 4 Channel, Microprocessor Compatible

TABLE 6. PROGRAMMABLE CONFIGURATION SINGLE 1 OF 16 OR DIFFERENTIAL 2 OF 8 (FIGURE 6)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	FEATURES
HI1-0516	-2, -5, -8	HI1-0516/883	750	2.4	0.8	33V CMOS-DI	0.03	120	140	Programmable, 1 of 16, Differential 2 of 8
HI3-0516	-5									
HI4-0516	-8	HI4-0516/883								
HI4P0516	-5									
HI9P0516	-5, -9									

TABLE 7. PROGRAMMABLE CONFIGURATION SINGLE 1 OF 8 OR DIFFERENTIAL 2 OF 4 (FIGURE 7)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	FEATURES
HI1-0518	-2, -5, -8, -9		750	2.4	0.8	33V CMOS-DI	0.015	120	140	Programmable, 1 of 8, Differential 2 of 4
HI3-0518	-5, -9									
HI4-0518	-8									
HI4P0518	-5, -9									

TABLE 8. 70V PEAK-TO-PEAK OVERVOLTAGE PROTECTED MULTIPLEXERS (NOTE 6)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	NO. OF CHANNELS	FEATURES
HI1-0506A	-2, -5, -7		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	1 x 16	
HI3-0506A	-5										
HI4-0506A	-8										
HI1-0507A	-2, -5, -7		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 8	Differential Inputs
HI3-0507A	-5										
HI4-0507A	-8										

TABLE 8. 70V PEAK-TO-PEAK OVERVOLTAGE PROTECTED MULTIPLEXERS (NOTE 6) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP ($\pm$nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	NO. OF CHANNELS	FEATURES
HI1-0508A	-2, -5, -7		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	1 x 8	
HI3-0508A	-5										
HI4-0508A	-8										
HI1-0509A	-2, -5, -7		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 4	Differential Inputs
HI3-0509A	-5										
HI4-0509A	-8										
HI1-0546	-2, -4, -5	HI1-0546/883	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	1 x 16	7% $R_{DS(ON)}$ Matching
HI3-0546	-5										
HI4P0546	-5										
HI9P0546	-5, -9										
		HI4-0546/883									
HI1-0547		HI1-0547/883	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 8	7% $R_{DS(ON)}$ Matching Differential Inputs
HI3-0547	-2, -4, -5										
HI4P0547	-5										
HI9P0547	-5, -9										
		HI4-0547/883									
HI1-0548	-2, -4, -5	HI1-0548/883	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	1 x 8	7% $R_{DS(ON)}$ Matching
HI3-0548	-5										
HI4P0548	-5										
HI9P0548	-5, -9										
		HI4-0548/883									

TABLE 8. 70V PEAK-TO-PEAK OVERVOLTAGE PROTECTED MULTIPLEXERS (NOTE 6) (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	NO. OF CHANNELS	FEATURES
HI1-0549	-2, -4, -5	HI1-0549/883	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 4	7% $R_{DS(ON)}$ Matching Differential Inputs
HI3-0549	-5										
HI4P0549	-5										
HI9P0549	-5, -9										
		HI4-0549/883									

TABLE 9. DIFFERENTIAL INPUT MULTIPLEXERS

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	NO. OF CHANNELS	FEATURES
DG507A	AK, BK, BY, CJ, CK, CY	DG507AAK/883B	450	2.4	0.8	44V CMOS-JI	0.03	250	250	8	
DG509A	AK, BK, CJ, CK	DG509AAK/883B	400	2.4	0.8	44V CMOS-JI	0.3	250	250	4	
HI1-0507	-2, -4, -5, -7, -8, -9	HI1-0507/883	400	2.4	0.8	44V CMOS-DI	0.1	250	250	2 x 8	
HI3-0507	-5										
HI4P0507	-5										
HI9P0507	-5, -9										
		HI4-0507/883									
HI1-0507A	-2, -5, -7, -8		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 8	Active Overvoltage Protection See Table 8 (Note 5)
HI3-0507A	-5										
HI4-0507A	-8										
HI1-0509	-2, -4, -5, -7, -8, -9	HI1-0509/883	450	2.4	0.8	44V CMOS-DI	0.3	250	250	2 x 4	
HI3-0509	-5										
HI4P0509	-5										
HI9P0509	-5, -9										
		HI4-0509/883									

TABLE 9. DIFFERENTIAL INPUT MULTIPLEXERS (Continued)

(NOTES 2, 3) DEVICE	SUFFIX CODES	MIL SPEC	(NOTE 1) $R_{DS(ON)}$ (Ω MAX)	V_{INH} MIN (V)	V_{INL} MAX (V)	TECHNOLOGY	I_{DOFF} TYP (±nA)	T_{ON} TYP (ns)	T_{OFF} TYP (ns)	NO. OF CHANNELS	FEATURES
HI1-0509A	-2, -5, -7, -8		1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 4	Active Overvoltage Protection See Table 8 (Note 5)
HI3-0509A	-5										
HI4-0509A	-8										
HI1-0516	-2, -5, -8	HI1-0516/883	1800	4.0	0.8	33V CMOS-DI	0.1	500	500	1 x 16	7% $R_{DS(ON)}$ Matching
HI3-0516	-5										
HI4-0516	-8	HI4-0516/883									
HI4P0516	-5										
HI9P0516	-5, -9										
HI1-0518	-2, -5, -8, -9		750	2.4	0.8	33V CMOS-DI	0.015	120	140	4	Programmable 1 of 8, Differential 2 of 4, Figure 2, See Table 7
HI3-0518	-5, -9										
HI4-0518	-8										
HI4P0518	-5, -9										
HI9P0518	-5, -9										
HI1-0539	-2, -4, -5, -8		850	4.0	0.8	33V CMOS-DI	0.001	250	160	4	Low Level Signals, 3% Max $R_{DS(ON)}$ Matching
HI3-0539	-5										
HI4P0539	-5										
HI1-0547	-2, -4, -5, -9	HI1-0547/883	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 8	Active Overvoltage Protection, 7% $R_{DS(ON)}$ Matching See Table 8 (Note 5)
HI3-0547	-5, -9										
HI4P0547	-5										
HI9P0547	-5, -9										
		HI4-0547/883									
HI1-0549	-2, -4, -5	HI1-0549/883	1800	4.0	0.8	44V CMOS-DI	0.1	300	300	2 x 4	70V Active Overvoltage Protection, 7% $R_{DS(ON)}$ Matching, See Table 8 (Note 5)
HI3-0549	-5, -9										
HI4P0549	-5										
HI9P0549	-5, -9										
		HI4-0549/883									
HI1-1828A	-2, -5, -7	HI1-1828A/883	400	4.0	0.4	40V CMOS-DI	125 Max	300	300	2 x 4	
HI3-1828A	-5										
HI4-1828A	-8	HI4-1828A/883									
HI4P1828A	-5										

NOTES:

1. The $R_{DS(ON)}$ of a CMOS switch varies as a function of supply voltage, analog signal voltage, and temperature. Values shown are maximum (unless noted "Typ" = typical) at +25°C.
   SWITCH "ON" V: Digital Threshold to "CLOSE" a particular switch. (Minimum if greater than "OFF". Maximum if less than "OFF").
   SWITCH "OFF" V: Digital Threshold to "OPEN" a particular switch. (Minimum if greater than "ON". Maximum if less than "ON").
   V_{INL}: Digital Threshold to represent a "Low" select signal. (Maximum, voltage levels greater than this value are not guaranteed to produce a "LOW").
   V_{INH}: Digital Threshold to represent a "HIGH" select signal. (Minimum, voltage levels less than this value are not guaranteed to produce a "HIGH").
2. Package codes:
   DG Types - SUFFIX:
   A 10 Lead TO-100 J Plastic DIP K Ceramic DIP P Ceramic DIP
   IH Types - Middle SUFFIX Letter:
   J Ceramic DIP P Plastic DIP T TO-100 Can B SOIC HI4P PLCC
   HI Types - PREFIX:
   HI1 Ceramic DIP HI2 Metal Can HI3 Plastic DIP HI4 Ceramic LCC HI9 Flatpack HI9P SOIC
3. Temperature Code Suffix:
   -1: 0° to +200°C
   -2, A, or M: -55°C to +125°C
   -4 or B: -25°C to +85°C
   -5: 0°C to +75°C
   C: 0°C to +70°C
   -7: 0°C to +75°C with Burn-In
   -8: -55°C to +125°C with Burn-In
   -9: -40°C to +85°C
   /883: Mil-Std-883, Class B, -55°C to +125°C with Burn-In
   I: Industrial, -25°C or -40°C to +85°C, see data sheet.
4. Double Throw switches have one switch ON and the other switch OFF for each input state. See data sheet.
5. Overvoltage Protection: Analog Inputs can withstand up to 70V peak to peak levels, with no channel interaction.
6. Fault Protection: All channels are OFF when supply power is off, up to +25V inputs. Any channel turns OFF when input exceeds supply rail.

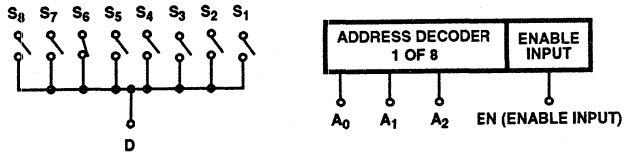


FIGURE 1. 1 x 8 MULTIPLEXER

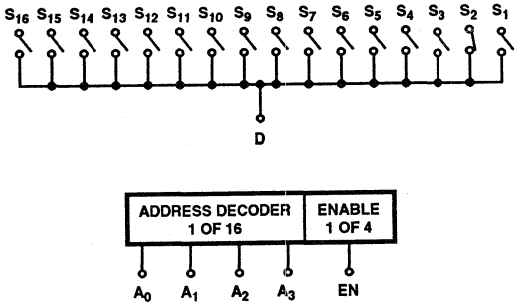


FIGURE 3. 1 x 16 MULTIPLEXER

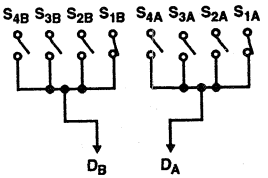
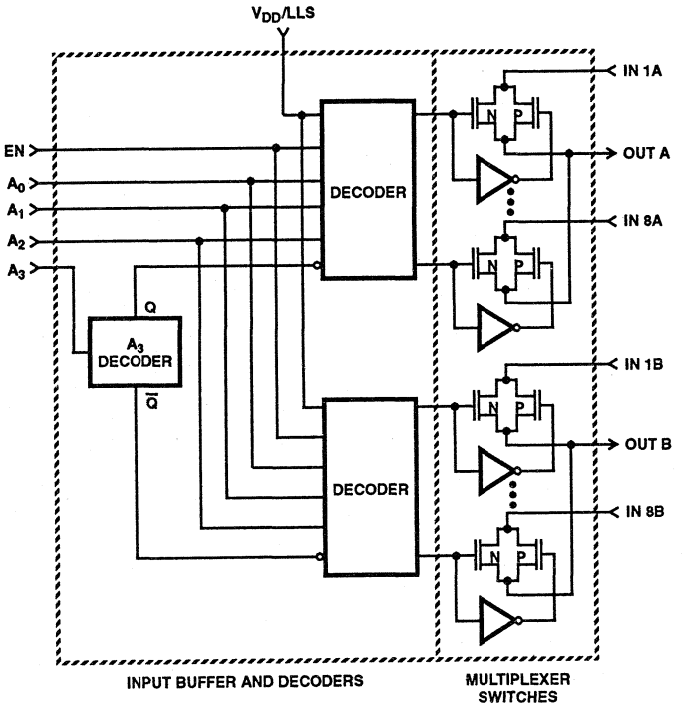


FIGURE 4. DUAL 1 x 4 MUX



A3 DECODER		
A3	Q	$\overline{Q}$
H	H	L
L	L	H
V-	L	L

FIGURE 2. PROGRAMMABLE

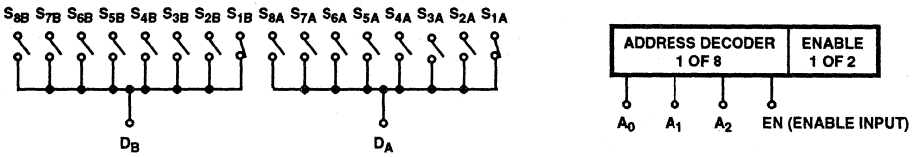
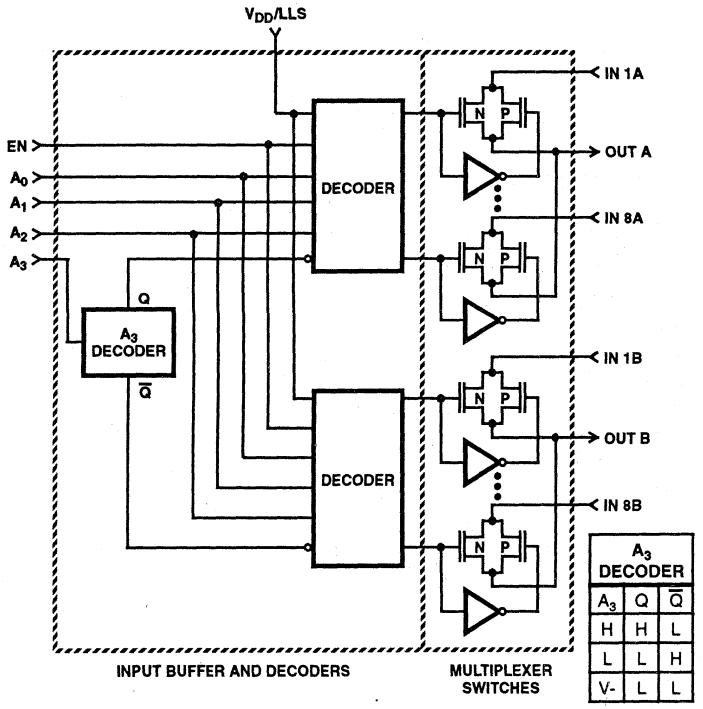
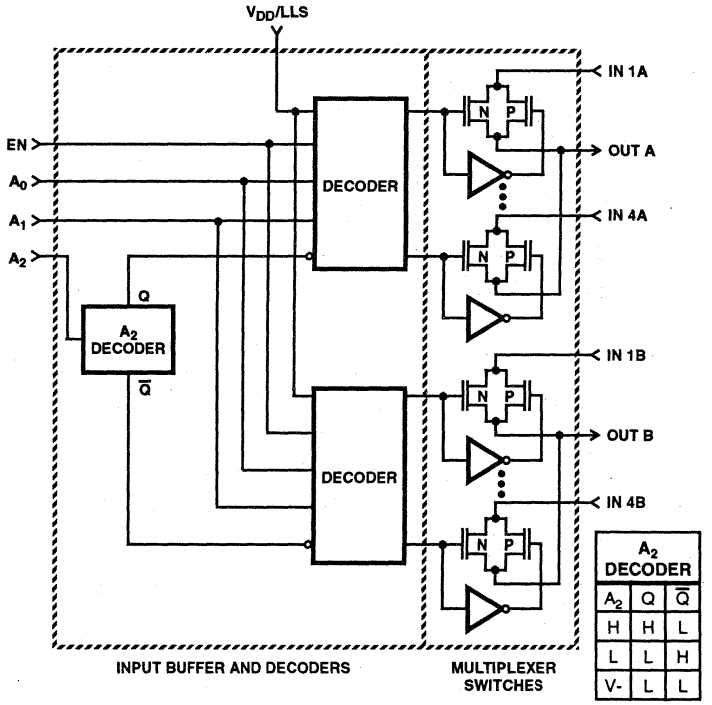


FIGURE 5. DUAL 1 x 8 MUX



A_3 DECODER		
A_3	Q	$\overline{Q}$
H	H	L
L	L	H
V-	L	L

FIGURE 6. PROGRAMMABLE SINGLE 16 OR DIFFERENTIAL 8



A_2 DECODER		
A_2	Q	$\overline{Q}$
H	H	L
L	L	H
V-	L	L

FIGURE 7. PROGRAMMABLE SINGLE 8 OR DIFFERENTIAL 4

HARRIS SEMICONDUCTOR

DG406, DG407

PRELIMINARY

December 1993

Single 16-Channel/Differential 8-Channel CMOS Analog Multiplexers

Features

- ON-Resistance 100Ω Max
- Low Power Consumption (P_D < 1.2mW)
- Fast Transition Time (300ns Max)
- Low Charge Injection
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Battery Operated Systems
- Data Acquisition
- Medical Instrumentation
- Hi-Rel Systems
- Communication Systems
- Automatic Test Equipment

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG406DJ	-40°C to +85°C	28 Lead Plastic DIP
DG406DY	-40°C to +85°C	28 Lead SOIC Narrow Body
DG407DJ	-40°C to +85°C	28 Lead Plastic DIP
DG407DY	-40°C to +85°C	28 Lead SOIC Narrow Body

Description

The DG406 and DG407 monolithic CMOS analog multiplexers are drop-in replacements for the popular DG506A and DG507A series devices. They each include an array of sixteen analog switches, a TTL and CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds, and an ENABLE input for device selection when several multiplexers are present.

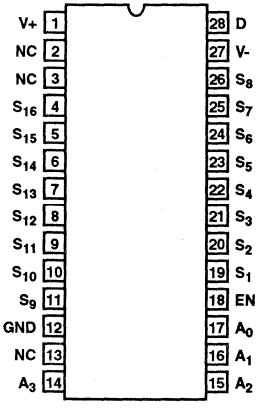
These multiplexers feature lower signal ON resistance (<100Ω) and faster transition time (t_{TRANS} < 250ns) compared to the DG506A and DG507A. Charge injection has been reduced, simplifying sample and hold applications.

The improvements in the DG406 series are made possible by using a high voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. The 44V maximum voltage range permits controlling 30V peak-to-peak signals when operating with ±15V power supplies.

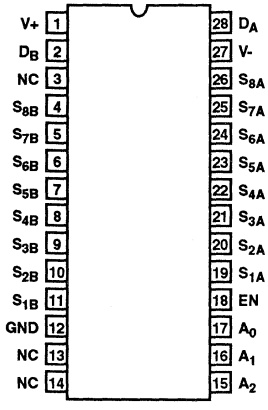
The sixteen switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

Pinouts

DG406
(PDIP, SOIC)
TOP VIEW



DG407
(PDIP, SOIC)
TOP VIEW

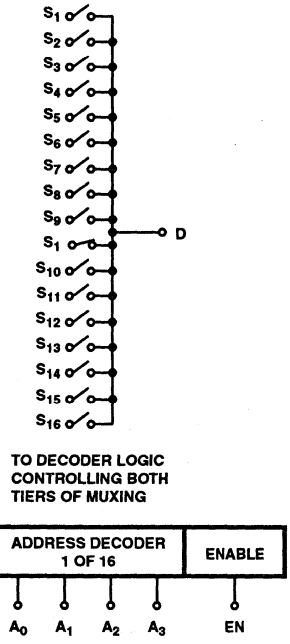


10 MULTIPLEXERS

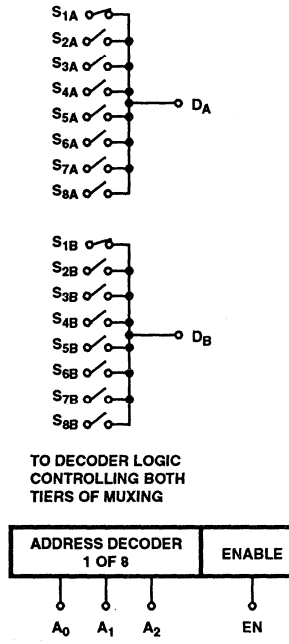
File Number 3116

Functional Block Diagrams

DG406



DG407



HARRIS SEMICONDUCTOR

DG408, DG409

Single 8-Channel/Differential 4-Channel CMOS Analog Multiplexers

December 1993

Features

- ON-Resistance 100Ω Maximum (+25°C)
- Low Power Consumption (P_D < 11mW)
- Fast Switching Action
  - t_{TRANS} < 250ns
  - $t_{ON/OFF(EN)}$ < 150ns
- Low Charge Injection
- Upgrade from DG508A/DG509A
- TTL, CMOS Compatible
- Single or Split Supply Operation

Applications

- Data Acquisition Systems
- Audio Switching Systems
- Automatic Testers
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Analog Selector Switch

Description

The DG408 Single 8-Channel and DG409 Differential 4-Channel monolithic CMOS analog multiplexers are drop-in replacements for the popular DG508A and DG509A series devices. They each include an array of eight analog switches, a TTL/CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds and an ENABLE input for device selection when several multiplexers are present.

The DG408 and DG409 feature lower signal ON resistance (< 100Ω) and faster switch transition time (t_{TRANS} < 250ns) compared to the DG508A or DG509A. Charge injection has been reduced, simplifying sample and hold applications. The improvements in the DG408 series are made possible by using a high-voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies. Power supplies may be single-ended from +5V to +34V, or split from ±5V to ±20V.

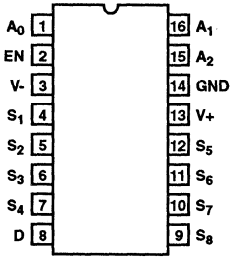
The analog switches are bilateral, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

Ordering Information

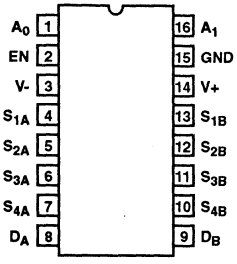
PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG408AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG408DJ	-40°C to +85°C	16 Lead Plastic DIP
DG408DY	-40°C to +85°C	16 Lead SOIC (N)
DG409AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG409DJ	-40°C to +85°C	16 Lead Plastic DIP
DG409DY	-40°C to +85°C	16 Lead SOIC (N)

Pinouts

DG408
TOP VIEW



DG409
TOP VIEW

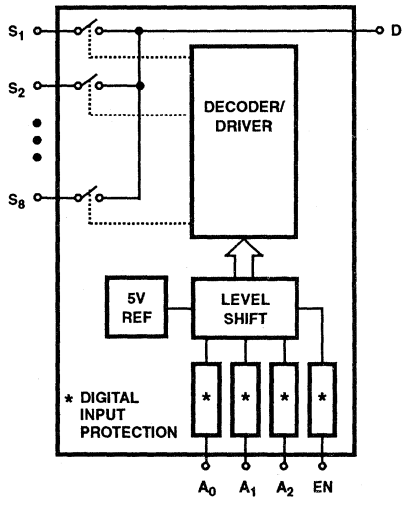


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

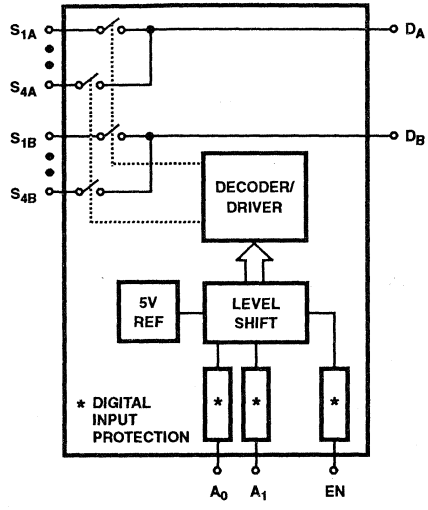
File Number 3283.1

Functional Block Diagrams

DG408



DG409



Absolute Maximum Ratings

V+ to V- ..... +44.0V
GND to V- 25V
Digital Inputs (Note 9) ..... (V-) -2V to (V+) + 2V or 20mA, Whichever Occurs First
Current (Any Terminal, Except S or D) 30mA
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed 1ms, 10% Duty Cycle)
Storage Temperature Range (D Suffix) ..... -65°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	70°C/W	19°C/W
Plastic DIP Package	100°C/W	-
SOIC (N) Package	120°C/W	-

Operating Temperature (D Suffix) ..... -40C to +85°C
Junction Temperature (D Suffix) ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITION	(NOTE 9) TEMP	D SUFFIX -40°C TO +85°C (NOTE 2) MIN	(NOTE 4) TYP	(NOTE 2) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Transition Time, t_{TRANS}	(See Figure 25)	Full	-	160	250	ns
Break-Before-Make Interval, t_{OPEN}	(See Figure 27)	Room	10	-	-	ns
Enable Turn-ON Time, $t_{ON(EN)}$	(See Figure 26)	Room	-	115	150	ns
		Full	-	-	225	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$	(See Figure 26)	Full	-	-	150	ns
Charge Injection, Q	C_L = 10nF, V_S = 0V	Room	-	20	-	pC
OFF Isolation	V_{EN} = 0V, R_L = 1kΩ, f = 100kHz (Note 7)	Room	-	75	-	dB
Logic Input Capacitance, C_{IN}	f = 1MHz	Room	-	8	-	pF
Source OFF Capacitance, $C_{S(OFF)}$	V_{EN} = 0V, V_S = 0V, f = 1MHz	Room	-	11	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$	V_{EN} = 0V, V_D = 0V, f = 1MHz					
DG408		Room	-	40	-	pF
DG409		Room	-	20	-	pF
Drain ON Capacitance, $C_{D(ON)}$	V_{EN} = 3V, V_D = 0V, f = 1MHz, V_A = 0V or 3V					
DG408		Room	-	54	-	pF
DG409		Room	-	34	-	pF
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}	(Note 3)	Full	-15	-	15	V
Drain-Source ON Resistance, $R_{DS(ON)}$	V_D = ±10V, I_S = -10mA (Note 5)	Room	-	40	100	Ω
		Full	-	-	125	Ω
$r_{DS(ON)}$ Matching Between Channels, $\Delta r_{DS(ON)}$	V_D = 10V, -10V	Room	-	-	15	Ω
Source OFF Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, V_S = ±10V, V_D = ∓10V	Room	-0.5	-	0.5	nA
		Full	-50	-	50	nA
Drain OFF Leakage Current, $I_{D(OFF)}$	V_{EN} = 0V, V_D = ±10V, V_S = ∓10V					
DG408		Room	-1	-	1	nA
		Full	-100	-	100	nA
DG409	V_{EN} = 0V, V_D = ±10V, V_S = ∓10V	Room	-1	-	1	nA
		Full	-50	-	50	nA

Electrical Specifications Test Conditions: V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITION	(NOTE 9) TEMP	D SUFFIX -40°C TO +85°C (NOTE 2) MIN	(NOTE 4) TYP	(NOTE 2) MAX	UNITS
ANALOG SWITCH (Continued)						
Drain ON Leakage Current, $I_{D(ON)}$ DG408	$V_S = V_D = \pm 10V$ Sequence Each Switch ON	Room	-1	-	1	nA
		Full	-100	-	100	nA
DG409		Room	-1	-	1	nA
		Full	-50	-	50	nA
DIGITAL CONTROL						
Logic Input Current, Input Voltage High, I_{AH}	V_A = 2.4V, 15V	Full	-10	-	10	µA
Logic Input Current, Input Voltage Low, I_{AL}	V_{EN} = 0V, 2.4V, V_A = 0V	Full	-10	-	10	µA
POWER SUPPLIES						
Positive Supply Current, I+	V_{EN} = 0V, V_A = 0V	Full	-	-	75	µA
Negative Supply Current, I-		Full	-75	-	-	µA
Positive Supply Current, I+	V_{EN} = 2.4V, V_A = 0V	Room Full	-	-	0.5 2	mA
Negative Supply Current, I-		Full	-500	-	-	µA

Electrical Specifications (Single Supply) Test Conditions: V+ = 12V, V- = 0V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITION	(NOTE 9) TEMP	D SUFFIX -40°C TO +85°C (NOTE 2) MIN	(NOTE 4) TYP	(NOTE 2) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Switching Time of Multiplexer, t_{TRANS}	V_{S1} = 8V, V_{S8} = 0V, V_{IN} = 2.4V	Room	-	180	-	ns
Enable Turn-ON Time, $T_{ON(EN)}$	V_{INH} = 2.4V, V_{INL} = 0V, V_{S1} = 5V	Room	-	180	-	ns
Enable Turn-OFF Time, $T_{OFF(EN)}$		Room	-	120	-	ns
Charge Injection, Q	C_L = 10nF, V_{GEN} = 0V, R_{GEN} = 0Ω	Room	-	5	-	pC
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}	(Note 3)	Full	0	-	12	V
Drain-Source ON-Resistance, $R_{DS(ON)}$	V_D = 3V, 10V, I_S = -1mA (Note 5)	Room	-	90	-	Ω

NOTES:

1. All leads soldered to PC Board.
2. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
3. Guaranteed by design, not subject to production test.
4. Typical values are for DESIGN AID ONLY, not guaranteed nor production tested.
5. Sequence each switch ON.
6. $\Delta r_{DS(ON)} = r_{DS(ON)}$ MAX - $r_{DS(ON)}$ MIN.
7. Worst case isolation occurs on channel 4 due to proximity to the drain pin.
8. Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
9. Room = +25°C, Cold and Hot = as determined by the operating temperature suffix.

Typical Performance Curves

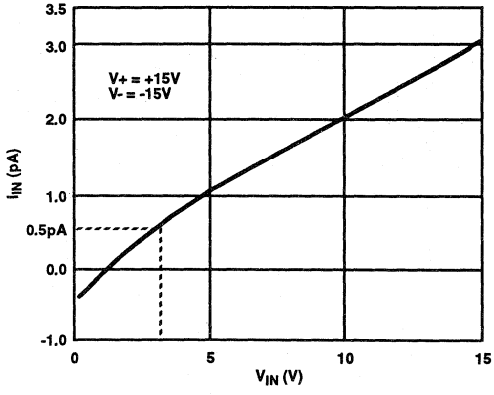


FIGURE 1. INPUT LOGIC CURRENT vs LOGIC INPUT VOLTAGE

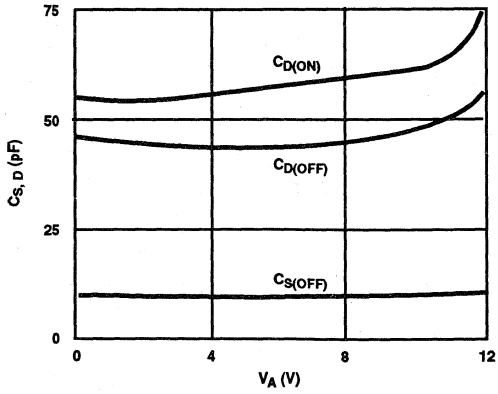


FIGURE 2. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE (SINGLE 12V SUPPLY)

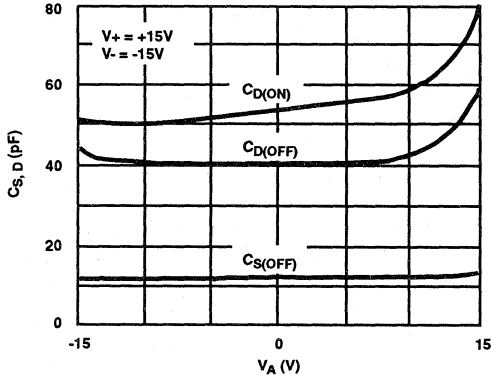


FIGURE 3. SOURCE/DRAIN CAPACITANCE vs ANALOG VOLTAGE

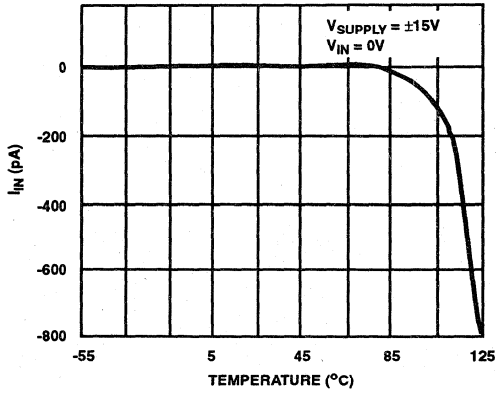


FIGURE 4. LOGIC INPUT CURRENT vs TEMPERATURE

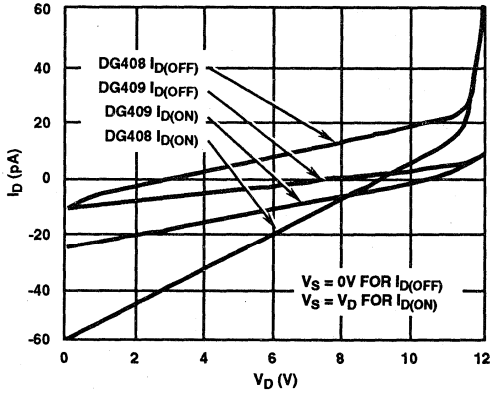


FIGURE 5. DRAIN LEAKAGE CURRENT vs SOURCE/DRAIN VOLTAGE (SINGLE 12V SUPPLY)

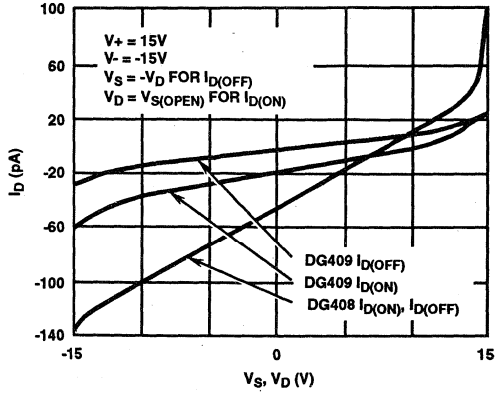


FIGURE 6. DRAIN LEAKAGE CURRENT vs SOURCE/DRAIN VOLTAGE

Typical Performance Curves (Continued)

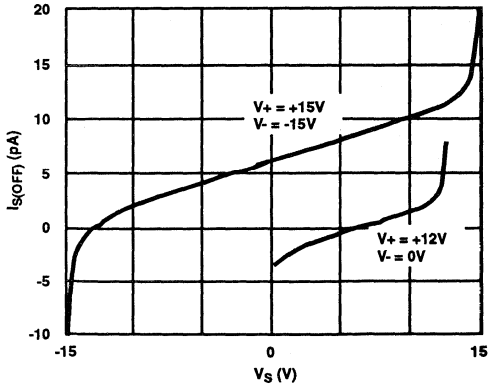


FIGURE 7. SOURCE LEAKAGE CURRENT vs SOURCE VOLTAGE

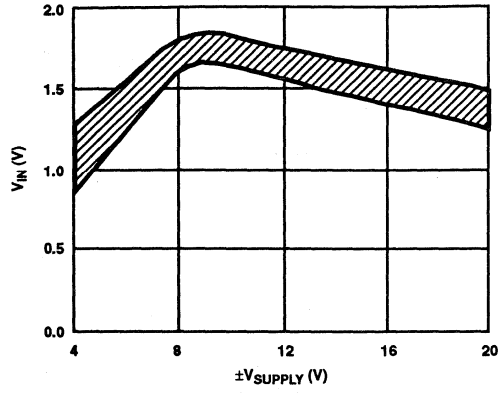


FIGURE 8. INPUT SWITCHING THRESHOLD vs SUPPLY VOLTAGE

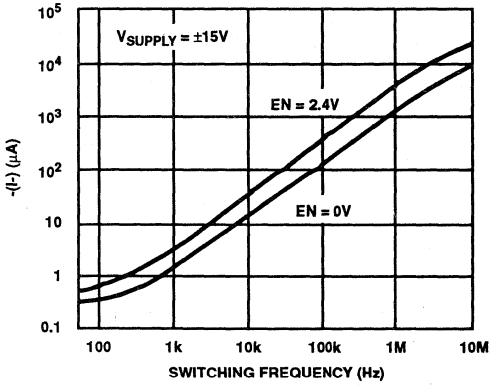


FIGURE 9. NEGATIVE SUPPLY CURRENT vs SWITCHING FREQUENCY

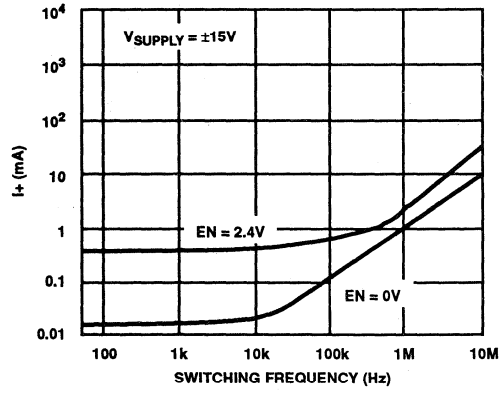


FIGURE 10. POSITIVE SUPPLY CURRENT vs SWITCHING FREQUENCY

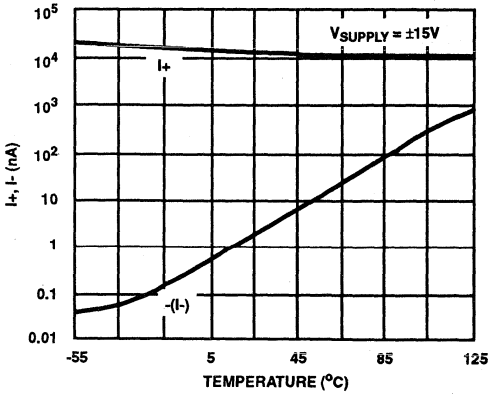


FIGURE 11. I_{SUPPLY} vs TEMPERATURE (LOG SCALE)

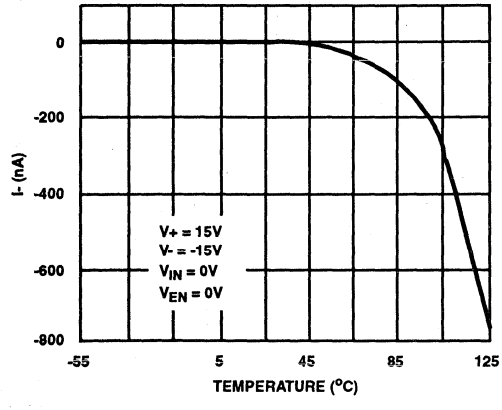


FIGURE 12. NEGATIVE SUPPLY CURRENT vs TEMPERATURE

Typical Performance Curves (Continued)

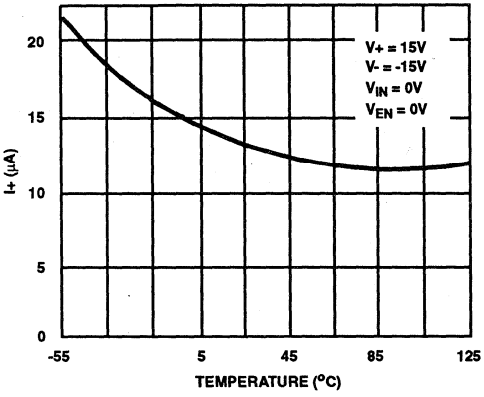


FIGURE 13. POSITIVE SUPPLY CURRENT vs TEMPERATURE (DG408)

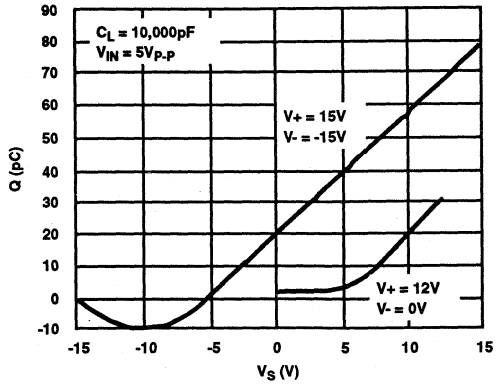


FIGURE 14. CHARGE INJECTION vs ANALOG VOLTAGE V_S (DG408, DG409)

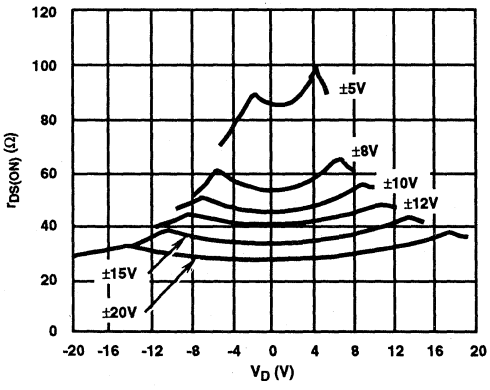


FIGURE 15. $r_{DS(ON)}$ vs V_D AND SUPPLY

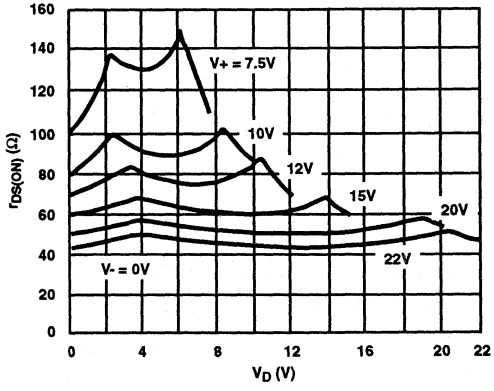


FIGURE 16. $r_{DS(ON)}$ vs V_D (SINGLE SUPPLY)

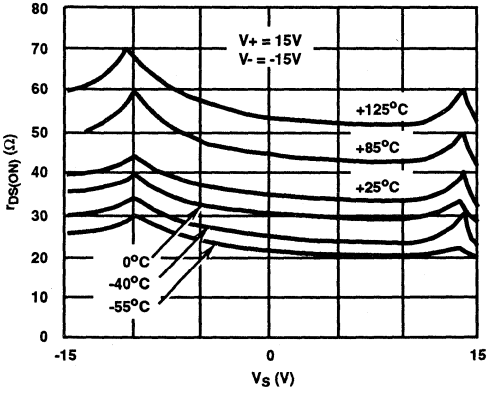


FIGURE 17. $r_{DS(ON)}$ vs V_S AND TEMPERATURE

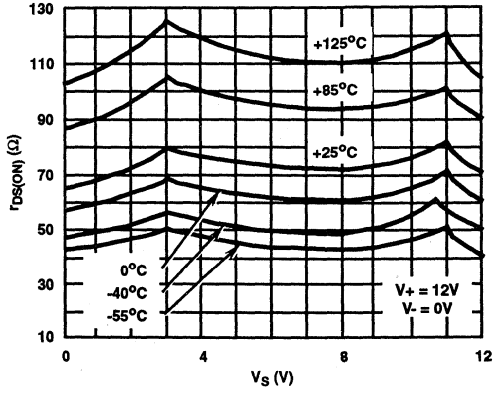


FIGURE 18. $r_{DS(ON)}$ vs V_S AND TEMPERATURE (SINGLE SUPPLY)

Typical Performance Curves (Continued)

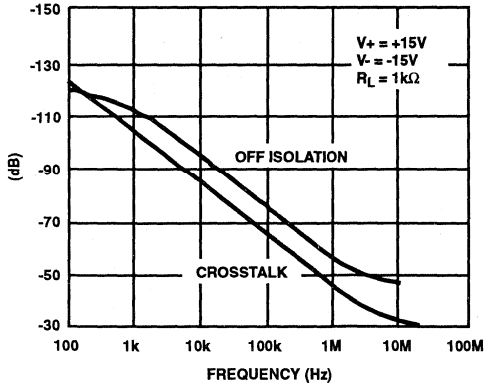


FIGURE 19. OFF ISOLATION AND CROSSTALK vs FREQUENCY

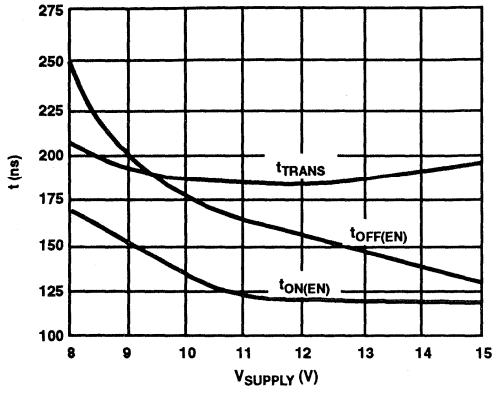


FIGURE 20. SWITCHING TIME vs SINGLE SUPPLY

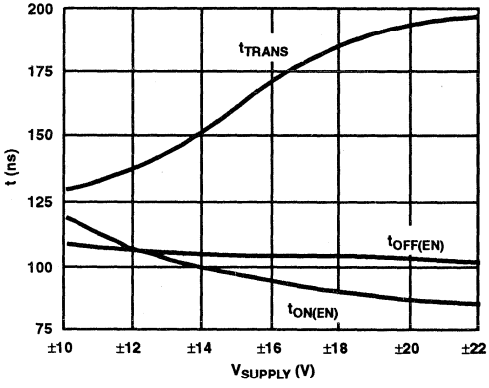


FIGURE 21. SWITCHING TIME vs BIPOLAR SUPPLY

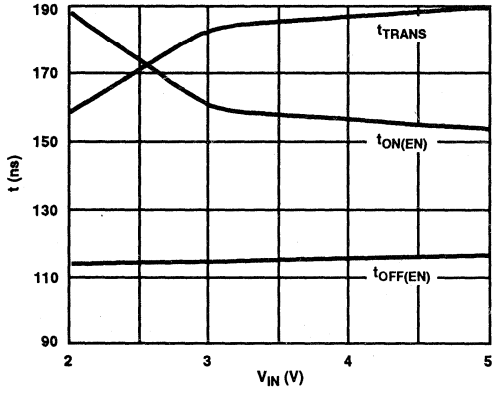


FIGURE 22. SWITCHING TIME vs V_{IN} (SINGLE SUPPLY)

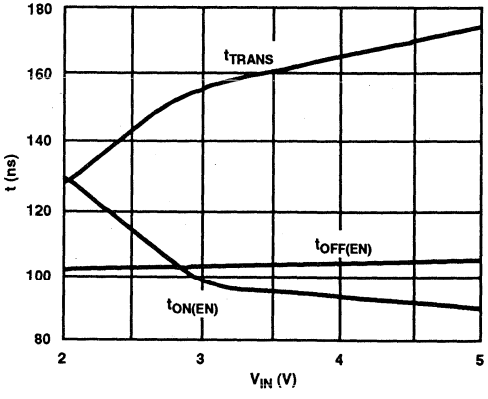


FIGURE 23. SWITCHING TIME vs V_{IN} (BIPOLAR SUPPLY)

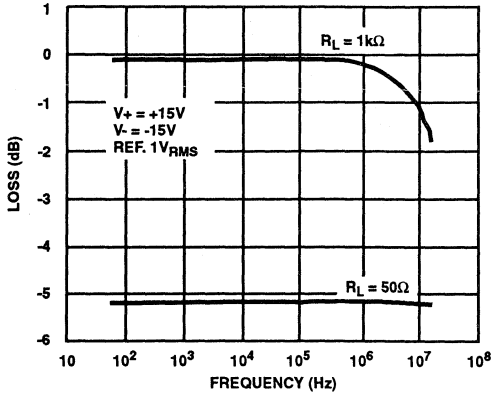


FIGURE 24. INSERTION LOSS vs FREQUENCY

Pin Description - (DG408)

PIN	SYMBOL	DESCRIPTION
1	A_0	Logic decode input (bit 0, LSB)
2	EN	Enable input
3	V-	Negative power supply terminal
4	S_1	Source (input) for channel 1
5	S_2	Source (input) for channel 2
6	S_3	Source (input) for channel 3
7	S_4	Source (input) for channel 4
8	D	Drain (output)
9	S_8	Source (input) for channel 8
10	S_7	Source (input) for channel 7
11	S_6	Source (input) for channel 6
12	S_5	Source (input) for channel 5
13	V+	Positive power supply terminal (substrate)
14	GND	Ground terminal (Logic Common)
15	A_2	Logic decode input (bit 2, MSB)
16	A_1	Logic decode input (bit 1)

Pin Description - (DG409)

PIN	SYMBOL	DESCRIPTION
1	A_0	Logic decode input (bit 0, LSB)
2	EN	Enable input
3	V-	Negative power supply terminal
4	S_{1A}	Source (input) for channel 1a
5	S_{2A}	Source (input) for channel 2a
6	S_{3A}	Source (input) for channel 3a
7	S_{4A}	Source (input) for channel 4a
8	D_A	Drain a (output a
9	D_B	Drain b (output b)
10	S_{4B}	Source (input) for channel 4b
11	S_{3B}	Source (input) for channel 3b
12	S_{2B}	Source (input) for channel 2b
13	S_{1B}	Source (input) for channel 1b
14	V+	Positive power supply terminal
15	GND	Ground terminal (Logic Common)
16	A_1	Logic decode input (bit 1, MSB))

TRUTH TABLE DG408

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

TRUTH TABLE DG409

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

NOTES:
1. V_{AH} Logic "1" ≥ 2.4V
2. V_{AL} Logic "0" ≤0.8V

Test Circuits

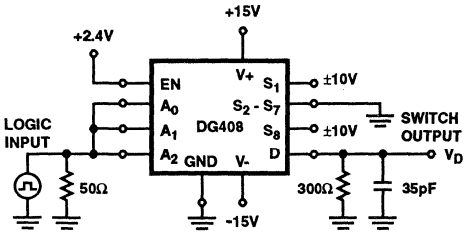


FIGURE 25A.

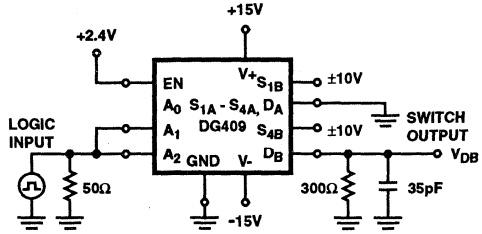


FIGURE 25B.

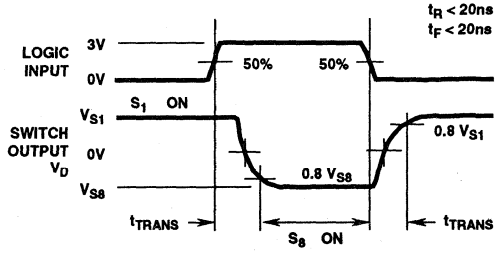


FIGURE 25C.

FIGURE 25. TRANSITION TIME

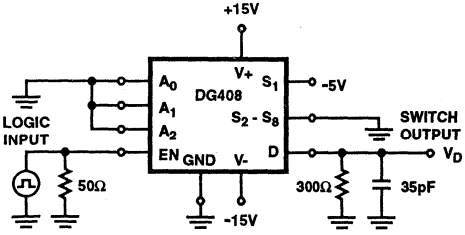


FIGURE 26A.

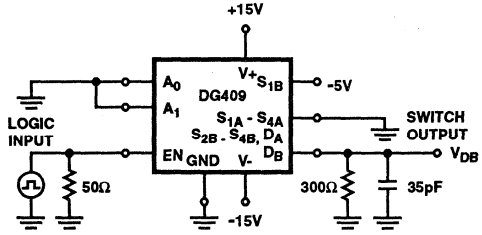


FIGURE 26B.

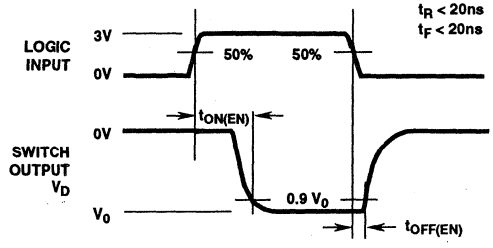


FIGURE 26C.

FIGURE 26. $t_{ON(EN)}$, $t_{OFF(EN)}$

Test Circuits (Continued)

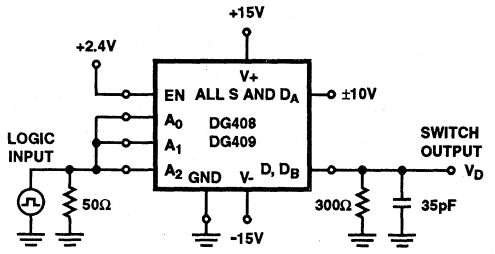


FIGURE 27A.

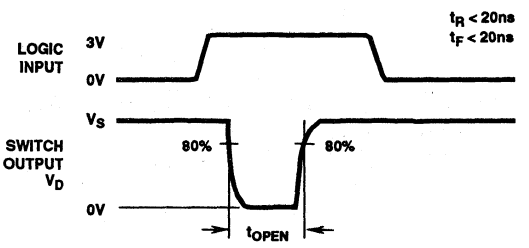


FIGURE 27B.

FIGURE 27. BREAK-BEFORE-MAKE INTERVAL

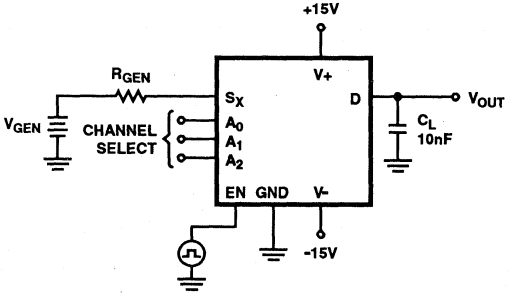
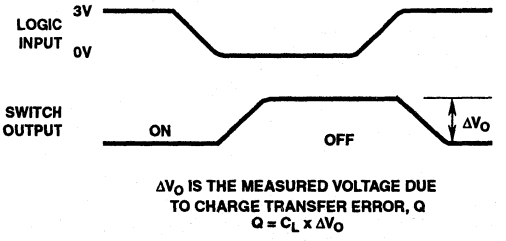


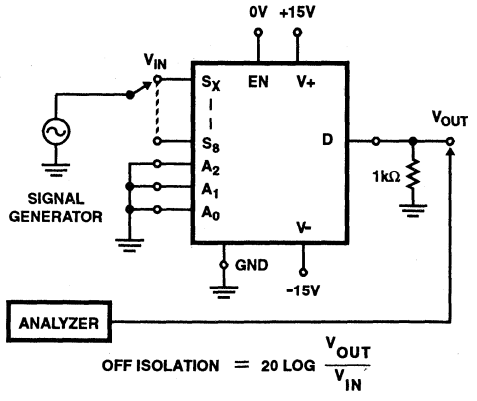
FIGURE 28A.



ΔV_O IS THE MEASURED VOLTAGE DUE TO CHARGE TRANSFER ERROR, Q
$Q = C_L \times \Delta V_O$

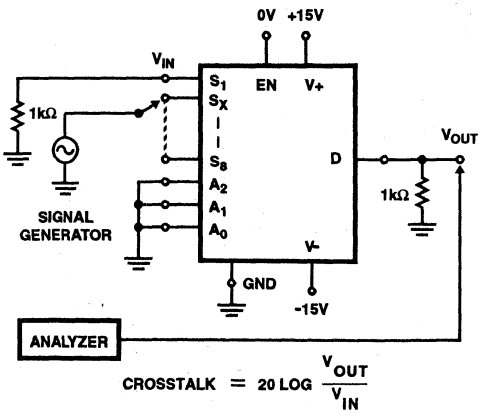
FIGURE 28B.

FIGURE 28. CHARGE INJECTION



OFF ISOLATION = 20 LOG $\frac{V_{OUT}}{V_{IN}}$

FIGURE 29. OFF ISOLATION



CROSSTALK = 20 LOG $\frac{V_{OUT}}{V_{IN}}$

FIGURE 30. CROSSTALK

Test Circuits (Continued)

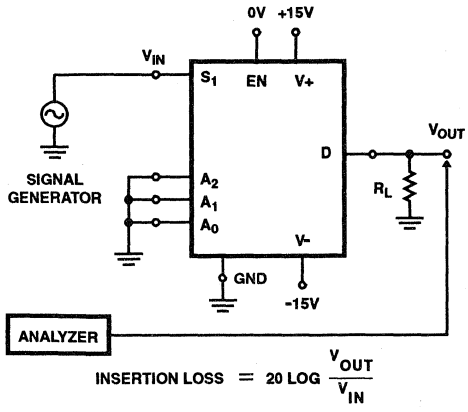


FIGURE 31. INSERTION LOSS

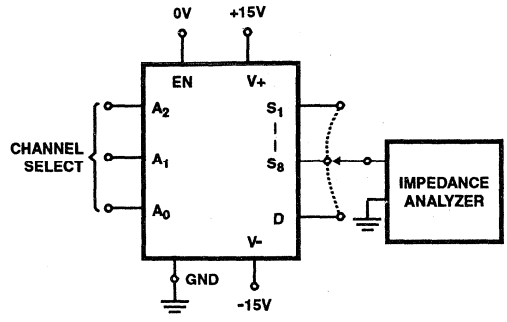


FIGURE 32. SOURCE/DRAIN CAPACITANCES

Typical Applications

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 33). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V- value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference V_S - (V-) doesn't exceed -44V. The addition of these diodes will reduce the analog signal range to 1V below V+ and 1V above V-, but it preserves the low channel resistance and low leakage characteristics.

Typical application information is for Design Aid Only, not guaranteed and not subject to production testing.

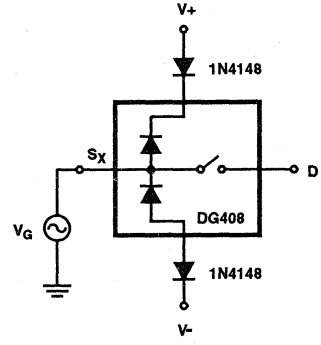


FIGURE 33. OVERVOLTAGE PROTECTION USING BLOCKING DIODES

Die Characteristics

DIE DIMENSIONS:
1800µm x 3320µm x 485 ± 25µm

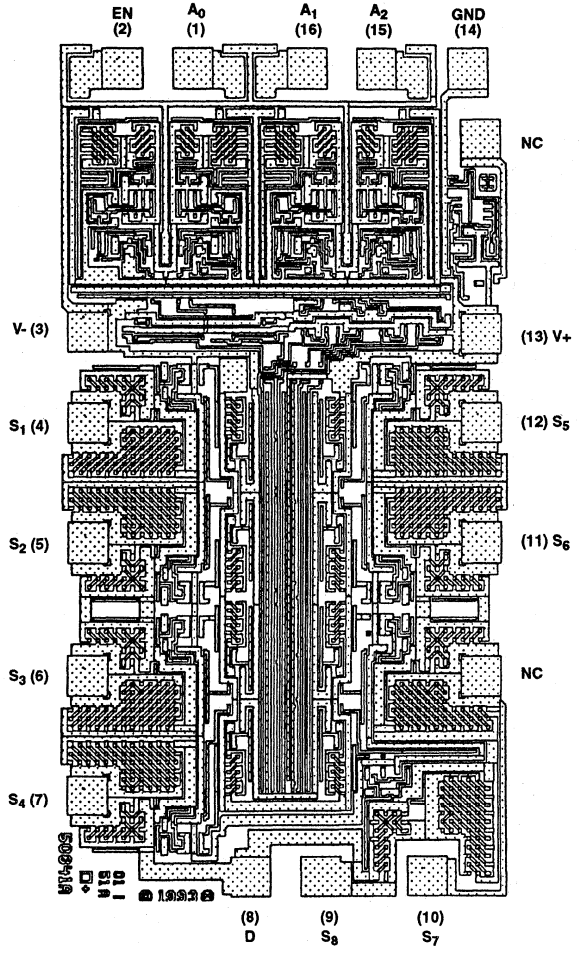
METALLIZATION:
Type: SiAl
Thickness: 12kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG408



Die Characteristics

DIE DIMENSIONS:
1800µm x 3320µm x 485 ± 25µm

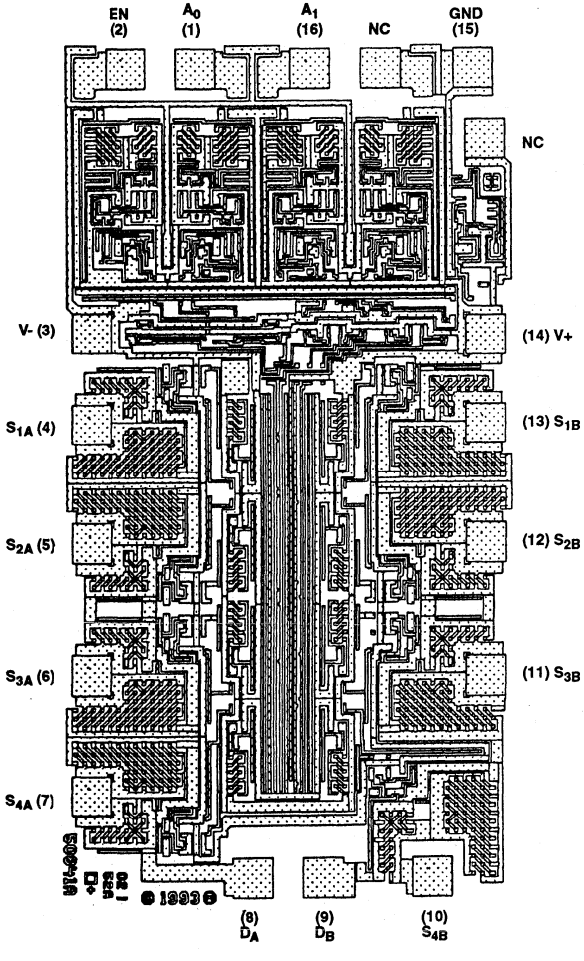
METALLIZATION:
Type: SiAl
Thickness: 12kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG409



HARRIS SEMICONDUCTOR

DG458, DG459

PRELIMINARY

December 1993

Single 8-Channel/Differential 4-Channel Fault Protected Analog Multiplexers

Features

- Fault and Overvoltage Protection
- ON-Resistance < 1.5kΩ (+25°C)
- Low Power Consumption (P_D < 3mW)
- Fast Switching Action
  - t_A < 500ns
  - $t_{ON/OFF(EN)}$ < 250ns
- Fail Safe with Power Loss (No Latch-Up)
- Upgrade from IH5108/IH5208
- TTL, CMOS Compatible Logic

Applications

- Data Acquisition Systems
- Audio Switching Systems
- Automatic Testers
- Hi-Rel Systems
- Sample and Hold Circuits
- Communication Systems
- Analog Selector Switch

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
DG458DJ	-40°C to +85°C	16 Lead Plastic DIP
DG458DY	-40°C to +85°C	16 Lead SOIC (W)
DG458AK/883	-55°C to +125°C	16 Lead Ceramic DIP
DG459DJ	-40°C to +85°C	16 Lead Plastic DIP
DG459DY	-40°C to +85°C	16 Lead SOIC (W)
DG459AK/883	-55°C to +125°C	16 Lead Ceramic DIP

Description

The DG458 Single 8-Channel and DG459 Differential 4-Channel monolithic CMOS analog multiplexers are drop-in replacements for the popular IH5108 and IH5208 series devices. They each include an array of eight analog switches, a series N-channel/P-channel/N-channel fault protection circuit, a TTL/CMOS compatible digital decode circuit for channel selection, a voltage reference for logic thresholds and an ENABLE input for device selection when several multiplexers are present.

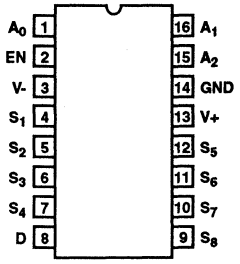
The DG458 and DG459 feature lower signal ON resistance (450Ω typical) and faster switch transition time (200ns typical) compared to the IH5108 or IH5208. The improvements in the DG458 series are made possible by using a high-voltage silicon-gate process. An epitaxial layer prevents the latch-up associated with older CMOS technologies.

The 44V maximum voltage range permits controlling 20V peak-to-peak signals, while withstanding continuous overvoltages up to ±35V, providing an open fault circuit.

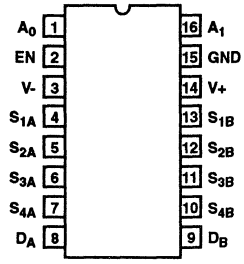
The analog switches are bilateral, break-before-make, equally matched for AC or bidirectional signals. The ON resistance variation with analog signals is quite low over a ±5V analog input range.

Pinouts

DG458 (CDIP, PDIP, SOIC)
TOP VIEW



DG459 (CDIP, PDIP, SOIC)
TOP VIEW

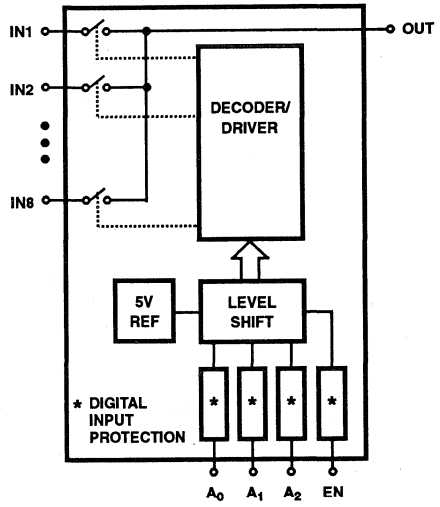


10 MULTIPLEXERS

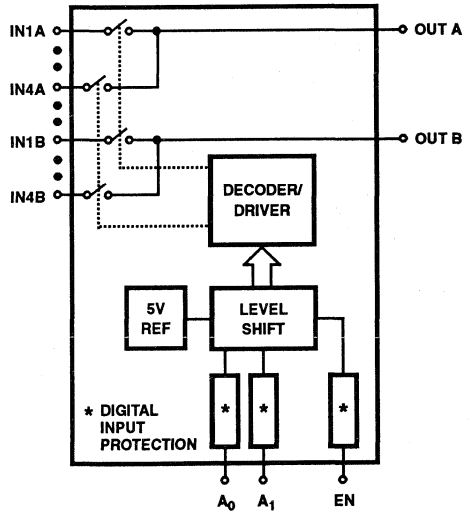
File Number 3280.1

Functional Block Diagrams

DG458



DG459



Absolute Maximum Ratings

V+ to V- ..... +44V
V+ to GND 22V
V- to GND ..... -25V
Digital Input, V_{EN}, V_A ..... (V-) -4V to (V+) +4V
Analog Input Overvoltage w/Power On, V_S .... (V-) -20V to (V+) +20V
Analog Input Overvoltage w/Power Off, V_S ..... -35V to +35V
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed 1ms, 10% Duty Cycle Max)
Storage Temperature Range (D Suffix) ..... -65°C to +125°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	100°C/W	-
Ceramic DIP Package	70°C/W	19°C/W
SOIC Package	100°C/W	-

Operating Temperature (D Suffix) ..... -40°C to +85°C
Ceramic DIP ..... -55°C to +125°C
Junction Temperature (D Suffix) ..... +150°C
Ceramic DIP ..... +175°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 1) TEMP	D SUFFIX -40°C TO +85°C (NOTE 3) MIN	(NOTE 2) TYP	(NOTE 3) MAX	UNITS
DYNAMIC CHARACTERISTICS						
Transition Time, t_A	See Figure 15	+25°C	-	200	500	ns
Break-Before-Make Time, t_{BBM}	See Figure 16	+25°C	10	45	-	ns
Enable Turn-ON Time, $t_{ON(EN)}$	See Figure 17	+25°C	-	140	250	ns
		Full	-	-	500	ns
Enable Turn-OFF Time, $t_{OFF(EN)}$		+25°C	-	50	250	ns
		Full	-	-	500	ns
Settling Time, t_S	To 0.1%	+25°C	-	1.2	-	µs
	To 0.01%	+25°C	-	3.5	-	µs
OFF Isolation	V_{EN} = 0V, R_L = 1kΩ C_L = 15pF V_S = $3V_{RMS}$, f = 100kHz (Note 7)	+25°C	-	90	-	dB
Logic Input Capacitance, C_{IN}	f = 1MHz	+25°C	-	5	-	pF
Source OFF Capacitance, $C_{S(OFF)}$		+25°C	-	5	-	pF
Drain OFF Capacitance, $C_{D(OFF)}$						
DG458		+25°C	-	15	-	pF
DG459		+25°C	-	10	-	pF
Drain ON Capacitance, $C_{D(ON)}$						
DG458		+25°C	-	40	-	pF
DG459		+25°C	-	35	-	pF
ANALOG SWITCH						
Analog Signal Range, V_{ANALOG}	Note 4	Full	-10	-	10	V
Drain-Source ON Resistance, $R_{DS(ON)}$	V_D = ±9.5V, I_S = -1mA (Note 5)	+25°C	-	0.45	1.5	kΩ
		Full	-	-	1.8	kΩ
	V_D = ±5V, I_S = -1mA (Note 5)	+25°C	-	180	400	Ω
$R_{DS(ON)}$ Matching Between Channels, $\Delta R_{DS(ON)}$	V_D = 0V, I_S = -1mA (Note 6)	+25°C	-	6	-	%
Source Off Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V, V_S = ±10V, V_D = ∓10V	+25°C	-1	0.03	1	nA
		Full	-50	-	50	nA
Drain Off Leakage Current, $I_{D(OFF)}$						

Electrical Specifications V+ = +15V, V- = -15V, V_{AL} = 0.8V, V_{AH} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 1) TEMP	D SUFFIX -40°C TO +85°C (NOTE 3) MIN	(NOTE 2) TYP	(NOTE 3) MAX	UNITS
ANALOG SWITCH (Continued)						
DG458	V_{EN} = 0V, V_S = ∓10V, V_D = ±10V	+25°C	-1	0.1	1	nA
		Full	-200	-	200	nA
DG459		+25°C	-2	0.1	2	nA
		Full	-100	-	100	nA
Differential Off Drain Leakage Current, I_{DIFF}	DG459 Only	Full	-50	-	50	nA
Drain On Leakage Current, $I_{D(ON)}$						
DG458	V_S = V_D = ±10V, V_{AL} = 0.8V, V_{AH} = 2.4V Sequence Each Switch On	+25°C	-5	0.1	5	nA
		Full	-200	-	200	nA
DG459		+25°C	-5	0.05	5	nA
		Full	-100	-	100	nA
DIGITAL CONTROL						
Input Low Threshold, V_{AL}		Full	-	-	0.8	V
Input Low Threshold, V_{AL}		Full	2.4	-	-	V
Logic Input Control, I_A	V_A = 2.4V or 0.3V	Full	-	-1	1	µA
FAULT						
Output Leakage Current (With Overvoltage), $I_{D(OFF)}$	V_S = ±33V, V_D = 0V (See Figure 14)	+25°C	-	0.02	-	nA
		Full	-2000	-	2000	nA
Input Leakage Current (With Overvoltage), $I_{S(OFF)}$	V_S = ±25V, V_D = ±10V (See Figure 14)	+25°C	-10	0.005	10	µA
Input Leakage Current (With Power Supplies Off), $I_{S(OFF)}$	V_A = ±25V, V_{SUPS} = 0V, V_D = A_0 = A_1 = A_2 = EN = 0V	+25°C	-5	0.001	5	µA
POWER SUPPLIES						
Positive Supply Current, I+	V_{EN} = High or Low V_A = 0V	+25°C	-	0.05	0.1	mA
		Full	-	-	0.2	mA
Negative Supply Current, I-		+25°C	-0.1	-0.01	-	mA
		Full	-0.2	-	-	mA
Power Supply Range for Continuous Operation		+25°C	±4.5	-	±18	V

NOTES:

1. Full = as determined by the operating temperature suffix.
2. Typical values are for Design Aid Only, not guaranteed nor subject to production testing.
3. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
4. When the analog signal exceeds the +13.5V or -12V $R_{DS(ON)}$ starts to rise until only leakage currents flow.
5. Electrical Characteristics such as $R_{DS(ON)}$ change when supplies other than ±15V are used.
6. $$\Delta R_{DS(ON)} = \frac{R_{DS(ON)}MAX - R_{DS(ON)}MIN}{\Delta R_{DS(ON)}AVE}$$
7. Worst case is channel 4 due to close proximity of input and output leads of package. This parameter varies with package style.

Typical Performance Curves +25°C, Unless Otherwise Specified

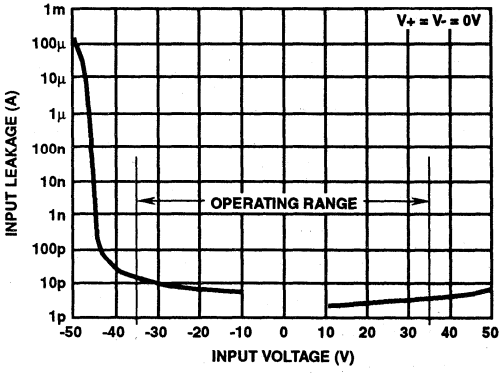


FIGURE 1. INPUT LEAKAGE vs INPUT VOLTAGE

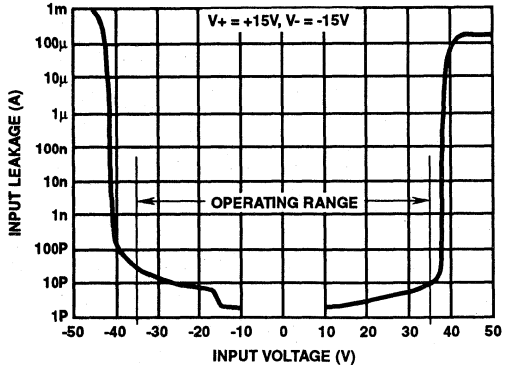


FIGURE 2. OFF CHANNEL LEAKAGE CURRENT vs INPUT VOLTAGE

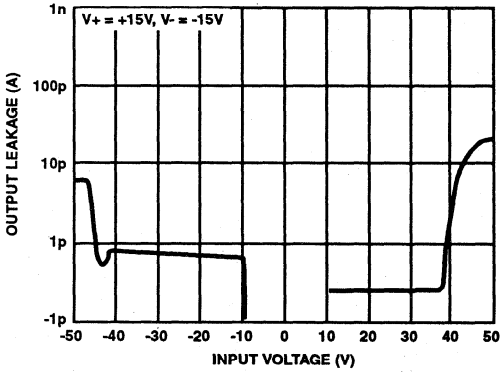


FIGURE 3. OUTPUT LEAKAGE vs OFF CHANNEL OVERVOLTAGE

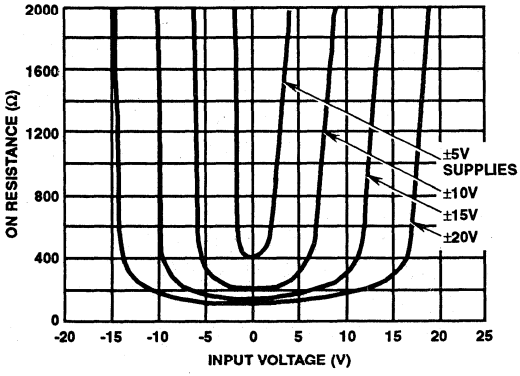


FIGURE 4. $R_{DS(ON)}$ vs INPUT VOLTAGE

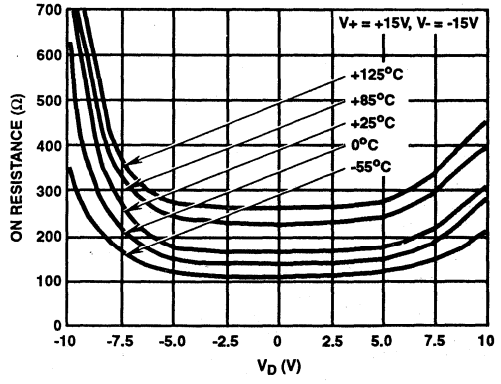


FIGURE 5. $R_{DS(ON)}$ vs V_D AND TEMPERATURE

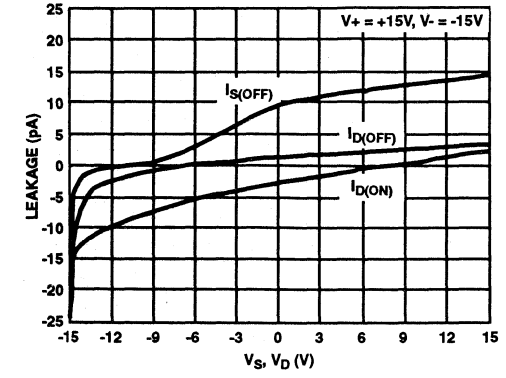


FIGURE 6. LEAKAGE CURRENT vs V_S, V_D

Typical Performance Curves +25°C, Unless Otherwise Specified (Continued)

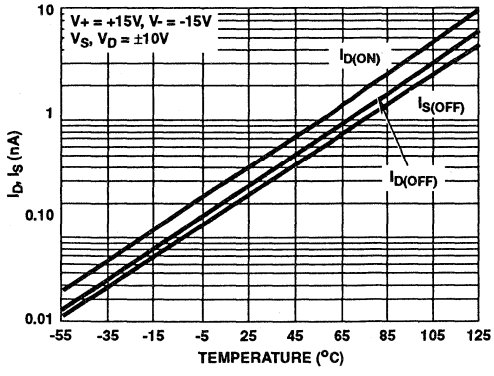


FIGURE 7. LEAKAGE CURRENT vs TEMPERATURE

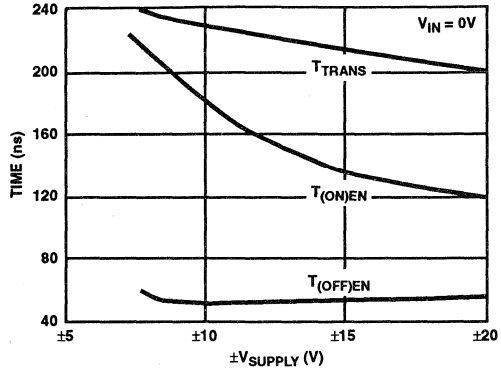


FIGURE 8. SWITCHING TIMES (t_{TRANS}, t_{ON}, t_{OFF}) vs ±V SUPPLIES

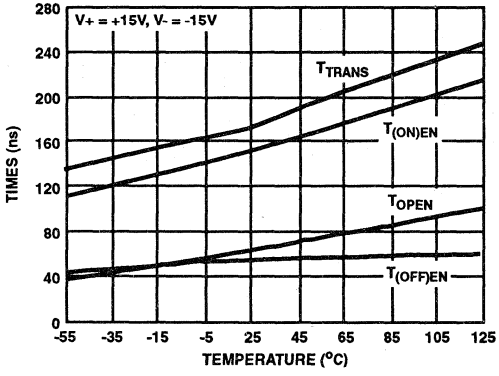


FIGURE 9. SWITCHING TIMES vs TEMPERATURE

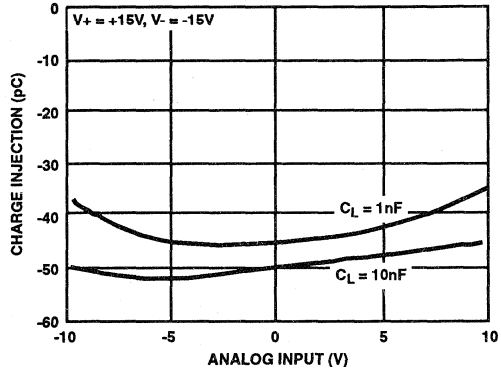


FIGURE 10. Q_{INJ} vs V_S

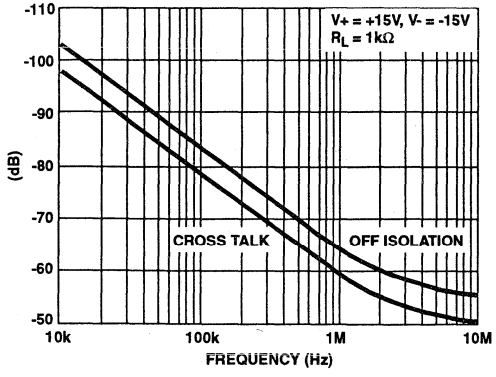


FIGURE 11. OFF ISOLATION AND $CROSS_{TALK}$ vs FREQUENCY3

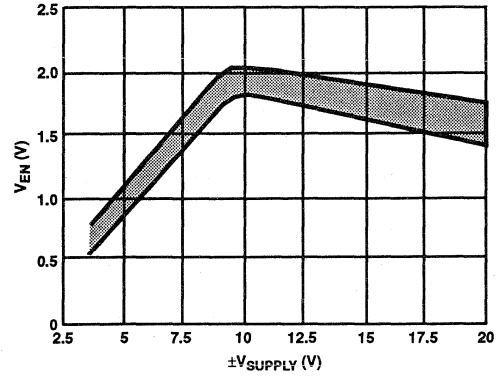


FIGURE 12. LOGIC INPUT SWITCHING THRESHOLD vs ±V SUPPLIES

Pin Description

PIN	SYMBOL	DESCRIPTION
DG458		
1	A_0	Logic decode input (bit 0, LSB)
2	EN	Enable input
3	V-	Negative power supply terminal
4	S_1	Source (input) for channel 1
5	S_2	Source (input) for channel 2
6	S_3	Source (input) for channel 3
7	S_4	Source (input) for channel 4
8	D	Drain (output)
9	S_8	Source (input) for channel 8
10	S_7	Source (input) for channel 7
11	S_6	Source (input) for channel 6
12	S_5	Source (input) for channel 5
13	V+	Positive power supply terminal (substrate)
14	GND	Ground terminal (Logic Common)
15	A_2	Logic decode input (bit 2, MSB)
16	A_1	Logic decode input (bit 1)
DG459		
1	A_0	Logic decode input (bit 0, LSB)
2	EN	Enable input
3	V-	Negative power supply terminal
4	S_{1A}	Source (input) for channel 1A
5	S_{2A}	Source (input) for channel 2A
6	S_{3A}	Source (input) for channel 3A
7	S_{4A}	Source (input) for channel 4A
8	D_A	Drain A (output a)
9	D_B	Drain B (output b)
10	S_{4B}	Source (input) for channel 4B
11	S_{3B}	Source (input) for channel 3B
12	S_{2B}	Source (input) for channel 2B
13	S_{1B}	Source (input) for channel 1B
14	V+	Positive power supply terminal
15	GND	Ground terminal (Logic Common)
16	A_1	Logic decode input (bit 1, MSB)

DG458 TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

DG459 TRUTH TABLE

A_1	A_0	EN	ON SWITCH
X	X	0	NONE
0	0	1	1A, 1B
0	1	1	2A, 2B
1	0	1	3A, 3B
1	1	1	4A, 4B

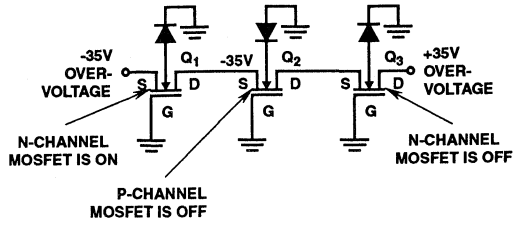
NOTES:
1. V_{AH} Logic "1" ≥ 2.4V
2. V_{AL} Logic "0" ≤0.8V

Detailed Description

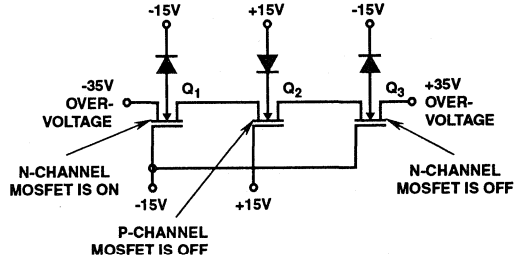
The DG458 and DG459 multiplexers are full fault and overvoltage protected for continuous input voltages up to ±35V whether or not voltage is applied to the power supply pins (V+, V-). These multiplexers are built on a high voltage junction-isolated silicon gate CMOS process. Two n-channel and one p-channel MOSFETs are connected in series to form each channel (Figure 13).

Within the normal analog signal range (±10V), the $R_{DS(ON)}$ variation as a function of analog signal voltage is comparable to that of the classic parallel n-MOS and p-MOS switches.

When the analog signal approaches or exceeds either supply rail, even for an on-channel, one of the three series MOSFETs gets cut off, providing inherent protection against overvoltages even if the multiplexer power supply voltages are lost. This protection is good up to the breakdown voltage of the respective series MOSFETs. Under fault conditions only sub microamp leakage currents can flow in or out of the multiplexer. This not only provides protection for the multiplexer and succeeding circuitry, but it allows normal, undisturbed operation of all other channels. Additionally, in case of power loss to the multiplexer, the loading caused on the transducers and signal sources is insignificant, therefore redundant multiplexers can be used on critical applications such as telemetry and avionics.



13A. OVERVOLTAGE WITH MUX POWER OFF



13B. OVERVOLTAGE WITH MUX POWER ON

FIGURE 13. OVERVOLTAGE PROTECTION

Test Circuits

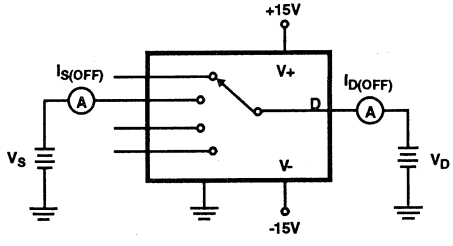


FIGURE 14. ANALOG INPUT OVERVOLTAGE

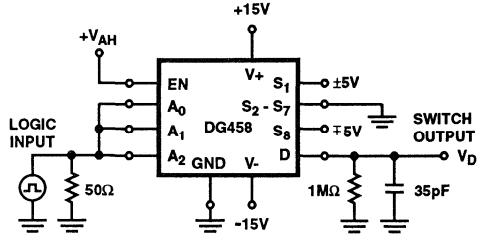


FIGURE 15A.

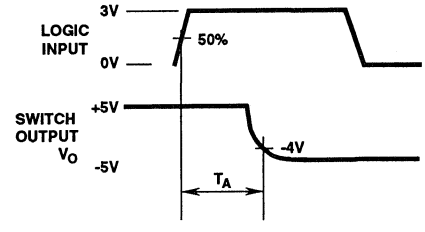


FIGURE 15B.

FIGURE 15. TRANSITION TIME

Test Circuits (Continued)

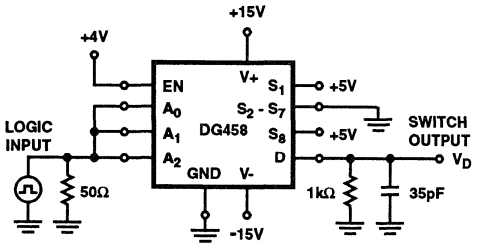


FIGURE 16A.

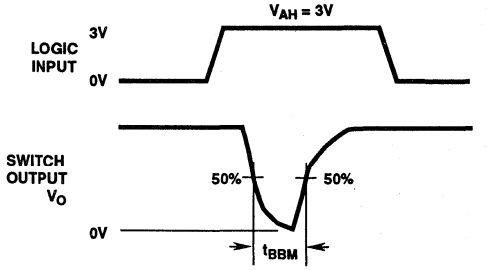


FIGURE 16B.

FIGURE 16. BREAK-BEFORE-MAKE TIME

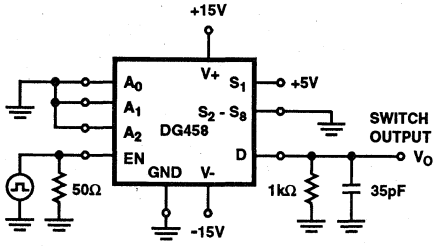


FIGURE 17A.

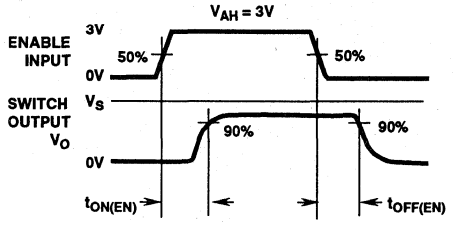


FIGURE 17B.

FIGURE 17. ENABLE DELAY

Die Characteristics

DIE DIMENSIONS:
2490µm x 4060µm x 485µm ±25µm

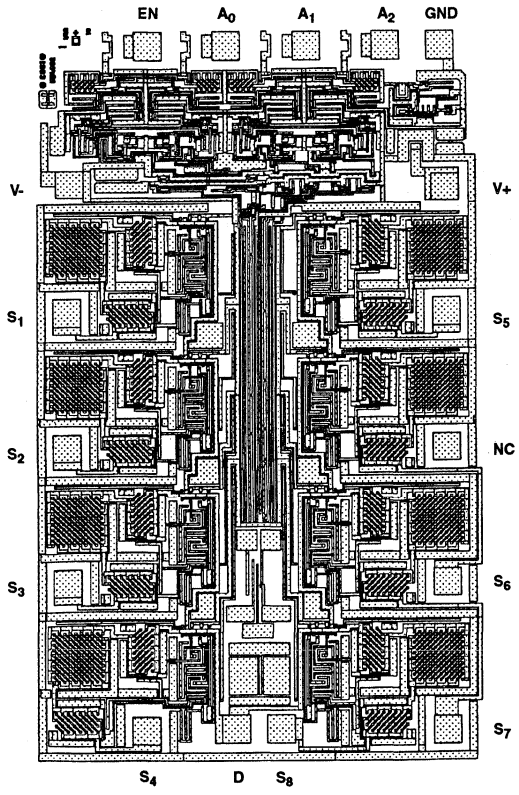
METALLIZATION:
Type: Si - Al
Thickness: 12kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride
Thickness: 8kÅ ± 1kÅ

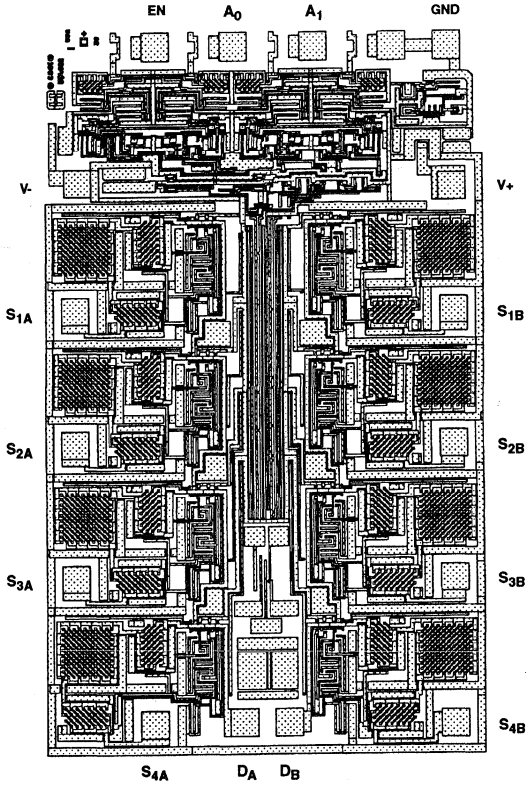
WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG458



DG459



HARRIS SEMICONDUCTOR

DG506A, DG507A DG508A, DG509A

December 1993

CMOS Analog Multiplexers

Features

- Low Power Consumption
- TTL and CMOS Compatible Address and Enable Inputs
- 44V Maximum Power Supply Rating
- High Latch-Up Immunity
- Break-Before-Make Switching
- Alternate Source

Applications

- Data Acquisition Systems
- Communication Systems
- Signal Multiplexing/Demultiplexing
- Audio Signal Multiplexing

Description

The DG506A, DG507A, DG508A and DG509A are CMOS monolithic 16-channel/dual 8-channel and 8-channel/dual 4-channel analog multiplexers, which can also be used as demultiplexers. An enable input is provided. When the enable input is high, a channel is selected by the address inputs, and when low, all channels are off.

A channel in the ON state conducts current equally well in both directions. In the OFF state each channel blocks voltages up to the supply rails. The address inputs and the enable input are TTL and CMOS compatible over the full specified operating temperature range.

The DG506A, DG507A, DG508A and DG509A are pinout compatible with the industry standard devices.

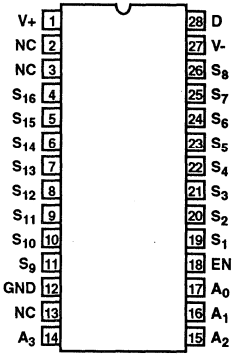
Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
DG506AAK	-55°C to +125°C	28 Lead Ceramic DIP
DG506AAK/883B	-55°C to +125°C	28 Lead Ceramic DIP
DG506ABK	-25°C to +85°C	28 Lead Ceramic DIP
DG506ABY	-25°C to +85°C	28 Lead Plastic DIP
DG506ACJ	0°C to +70°C	28 Lead Plastic DIP
DG506ACK	0°C to +70°C	28 Lead Ceramic DIP
DG506ACY	0°C to +70°C	28 Lead SOIC
DG507AAK	-55°C to +125°C	28 Lead Ceramic DIP
DG507AAK/883B	-55°C to +125°C	28 Lead Ceramic DIP
DG507ABK	-25°C to +85°C	28 Lead Ceramic DIP
DG507ABY	-25°C to +85°C	28 Lead Plastic DIP
DG507ACJ	0°C to +70°C	28 Lead Plastic DIP
DG507ACK	0°C to +70°C	28 Lead Ceramic DIP
DG507ACY	0°C to +70°C	28 Lead SOIC

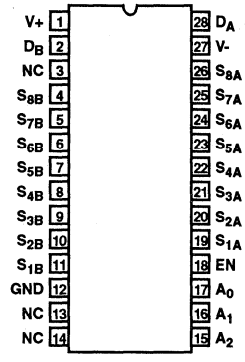
PART NUMBER	TEMP. RANGE	PACKAGE
DG508AAK	-55°C to +125°C	16 Lead Ceramic DIP
DG508AAK/883B	-55°C to +125°C	16 Lead Ceramic DIP
DG508ABK	-25°C to +85°C	16 Lead Ceramic DIP
DG508ABY	-25°C to +85°C	16 Lead Plastic DIP
DG508ACJ	0°C to +70°C	16 Lead Plastic DIP
DG508ACK	0°C to +70°C	16 Lead Ceramic DIP
DG508ACY	0°C to +70°C	16 Lead SOIC (W)
DG509AAK	-55°C to +125°C	16 Lead Ceramic DIP
DG509AAK/883B	-55°C to +125°C	16 Lead Ceramic DIP
DG509ABK	-25°C to +85°C	16 Lead Ceramic DIP
DG509ABY	-25°C to +85°C	16 Lead Plastic DIP
DG509ACJ	0°C to +70°C	16 Lead Plastic DIP
DG509ACK	0°C to +70°C	16 Lead Ceramic DIP
DG509ACY	0°C to +70°C	16 Lead SOIC (W)

Pinouts

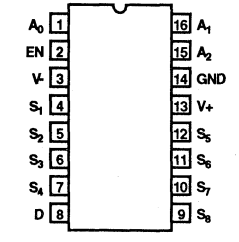
DG506A (PDIP, CDIP, SOIC)
TOP VIEW



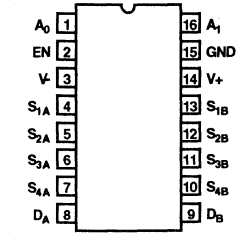
DG507A (PDIP, CDIP, SOIC)
TOP VIEW



DG508A (PDIP, CDIP, SOIC)
TOP VIEW



DG509A (PDIP, CDIP, SOIC)
TOP VIEW

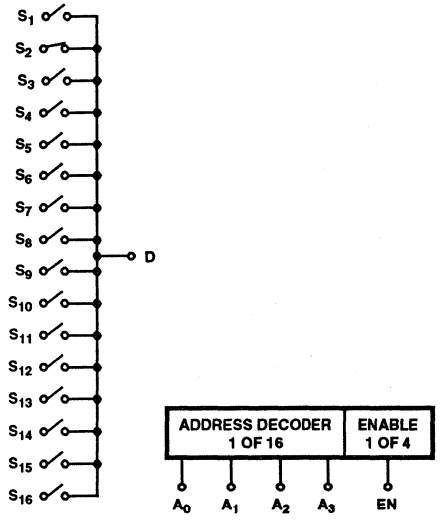


CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3137

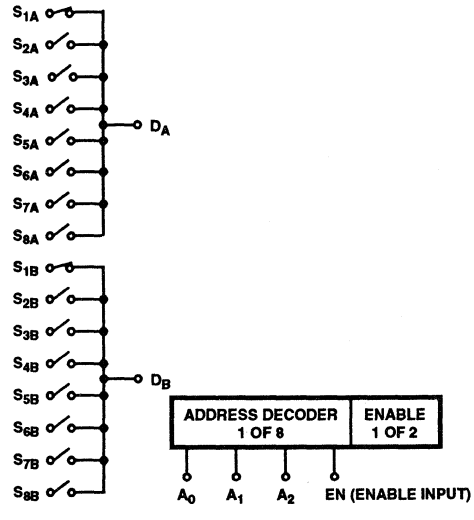
Functional Block Diagrams

DG506A



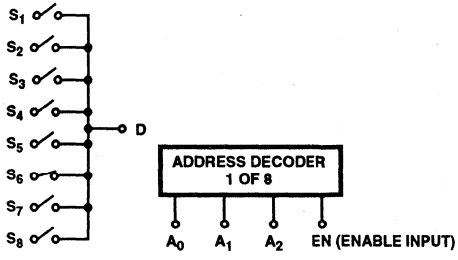
4 Line Binary Address Inputs
(0 0 0 1) and EN = 5V
Above example shows channel 2 turned ON.

DG507A



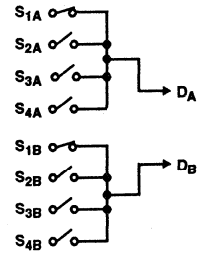
3 Line Binary Address Inputs
(0 0 0) and EN = 5V
Above example shows channels 1_A and 1_B turned ON.

DG508A



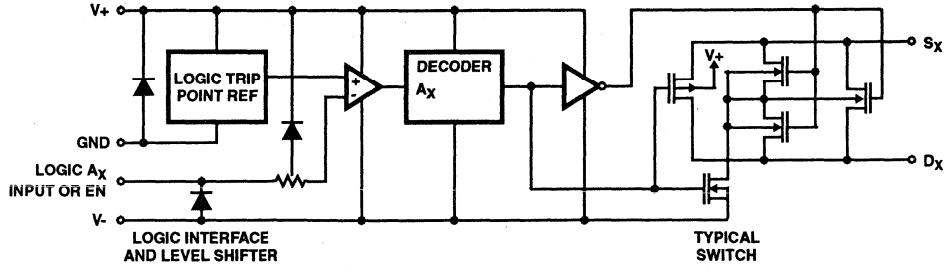
3 Line Binary Address Inputs
(1 0 1) and EN = 1
Above example shows channel 6 turned ON.

DG509A



2 Line Binary Address Inputs
(0 0) and EN = 1
Above example shows channels 1_A and 1_B turned ON.

Schematic Diagram



Absolute Maximum Ratings

V+ to V- 44V
V- to Ground ..... -25V
V_{IN} to Ground (Note 1) ..... (V- -2V), (V+ +2V)
V_S or V_D to V+ (Note 1) ..... +2, (V- -2V)
V_S or V_D to V- (Note 1) ..... -2, (V+ +2V)
Current, any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D (Pulsed at 1ms, 10% Duty Cycle Max.) . 40mA
Storage Temperature
C Suffix ..... -65°C to +125°C
A & B Suffix ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
16 Lead Ceramic DIP Package	77°C/W	23°C/W
28 Lead Ceramic DIP Package	55°C/W	17°C/W
16 Lead Plastic DIP Package	100°C/W	-
28 Lead Plastic DIP Package	60°C/W	-
16 Lead SOIC (W) Package	100°C/W	-
28 Lead SOIC Package	70°C/W	-

Operating Temperature Range
C Suffix ..... 0°C to +70°C
B Suffix ..... -25°C to +85°C
A Suffix ..... -55°C to +125°C
Junction Temperature
Ceramic DIP Package ..... +175°C
Plastic DIP Package ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

T_A = +25°C, V+ = +15V, V- = -15V, GND = 0V, V_{EN} = 2.4V, Unless Otherwise Specified

PARAMETERS	TEST CONDITIONS		DG506AA, DG507AA, DG508AA, DG509AA MIN	(NOTE 2) TYP	MAX	DG506AB/C, DG507AB/C, DG508AB/C, DG509AB/C MIN	(NOTE 2) TYP	MAX	UNITS
DYNAMIC CHARACTERISTICS									
Switching Time of Multiplexer, $t_{TRANSITION}$	See Figure 3		-	0.6	1	-	0.6	-	µs
Break-Before-Make Interval, t_{OPEN}	See Figure 5		-	0.2	-	-	0.2	-	µs
Enable Turn-On Time, $t_{ON(EN)}$	See Figure 4		-	1	1.5	-	1	-	µs
Enable Turn-Off Time, $t_{OFF(EN)}$	See Figure 4		-	0.4	1.0	-	0.4	-	µs
Off Isolation, OIRR	V_{EN} = 0V, R_L = 1kΩ, C_L = 15pF, V_S = $7V_{RMS}$, f = 500kHz (Note 4)		-	68	-	-	68	-	dB
Source Off Capacitance, $C_{S(OFF)}$	V_S = 0V, V_{EN} = 0V, f = 140kHz								
DG506A, DG507A			-	6	-	-	6	-	pF
DG508A, DG509A			-	5	-	-	5	-	pF
Drain Off Capacitance, $C_{D(OFF)}$	V_D = 0V, V_{EN} = 0V, f = 140kHz								
DG506A			-	45	-	-	45	-	pF
DG507A			-	23	-	-	23	-	pF
DG508A			-	25	-	-	25	-	pF
DG509A			-	12	-	-	12	-	pF
Charge Injection, Q	See Figure 6								
DG506A, DG507A			-	6	-	-	6	-	pC
DG508A, DG509A			-	4	-	-	4	-	pC
INPUT									
Address Input Current, Input Voltage High, I_{AH}	V_A = 2.4V		-10	-0.002	-	-10	-0.002	-	µA
	V_A = 15V		-	0.006	10	-	0.006	10	µA
Address Input Current Input Voltage Low, I_{AL}	V_{EN} = 2.4V	V_A = 0V	-10	-0.002	-	-10	-0.002	-	µA
	V_{EN} = 0V		-10	-0.002	-	-10	-0.0002	-	µA

Electrical Specifications T_A = +25°C, V+ = +15V, V- = -15V, GND = 0V, V_{EN} = 2.4V, Unless Otherwise Specified **(Continued)**

PARAMETERS	TEST CONDITIONS		DG506AA, DG507AA, DG508AA, DG509AA MIN	(NOTE 2) TYP	MAX	DG506AB/C, DG507AB/C, DG508AB/C, DG509AB/C MIN	(NOTE 2) TYP	MAX	UNITS
SWITCH									
Analog Signal Range, V_{ANALOG}	(Note 6)		-15	-	+15	-15	-	+15	V
Drain Source On Resistance, $R_{DS(ON)}$	Sequence Each Switch On V_{AL} = 0.8V V_{AH} = 2.4V	I_S = -200µA, V_D = +10V	-	270	400	-	270	450	Ω
		I_S = -200µA, V_D = -10V	-	230	400	-	230	450	Ω
Greatest Change in Drain Source On Resistance Between Channels, $\Delta R_{DS(ON)}$	-10V ≤ V_S ≤ +10V $\Delta R_{DS(ON)} = \frac{R_{DS(ON)MAX} - R_{DS(ON)MIN}}{R_{DS(ON)AVG}}$		-	6	-	-	6	-	%
Source Off Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V	V_S = +10V, V_D = -10V	-1	0.002	1	-5	0.002	5	nA
		V_S = -10V, V_D = +10V	-1	-0.005	1	-5	-0.005	5	nA
Drain Off Leakage Current, $I_{D(OFF)}$	V_{EN} = 0V								
DG506A		V_S = -10V, V_D = +10V	-10	0.02	10	-20	0.02	20	nA
		V_S = +10V, V_D = -10V	-10	-0.03	10	-20	-0.03	20	nA
DG507A		V_S = -10V, V_D = +10V	-5	0.007	5	-10	0.007	10	nA
		V_S = +10V, V_D = -10V	-5	-0.015	5	-10	-0.015	10	nA
DG508A		V_S = -10V, V_D = +10V	-	0.01	10	-	0.01	20	nA
		V_S = +10V, V_D = -10V	-10	-0.015	-	-20	-0.015	-	nA
DG509A		V_S = -10V, V_D = +10V	-	0.005	10	-	0.005	20	nA
		V_S = +10V, V_D = -10V	-10	-0.008	-	-20	-0.008	-	nA
Drain On Leakage Current, $I_{D(ON)}$	(Note 5) Sequence Each Switch On V_{AL} = 0.8V V_{AH} = 2.4V								
DG506A		V_D = $V_{S(ALL)}$ = +10V	-10	0.03	10	-20	0.03	20	nA
		V_D = $V_{S(ALL)}$ = -10V	-10	-0.06	10	-20	-0.06	20	nA
DG507A		V_D = $V_{S(ALL)}$ = +10V	-5	0.015	5	-10	0.015	10	nA
		V_D = $V_{S(ALL)}$ = -10V	-5	-0.03	5	-10	-0.03	10	nA
DG508A		V_D = $V_{S(ALL)}$ = +10V	-	0.015	10	-	0.015	20	nA
		V_D = $V_{S(ALL)}$ = -10V	-10	-0.03	-	-20	-0.03	-	nA
DG509A		V_D = $V_{S(ALL)}$ = +10V	-	0.007	10	-	0.007	20	nA
		V_D = $V_{S(ALL)}$ = -10V	-10	-0.015	-	-20	-0.015	-	nA
POWER SUPPLY CHARACTERISTICS									
Positive Supply Current, I+	V_{EN} = 5.0V, V_A = 0V		-	1.3	2.4	-	1.3	2.4	mA
Negative Supply Current, I-	V_{EN} = 5.0V, V_A = 0V		-1.5	-0.7	-	-1.5	-0.7	-	mA
Positive Supply Current, I+ Standby	V_{EN} = 0V, V_A = 0V		-	1.3	2.4	-	1.3	2.4	mA
Negative Supply Current, I- Standby	V_{EN} = 0V, V_A = 0V		-1.5	-0.7	-	-1.5	-0.7	-	mA

Electrical Specifications T_A = Over Operating Temperature Range, V+ = +15V, V- = -15V, GND = 0V, V_{EN} = 2.4V, Unless Otherwise Specified

PARAMETERS	TEST CONDITIONS		DG506AA, DG507AA, DG508AA, DG509AA			DG506AB/C, DG507AB/C, DG508AB/C, DG509AB/C			UNITS
			MIN	(NOTE 2) TYP	MAX	MIN	(NOTE 2) TYP	MAX	
INPUT									
Address Input Current, Input Voltage High, I_{AH}	V_A = 2.4V		-30	-	-	-30	-	-	µA
	V_A = 15V		-	-	30	-	-	30	µA
Address Input Current Input Voltage Low, I_{AL}	V_{EN} = 2.4V	V_A = 0V	-30	-	-	-30	-	-	µA
	V_{EN} = 0V		-30	-	-	-30	-	-	µA
SWITCHING CHARACTERISTICS									
Analog Signal Range, V_{ANALOG}	(Note 6)		-15	-	+15	-15	-	+15	V
Drain Source On Resistance, $R_{DS(ON)}$	Sequence Each Switch On V_{AL} = 0.8V V_{AH} = 2.4V	I_S = -200µA, V_D = +10V	-	-	500	-	-	550	Ω
		I_S = -200µA, V_D = -10V	-	-	500	-	-	550	Ω
Source Off Leakage Current, $I_{S(OFF)}$	V_{EN} = 0V	V_S = +10V, V_D = -10V	-	-	50	-	-	50	nA
		V_S = -10V, V_D = +10V	-50	-	-	-50	-	-	nA
Drain Off Leakage Current, $I_{D(OFF)}$	V_{EN} = 0V								
DG506A		V_S = -10V, V_D = +10V	-	-	300	-	-	300	nA
		V_S = +10V, V_D = -10V	-300	-	-	-300	-	-	nA
DG507A		V_S = -10V, V_D = +10V	-	-	200	-	-	200	nA
		V_S = +10V, V_D = -10V	-200	-	-	-200	-	-	nA
DG508A		V_S = -10V, V_D = +10V	-	-	200	-	-	200	nA
		V_S = +10V, V_D = -10V	-200	-	-	-200	-	-	nA
DG509A		V_S = -10V, V_D = +10V	-	-	100	-	-	100	nA
		V_S = +10V, V_D = -10V	-100	-	-	-100	-	-	nA
Drain On Leakage Current, $I_{D(ON)}$	(Note 5) Sequence Each Switch On V_{AL} = 0.8V V_{AH} = 2.4V								
DG506A		$V_D = V_{S(ALL)}$ = +10V	-	-	300	-	-	300	nA
		$V_D = V_{S(ALL)}$ = -10V	-300	-	-	-300	-	-	nA
DG507A		$V_D = V_{S(ALL)}$ = +10V	-	-	200	-	-	200	nA
		$V_D = V_{S(ALL)}$ = -10V	-200	-	-	-200	-	-	nA
DG508A		$V_D = V_{S(ALL)}$ = +10V	-	-	200	-	-	200	nA
		$V_D = V_{S(ALL)}$ = -10V	-200	-	-	-200	-	-	nA
DG509A		$V_D = V_{S(ALL)}$ = +10V	-	-	100	-	-	100	nA
		$V_D = V_{S(ALL)}$ = -10V	-100	-	-	-100	-	-	nA

NOTES:

1. Signals on V_S, V_D or V_{IN} exceeding V+ or V- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. The algebraic convention whereby the most negative value is a minimum, and the most positive value is a maximum, is used in this data sheet.
4. Off isolation = 20log $|V_S|/|V_D|$, where V_S = input to Off switch, and V_D = output due to V_S.
5. $I_{D(ON)}$ is leakage from driver into "ON" switch.
6. Parameter not tested. Parameter guaranteed by design or characterization.

Typical Performance Curves

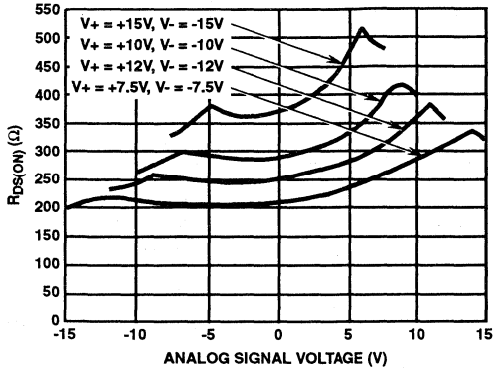


FIGURE 1. $R_{DS(ON)}$ vs ANALOG SIGNAL VOLTAGE vs SUPPLY VOLTAGE

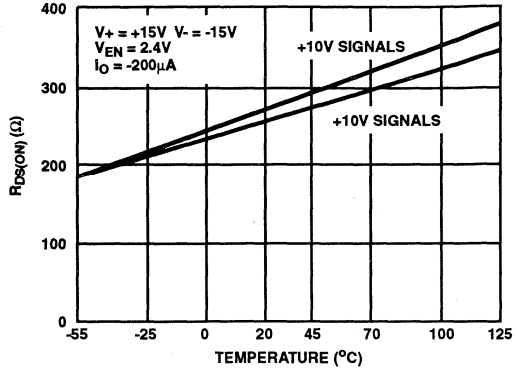
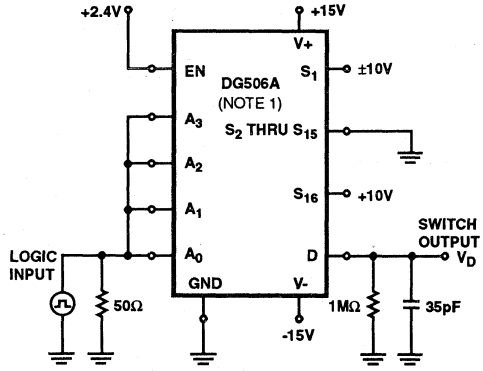
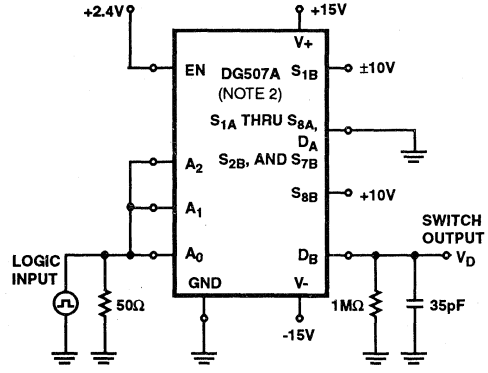


FIGURE 2. TYPICAL $R_{DS(ON)}$ VARIATION WITH TEMPERATURE



NOTE: 1. Similar connections for DG508A

FIGURE 3A. $t_{TRANSITION}$ SWITCHING TIME TEST CIRCUIT



NOTE: 2. Similar connections for DG509A

FIGURE 3B. $t_{TRANSITION}$ SWITCHING TIME TEST CIRCUIT

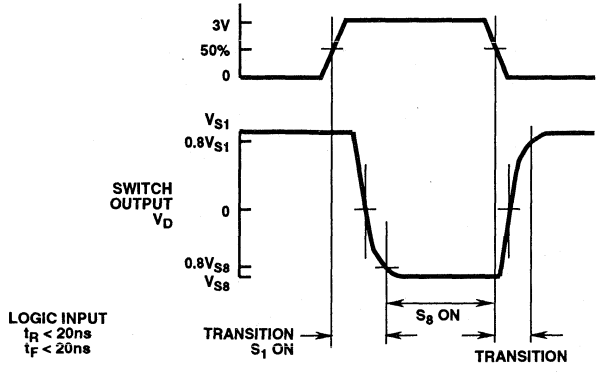
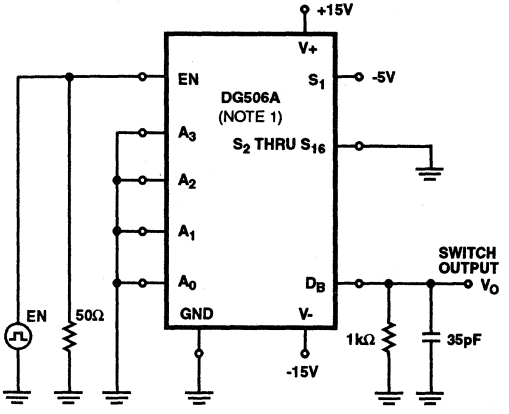


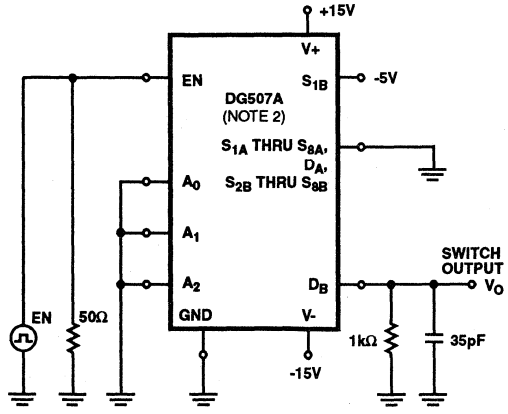
FIGURE 3C. $t_{TRANSITION}$ SWITCHING TIME WAVEFORMS

Typical Performance Curves (Continued)



NOTE: 1. Similar connections for DG508A

FIGURE 4A. ENABLE t_{ON} and t_{OFF} SWITCHING TIME TEST CIRCUIT



NOTE: 2. Similar connections for DG509A

FIGURE 4B. ENABLE t_{ON} and t_{OFF} SWITCHING TIME TEST CIRCUIT

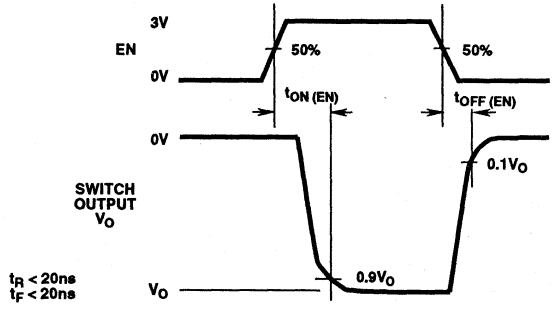
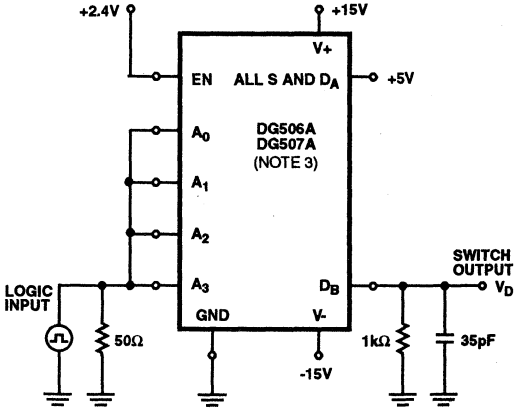


FIGURE 4C. ENABLE t_{ON} and t_{OFF} SWITCHING TIME WAVEFORMS



NOTE: 3. Similar connections for DG508A, DG509A.

FIGURE 5A. t_{OPEN} (BREAK-BEFORE-MAKE) SWITCHING TIME TEST CIRCUIT

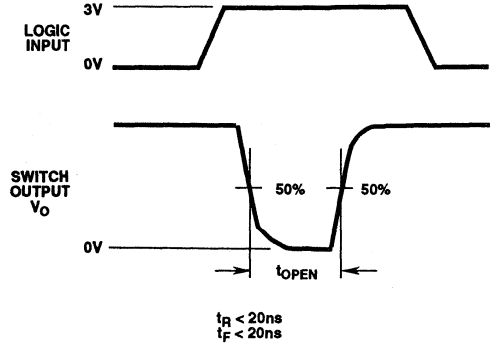
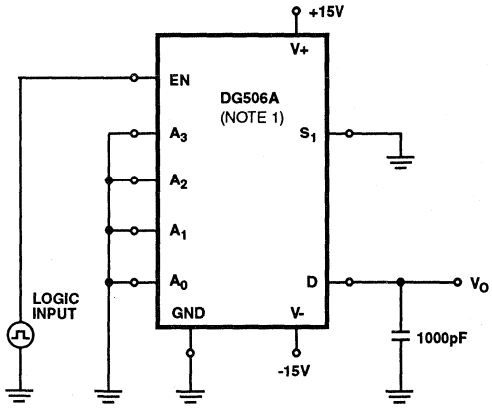


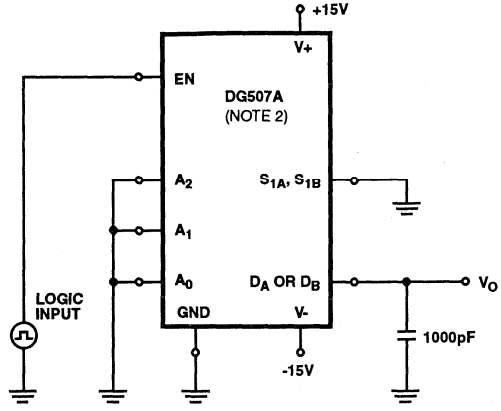
FIGURE 5B. t_{OPEN} (BREAK-BEFORE-MAKE) SWITCHING TIME WAVEFORMS

Typical Performance Curves (Continued)



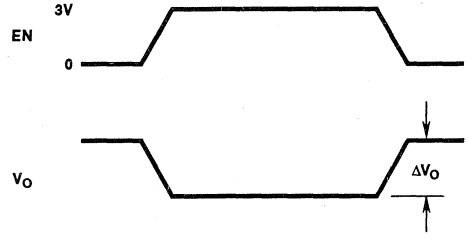
NOTE: 1. Similar connections for DG508A

FIGURE 6A. CHARGE INJECTION TEST CIRCUIT



NOTE: 2. Similar connections for DG509A

FIGURE 6B. CHARGE INJECTION TEST CIRCUIT



ΔV_O is the measured voltage error due to charge injection.
The error voltage in Coulombs is $Q = C_L \times \Delta V_O$.

FIGURE 6C. CHARGE INJECTION WAVEFORMS

Truth Tables

DG506A

A_3	A_2	A_1	A_0	EN	ON SWITCH
X	X	X	X	0	None
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "0" = V_{AL}, $V_{ENL} \leq 0.8V$, Logic "1" = V_{AH}, $V_{ENH} \geq 2.4V$.

DG507A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Logic "0" = V_{AL}, $V_{ENL} \leq 0.8V$, Logic "1" = V_{AH}, $V_{ENH} \geq 2.4V$.

DG508A

A_2	A_1	A_0	EN	ON SWITCH
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2, EN
Logic "1" = $V_{AH} \geq 2.4V$, Logic "0" = $V_{AL} \leq 0.8V$

DG509A

A_1	A_0	EN	ON SWITCH
X	X	0	None
0	0	1	1A, 1B
0	1	1	2A, 2B
1	0	1	3A, 3B
1	1	1	4A, 4B

A_0, A_1, EN
Logic "1" = $V_{AH} \geq 2.4V$, Logic "0" = $V_{AL} \leq 0.8V$

Die Characteristics

DIE DIMENSIONS:
3810µm x 2770µm

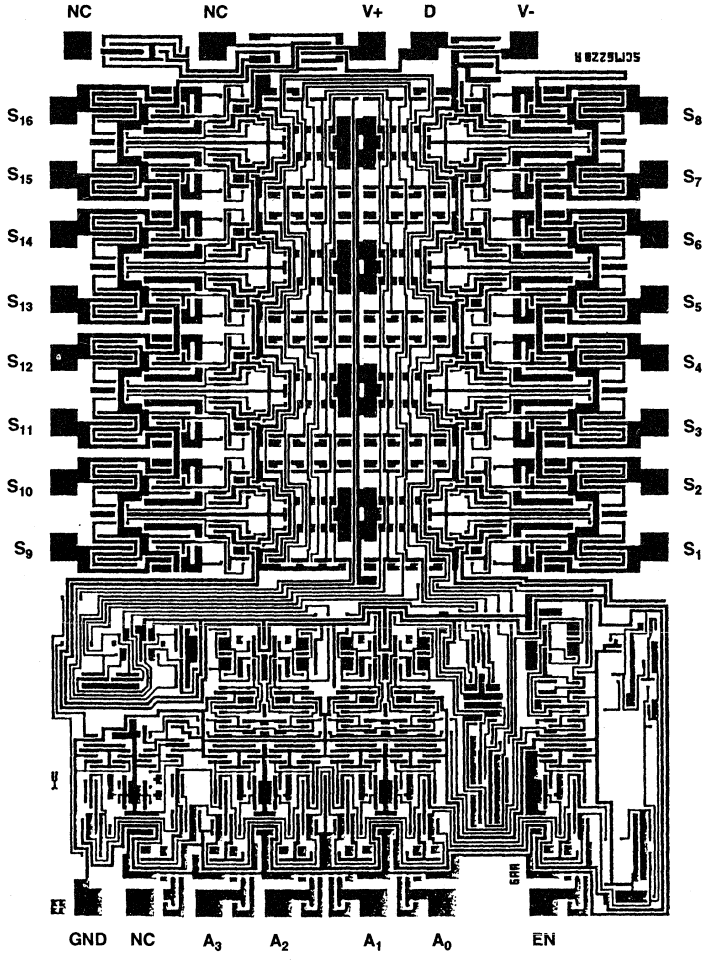
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
Thickness: PSG: 7kÅ ± 1.4kÅ, Nitride: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG506A



Die Characteristics

DIE DIMENSIONS:
3810µm x 2770µm

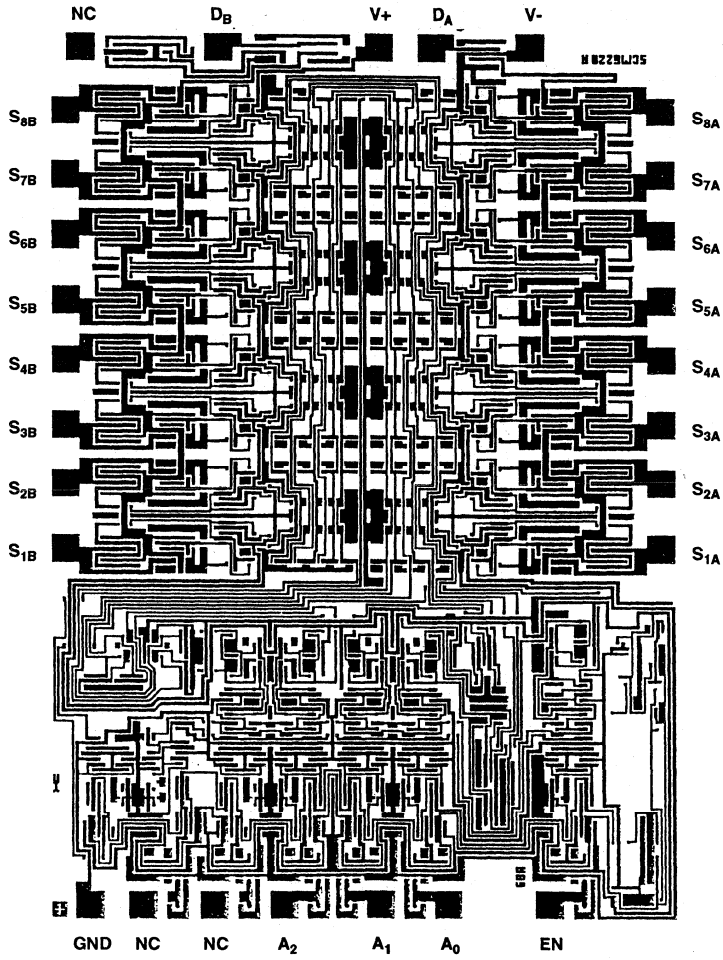
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
Thickness: PSG: 7kÅ ± 1.4kÅ, Nitride: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG507A



Die Characteristics

DIE DIMENSIONS:
3100µm x 2083µm

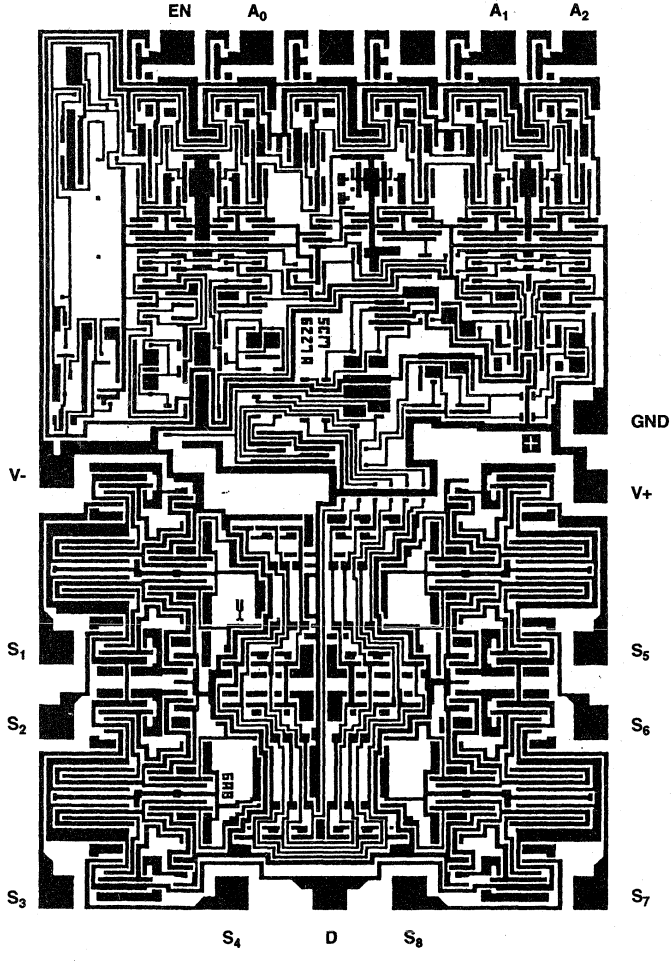
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
Thickness: PSG: 7kÅ ± 1.4kÅ, Nitride: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG508A



Die Characteristics

DIE DIMENSIONS:
3100µm x 2083µm

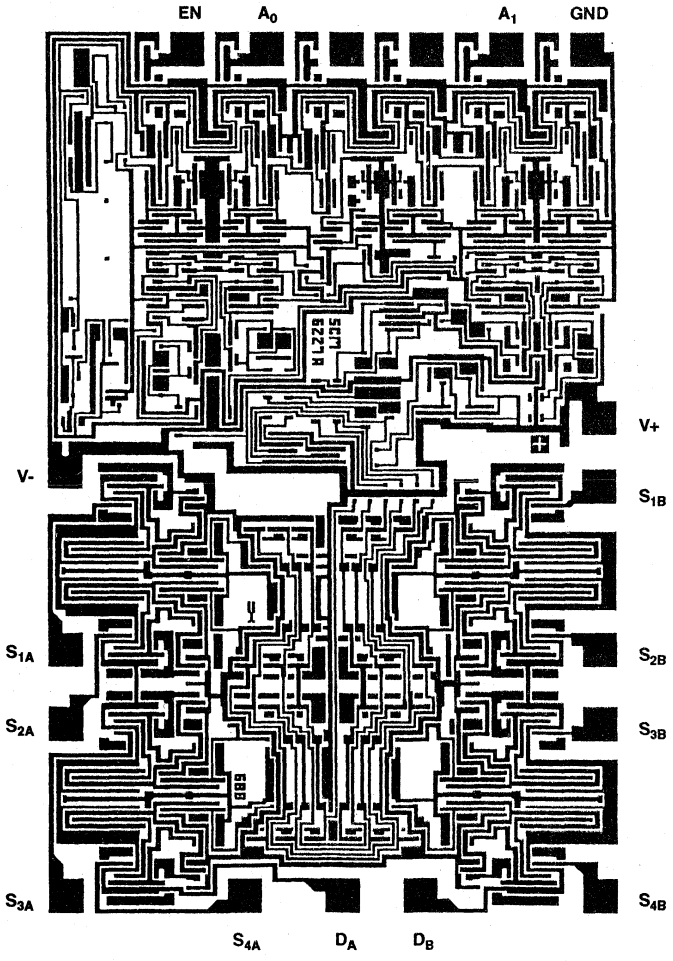
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
Thickness: PSG: 7kÅ ± 1.4kÅ, Nitride: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG509A



HARRIS SEMICONDUCTOR

DG526, DG527 DG528, DG529

December 1993

Analog CMOS Latchable Multiplexers

Features

- Direct RESET
- TTL and CMOS Compatible Address and Enable Inputs
- 44V Maximum Power Supply Rating
- Break-Before-Make Switching
- Alternate Source

Applications

- Data Acquisition Systems
- Communication Systems
- Automatic Test Equipment
- Microprocessor Controlled System

Description

The DG526, DG527, DG528, and DG529 are CMOS monolithic 16 channel/dual 4 channel analog multiplexers. Each device has on-chip address and control latches to simplify design in microprocessor based applications. The DG526 uses 4 address lines to control its 16 channels; the DG527, DG528 both use 3 address lines to control their 8 channels; and the DG529 uses 2 address lines to control its 4 channels. The enable pin is used to enable the address latches during the $\overline{WR}$ pulse. It can be hard wired to the logic supply if one of the channels will always be used (except during a reset) or it can be tied to address decoding circuitry for memory mapped operation. The $\overline{RS}$ pin is used to clear all latches regardless of the state of any other latch or control line. The $\overline{WR}$ pin is used to transfer the state of the address control lines to their latches, except during a reset or when EN is low.

A channel in the ON state conducts signals equally well in both directions. In the OFF state each channel blocks voltages up to the supply rails. The address inputs, $\overline{WR}$, $\overline{RS}$ and the enable input are TTL and CMOS compatible over the full specified operation temperature range.

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
DG526AK	-55°C to +125°C	28 Lead Ceramic DIP
DG526AK/883B	-55°C to +125°C	28 Lead Ceramic DIP
DG526BK	-25°C to +85°C	28 Lead Ceramic DIP
DG526BY	-25°C to +85°C	28 Lead Plastic SOIC
DG526CJ	0°C to +70°C	28 Lead Plastic DIP
DG526CK	0°C to +70°C	28 Lead Ceramic DIP
DG526CY	0°C to +70°C	28 Lead Plastic SOIC
DG527AK	-55°C to +125°C	28 Lead Ceramic DIP
DG527AK/883B	-55°C to +125°C	28 Lead Ceramic DIP
DG527BK	-25°C to +85°C	28 Lead Ceramic DIP
DG527BY	-25°C to +85°C	28 Lead Plastic SOIC
DG527CJ	0°C to +70°C	28 Lead Plastic DIP
DG527CK	0°C to +70°C	28 Lead Ceramic DIP
DG527CY	0°C to +70°C	28 Lead Plastic SOIC

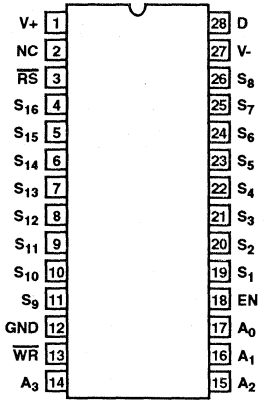
PART NUMBER	TEMPERATURE	PACKAGE
DG528AK	-55°C to +125°C	18 Lead Ceramic DIP
DG528AK/883B	-55°C to +125°C	18 Lead Ceramic DIP
DG528BK	-25°C to +85°C	18 Lead Ceramic DIP
DG528BY	-25°C to +85°C	18 Lead Plastic SOIC
DG528CJ	0°C to +70°C	18 Lead Plastic DIP
DG528CK	0°C to +70°C	18 Lead Ceramic DIP
DG528CY	0°C to +70°C	18 Lead Plastic SOIC
DG529AK	-55°C to +125°C	18 Lead Ceramic DIP
DG529AK/883B	-55°C to +125°C	18 Lead Ceramic DIP
DG529BK	-25°C to +85°C	18 Lead Ceramic DIP
DG529BY	-25°C to +85°C	18 Lead Plastic SOIC
DG529CJ	0°C to +70°C	18 Lead Plastic DIP
DG529CK	0°C to +70°C	18 Lead Ceramic DIP
DG529CY	0°C to +70°C	18 Lead Plastic SOIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

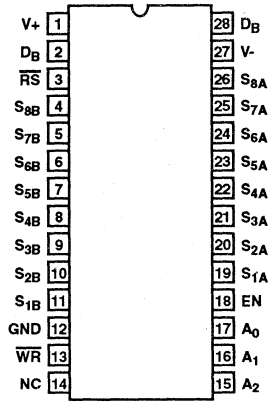
File Number **3139**

Pinouts

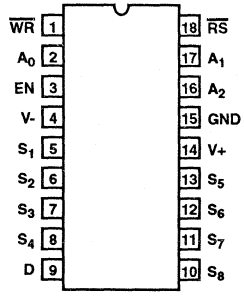
DG526
(PDIP, SOIC)
TOP VIEW



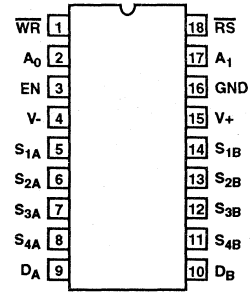
DG527
(PDIP, SOIC)
TOP VIEW



DG528
(PDIP, SOIC)
TOP VIEW

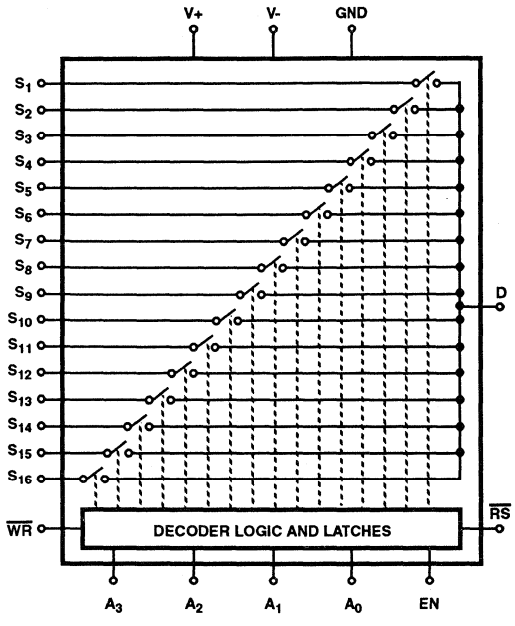


DG529
(PDIP, SOIC)
TOP VIEW

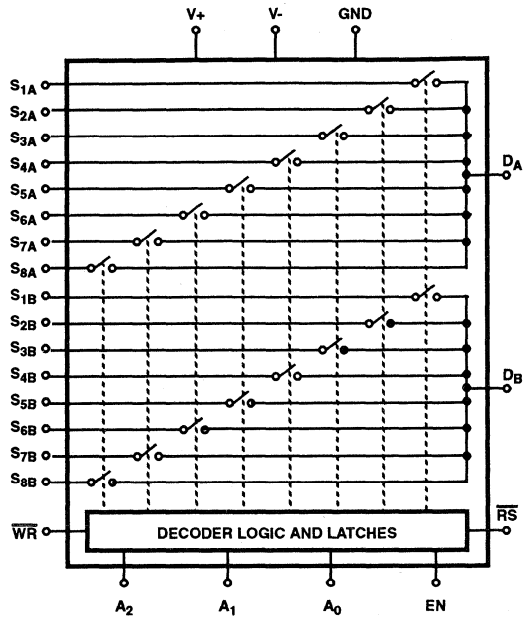


Functional Diagrams

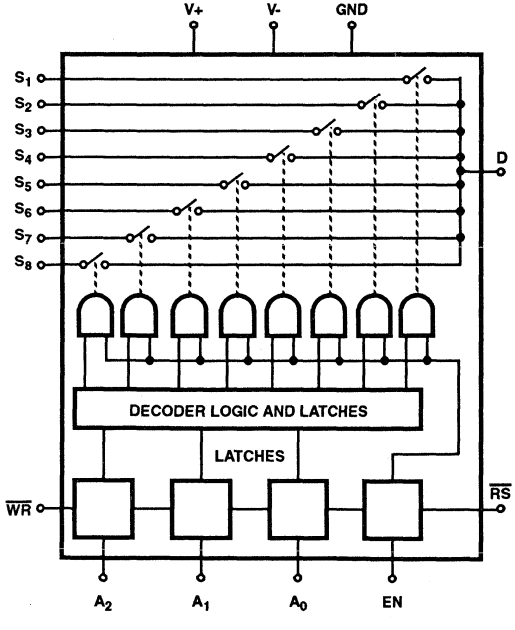
DG526
16 CHANNEL SINGLE ENDED MULTIPLEXER



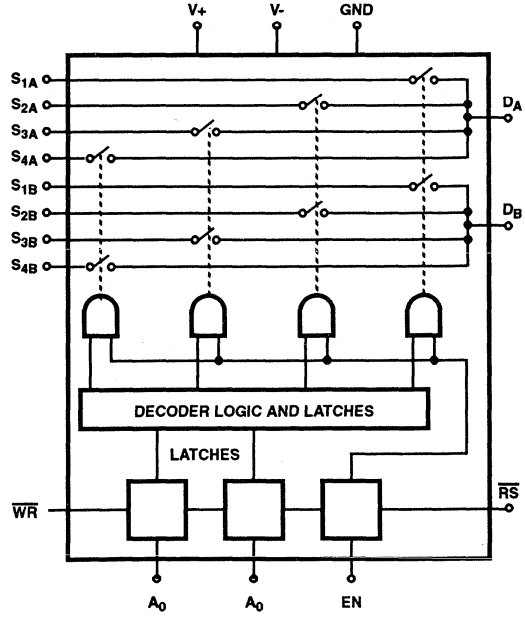
DG527
DIFFERENTIAL 8 CHANNEL MULTIPLEXER



DG528
8 CHANNEL SINGLE ENDED MULTIPLEXER

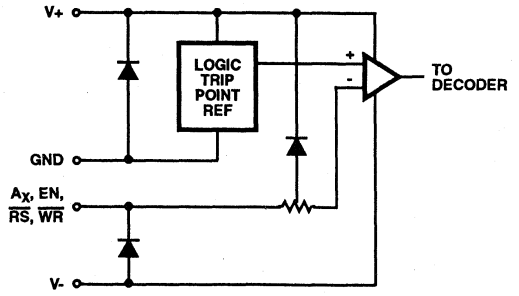


DG529
DUAL 4 CHANNEL MULTIPLEXER

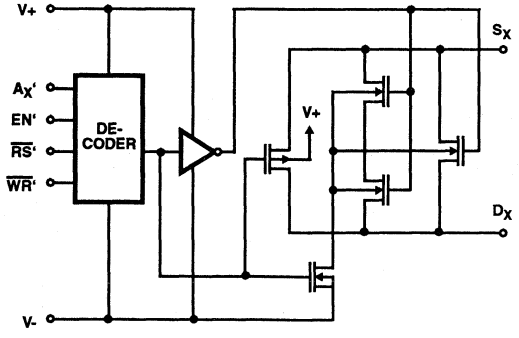


Schematic Diagrams

LOGIC INTERFACE AND LEVEL SHIFTER



DECODER AND SWITCH



Absolute Maximum Ratings

V+ to V- ..... +44V
V- to Ground ..... -25V
V_{IN} to Ground (Note 1) ..... (V- - 2V), (V+ + 2V)
V_S or V_D to V+ (Note 1) ..... +2V, (V- - 2V)
V_S or V_D to V- (Note 1) ..... -2V, (V+ + 2V)
Current, Any Terminal Except S or D 30mA
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed at 1ms, 10% Duty Cycle Max)
Storage Temperature Range
C Suffix ..... -65°C to +125°C
A and B Suffix ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
18 Lead Plastic DIP Package	90°C/W	-
18 Lead Ceramic DIP Package	75°C/W	22°C/W
18 Lead SOIC Package	95°C/W	-
28 Lead Plastic DIP Package	60°C/W	-
28 Lead Ceramic DIP Package	55°C/W	17°C/W
28 Lead SOIC Package	70°C/W	-

Operating Temperature
C Suffix ..... 0°C to +70°C
B Suffix ..... -25°C to +85°C
A Suffix ..... -55°C to +125°C
Junction Temperature
Ceramic Package ..... +175°C
Plastic Packages ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

(Note 3) V+ = +15V, V- = -15V, GND = 0V, WR = 0V, RS = 2.4V, EN = 2.4V, T_A = +25°C, Unless Otherwise Specified

PARAMETER		(NOTE 6) TEST CONDITIONS		A SUFFIX MIN	A SUFFIX (NOTE 2) TYP	A SUFFIX MAX	B AND C SUFFIX MIN	B AND C SUFFIX (NOTE 2) TYP	B AND C SUFFIX MAX	UNITS
DYNAMIC										
Switching Time of Multiplexer, $t_{TRANSITION}$	DG526, DG527	See Figure 3 (Note 7)		-	0.65	1	-	0.65	-	µs
	DG528, DG529	See Figure 3		-	0.6	1	-	0.6	-	µs
Break-Before-Make Interval, t_{OPEN}	DG526, DG527	See Figure 4		-	0.2	-	-	0.2	-	µs
	DG528, DG529			-	0.2	-	-	0.2	-	µs
Enable and Write Turn-ON Time, t_{ON} (EN, $\overline{WR}$)	DG526, DG527	See Figures 1, 6 (Note 7)		-	0.7	1.5	-	0.7	-	µs
	DG528, DG529	See Figures 5, 6 (Note 7)		-	1	1.5	-	1	-	µs
Enable and Reset Turn OFF Time, t_{OFF} (EN, $\overline{RS}$)	DG526, DG527	See Figures 2, 7 (Note 7)		-	0.4	1	-	0.4	-	µs
	DG528, DG529	See Figures 5, 6 (Note 7)		-	0.4	1	-	0.4	-	µs
Off Isolation, OIRR	DG526, DG527	V_{EN} = 0V, R = 1kΩ, C_L = 15pF, V_S = 7V_{RMS}, f = 500kHz (Note 4)		-	55	-	-	55	-	dB
	DG528, DG529			-	68	-	-	68	-	dB
Logic Input Capacitance, C_{IN}	DG526, DG527	f = 1MHz		-	6	-	-	6	-	pF
	DG528, DG529			-	2.5	-	-	2.5	-	pF
Source OFF Capacitance, $C_{S(OFF)}$	DG526, DG527	V_S = 0V	V_{EN} = 0V, f = 140kHz	-	10	-	-	10	-	pF
	DG528, DG529			-	5	-	-	5	-	pF

Electrical Specifications (Note 3) V+ = +15V, V- = -15V, GND = 0V, WR = 0V, RS = 2.4V, EN = 2.4V, T_A = +25°C, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 6) TEST CONDITIONS		A SUFFIX MIN	A SUFFIX (NOTE 2) TYP	A SUFFIX MAX	B AND C SUFFIX MIN	B AND C SUFFIX (NOTE 2) TYP	B AND C SUFFIX MAX	UNITS
Drain OFF Capacitance, $C_{D(OFF)T}$	DG526	V_D = 0V	V_{EN} = 0V, f = 140kHz	-	65	-	-	65	-	pF
	DG527			-	35	-	-	35	-	pF
	DG528			-	25	-	-	25	-	pF
	DG529			-	12	-	-	12	-	pF
Charge Injection, Q	DG526, DG527	See Figure 8		-	6	-	-	6	-	pC
	DG528, DG529			-	4	-	-	4	-	pC
INPUT										
Address Input Current, Input Voltage High, I_{AH}	DG526, DG527	V_A = 2.4V		-10	0.02	-	-10	0.02	-	µA
		V_A = 15V		-	0.02	10	-	0.02	10	µA
	DG528, DG529	V_A = 2.4V		-10	-0.002	-	-10	-0.002	-	µA
		V_A = 15V		-	0.006	10	-	0.006	10	µA
Address Input Current, Input Voltage Low, I_{AL}	DG526 DG527	V_{EN} = 2.4V	All V_A = 0V, $\overline{RS}$ = 0V, $\overline{WR}$ = 0V	-10	0.01	-	-10	0.01	-	µA
		V_{EN} = 0V		-10	0.01	-	-10	0.01	-	µA
	DG528 DG529	V_{EN} = 2.4V		-10	-0.002	-	-10	-0.002	-	µA
		V_{EN} = 0V		-10	-0.002	-	-10	-0.002	-	µA
SWITCH										
Analog Signal Range, $V_{ANA:LOG}$		(Note 7)		-15	-	+15	-15	-	+15	V
Drain Source ON Resistance, $R_{DS(ON)}$		V_D = ± 10V, V_{AL} = 0.8V, V_{AH} = 2.4V, I_L = -200µA Sequence Each Switch ON		-	270	400	-	270	450	Ω
Greatest Change in Drain Source ON Resistance Between Channels, $\Delta R_{DS(ON)}$		-10V ≤ V_S ≤ 10V $\Delta R_{DS(ON)} = \frac{R_{DS(ON)MAX} - R_{DS(ON)MIN}}{R_{DS(ON)AVG.}}$		-	6	-	-	6	-	%
Source OFF Leakage Current, $I_{S(OFF)}$	DG526, DG527	V_{EN} = 0V	V_S = ±10V, V_D = ∓10V	-1	0.02	1	-	0.02	-	nA
	DG528, DG529		V_S = ±10V, V_D = ∓10V	-1	-0.005	1	-5	-0.005	5	nA
Drain OFF Leakage Current, $I_{D(OFF)}$	DG526	V_{EN} = 0V	V_S = ±10V, V_D = ∓10V	-10	0.2	10	-	0.2	-	nA
	DG527		V_S = ±10V, V_D = ∓10V	-5	0.2	5	-	0.2	-	nA
	DG528		V_S = ±10V, V_D = ∓10V	-10	-0.015	10	-20	0.015	20	nA
	DG529		V_S = ±10V, V_D = ∓10V	-10	-0.008	10	-20	0.008	20	nA
Drain ON Leakage Current, $I_{D(ON)}$	DG526	Sequence Each Switch On V_{AL} = 0.8V and V_{AH} = 2.4V (Note 5)	$V_D = V_{S(ALL)}$ = ±10V	-10	0.2	10	-	0.2	-	nA
	DG527		$V_D = V_{S(ALL)}$ = ±10V	-5	0.2	5	-	0.2	-	nA

Electrical Specifications (Note 3) V+ = +15V, V- = -15V, GND = 0V, WR = 0V, RS = 2.4V, EN = 2.4V, T_A = +25°C, Unless Otherwise Specified **(Continued)**

PARAMETER		(NOTE 6) TEST CONDITIONS		A SUFFIX MIN	A SUFFIX (NOTE 2) TYP	A SUFFIX MAX	B AND C SUFFIX MIN	B AND C SUFFIX (NOTE 2) TYP	B AND C SUFFIX MAX	UNITS
Drain ON Leakage Current, $I_{D(ON)}$ (Continued)	DG528	Sequence Each Switch On V_{AL} = 0.8V and V_{AH} = 2.4V (Note 5)	$V_D = V_{S(ALL)}$ = ±10V	-10	-0.03	10	-20	-0.03	20	nA
	DG529		$V_D = V_{S(ALL)}$ = ±10V	-10	-0.015	10	-20	-0.015	20	nA
SUPPLY										
Positive Supply Current, I+	DG526, DG527	V_{EN} = 0V	All V_A = 0V	-	2.0	3.0	-	2.0	-	mA
	DG528, DG529			-	-	2.5	-	-	-2.5	mA
Positive Supply Current, I-	DG526, DG527	V_{EN} = 0V	All V_A = 0V	-2.0	-1.2	-	-	-1.2	-	mA
	DG528, DG529			-1.5	-	-	-1.5	-	-	mA

Electrical Specifications T_A = Over Operating Temperature Range, V+ = +15V, V- = -15V, GND = 0V, WR = 0V, RS = 2.4V, EN = 2.4V Unless Otherwise Specified

PARAMETER		(NOTE 6) TEST CONDITIONS		A SUFFIX MIN	A SUFFIX (NOTE 2) TYP	A SUFFIX MAX	B AND C SUFFIX MIN	B AND C SUFFIX (NOTE 2) TYP	B AND C SUFFIX MAX	UNITS
INPUT										
Address Input Current Input Voltage High, I_{AH}		V_A = 2.4V		-30	-	-	-30	-	-	µA
		V_A = 15V		-	-	30	-	-	30	µA
Address Input Current, Input Voltage Low, I_{AL}	DG526, DG527	V_A = 2.4V	$V_{A(ALL)}$=0V, $\overline{RS}$ = 0V, $\overline{WR}$ = 0V	-10	-	-	-	-	-	µA
		V_A = 0V		-10	-	-	-	-	-	µA
	DG528, DG529			-30	-	-	-30	-	-	µA
		V_A = 0V		-30	-	-	-30	-	-	µA
SWITCH										
Analog Signal Range, V_{ANALOG}		Note 7		-15	-	+15	-	-	-	%
Drain Source ON Resistance, $R_{DS(ON)}$		V_D = ±10V, V_{AL} = 0.8V, V_{AH} = 2.4V, I_S = -200µA, Sequence Each Switch ON		-	-	500	-	-	500	Ω
Source Off Leakage Current, $I_{S(OFF)}$		V_{EN} = 0V	V_S = ±10V, V_D = ∓ 10V	-50	-	50	-	-	-	nA
Drain OFF Leakage Current, $I_{D(OFF)}$	DG526	V_{EN} = 0V	V_S = ±10V, V_D = ∓ 10V	-300	-	300	-300	-	300	nA
	DG527			-200	-	200	-200	-	200	nA
	DG528		V_S = ∓10V, V_D = ±10V	-200	-	200	-200	-	200	nA
	DG529			-100	-	100	-100	-	100	nA
Drain ON Leakage Current, $I_{D(ON)}$	DG526	Sequence Each Switch On, V_{AL} = 0.8V, V_{AH} = 2.4V (Note 5)	$V_D = V_{S(ALL)}$ = ±10V	-300	-	300	-300	-	300	nA
	DG527			-200	-	200	-200	-	200	nA
	DG528			-200	-	200	-200	-	200	nA
	DG529			-100	-	100	-100	-	100	nA

Minimum Input Timing Requirements Over Full Temperature Range

PARAMETER	MEASURED TERMINAL	MIN.	UNITS
WRITE Pulse Width, t_{WW}	$\overline{WR}$, See Figure 1	300	ns
A, EN Data Valid After WRITE (Stabilization Time), t_{DW}	A_0, A_1, (A_2), EN, $\overline{WR}$; See Figure 1	180	ns
A, EN Data Valid After WRITE (Hold Time), t_{WD}	A_0, A_1, (A_2), EN, $\overline{WR}$; See Figure 1	30	ns
RESET Pulse Width, $t_{\overline{RS}}$	$\overline{RS}$, (Note 6), V_S = 5V, See Figure 2	500	ns

NOTES:

1. Signals on V_S, V_D or V_{IN} exceeding V+ or V- will be clamped by internal diodes. Limit diode forward current to maximum current ratings.
2. Typical values are for design aid only, not guaranteed and not subject to production testing.
3. The algebraic convention whereby the most negative value is a minimum, and most positive value is a maximum, is used in this datasheet.
4. $\text{OFFisolation} = 20\dfrac{|V_S|}{|V_D|}$, where V_S = input to OFF switch, and V_D = output due to V_S.
5. $I_{D(ON)}$ is leakage from driver into "ON" switch.
6. Period of Reset ($\overline{RS}$) pulse must be at least 50µs during or after power ON.
7. Parameter not tested. Parameter guaranteed by design or characterization.

Waveforms and Test Circuits

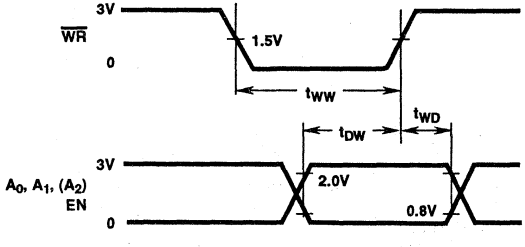


FIGURE 1. $\overline{WR}$ TIMING WAVEFORMS

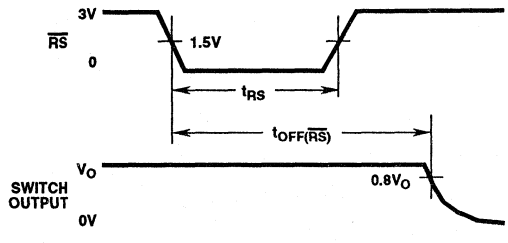


FIGURE 2. $\overline{RS}$ TIMING WAVEFORMS

Waveforms and Test Circuits (Continued)

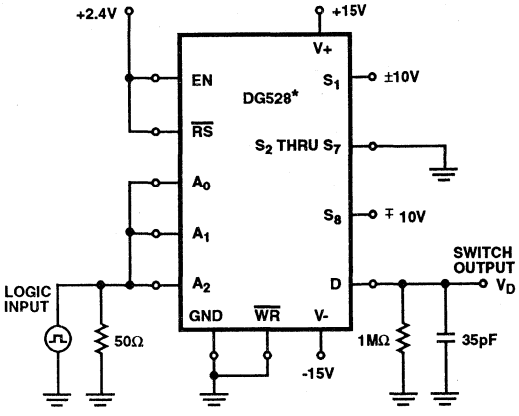


FIGURE 3A. $t_{TRANSITION}$ SWITCHING TIME TEST CIRCUIT

* Similar connections for DG526

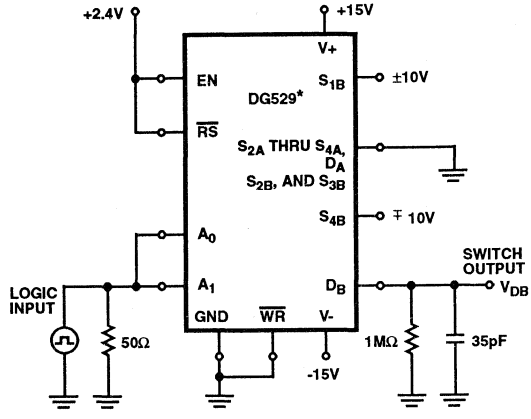


FIGURE 3B. $t_{TRANSITION}$ SWITCHING TIME TEST CIRCUIT

* Similar connections for DG527

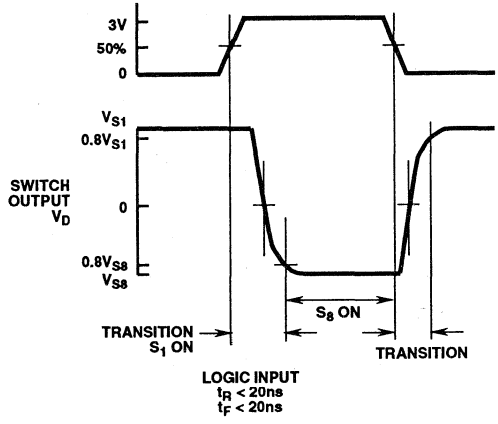


FIGURE 3C. $t_{TRANSITION}$ SWITCHING TIME WAVEFORM

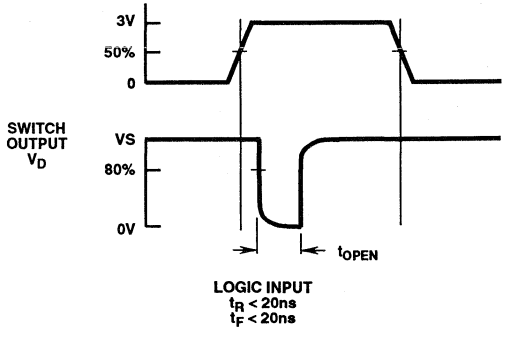


FIGURE 4A. t_{OPEN} (BREAK-BEFORE-MAKE) SWITCHING TIME WAVEFORM

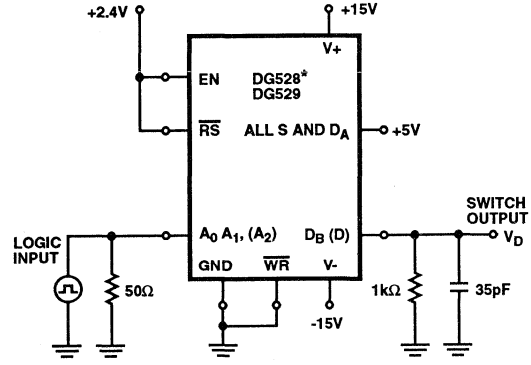


FIGURE 4B. t_{OPEN} (BREAK-BEFORE-MAKE) SWITCHING TIME TEST CIRCUIT

* Similar connections for DG526, DG527

Waveforms and Test Circuits (Continued)

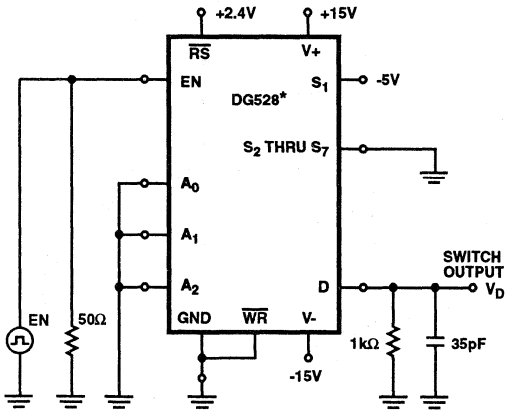


FIGURE 5A. ENABLE t_{ON} AND t_{OFF} SWITCHING TIME TEST CIRCUIT

* Similar connections for DG526

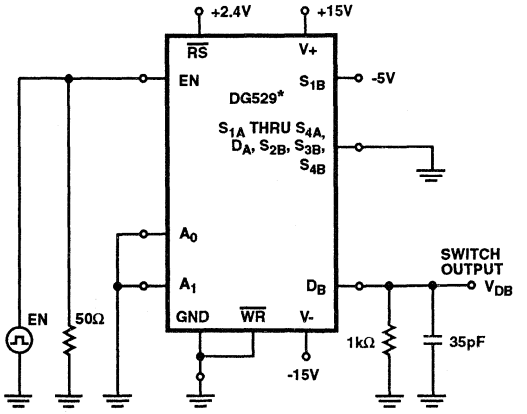


FIGURE 5B. ENABLE t_{ON} AND t_{OFF} SWITCHING TIME TEST CIRCUIT

* Similar connections for DG527

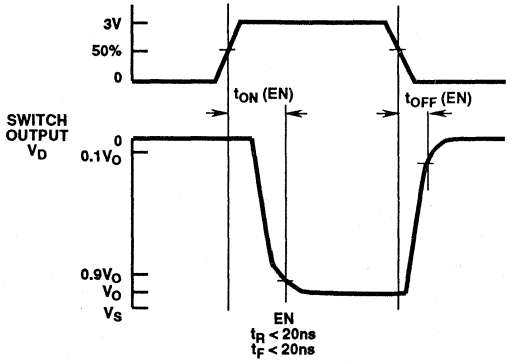
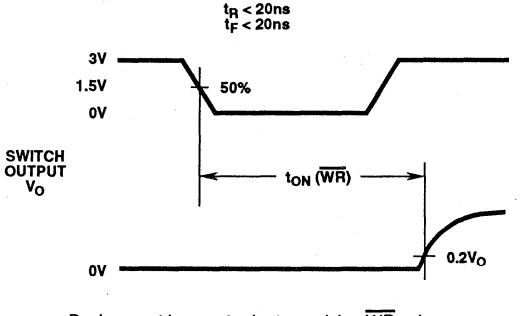


FIGURE 5C. ENABLE t_{ON} AND t_{OFF} SWITCHING TIME WAVEFORMS



Device must be reset prior to applying $\overline{WR}$ pulse.

FIGURE 6A. WRITE t_{ON} SWITCHING TIME WAVEFORMS

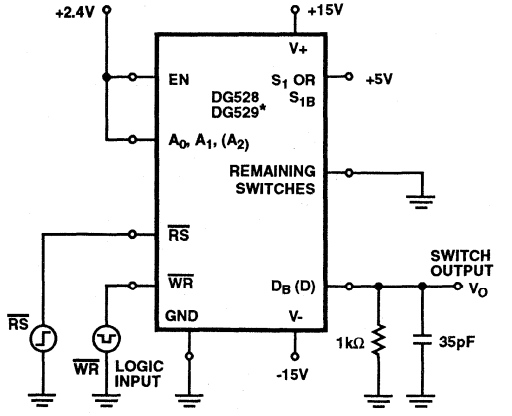


FIGURE 6B. WRITE t_{ON} SWITCHING TIME TEST CIRCUIT

* Similar connections for DG526, DG527

Waveforms and Test Circuits (Continued)

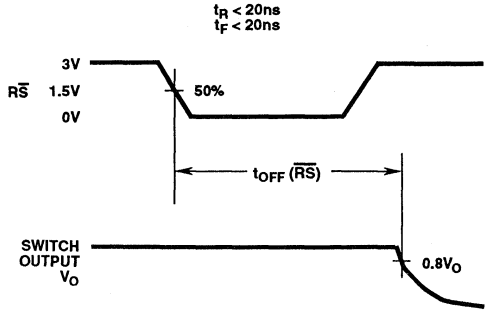


FIGURE 7A. RESET t_{OFF} SWITCHING TIME WAVEFORMS

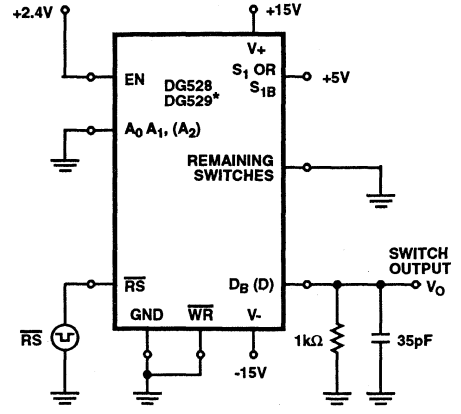
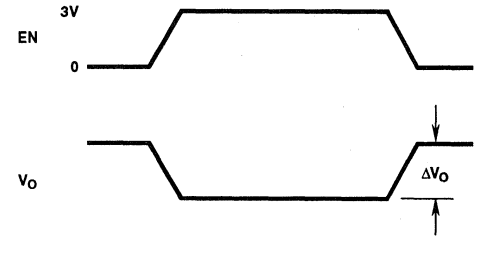


FIGURE 7B. RESET t_{OFF} SWITCHING TIME TEST CIRCUIT

* Similar connections for DG526, DG527



ΔV_O is the measured voltage error due to charge injection. The error voltage in Coulombs is $Q = C_L \times \Delta V_O$.

FIGURE 8A. CHARGE INJECTION WAVEFORMS

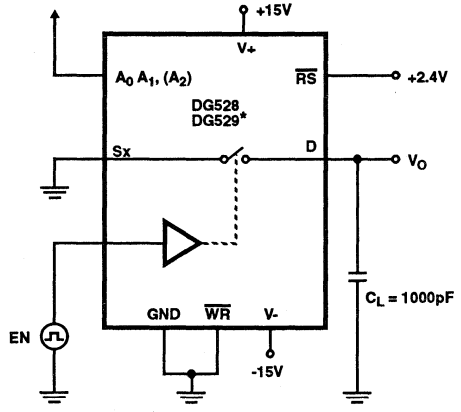


FIGURE 8B. CHARGE INJECTION TEST CIRCUIT

* Similar connections for DG526, DG527

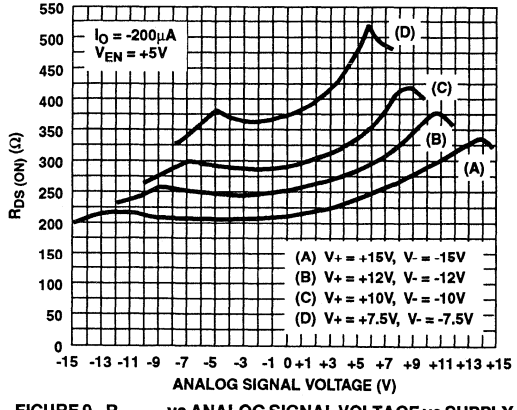


FIGURE 9. $R_{DS(ON)}$ vs ANALOG SIGNAL VOLTAGE vs SUPPLY VOLTAGE

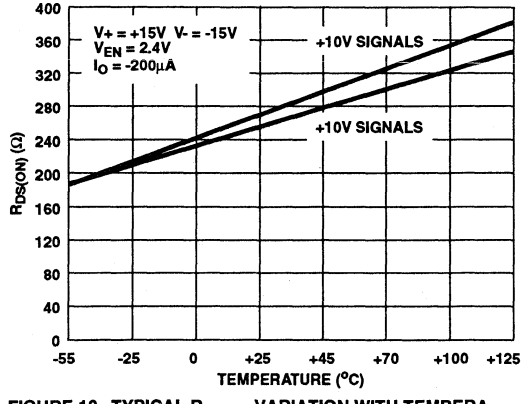


FIGURE 10. TYPICAL $R_{DS(ON)}$ VARIATION WITH TEMPERATURE

Truth Tables

DG526

	A_3	A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching	X	X	X	X	X	↗	1	Maintains Previous Switch State
Reset	X	X	X	X	X	X	0	None (Latches Cleared)
Transparent Operation	X	X	X	X	0	0	1	None
	0	0	0	0	1	0	1	1
	0	0	0	1	1	0	1	2
	0	0	1	0	1	0	1	3
	0	0	1	1	1	0	1	4
	0	1	0	0	1	0	1	5
	0	1	0	1	1	0	1	6
	0	1	1	0	1	0	1	7
	0	1	1	1	1	0	1	8
	1	0	0	0	1	0	1	9
	1	0	0	1	1	0	1	10
	1	0	1	0	1	0	1	11
	1	0	1	1	1	0	1	12
	1	1	0	0	1	0	1	13
	1	1	0	1	1	0	1	14
	1	1	1	0	1	0	1	15
	1	1	1	1	1	0	1	16

Logic "0" = V_{AL}, $V_{ENL} \leq 0.8V$

DG527

	A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
Latching	X	X	X	X	↗	1	Maintains Previous Switch State
Reset	X	X	X	X	X	0	None (Latches Cleared)
Transparent Operation	X	X	X	0	0	1	None
	0	0	0	1	0	1	1
	0	0	1	1	0	1	2
	0	1	0	1	0	1	3
	0	1	1	1	0	1	4
	1	0	0	1	0	1	5
	1	0	1	1	0	1	6
	1	1	0	1	0	1	7
	1	1	1	1	0	1	8

Logic "1" = V_{AH}, $V_{ENH} \geq 2.4V$

DG528

A_2	A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	X	↗	1	Maintains Previous Switch Condition
X	X	X	X	X	0	None (Latches Cleared)
X	X	X	0	0	1	None
0	0	0	1	0	1	1
0	0	1	1	0	1	2
0	1	0	1	0	1	3
0	1	1	1	0	1	4
1	0	0	1	0	1	5
1	0	1	1	0	1	6
1	1	0	1	0	1	7
1	1	1	1	0	1	8

DG529

A_1	A_0	EN	$\overline{WR}$	$\overline{RS}$	ON SWITCH
X	X	X	↗	1	Maintains Previous Switch Condition
X	X	X	X	0	None (Latches Cleared)
X	X	0	0	1	None
0	0	1	0	1	1
0	1	1	0	1	2
1	0	1	0	1	3
1	1	1	0	1	4

Logic "1": $V_{AH} \geq 2.4V$
Logic "0": $V_{AL} \leq 0.8V$

Die Characteristics

DIE DIMENSIONS:
3810µm x 2769µm

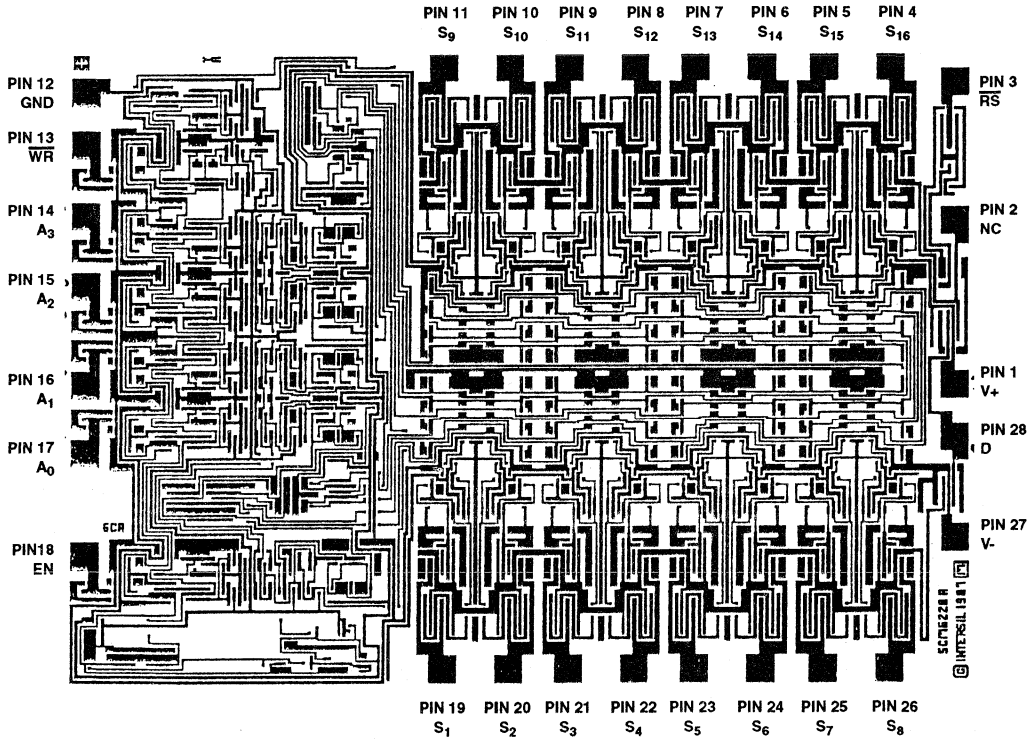
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG Over Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG526



Die Characteristics

DIE DIMENSIONS:
3810µm x 2769µm

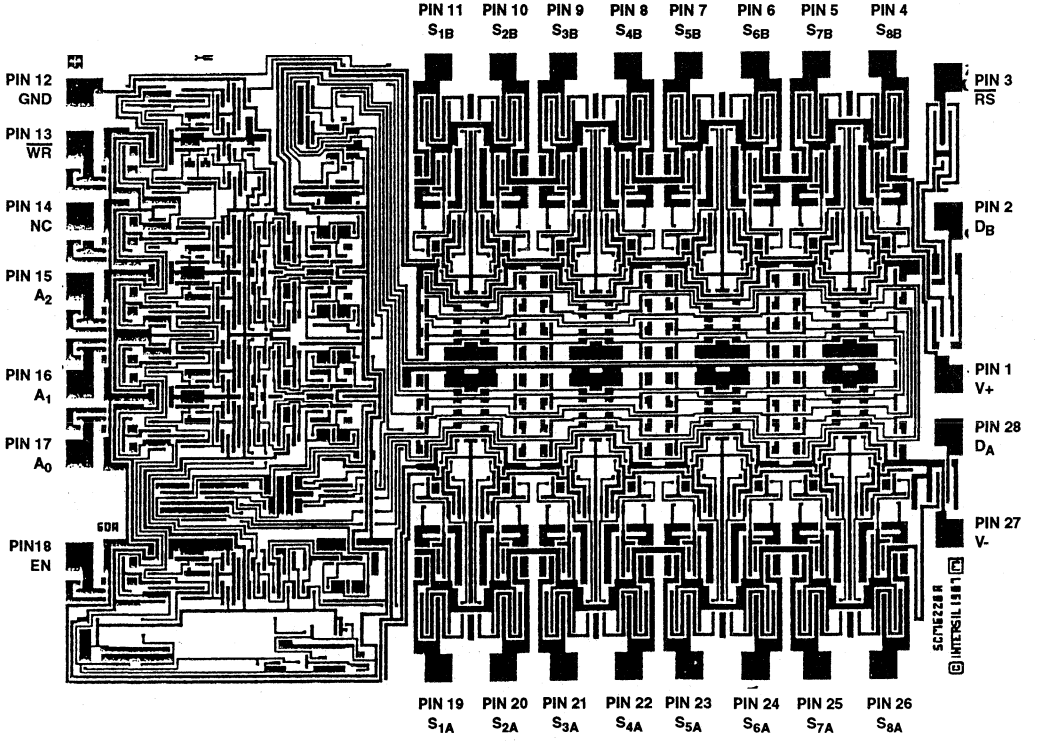
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG Over Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG527



Die Characteristics

DIE DIMENSIONS:
3100µm x 2083µm

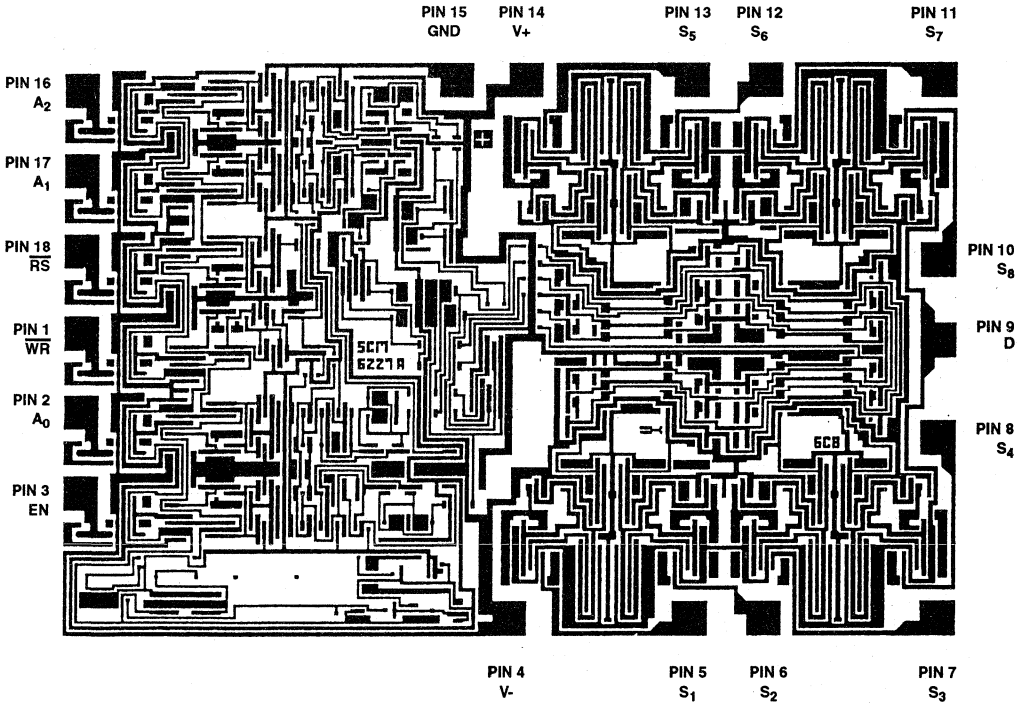
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG Over Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1 x 10^4 A/cm^2

Metallization Mask Layout

DG528



Die Characteristics

DIE DIMENSIONS:
3100µm x 2083µm

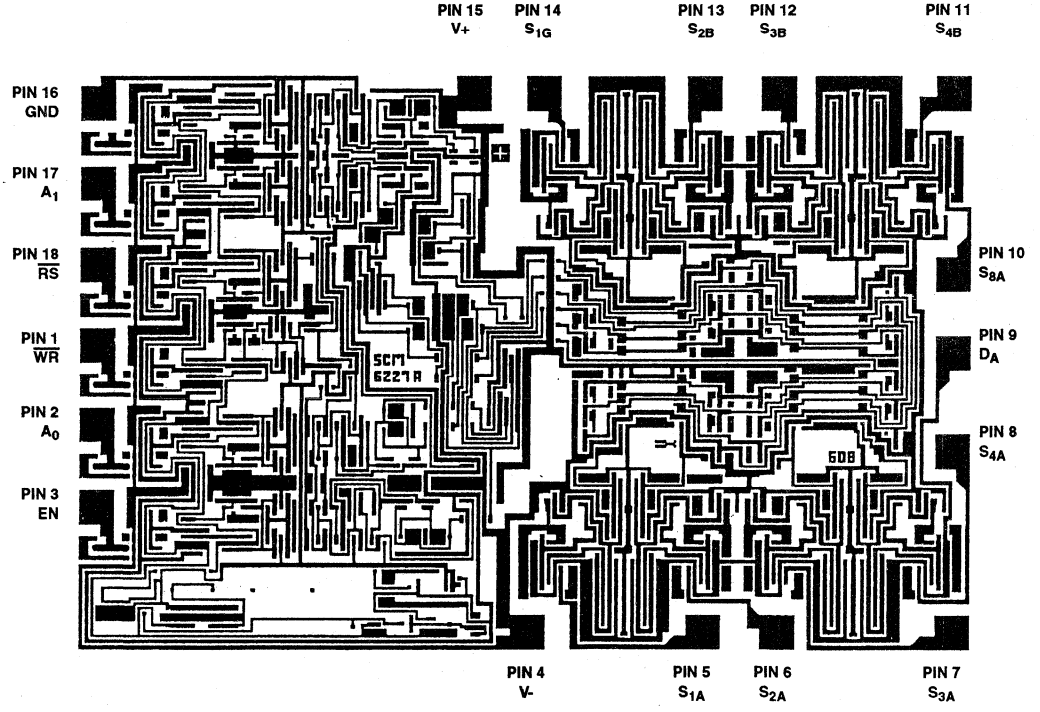
METALLIZATION:
Type: Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: PSG Over Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

WORST CASE CURRENT DENSITY:
9.1×10^4 A/cm^2

Metallization Mask Layout

DG529



HARRIS SEMICONDUCTOR HI-1818A, HI-1828A

Low Resistance, Single 8 Channel and Differential 4 Channel CMOS Analog Multiplexers

December 1993

Features

- Signal Range of +15V
- "ON" Resistance 250Ω
- Input Leakage (Max) 50nA
- Access Time 350ns
- Power Consumption 5mW
- DTL/TTL Compatible Address
- -55°C to +125°C Operation

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

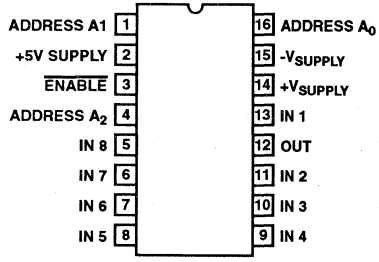
The HI-1818A and HI-1828A are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250Ω) assure optimum performance in low level or current mode applications.

The HI-1818A is a single-ended 8 channel multiplexer, while the HI-1828A is a differential 4 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

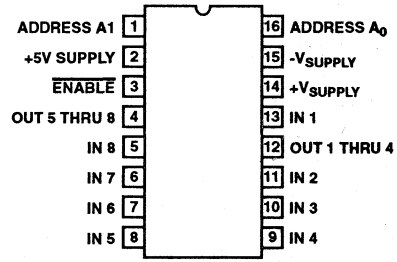
For MIL-STD-883 compliant parts, request the HI-1818A/883; HI-1828A/883 data sheet.

Pinouts

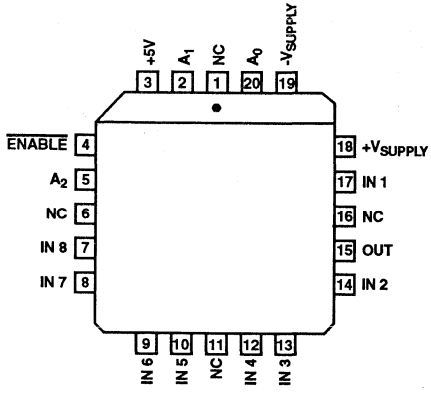
HI-1818A (CDIP, PDIP)
TOP VIEW



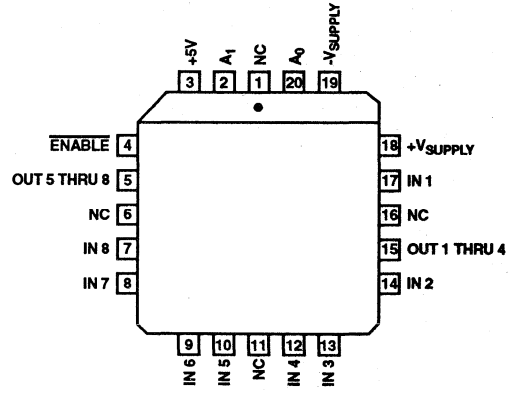
HI-1828A (CDIP, PDIP)
TOP VIEW



HI-1818A (PLCC)
TOP VIEW



HI-1828A (CLCC, PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3141**

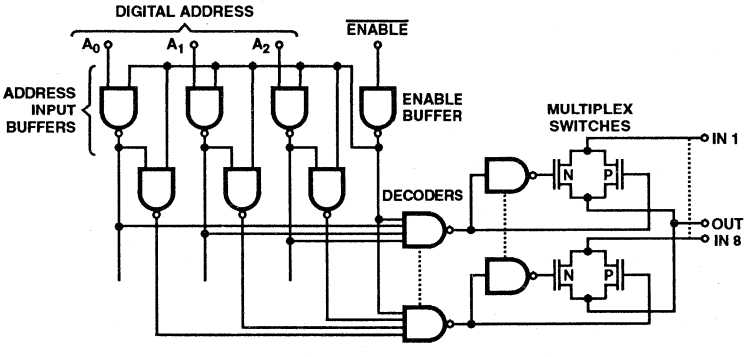
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI3-1818A-5	0°C to +75°C	16 Lead Plastic DIP
HI1-1818A-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-1818A-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-1818A-7	0°C to +75°C + 96 Hour Burn-In	16 Lead Ceramic DIP
HI4P1818A-5	0°C to +75°C	20 Lead PLCC
HI1-1818A/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-1828A-5	0°C to +75°C	16 Lead Ceramic DIP

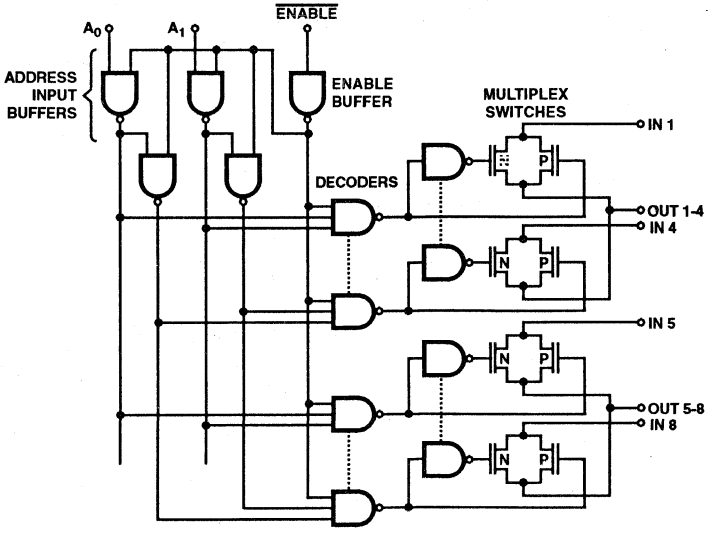
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-1828A-7	0°C to +75°C + 96 Hour Burn-In	16 Lead Ceramic DIP
HI3-1828A-5	0°C to +75°C	16 Lead Plastic DIP
HI4P1828A-5	0°C to +75°C	20 Lead PLCC
HI1-1828A-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-1828A/883	-55°C to +125°C	16 Lead Ceramic DIP
HI4-1828A/883	-55°C to +125°C	20 Lead CLCC
HI4-1828A-8	-55°C to +125°C	20 Lead CLCC

Functional Diagrams

HI-1818A



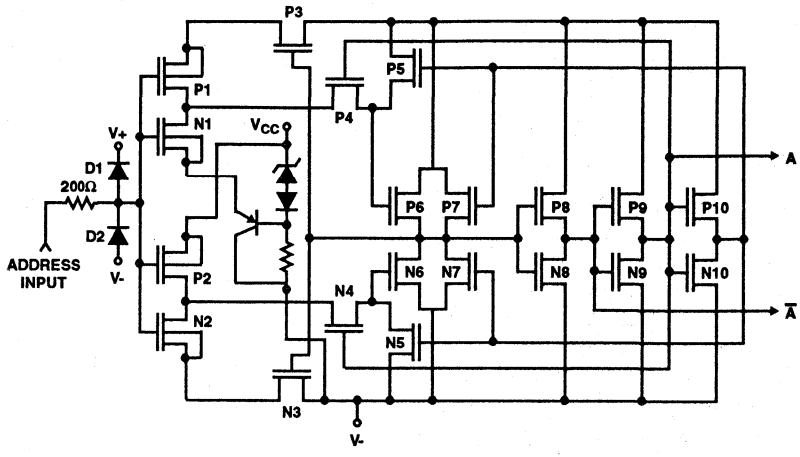
HI-1828A



Schematic Diagrams

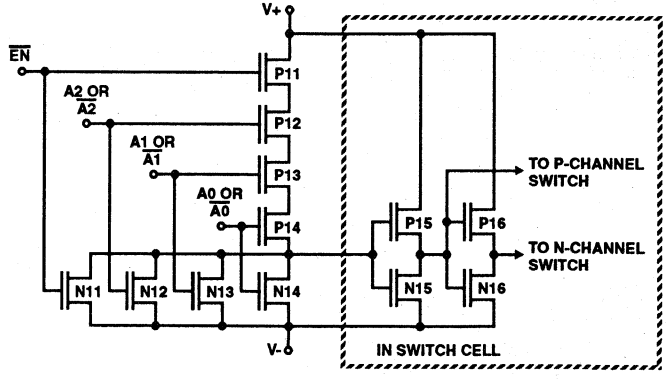
ADDRESS INPUT BUFFER

All N- Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Specified



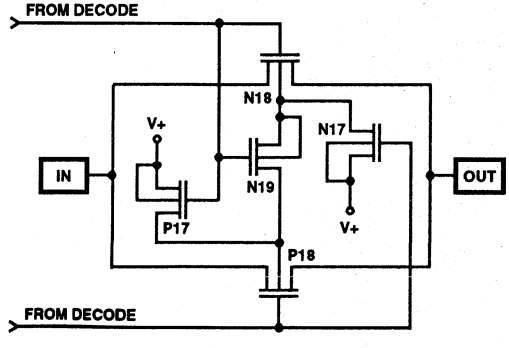
ADDRESS DECODER

All N- Channel Bodies to V-
All P-Channel Bodies to V+
A2 or $\overline{A2}$ not used for HI-1828A



MULTIPLEXER SWITCH

All N- Channel Bodies to V-
All P-Channel Bodies to V+
Unless Otherwise Specified



Absolute Maximum Ratings (Note 1)

Voltage Between Supply Pins 40.0V
Logic Supply Voltage 30.0V
Analog Input Voltage:
$+V_{IN}$ . . . . . $+V_{SUPPLY}$ +2V
$-V_{IN}$ . . . . . $-V_{SUPPLY}$ -2V
Digital Input Voltage . . . . . $-V_{SUPPLY}$ to $+V_{SUPPLY}$
Storage Temperature
PDIP, PLCC . . . . . -65°C to +150°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	77°C/W	23°C/W
Ceramic LCC Package	75°C/W	20°C/W
Plastic DIP Package	100°C/W	-
Plastic PLCC Package	80°C/W	-

Operating Temperature Ranges
HI-1818A/HI-1828A-2, -8 . . . . . -55°C to +125°C
HI-1818A/HI-1828A-5, -7 . . . . . 0°C to +75°C
Junction Temperature
CDIP, CLCC . . . . . +175°C
PDIP, PLCC . . . . . +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V, +5V; V_{AL} = 0.4V, V_{AH} = 4.0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP	HI-1818A/1828A -2, -8			HI-1818A/1828A -5, -7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, T_A	(Note 4)	+25°C	-	350	500	-	350	-	ns
		Full	-	-	1000	-	-	1000	ns
Break-Before-Make Delay		+25°C	-	25	-	-	100	-	ns
Settling Time									
0.1%		+25°C	-	1.08	-	-	1.08	-	µs
0.025 %		+25°C	-	2.8	-	-	2.8	-	µs
Channel Input Capacitance, C_{IN}		+25°C	-	4	-	-	4	-	pF
Channel Output Capacitance, C_{OUT}								-	
HI-1818A		+25°C	-	20	-	-	20	-	pF
HI-1828A		+25°C	-	10	-	-	10	-	pF
Drain-To-Source Capacitance, $C_{DS(OFF)}$		+25°C	-	0.6	-	-	0.6	-	pF
Digital Input Capacitance, C_D		+25°C	-	5	-	-	5	-	pF
Enable Delay (ON), $t_{ON(EN)}$		+25°C	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$		+25°C	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL}		Full	-	-	0.4	-	-	0.4	V
Input High Threshold, V_{AH}	(Note 3)	Full	4.0	-	-	4.0	-	-	V
Input Leakage Current, I_A		Full	-	-	1	-	-	1	µA
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_{IN}		Full	-15	-	+15	-15	-	+15	V
ON Resistance, R_{ON}	(Note 2)	+25°C	-	250	400	-	250	400	Ω
		Full	-	-	500	-	-	500	Ω
Input Leakage Current, $I_{S(OFF)}$		Full	-	-	50	-	-	50	nA
On Channel Leakage Current, $I_{D(ON)}$									
HI-1818A		Full	-	-	250	-	-	250	nA
HI-1828A		Full	-	-	125	-	-	125	nA
Output Leakage Current, $I_{D(OFF)}$									
HI-1818A		Full	-	-	250	-	-	250	nA
HI-1828A		Full	-	-	125	-	-	125	nA

Electrical Specifications

Supplies = +15V, -15V, +5V; V_{AL} = 0.4V, V_{AH} = 4.0V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP	HI-1818A/1828A -2, -8			HI-1818A/1828A -5, -7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, P_D		Full	-	-	27.5	-	-	27.5	mW
Current, I+		Full	-	-	0.5	-	-	0.5	mA
Current, I-		Full	-	-	1	-	-	1	mA
Current, I_L		Full	-	-	1	-	-	1	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{OUT} = ±10V, I_{OUT} = ∓ 1mA.
3. To drive from DTL/TTL circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.
4. Time measured to 90% of final output level; V_{OUT} = -5.0V to +5.0V, Digital Inputs = 0V to +4.0V.

Switching Waveforms

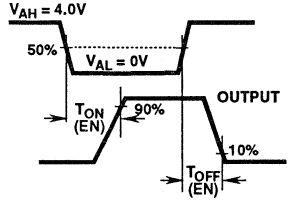
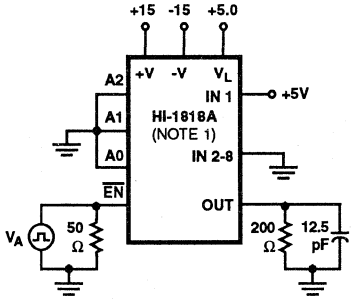


FIGURE 1A.



NOTE: 1. Similar connections for HI-1828A

FIGURE 1B.

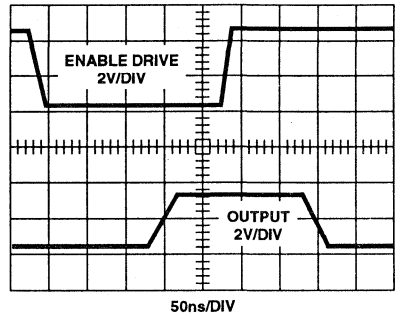


FIGURE 1C.

FIGURE 1. ENABLE DELAY, $t_{ON(EN)}$, $t_{OFF(EN)}$

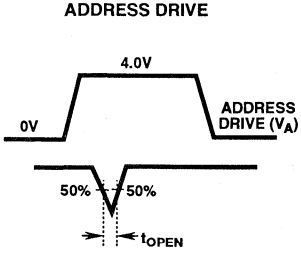
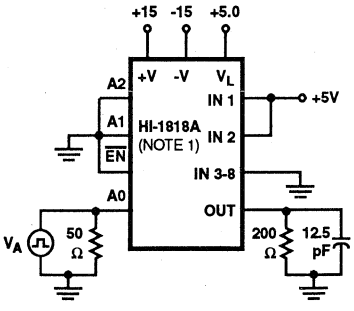


FIGURE 2A.



NOTE: 1. Similar connections for HI-1828A

FIGURE 2B.

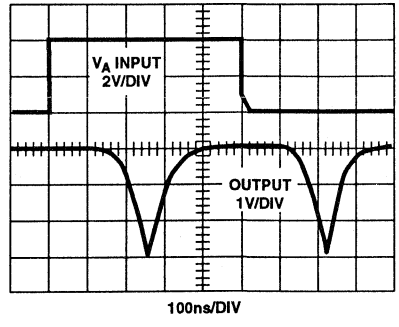
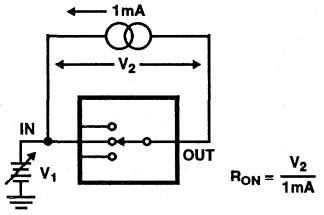


FIGURE 2C.

FIGURE 2. BREAK-BEFORE-MAKE DELAY, t_{OPEN}

Typical Performance Curves



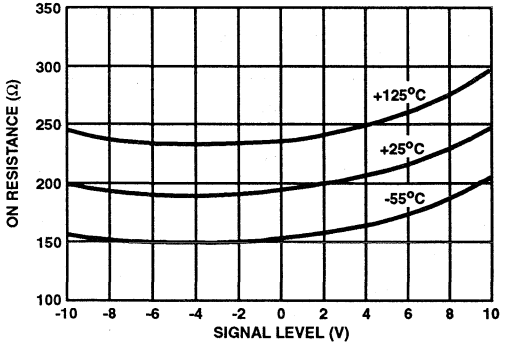
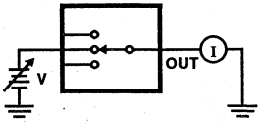


FIGURE 3. ON RESISTANCE vs ANALOG SIGNAL LEVEL



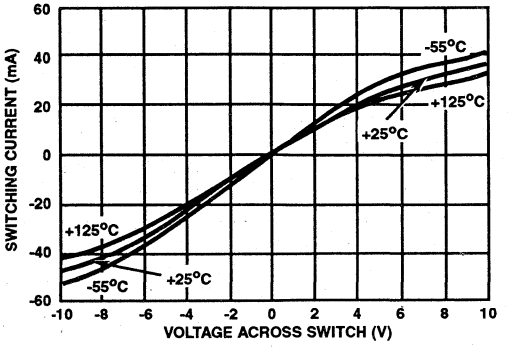
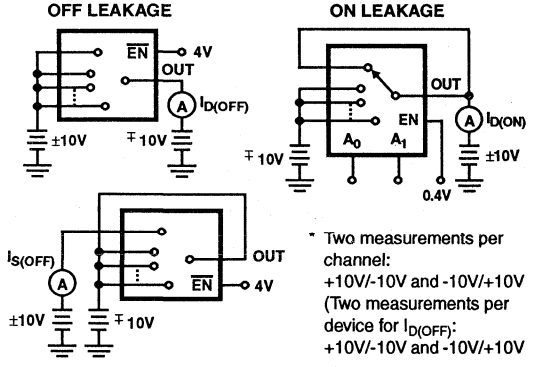
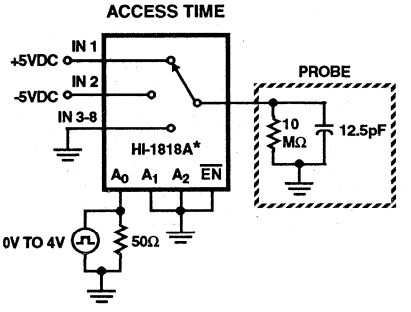


FIGURE 4. ON CHANNEL CURRENT vs VOLTAGE





* Similar connection for HI-1828A.

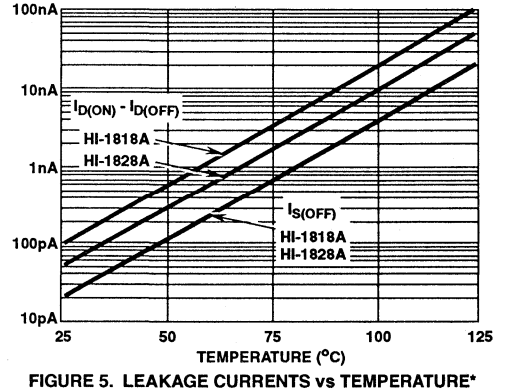


FIGURE 5. LEAKAGE CURRENTS vs TEMPERATURE*

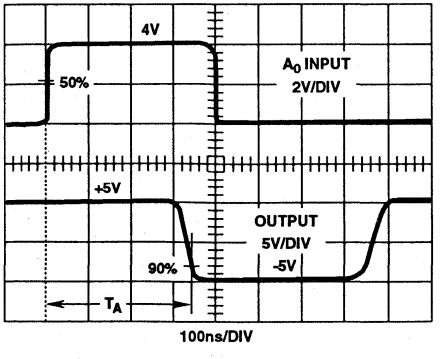


FIGURE 6. ACCESS TIME

HI-1818A TRUTH TABLE

ADDRESS				
A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	None

HI-1828A TRUTH TABLE

ADDRESS			
A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	None

Die Characteristics

DIE DIMENSIONS:
67.7x 103.5 mils

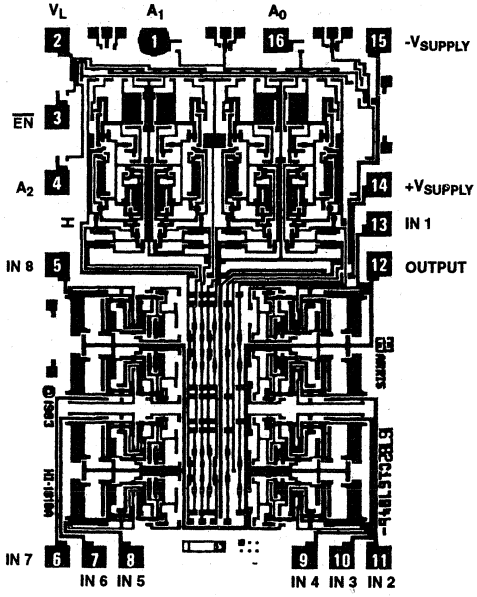
METALLIZATION:
Type: Cu/Al
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride/Silox
Thickness: Silox: 12kÅ ± 2kÅ, Nitride: 3.5kÅ ± 1kÅ

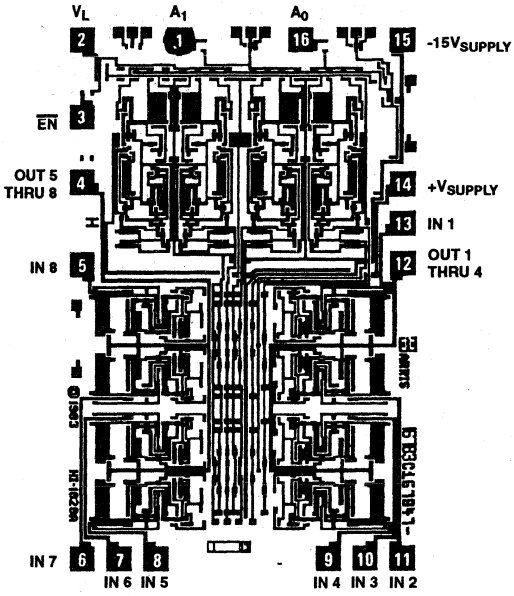
WORST CASE CURRENT DENSITY:
1.43 x 10^5 A/cm^2 at 25mA

Metallization Mask Layout

HI-1818A



HI-1828A



HARRIS SEMICONDUCTOR

HI-506, HI-507 HI-508, HI-509

Single 16 and 8/Differential 8 and 4 Channel CMOS Analog Multiplexers

December 1993

Features

- Low On Resistance 180Ω
- Wide Analog Signal Range ±15V
- TTL/CMOS Compatible
- Access Time 250ns
- 44V Maximum Power Supply
- Break-Before-Make Switching
- No Latch-Up
- Replaces DG506A/DG506AA and DG507A/DG507AA
- Replaces DG508A/DG508AA and DG509A/DG509AA

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Demultiplexing
- Selector Switch

Description

The HI-506/HI-507 and HI-508/HI-509 monolithic CMOS multiplexers each include an array of sixteen and eight analog switches respectively, a digital decoder circuit for channel selection, voltage reference for logic thresholds, and an enable input for device selection when several multiplexers are present. The Dielectric Isolation (DI) process used in fabrication of these devices eliminates the problem of latchup. DI also offers much lower substrate leakage and parasitic capacitance than conventional junction isolated CMOS (see Application Note AN521).

The switching threshold for each digital input is established by an internal +5V reference, providing a guaranteed minimum 2.4V for logic "1" and maximum 0.8V for logic "0". This allows direct interface without pullup resistors to signals from most logic families: CMOS, TTL, DTL and some PMOS. For protection against transient overvoltage, the digital inputs include a series 200Ω resistor and diode clamp to each supply.

The HI-506 is a single 16 channel, the HI-507 is an 8 channel differential, the HI-508 is a single 8 channel and the HI-509 is a 4 channel differential multiplexer. The HI-506/HI-507 are available in a 28 pin ceramic or plastic DIP, 28 pad leadless chip carrier (LCC), 28 pin plastic leaded chip carrier (PLCC) and 28 lead SOIC packages. The HI-508/HI-509 are available in a 16 pin plastic or ceramic DIP, a 20 pin plastic leaded chip carrier (PLCC), 20 pad ceramic leadless chip carrier (LCC) and 16 lead SOIC packages.

If input overvoltages are present the HI-546/HI-547/HI-548/HI-549 multiplexers are recommended. For further information see Application Notes AN520 and AN521. The HI-506/HI-507/HI-508/HI-509 is offered in both commercial and military grades. For additional High Reliability Screening including 160 hour burn-in specify the "-8" suffix. For Mil-Std-883 compliant parts, request the HI-506/883, HI-507/883, HI-508/883 or HI-509/883 datasheet

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3142**

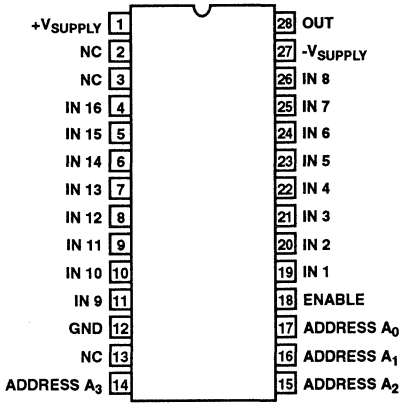
Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0506/883	-55°C to +125°C	28 Lead Ceramic DIP
HI1-0506-8	Hi-Rel Processing with Burn-In	28 Lead Ceramic DIP
HI1-0506-9	-40°C to +85°C	28 Lead Ceramic DIP
HI4-0506/883	-55°C to +125°C	28 Lead Ceramic LCC
HI1-0507/883	-55°C to +125°C	28 Lead Ceramic DIP
HI9P0506-9	-40°C to +85°C	28 Lead SOIC
HI3-0506-5	0°C to +75°C	28 Lead Plastic DIP
HI1-0506-7	0°C to +75°C + 96 Hour Burn-In	28 Lead Ceramic DIP
HI9P0506-5	0°C to +75°C	28 Lead SOIC
HI40506-5	0°C to +75°C	28 Lead PLCC
HI1-0506-5	0°C to +75°C	28 Lead Ceramic DIP
HI1-0506-4	-25°C to +85°C	28 Lead Ceramic DIP
HI1-0506-2	-55°C to +125°C	28 Lead Ceramic DIP
HI1-0507-8	Hi-Rel Processing with Burn-In	28 Lead Ceramic DIP
HI1-0507-9	-40°C to +85°C	28 Lead Ceramic DIP
HI4-0507/883	-55°C to +125°C	28 Lead Ceramic LCC
HI1-0507-4	-25°C to +85°C	28 Lead Ceramic DIP
HI4P0507-5	0°C to +75°C	28 Lead PLCC
HI9P0507-5	0°C to +75°C	28 Lead SOIC
HI1-0507-5	0°C to +75°C	28 Lead Ceramic DIP
HI3-0507-5	0°C to +75°C	28 Lead Plastic DIP
HI1-0507-7	0°C to +75°C + 96 Hour Burn-In	28 Lead Ceramic DIP
HI9P0507-9	-40°C to +85°C	28 Lead SOIC
HI1-0507-2	-55°C to +125°C	28 Lead Ceramic DIP

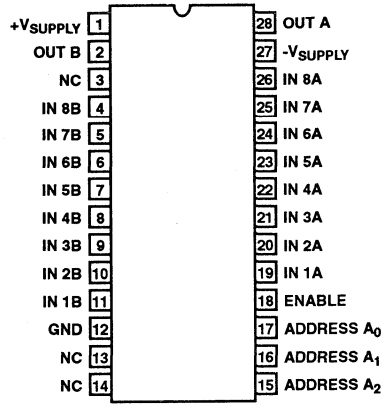
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0508/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0508-8	Hi-Rel Processing with Burn-In	16 Lead Ceramic DIP
HI1-0508-9	-40°C to +85°C	16 Lead Ceramic DIP
HI4-0508/883	-55°C to +125°C	20 Lead Ceramic LCC
HI1-0509/883	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0508-5	0°C to +75°C	16 Lead Ceramic DIP
HI3-0508-5	0°C to +75°C	16 Lead Plastic DIP
HI1-0508-4	-25°C to +85°C	16 Lead Ceramic DIP
HI1-0508-2	-55°C to +125°C	16 Lead Ceramic DIP
HI4P0508-5	0°C to +75°C	20 Lead PLCC
HI1-0508-7	0°C to +75°C + 96 Hour Burn-In	16 Lead Ceramic DIP
HI9P0508-9	-40°C to +85°C	16 Lead SOIC (N)
HI9P0508-5	0°C to +75°C	16 Lead SOIC (N)
HI1-0509-8	Hi-Rel Processing with Burn-In	16 Lead Ceramic DIP
HI1-0509-9	-40°C to +85°C	16 Lead Ceramic DIP
HI4-0509/883	-55°C to +125°C	20 Lead Ceramic LCC
HI9P0509-5	0°C to +75°C	16 Lead SOIC (N)
HI9P0509-9	-40°C to +85°C	16 Lead SOIC (N)
HI1-0509-4	-25°C to +85°C	16 Lead Ceramic DIP
HI1-0509-5	0°C to +75°C	16 Lead Ceramic DIP
HI3-0509-5	0°C to +75°C	16 Lead Plastic DIP
HI4P0509-5	0°C to +75°C	20 Lead PLCC
HI1-0509-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0509-7	0°C to +75°C + 96 Hour Burn-In	16 Lead Ceramic DIP

Pinouts

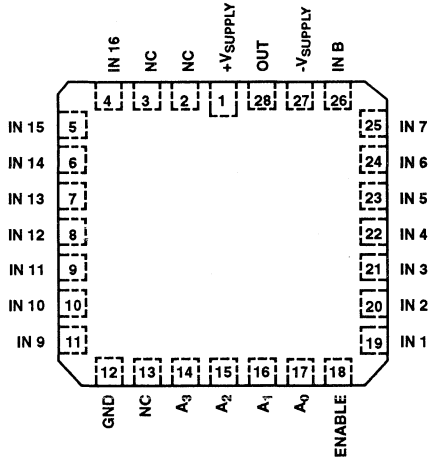
HI-506
(PDIP, CDIP, SOIC)
TOP VIEW



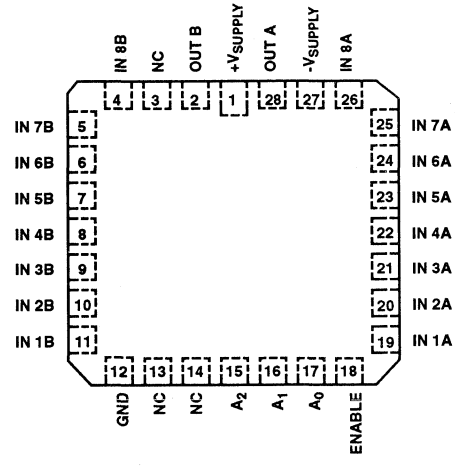
HI-507
(PDIP, CDIP, SOIC)
TOP VIEW



HI-506
(LCC, PLCC)
TOP VIEW

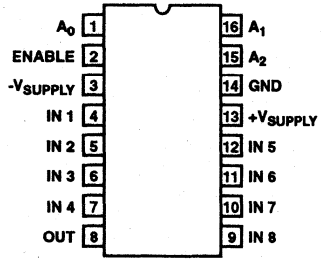


HI-507
(LCC, PLCC)
TOP VIEW

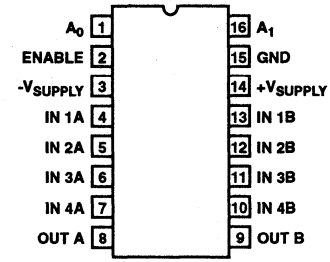


Pinouts (Continued)

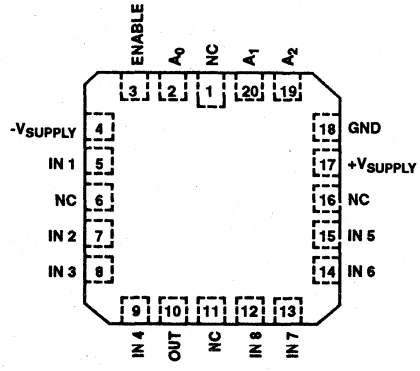
HI-508
(PDIP, CDIP, SOIC)
TOP VIEW



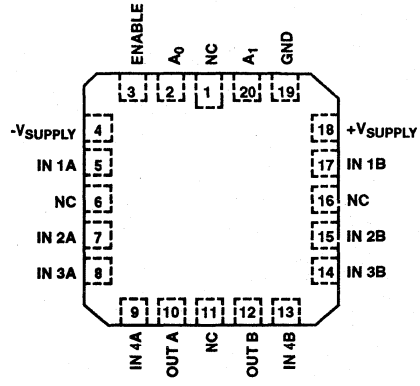
HI-509
(PDIP, CDIP, SOIC)
TOP VIEW



HI-508
(LCC, PLCC)
TOP VIEW

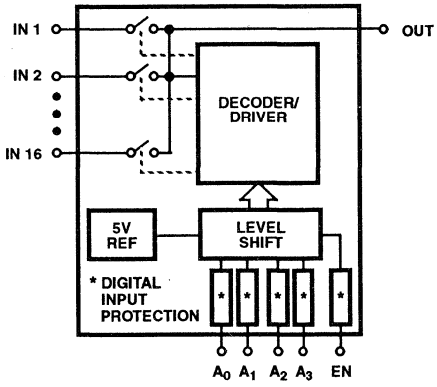


HI-509
(LCC, PLCC)
TOP VIEW

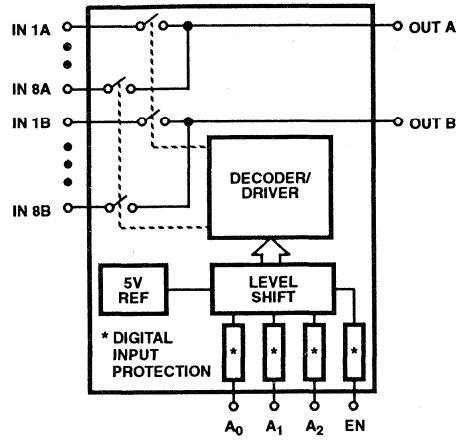


Functional Diagrams

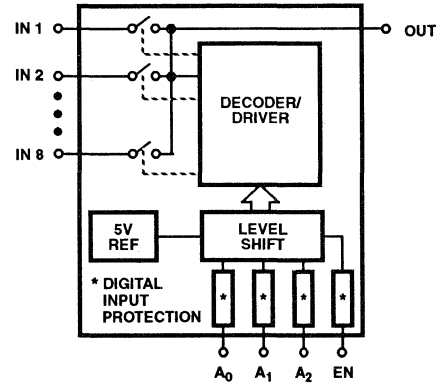
HI-506



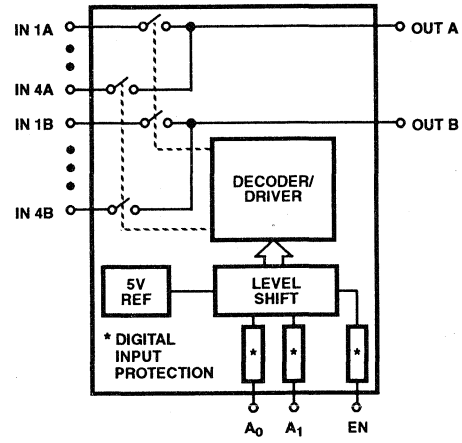
HI-507



HI-508

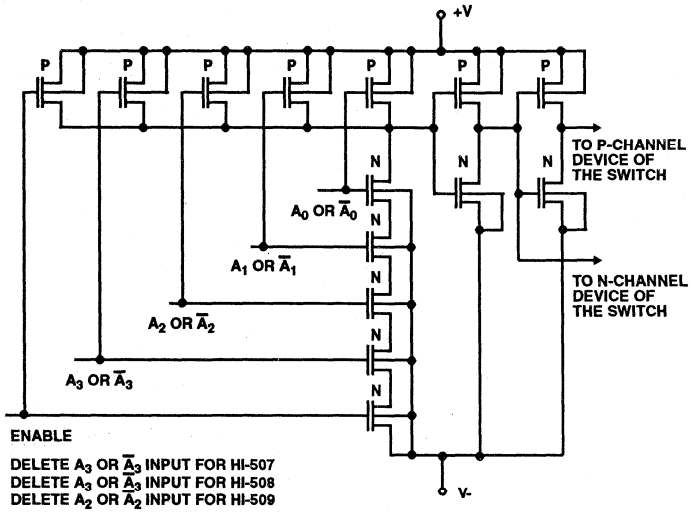


HI-509



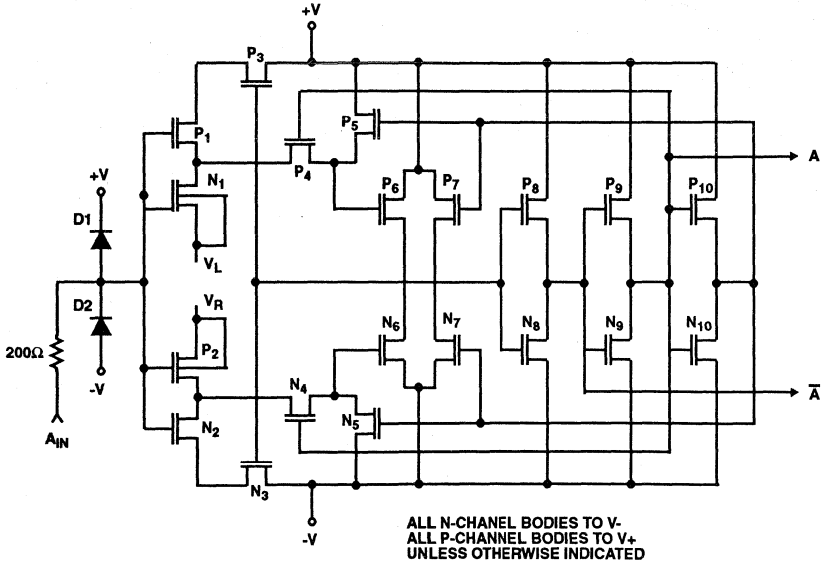
Schematic Diagrams

ADDRESS DECODER



DELETE A_3 OR $\overline{A}_3$ INPUT FOR HI-507
DELETE A_3 OR $\overline{A}_3$ INPUT FOR HI-508
DELETE A_2 OR $\overline{A}_2$ INPUT FOR HI-509

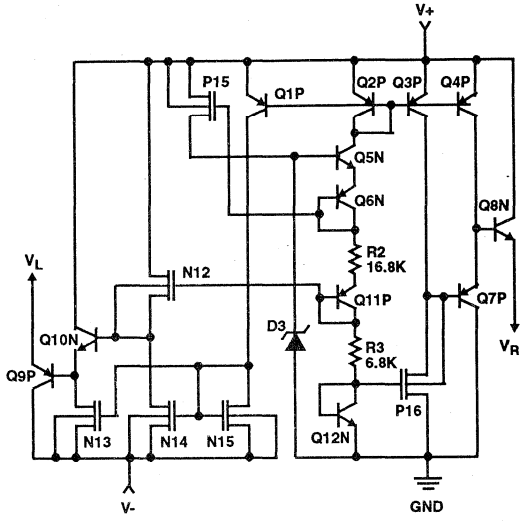
ADDRESS INPUT BUFFER
LEVER SHIFTER



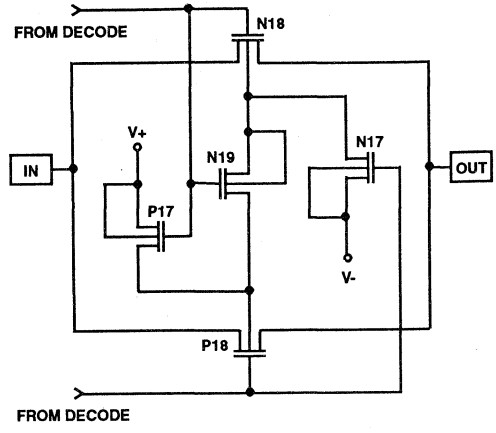
ALL N-CHANEL BODIES TO V-
ALL P-CHANNEL BODIES TO V+
UNLESS OTHERWISE INDICATED

Schematic Diagrams (Continued)

TTL REFERENCE CIRCUIT



MULTIPLEX SWITCH



Absolute Maximum Ratings

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ . . . . . +44V
$V_{SUPPLY(+)}$ to GND . . . . . +22V
$V_{SUPPLY(-)}$ to GND . . . . . -25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ . . . . . $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ . . . . . $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage (Note 7)
$+V_S$ . . . . . $+V_{SUPPLY}$ +2V
$-V_S$ . . . . . $-V_{SUPPLY}$ -2V
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed at 1ms, 10% duty cycle max)
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
16 Lead Ceramic DIP Packages	80°C/W	24°C/W
16 Lead SOIC Packages	115°C/W	-
16 Lead Plastic DIP	100°C/W	-
20 Lead Ceramic LCC Packages	75°C/W	20°C/W
20 Lead PLCC	80°C/W	-
28 Lead Ceramic DIP Packages	55°C/W	20°C/W
28 Lead Plastic DIP Package	60°C/W	-
28 Lead SOIC Package	70°C/W	-
28 Lead Ceramic LCC Packages	60°C/W	11°C/W
28 Lead PLCC Packages	70°C/W	-

Operating Temperature Ranges
HI-506/507/508/509-2, -8 . . . . . -55°C to +125°C
HI-506/507/508/509-4 . . . . . -25°C to +85°C
HI-506/507/508/509-5 . . . . . -65°C to +150 °C
Junction Temperature
Ceramic . . . . . +175°C
Plastic . . . . . +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves.

PARAMETER	TEST CONDITIONS	TEMP	HI-5XX-2, HI-5XX-8			HI-5XX-4, HI-5XX-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, I_A	(Note 1)	+25°C	-	250	500	-	250	-	ns
		Full	-	-	1000	-	-	1000	ns
Break-Before-Make Delay, t_{OPEN}	(Note 1)	+25°C	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$	(Note 1)	+25°C	-	250	500	-	250	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$	(Note 1)	+25°C	-	250	500	-	250	-	ns
		Full	-	-	1000	-	-	1000	ns
Settling Time to 0.1%, t_S (HI-506 and HI-507)		+25°C	-	1.2	-	-	1.2	-	µs
Settling Time to 0.01%, t_S (HI-506 and HI-507)		+25°C	-	2.4	-	-	2.4	-	µs
Settling Time to 0.1%, t_S (HI-508 and HI-509)		+25°C	-	360	-	-	360	-	ns
Settling Time to 0.01%, t_S (HI-508 and HI-509)		+25°C	-	600	-	-	600	-	ns
"Off Isolation"	(Note 5)	+25°C	50	68	-	50	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		+25°C	-	10	-	-	10	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-506)		+25°C	-	52	-	-	52	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-507)		+25°C	-	30	-	-	30	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-508)		+25°C	-	17	-	-	17	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-509)		+25°C	-	12	-	-	12	-	pF
Digital Input Capacitance, C_A		+25°C	-	6	-	-	6	-	pF

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP	HI-5XX-2, HI-5XX-8			HI-5XX-4, HI-5XX-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input to Output Capacitance, $C_{DS(OFF)}$		+25°C	-	0.08	-	-	0.08	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL}	(Note 1)	Full	-	-	+0.8	-	-	+0.8	V
Input High Threshold, V_{AH}	(Note 1)	Full	+2.4	-	-	+2.4	-	-	V
Input Leakage Current (High or Low), I_A	(Notes 1, 4)	Full	-	-	1.0	-	-	1.0	µA
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_S		Full	-15	-	+15	-15	-	+15	V
On Resistance, R_{ON}	(Notes 1, 2)	+25°C	-	180	300	-	180	400	Ω
ΔR_{ON}, (Any Two Channels)		+25°C	-	5	-	-	5	-	%
Off Input Leakage Current, $I_{S(OFF)}$	(Note 3)	+25°C	-	0.03	-	-	0.03	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$	(Note 3)	+25°C	-	0.3	-	-	0.3	-	nA
HI-506		Full	-	-	300	-	-	300	nA
HI-507		Full	-	-	200	-	-	200	nA
HI-508		Full	-	-	200	-	-	200	nA
HI-509		Full	-	-	100	-	-	100	nA
On Channel Leakage Current, $I_{D(ON)}$	(Note 3)	+25°C	-	0.3	-	-	0.3	-	nA
HI-506		Full	-	-	300	-	-	300	nA
HI-507		Full	-	-	200	-	-	200	nA
HI-508		Full	-	-	200	-	-	200	nA
HI-509		Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current, I_{DIFF} (HI-507, HI-509 Only)	(Note 1)	Full	-	-	50	-	-	50	nA
POWER REQUIREMENTS									
Current, I+, Pin 1 HI-506/HI-507	(Note 6)	Full	-	1.5	3.0	-	1.5	3.0	mA
Current, I+, HI-508/HI-509	(Note 6)	Full	-	1.5	2.4	-	1.5	2.4	mA
Current, I-, Pin 27 HI-506/HI-507	(Note 6)	Full	-	0.4	1.0	-	0.4	1.0	mA
Current, I-, HI-508/HI-509	(Note 6)	Full	-	0.4	1.0	-	0.4	1.0	mA
Power Dissipation, P_D									
HI-506/HI-507		Full	-	-	60	-	-	60	mW
HI-508/HI-509		Full	-	-	51	-	-	51	mW

NOTES:

1. 100% tested for Dash 8. Leakage currents not tested at -55°C.
2. $V_{OUT} = \pm 10V$, $I_{OUT} = \mp 1mA$.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at +25°C.
5. $V_{EN} = 0.8V$, $R_L = 1K$, $C_L = 15pF$, $V_S = 7V_{RMS}$, f = 100kHz.
6. V_{EN}, $V_A = 0V$ or 2.4V.
7. Signal voltage at any analog input or output (S or D) will be clamped to the supply rail by internal diodes. Limit the resulting current as shown under absolute maximum ratings. If an overvoltage condition is anticipated (analog input exceeds either power supply voltage), the Harris HI-546/HI-547/HI-548/HI-549 multiplexers are recommended.

Performance Curves $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$, Unless Otherwise Specified

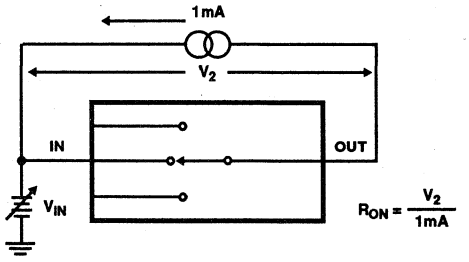


FIGURE 1A. TEST CIRCUIT

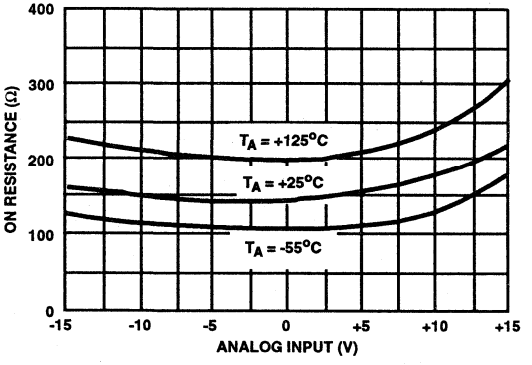


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE, TEMPERATURE

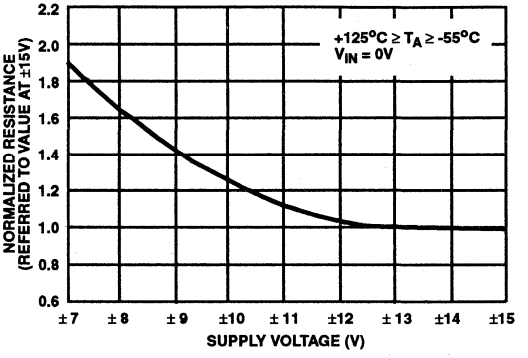


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

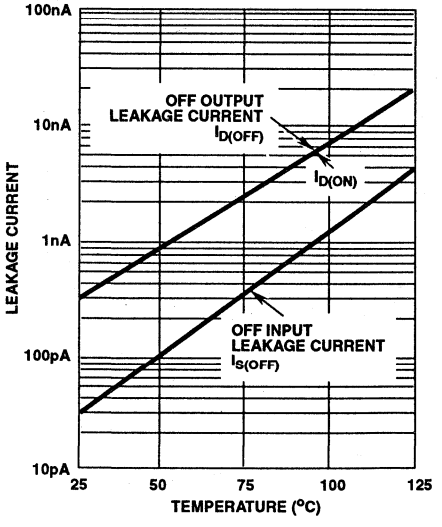


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

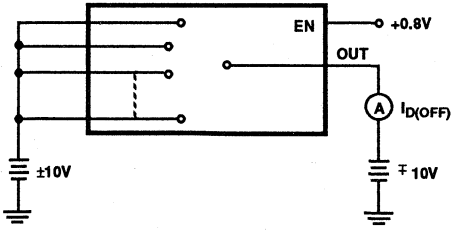


FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT

Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $V_{AH} = 2.4V$, $V_{AL} = 0.8V$, Unless Otherwise Specified (Continued)

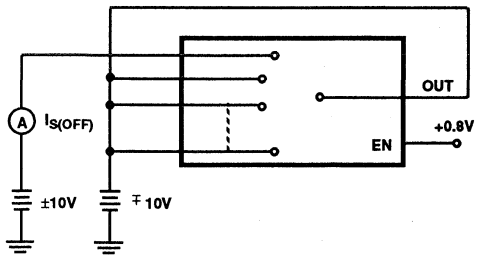


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT

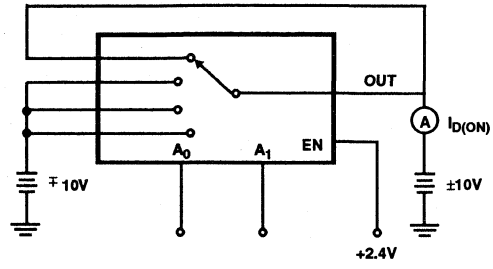


FIGURE 2D. $I_{D(ON)}$ TEST CIRCUIT

FIGURE 2. ON RESISTANCE

NOTE:

1. Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$ +10V/-10V and -10V/+10V)

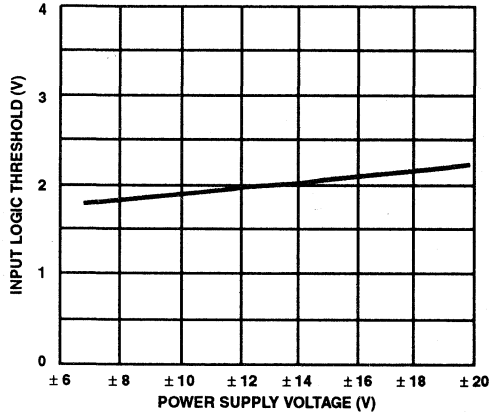


FIGURE 3. LOGIC THRESHOLD vs POWER SUPPLY VOLTAGE

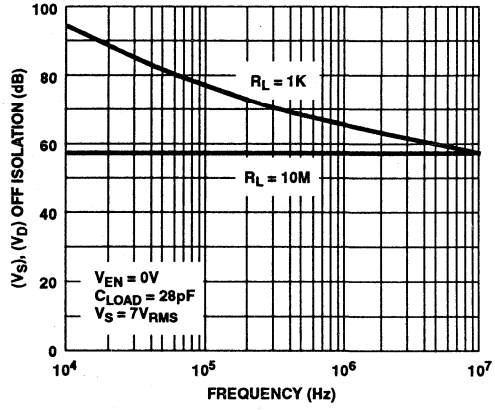


FIGURE 4. OFF ISOLATION vs FREQUENCY

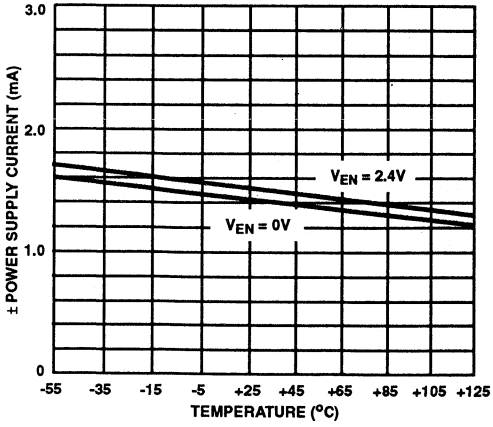


FIGURE 5A. HI-506/HI-507

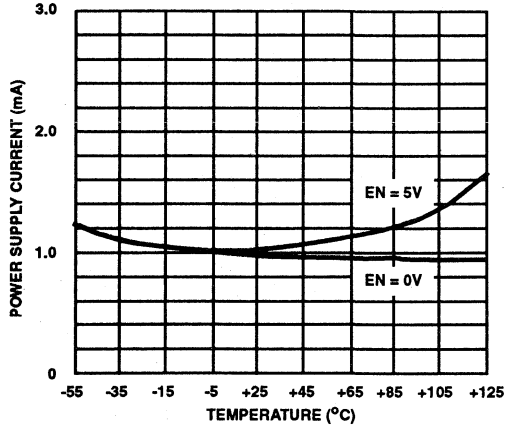


FIGURE 5B. HI-508/HI-509

FIGURE 5. POWER SUPPLY CURRENT vs TEMPERATURE

Performance Curves T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified (Continued)

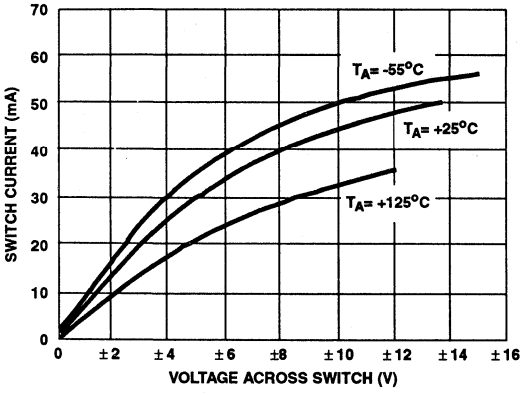


FIGURE 6A. ON CHANNEL CURRENT vs VOLTAGE

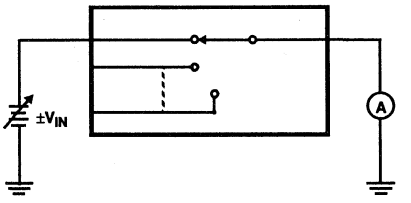


FIGURE 6B. TEST CIRCUIT

FIGURE 6. ON CHANNEL CURRENT vs VOLTAGE

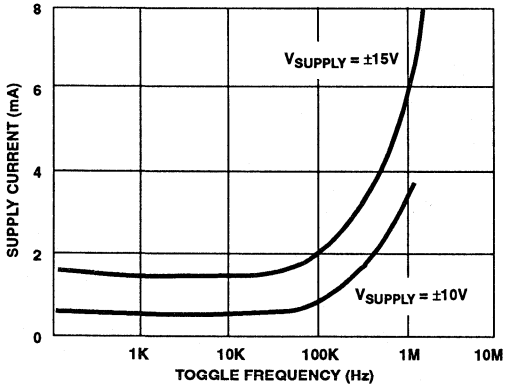


FIGURE 7A. SUPPLY CURRENT vs TOGGLE FREQUENCY

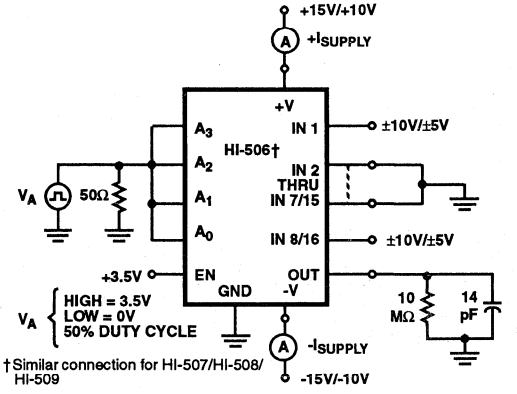


FIGURE 7B. TEST CIRCUIT

FIGURE 7. SUPPLY CURRENT

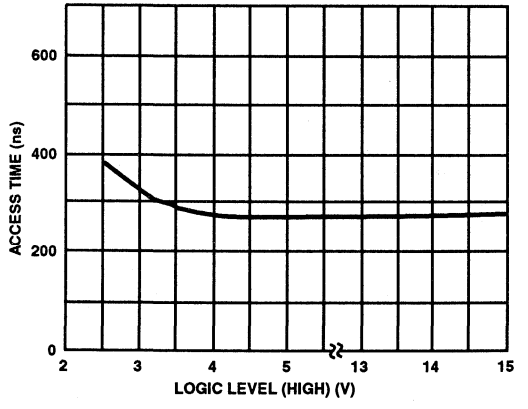


FIGURE 8A. ACCESS TIME vs LOGIC LEVEL (HIGH)

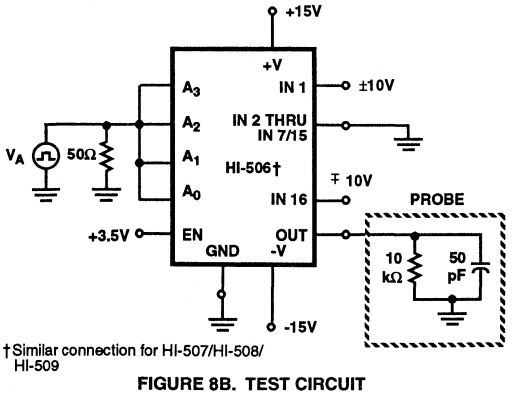


FIGURE 8B. TEST CIRCUIT

Switching Waveforms

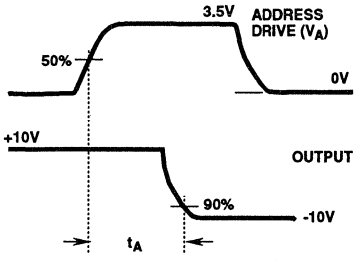


FIGURE 8C. WAVEFORMS

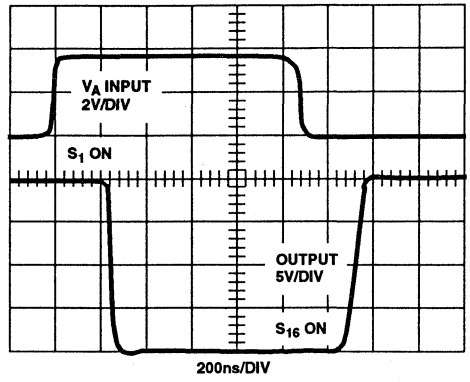
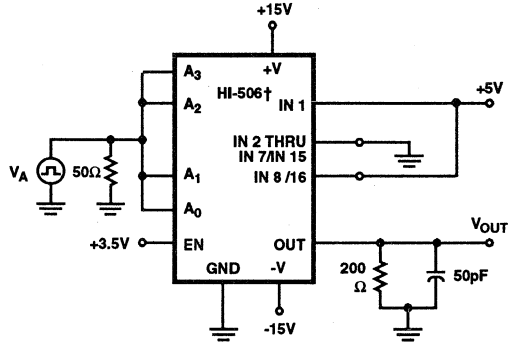


FIGURE 8D. ACCESS TIME

FIGURE 8. ACCESS TIME



† Similar connection for HI-507/HI-508/HI-509

FIGURE 9A. TEST CIRCUIT

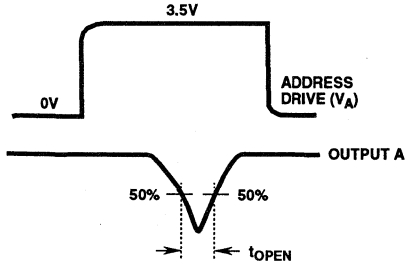


FIGURE 9B. WAVEFORMS

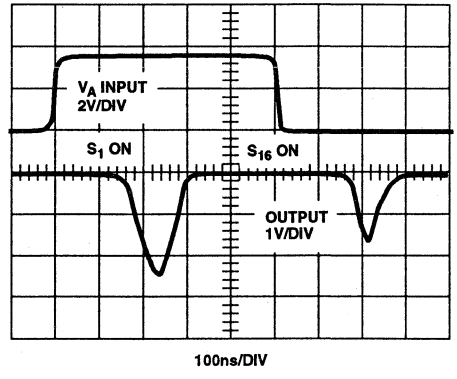
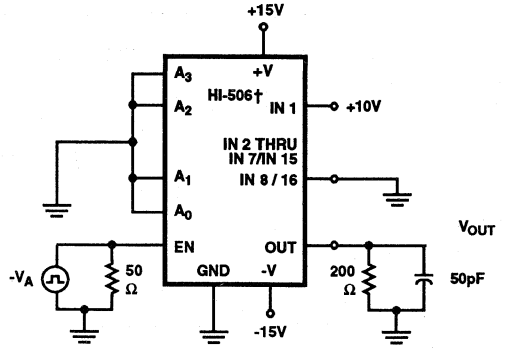


FIGURE 9C. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

FIGURE 9. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

Switching Waveforms (Continued)



†Similar connection for HI-507/HI-508/HI-509

FIGURE 10A. TEST CIRCUIT

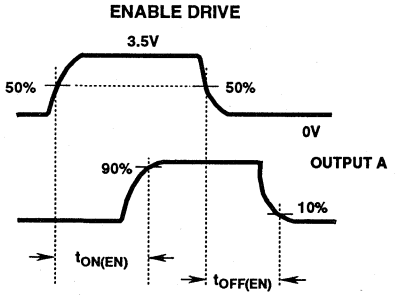


FIGURE 10B. WAVEFORMS

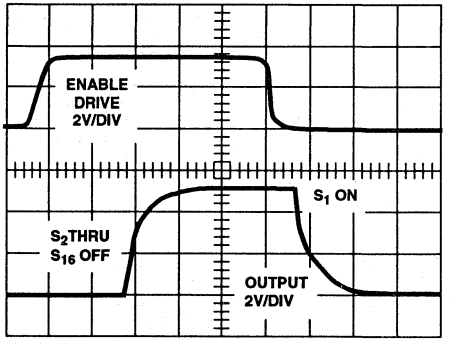


FIGURE 10C. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

FIGURE 10. ENABLE DELAY

Truth Tables

HI-506

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-508

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Die Characteristics

DIE DIMENSIONS:
129 mils x 82 mils

METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride/Silox
Nitride Thickness: 3.5kÅ ± 1kÅ
Silox Thickness: 12kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.4 \times 10^5 A/cm^2$

TRANSISTOR COUNT: 421

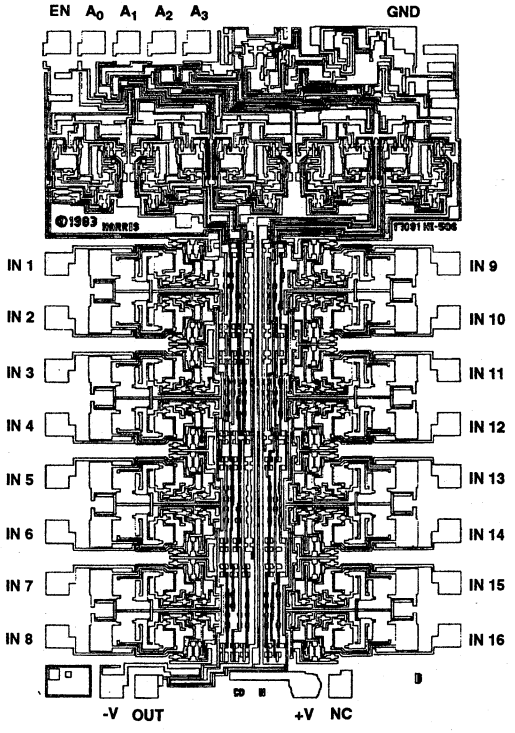
PROCESS: CMOS-DI

SUBSTRATE POTENTIAL*: $-V_{SUPPLY}$

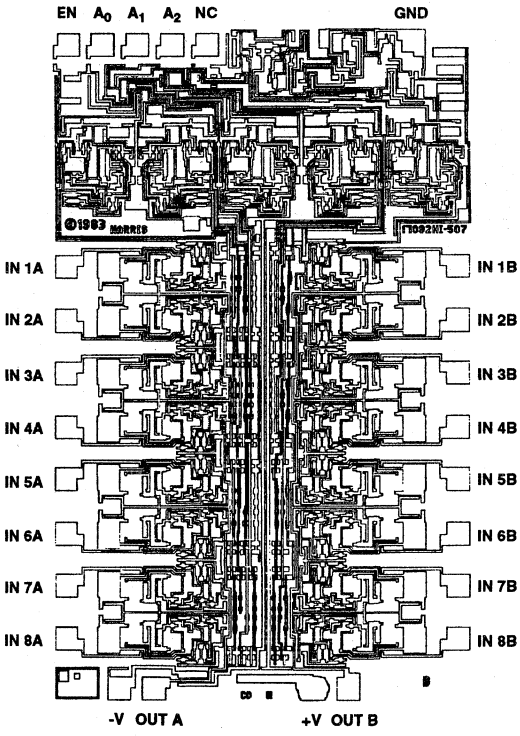
* The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential

Metallization Mask Layout

HI-506



HI-507



NOTE: Pad numbers correspond to DIP pin numbers only.

Die Characteristics

DIE DIMENSIONS:
81.9 mils x 90.2 mils

METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride/Silox
Nitride Thickness: 3.5kÅ ± 1kÅ
Silox Thickness: 12kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.4 \times 10^5 A/cm^2$

TRANSISTOR COUNT: 234

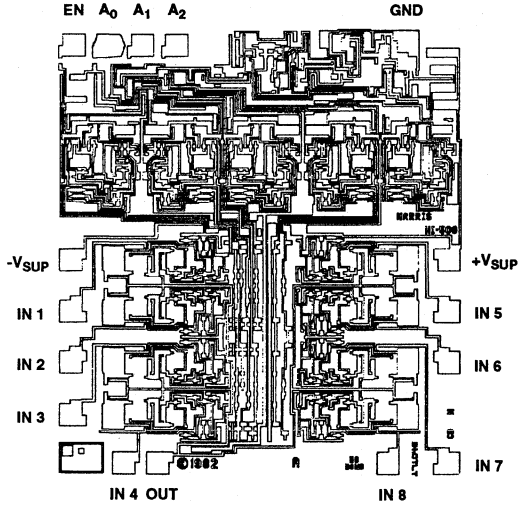
PROCESS: CMOS-DI

SUBSTRATE POTENTIAL*: $-V_{SUPPLY}$

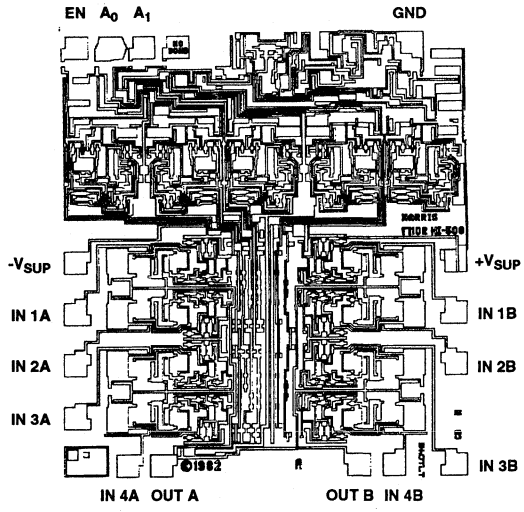
* The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential

Metallization Mask Layout

HI-508



HI-509



NOTE: Pad numbers correspond to DIP pin numbers only.

HARRIS SEMICONDUCTOR

HI-506A, HI-507A HI-508A, HI-509A

16 Channel, 8 Channel, Differential 8 and Differential 4 Channel, CMOS Analog MUXs with Active Overvoltage Protection

December 1993

Features

- Analog Overvoltage $70V_{P-P}$
- No Channel Interaction During Overvoltage
- 44V Maximum Power Supply
- Fail Safe with Power Loss (No Latch-Up)
- Break-Before-Make Switching
- Analog Signal Range ±15V
- Access Time 500ns
- Power Dissipation 7.5mW

Applications

- Data Acquisition Systems
- Industrial Controls
- Telemetry

Description

The HI-506A, HI-507A, HI-508A and HI-509A are analog multiplexers with active overvoltage protection. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers. Analog inputs can withstand constant 70V peak-to-peak levels with ±15V supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents 1kΩ of resistance under this condition. These features make the HI-506A, HI-507A, HI-508A and HI-509A ideal for use in systems where the analog inputs originate from external equipment, or separately powered circuitry. All devices are fabricated with 44V dielectrically isolated CMOS technology. The HI-506A is a single 16 channel multiplexer, the HI-507A is an 8 channel differential multiplexer, the HI-508A is a single 8 channel multiplexer and the HI-509A is a differential 4 channel multiplexer. If input overvoltage protection is not needed the HI-506/507/508/509 multiplexers are recommended. For further information see Application Notes AN520 and AN521.

The HI-506A/507A devices are available in a 28 lead Plastic or Ceramic DIP and the HI-508A/509A devices are available in a 16 lead Plastic or Ceramic DIP package.

The HI-50XA are offered in industrial/commercial and military grades, additional Hi-Rel screening including 160 hour burn-in is specified by the "8" suffix. For Mil-Std-883 compliant parts, request the HI-546/883, HI-547/883, HI-548/883 or HI-549/883 data sheets.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0506A-2	-55°C to +125°C	28 Lead Ceramic DIP
HI1-0506A-5	0°C to +75°C	28 Lead Ceramic DIP
HI1-0506A-7	0°C to +75°C + 96 Hour Burn-In	28 Lead Ceramic DIP
HI1-0506A-8	-55°C to +125°C + 160 Hour Burn-In	28 Lead Ceramic DIP
HI3-0506A-5	+0°C to +75°C	28 Lead Plastic DIP
HI1-0507A-2	-55°C to +125°C	28 Lead Ceramic DIP
HI1-0507A-5	0°C to +75°C	28 Lead Ceramic DIP
HI1-0507A-7	0°C to +75°C + 96 Hour Burn-In	28 Lead Ceramic DIP
HI1-0507A-8	-55°C to +125°C + 160 Hour Burn-In	28 Lead Ceramic DIP
HI3-0507A-5	0°C to +75°C	28 Lead Plastic DIP

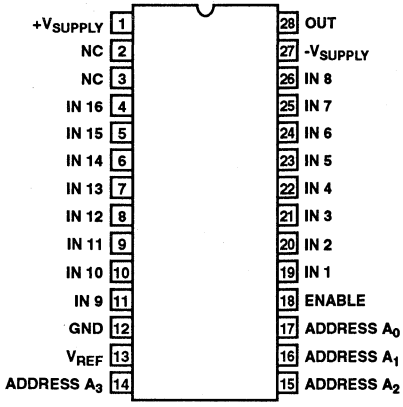
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0508A-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0508A-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-0508A-7	0°C to +75°C + 96 Hour Burn-In	16 Lead Ceramic DIP
HI1-0508A-8	-55°C to +125°C + 160 Hour Burn-In	16 Lead Ceramic DIP
HI3-0508A-5	+0°C to +75°C	16 Lead Plastic DIP
HI1-0509A-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0509A-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-0509A-7	0°C to +75°C + 96 Hour Burn-In	16 Lead Ceramic DIP
HI1-0509A-8	-55°C to +125°C + 160 Hour Burn-In	16 Lead Ceramic DIP
HI3-0509A-5	0°C to +75°C	16 Lead Plastic DIP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

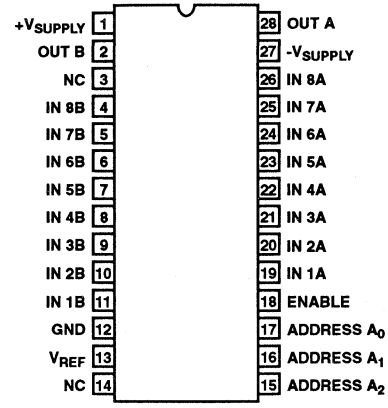
File Number **3143**

Pinouts

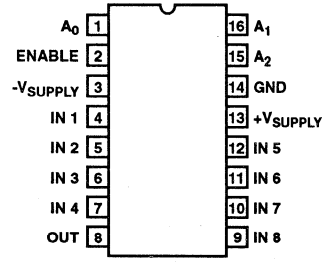
HI1-506A (CDIP)
HI3-506A (PDIP)
TOP VIEW



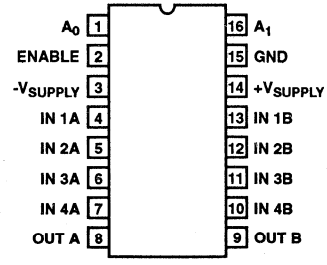
HI1-507A (CDIP)
HI3-507A (PDIP)
TOP VIEW



HI1-508A (CDIP)
HI3-508A (PDIP)
TOP VIEW

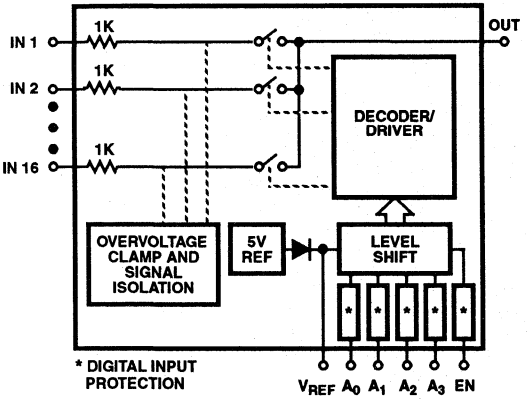


HI1-509A (CDIP)
HI3-509A (PDIP)
TOP VIEW

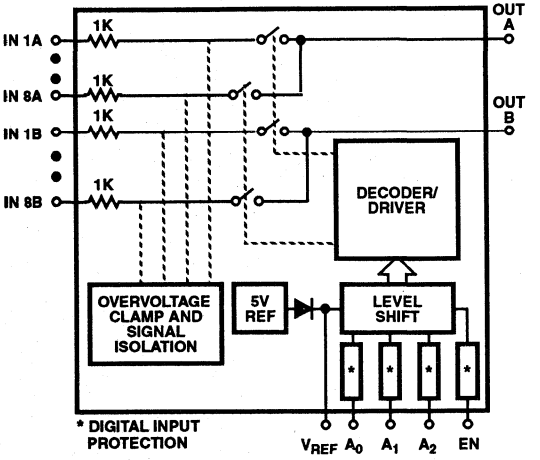


Functional Diagrams

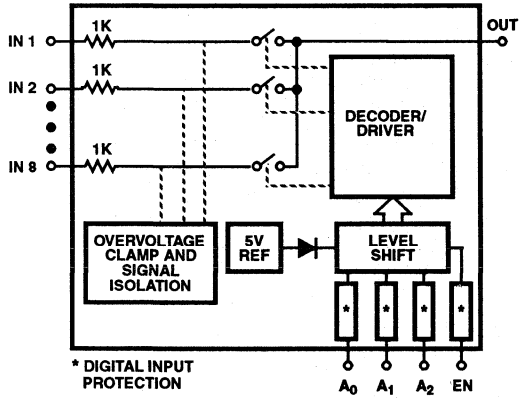
HI-506A



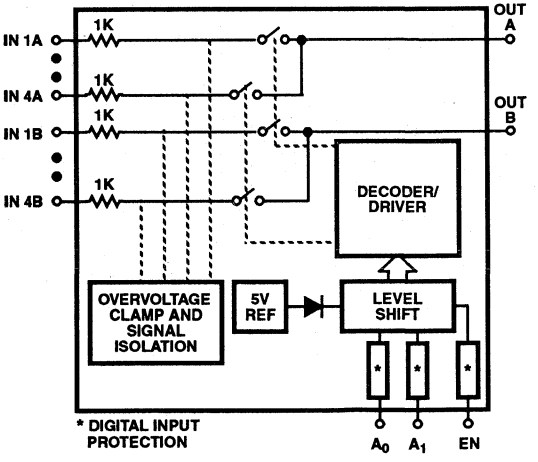
HI-507A



HI-508A

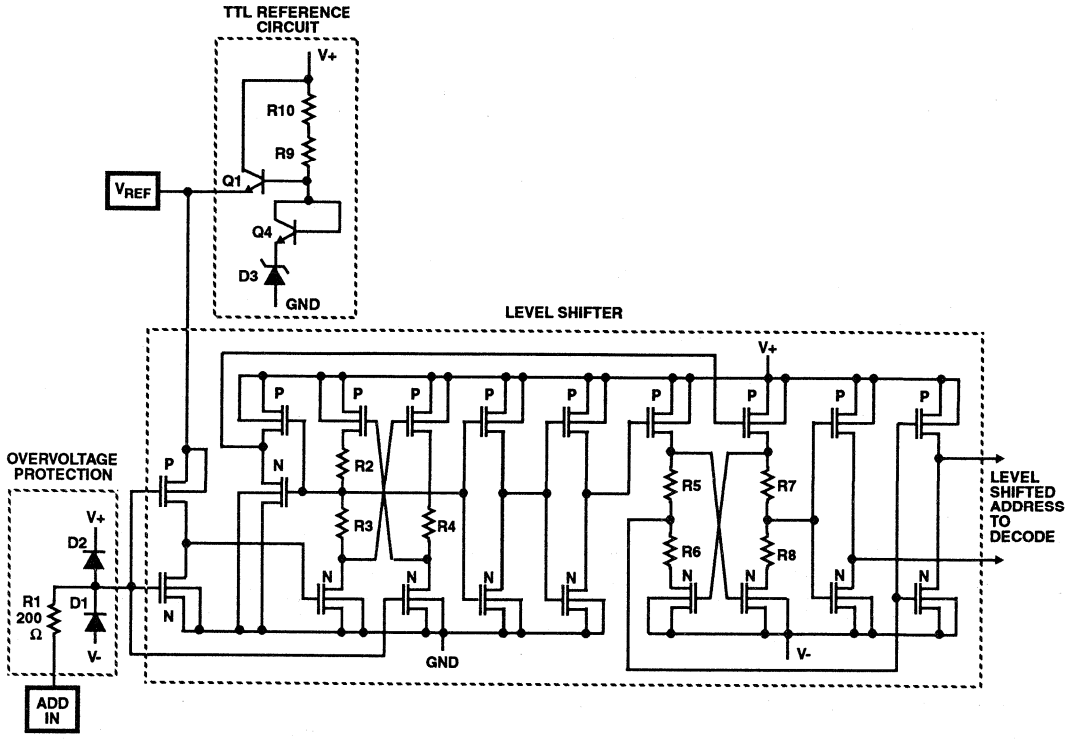


HI-509A

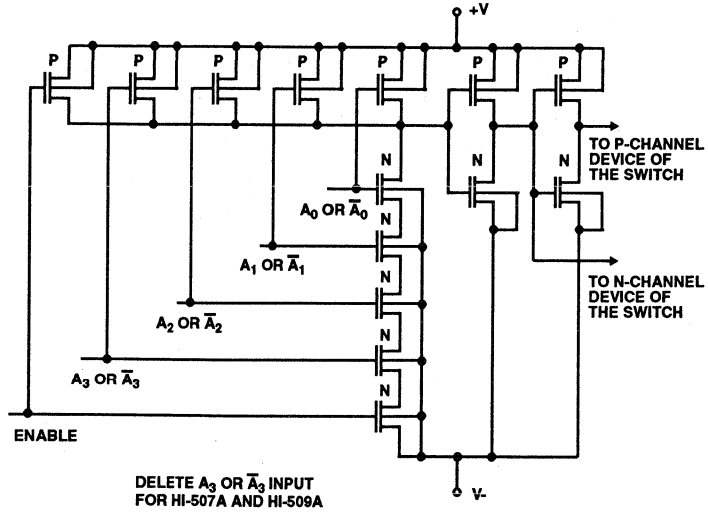


Schematic Diagrams

ADDRESS INPUT BUFFER AND LEVEL SHIFTER

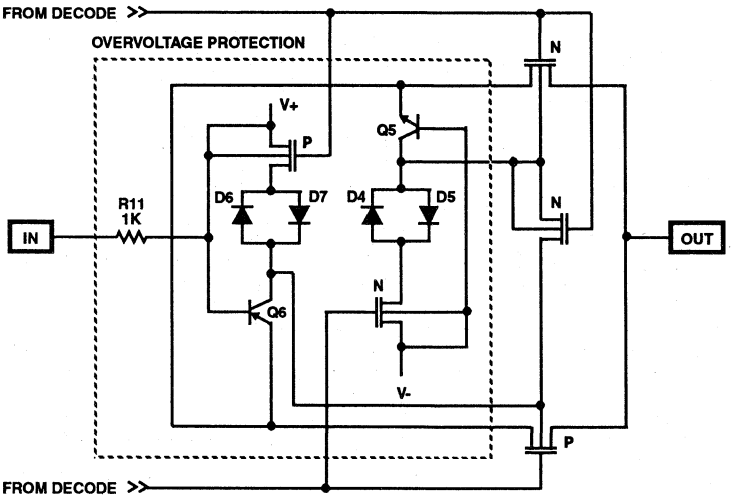


ADDRESS DECODER



Schematic Diagrams (Continued)

MULTIPLEX SWITCH



Absolute Maximum Ratings

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ ..... +44V
$V_{SUPPLY(+)}$ to GND ..... +22V
$V_{SUPPLY(-)}$ to GND ..... +25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed at 1ms, 10% duty cycle max)
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
28 Lead Ceramic DIP Packages (HI-506A, HI-507A)	20°C/W	55°C/W
16 Lead Ceramic DIP Packages (HI-508A, HI-509A)	24°C/W	80°C/W
28 Lead Plastic DIP Packages (HI-506A, HI-507A)		60°C/W
16 Lead Plastic DIP Packages (HI-508A, HI-509A)		100°C/W

Operating Temperature Ranges
HI-506A/507A/508A/509A-2, -8 ..... -55°C to +125°C
HI-506A/507A/508A/509A-5, -7 ..... 0°C to +75 °C
Junction Temperature
Ceramic DIP ..... +175°C
Plastic DIP ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves.

PARAMETER	TEMP	HI-50XA-2, -8			HI-50XA-5, -7			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS								
Access Time, t_A (Note 1)	+25°C	-	0.5	-	-	0.5	-	µs
	Full	-	-	1.0	-	-	1.0	µs
Break-Before-Make Delay, t_{OPEN} (Note 1)	+25°C	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$ (Note 1)	+25°C	-	300	500	-	300	-	ns
	Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$ (Note 1)	+25°C	-	300	500	-	300	-	ns
	Full	-	-	1000	-	-	1000	ns
Settling Time to 0.1%, t_S (HI-506A and HI-507A)	+25°C	-	1.2	-	-	1.2	-	µs
Settling Time to 0.01%, t_S (HI-506A and HI-507A)	+25°C	-	3.5	-	-	3.5	-	µs
Settling Time to 0.1%, t_S (HI-508A and HI-509A)	+25°C	-	1.2	-	-	1.2	-	µs
Settling Time to 0.01%, t_S (HI-508A and HI-509A)	+25°C	-	3.5	-	-	3.5	-	µs
"Off Isolation" (Note 6)	+25°C	50	68	-	50	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$	+25°C	-	12	-	-	12	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-506A)	+25°C	-	52	-	-	52	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-507A)	+25°C	-	30	-	-	30	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-508A)	+25°C	-	25	-	-	25	-	pF
Channel Output Capacitance, $C_{D(OFF)}$ (HI-509A)	+25°C	-	12	-	-	12	-	pF
Digital Input Capacitance, C_A	+25°C	-	10	-	-	10	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$	+25°C	-	0.1	-	-	0.1	-	pF
DIGITAL INPUT CHARACTERISTICS								
Input Low Threshold, TTL Drive, V_{AL} (Note 1)	Full	-	-	+0.8	-	-	+0.8	V
Input High Threshold, V_{AH} (Notes 1, 8)	Full	+4.0	-	-	+4.0	-	-	V
Input Leakage Current (High or Low), I_A (Notes 1, 5)	Full	-	-	1.0	-	-	1.0	µA
MOS Drive, V_{AL}, HI-506A/HI-507A (Note 9)	+25°C	-	-	0.8	-	-	0.8	V
MOS Drive, V_{AH}, HI-506A/HI-507A (Note 9)	+25°C	6.0	-	-	6.0	-	-	V

Electrical Specifications Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V, Unless Otherwise Specified. For Test Conditions, Consult Performance Curves. **(Continued)**

PARAMETER	TEMP	HI-50XA-2, -8			HI-50XA-5, -7			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS								
Analog Signal Range, V_S (Note 1)	Full	-15	-	+15	-15	-	+15	V
On Resistance, R_{ON}, (Notes 1, 2)	+25°C	-	1.2	1.5	-	1.5	1.8	kΩ
	Full	-	1.5	1.8	-	1.8	2.0	kΩ
Off Input Leakage Current, $I_{S(OFF)}$ (Notes 1, 3)	+25°C	-	0.03	-	-	0.03	-	nA
	Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$ (Notes 1, 3)	+25°C	-	0.1	-	-	0.1	-	nA
HI-506A	Full	-	-	300	-	-	300	nA
HI-507A	Full	-	-	200	-	-	200	nA
HI-508A	Full	-	-	200	-	-	200	nA
HI-509A	Full	-	-	100	-	-	100	nA
With Input Overvoltage Applied, (I_{DOFF}) (Note 4)	+25°C	-	4.0	-	-	4.0	-	nA
	Full	-	-	2.0	-	-	-	µA
On Channel Leakage Current, $I_{D(ON)}$ (Notes 1, 3)	+25°C	-	0.1	-	-	0.1	-	nA
HI-506A	Full	-	-	300	-	-	300	nA
HI-507A	Full	-	-	200	-	-	200	nA
HI-508A	Full	-	-	200	-	-	200	nA
HI-509A	Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current, I_{DIFF}, (HI-507A, HI-509A Only)	Full	-	-	50	-	-	50	nA
POWER REQUIREMENTS								
Current, I+, Pin 1 (Notes 1, 7)	Full	-	1.5	2.0	-	1.5	2.0	mA
Current, I+, HI-508A/HI-509A (Notes 1, 7)	Full	-	1.5	2.4	-	1.5	2.0	mA
Current, I-, Pin 27 (Notes 1, 7)	Full	-	0.02	1.0	-	0.02	1.0	mA
Power Dissipation, P_D	Full	-	7.5	-	-	7.5	-	mW

NOTES:

1. 100% tested for Dash 8. Leakage currents not tested at -55°C.
2. $V_{OUT} = \pm 10V$, $I_{OUT} = \mp 100\mu A$.
3. Ten nanoamps is the practical lower limit for high speed measurement in the production test environment.
4. Analog Overvoltage = ±33V.
5. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at +25°C.
6. $V_{EN} = 0.8V$, $R_L = 1K$, $C_L = 15pF$, $V_S = 7V_{RMS}$, f = 100kHz.
7. V_{EN}, $V_A = 0V$ or 4.0V.
8. To drive from DTL/TTL Circuits, 1kΩ pull-up resistors to +5.0V supply are recommended.
9. $V_{REF} = +10V$.

Performance Curves and Test Circuits

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified

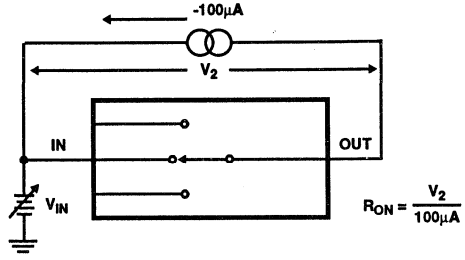


FIGURE 1A. TEST CIRCUIT

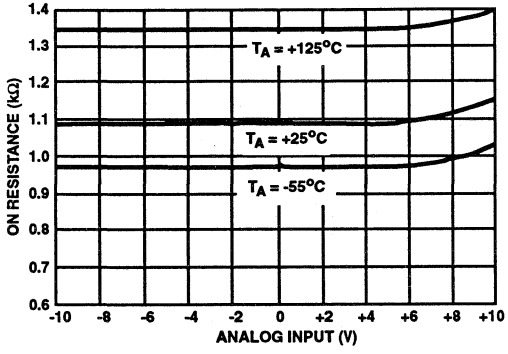


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

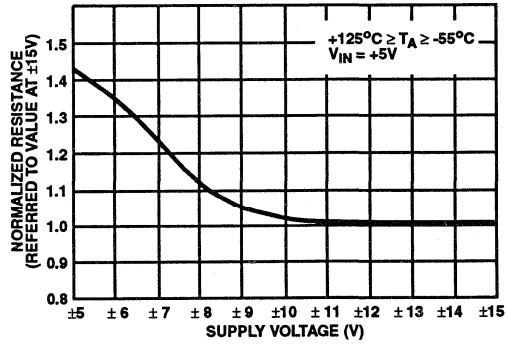


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

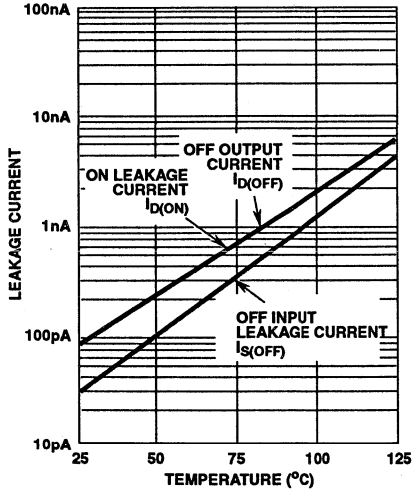


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

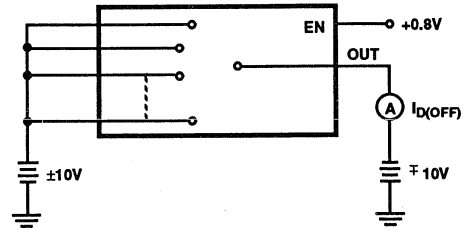


FIGURE 2B. $I_{D(OFF)}$ (NOTE 1)

NOTE:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V)

FIGURE 2. LEAKAGE CURRENTS

Performance Curves and Test Circuits

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified **(Continued)**

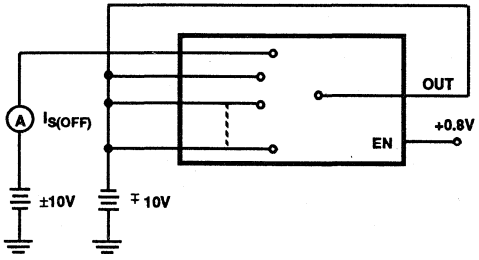


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT (NOTE 1)

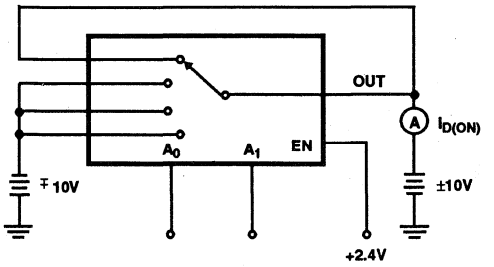


FIGURE 2D. $I_{D(On)}$ TEST CIRCUIT (NOTE 1)

NOTE:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V)

FIGURE 2. LEAKAGE CURRENTS (Continued)

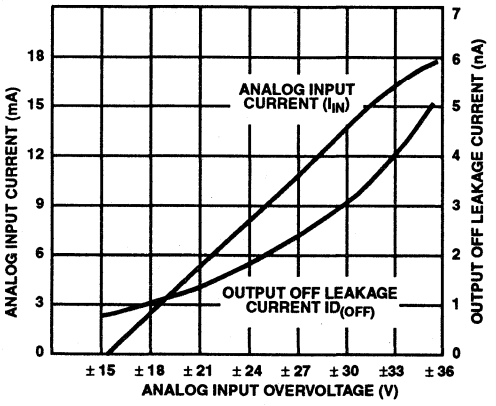


FIGURE 3A. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

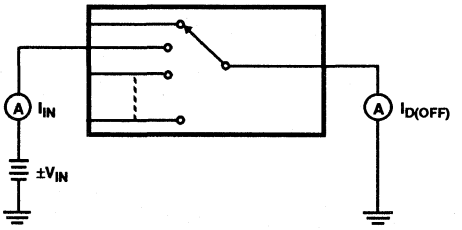


FIGURE 3B. TEST CIRCUIT

FIGURE 3. OVERVOLTAGE CHARACTERISTICS

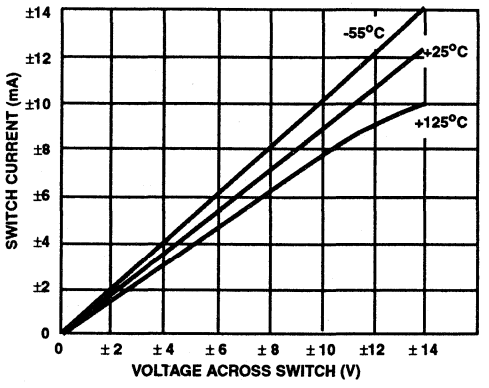


FIGURE 4A. ON CHANNEL CURRENT vs VOLTAGE

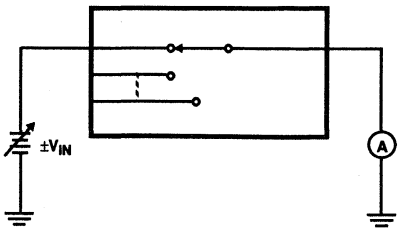


FIGURE 4B. TEST CIRCUIT

FIGURE 4. ON CHANNEL CURRENT

Performance Curves and Test Circuits

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified **(Continued)**

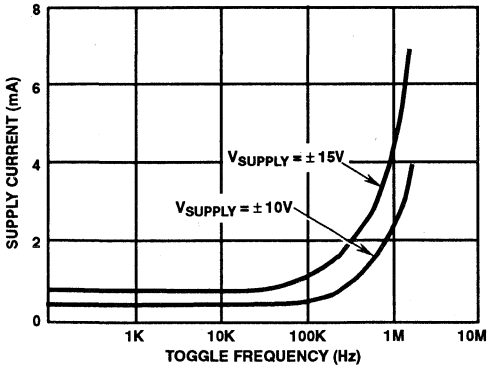
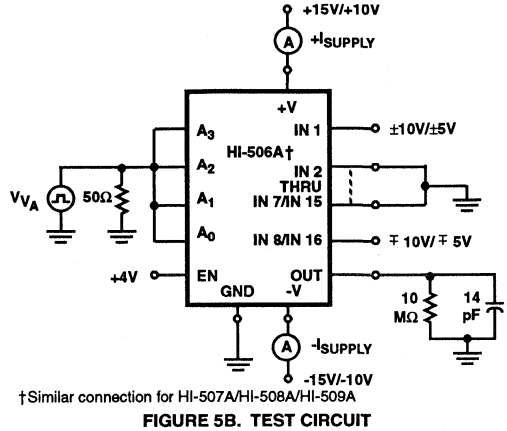


FIGURE 5A. SUPPLY CURRENT vs TOGGLE FREQUENCY



†Similar connection for HI-507A/HI-508A/HI-509A

FIGURE 5B. TEST CIRCUIT

FIGURE 5. SUPPLY CURRENTS

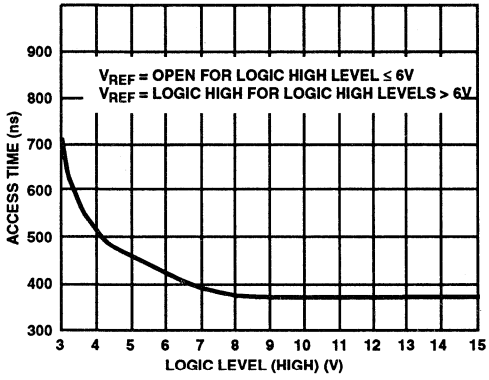
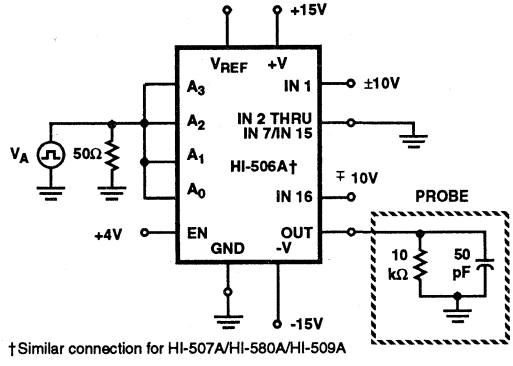


FIGURE 6A. ACCESS TIME vs LOGIC LEVEL (HIGH)



†Similar connection for HI-507A/HI-580A/HI-509A

FIGURE 6B. TEST CIRCUIT

FIGURE 6. ACCESS TIME

Switching Waveforms

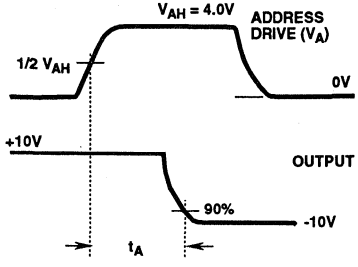


FIGURE 7A.

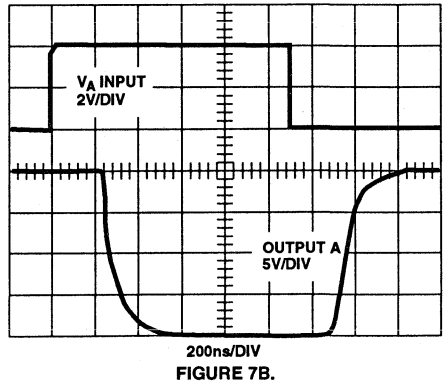
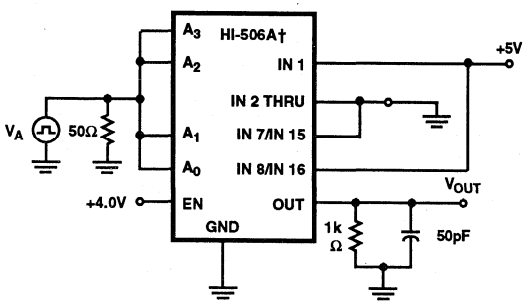


FIGURE 7B.

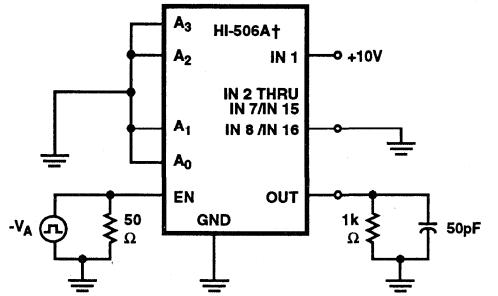
FIGURE 7. ACCESS TIME

Switching Waveforms (Continued)



†Similar connection for HI-507A/HI-508A/HI-509A

FIGURE 8A.



†Similar connection for HI-507A//HI-508A/HI-509A

FIGURE 9A.

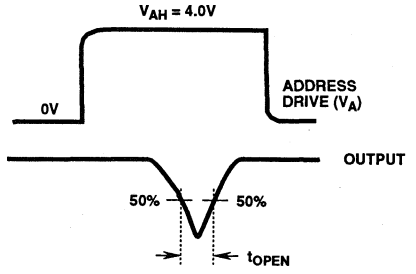


FIGURE 8B.

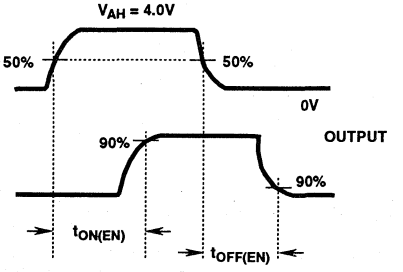


FIGURE 9B.

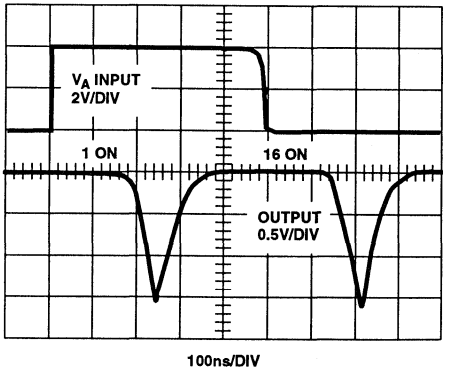


FIGURE 8C.

FIGURE 8. BREAK-BEFORE-MAKE DELAY

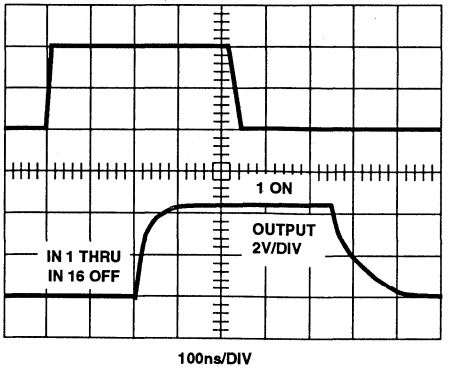


FIGURE 9C.

FIGURE 9. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

Truth Tables

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-508A

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Die Characteristics

DIE DIMENSIONS: 159 mils x 83.9 mils x 19 mils

METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Silox: 12kÅ ± 2kÅ
Nitride: 3.5kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
$1.4 \times 10^5 A/cm^2$

TRANSISTOR COUNT: 485

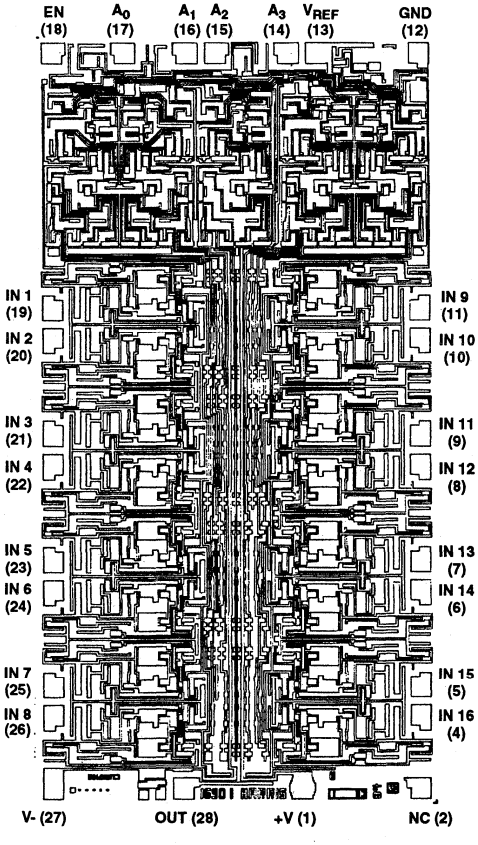
PROCESS: CMOS-DI

SUBSTRATE POTENTIAL*: $-V_{SUPPLY}$

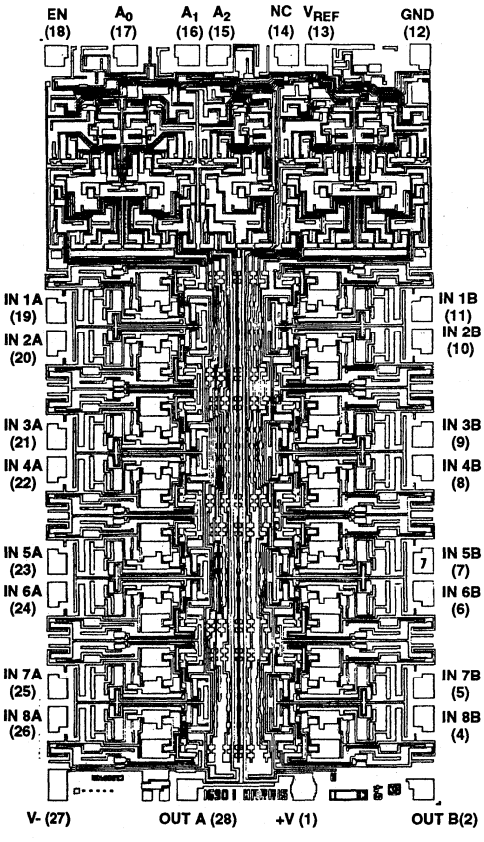
* The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential

Metallization Mask Layout

HI-506A



HI-507A



Die Characteristics

DIE DIMENSIONS: 108 mils x 83 mils

METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Silox: 12kÅ ± 2kÅ
Nitride: 3.5kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
$1.4 \times 10^5 A/cm^2$

TRANSISTOR COUNT: 253

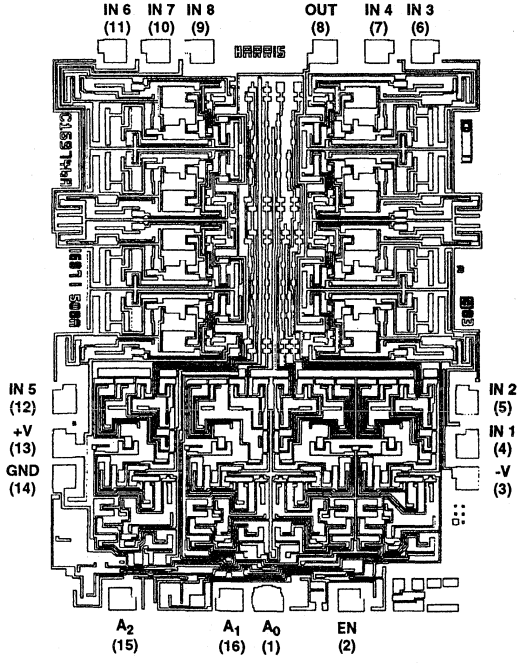
PROCESS: CMOS-DI

SUBSTRATE POTENTIAL*: $-V_{SUPPLY}$

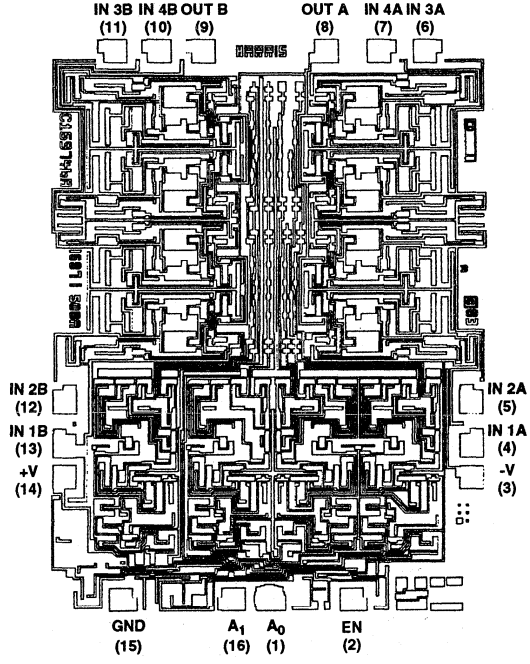
* The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential

Metallization Mask Layout

HI-508A



HI-509A



HARRIS SEMICONDUCTOR

HI-516

16 Channel/Differential 8 Channel CMOS High Speed Analog Multiplexer

December 1993

Features

- Access Time (Typical) 130ns
- Settling Time 250ns (0.1%)
- Low Leakage (Typical)
  - $I_{S(OFF)}$ 10pA
  - $I_{D(OFF)}$ 30pA
- Low Capacitance (Max)
  - $C_{S(OFF)}$ 10pF
  - $C_{D(OFF)}$ 25pF
- Off Isolation at 500kHz 55dB (Min)
- Low Charge Injection Error 20mV
- Single Ended to Differential Selectable (SDS)
- Logic Level Selectable (LLS)

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Industrial Control

Description

The HI-516 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_3 enables the HI-516 to be user programmed either as a single ended 16-channel multiplexer by connecting 'out A' to 'out B' and using A_3 as a digital address input, or as an 8-channel differential multiplexer by connecting A_3 to the V- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris Dielectric Isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I_{DOFF} < 100pA at +25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

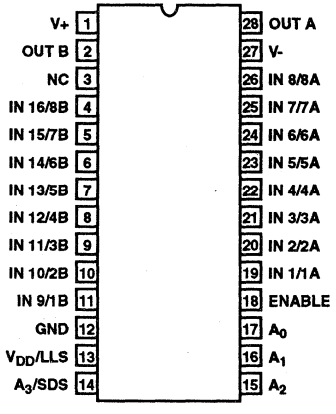
For MIL-STD-883 compliant parts, request the HI-516/883 data sheet.

Ordering Information

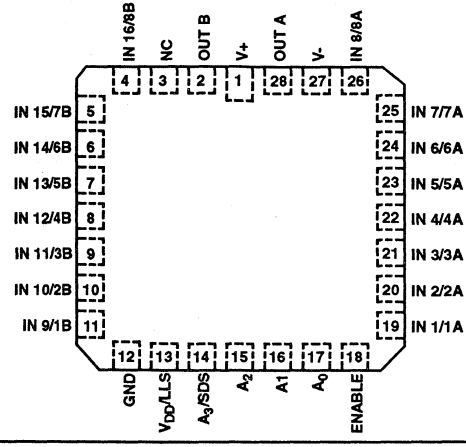
PART NUMBER	TEMP. RANGE	PACKAGE
HI4P0516-5	0°C to +75°C	28 Lead PLCC
HI3-0516-5	0°C to +75°C	28 Lead Plastic DIP
HI1-0516-5	0°C to +75°C	28 Lead Ceramic DIP
HI1-0516-2	-55°C to +125°C	28 Lead Ceramic DIP
HI1-0516-8	-55°C to +125°C	28 Lead Ceramic DIP
HI4-0516-8	-55°C to +125°C	28 Lead Ceramic LCC
HI9P0516-5	0°C to +75°C	28 Lead SOIC
HI9P0516-9	-40°C to +85°C	28 Lead SOIC
HI1-0516/883	-55°C to +125°C	28 Lead Ceramic DIP
HI4-0516/883	-55°C to +125°C	28 Lead Ceramic LCC

Pinouts

HI-516 (CDIP, PDIP, SOIC)
TOP VIEW



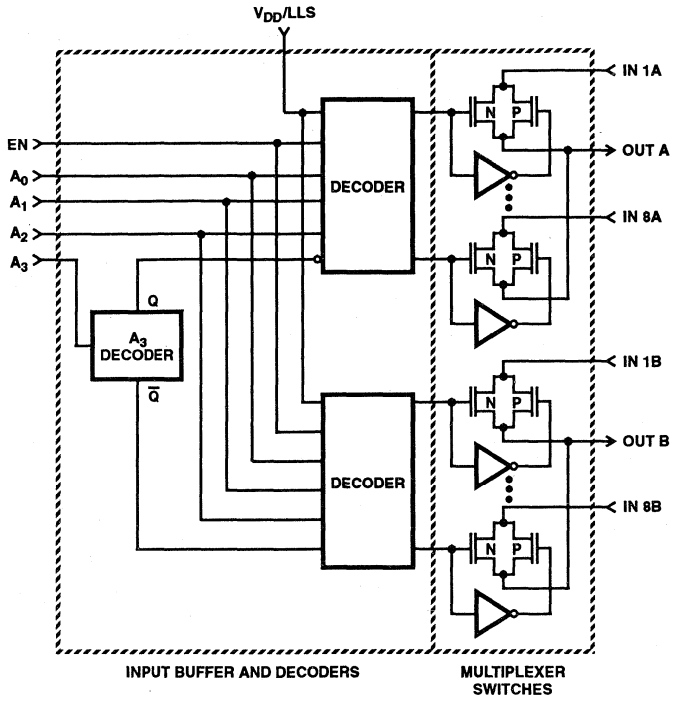
HI-516 (LCC, PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3146

Functional Block Diagram



A_3 DECODE		
A_3	Q	$\overline{Q}$
H	H	L
L	L	H
V-	L	L

Absolute Maximum Ratings (Note 1)

Voltage Between Supply Pins 33V
Analog Input Voltage
$+V_{IN}$ ..... $+V_{SUPPLY}$ +2V
$-V_{IN}$ ..... $-V_{SUPPLY}$ -2V
Digital Input Voltage
TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
$+V_A$ ..... +6V
$-V_A$ ..... -6V
$+A_3$/SDS ..... $+V_{SUPPLY}$ +2V
$-A_3$/SDS ..... $-V_{SUPPLY}$ -2V
CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
$+V_A$ ..... $+V_{SUPPLY}$ +2V
$-V_A$ ..... -2V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	60°C/W	-
Plastic SOIC Package	70°C/W	-
Plastic PLCC Package	70°C/W	-
Ceramic DIP Package	50°C/W	18°C/W
Ceramic LCC Package	60°C/W	8°C/W

Junction Temperature
Ceramic DIP, Ceramic LCC ..... +175°C
Plastic DIP, Plastic SOIC, Plastic PLCC ..... +150°C
Operating Temperature Ranges
HI-516-2,-8 ..... -55°C to +125°C
HI-516-5 ..... 0°C to +75°C
HI-516-9 ..... -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 1) Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP	HI-516-2, -8			HI-516-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_I	Note 2	Full	-14	-	+14	-15	-	+15	V
On Resistance, R_{ON}	Note 3	+25°C	-	620	750	-	620	750	Ω
		Full	-	-	1,000	-	-	1,000	Ω
Off Input Leakage Current, $I_{S(OFF)}$		+25°C	-	0.01	-	-	0.01	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$		+25°C	-	0.03	-	-	0.03	-	nA
		Full	-	-	100	-	-	100	nA
On Channel Leakage Current, $I_{D(ON)}$		+25°C	-	0.04	-	-	0.04	-	nA
		Full	-	-	100	-	-	100	nA
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL} (TTL)		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH} (TTL)		Full	2.4	-	-	2.4	-	-	V
Input Low Threshold, V_{AL} (CMOS)		Full		-	$0.3V_{DD}$	-	-	$0.3V_{DD}$	V
Input High Threshold, V_{AH} (CMOS)		Full	$0.7V_{DD}$	-	-	$0.7V_{DD}$	-	-	V
Input Leakage Current, I_{AH} (High)		Full	-	-	1	-	-	1	µA
Current, I_{AL} (Low)		Full	-	-	25	-	-	25	µA
SWITCHING CHARACTERISTICS									
Access Time, t_A		+25°C	-	130	175	-	130	175	ns
		Full	-	-	225	-	-	225	ns
Break-Before-Make Delay, t_{OPEN}		+25°C	10	20	-	10	20	-	ns
Enable Delay (ON), $t_{ON(EN)}$		+25°C	-	120	175	-	120	175	ns
Enable Delay (OFF), $t_{OFF(EN)}$		+25°C	-	140	175	-	140	175	ns
Settling Time									
0.1%		+25°C	-	250	-	-	250	-	ns
0.01%		+25°C	-	800	-	-	800	-	ns
Charge Injection Error	Note 4	+25°C	-	-	20	-	-	20	mV

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 1) Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP	HI-516-2, -8			HI-516-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS (Continued)									
Off Isolation	Note 5	+25°C	55	-	-	55	-	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		+25°C	-	-	10	-	-	10	pF
Channel Output Capacitance, $C_{D(OFF)}$		+25°C	-	-	25	-	-	25	pF
Digital Input Capacitance, C_A		+25°C	-	-	10	-	-	10	pF
Input to Output Capacitance, $C_{DS(OFF)}$		+25°C	-	0.02	-	-	0.02	-	pF
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, PD		Full	-	-	750	-	-	900	mW
I+, Current	Note 6	Full	-	-	25	-	-	30	mA
I-, Current	Note 6	Full	-	-	25	-	-	30	mA

NOTES:

1. V_{DD}/LLS pin = open or grounded for TTL compatibility. V_{DD}/LLS pin = V_{DD} for CMOS compatibility.
2. At temperatures above +90°C, care must be taken to assure V_{IN} remains at least 1.0V below the V_{SUPPLY} for proper operation.
3. V_{IN} = ±10V, I_{OUT} = -100µA.
4. V_{IN} = 0V, C_L = 100pF, enable input pulse = 3V, f = 500kHz.
5. V_{EN} = 0.8V, V_S = $3V_{RMS}$, f = 500kHz, C_L = 40pF, R_L = 1K, Pin 3 grounded.
6. V_{EN} = +2.4V.

TRUTH TABLE HI-516 Used as a 16-Channel Multiplexer or 8-Channel Differential Multiplexer (Note 1)

USE A_3 AS DIGITAL ADDRESS INPUT					ON CHANNEL TO	
ENABLE	A_3	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	X	None	None
H	L	L	L	L	1A	None
H	L	L	L	H	2A	None
H	L	L	H	L	3A	None
H	L	L	H	H	4A	None
H	L	H	L	L	5A	None
H	L	H	L	H	6A	None
H	L	H	H	L	7A	None
H	L	H	H	H	8A	None
H	H	L	L	L	None	1B
H	H	L	L	H	None	2B
H	H	L	H	L	None	3B
H	H	L	H	H	None	4B
H	H	H	L	L	None	5B
H	H	H	L	H	None	6B
H	H	H	H	L	None	7B
H	H	H	H	H	None	8B

NOTE:

1. For 16-channel single-ended function, tie 'out A' to 'out B', for dual 8-channel function use the A_3 address pin to select between MUX A and MUX B, where MUX A is selected with A_3 low.

TRUTH TABLE HI-516 Used as a Differential 8-Channel Multiplexer

A_3 CONNECT TO V- SUPPLY				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	1B
H	L	L	H	2A	2B
H	L	H	L	3A	3B
H	L	H	H	4A	4B
H	H	L	L	5A	5B
H	H	L	H	6A	6B
H	H	H	L	7A	7B
H	H	H	H	8A	8B

Test Circuits

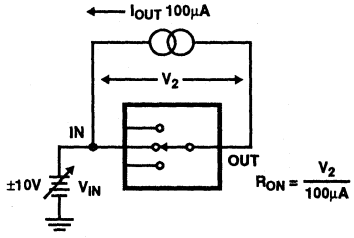


FIGURE 1. ON RESIGTANCE vs INPUT SIGNAL LEVEL

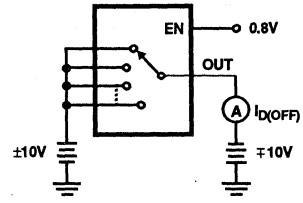


FIGURE 2. $I_{D(OFF)}$ (NOTE 1)

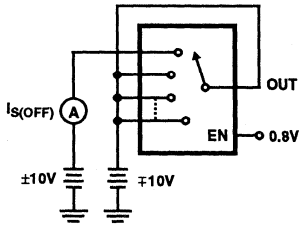


FIGURE 3. $I_{S(OFF)}$ (NOTE 1)

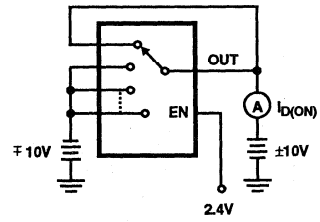


FIGURE 4. $I_{D(ON)}$ (NOTE 1)

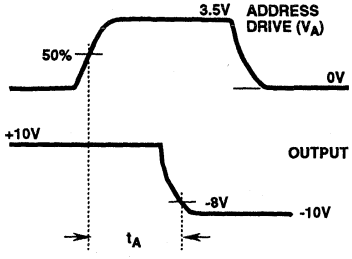


FIGURE 5A.

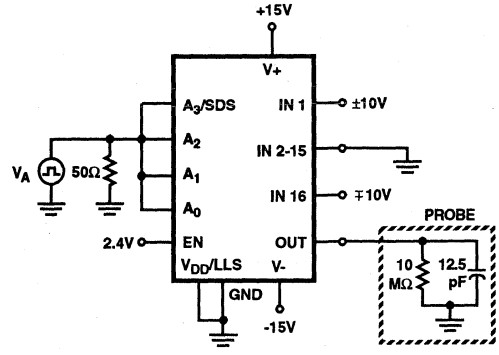


FIGURE 5B.

FIGURE 5. ACCESS TIME

NOTE:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V)

Test Circuits (Continued)

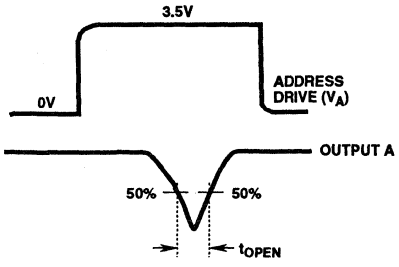


FIGURE 6A. ENABLE DRIVE

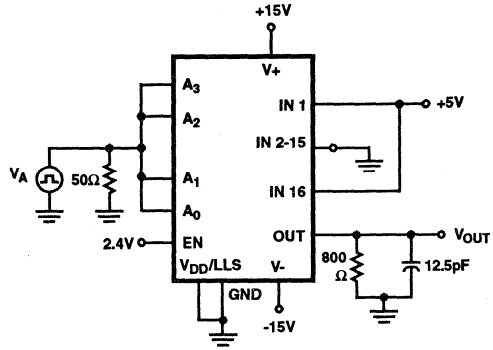


FIGURE 6B.

FIGURE 6. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

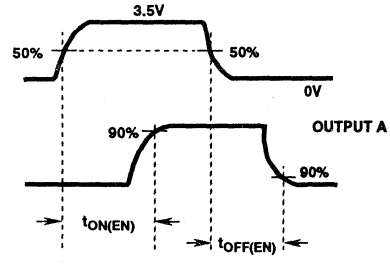


FIGURE 7A. ENABLE DRIVE

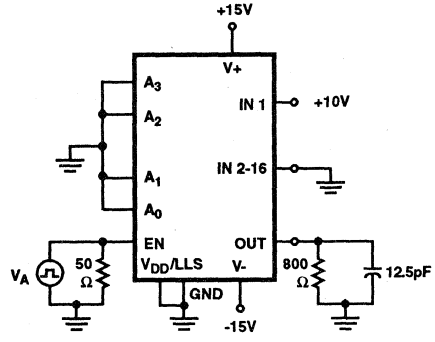


FIGURE 7B.

FIGURE 7. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

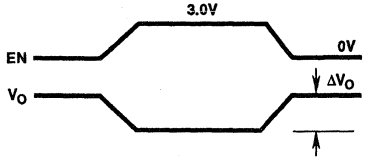


FIGURE 8A.

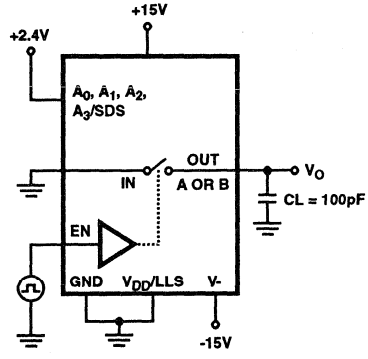


FIGURE 8B.

ΔV_O is the measured voltage error due to charge injection. The error voltage in coulombs is $Q = C_L \times \Delta V_O$

FIGURE 8. CHARGE INJECTION TEST CIRCUIT

Die Characteristics

DIE DIMENSIONS:
2250µm x 3720µm x 485µm ±25µm

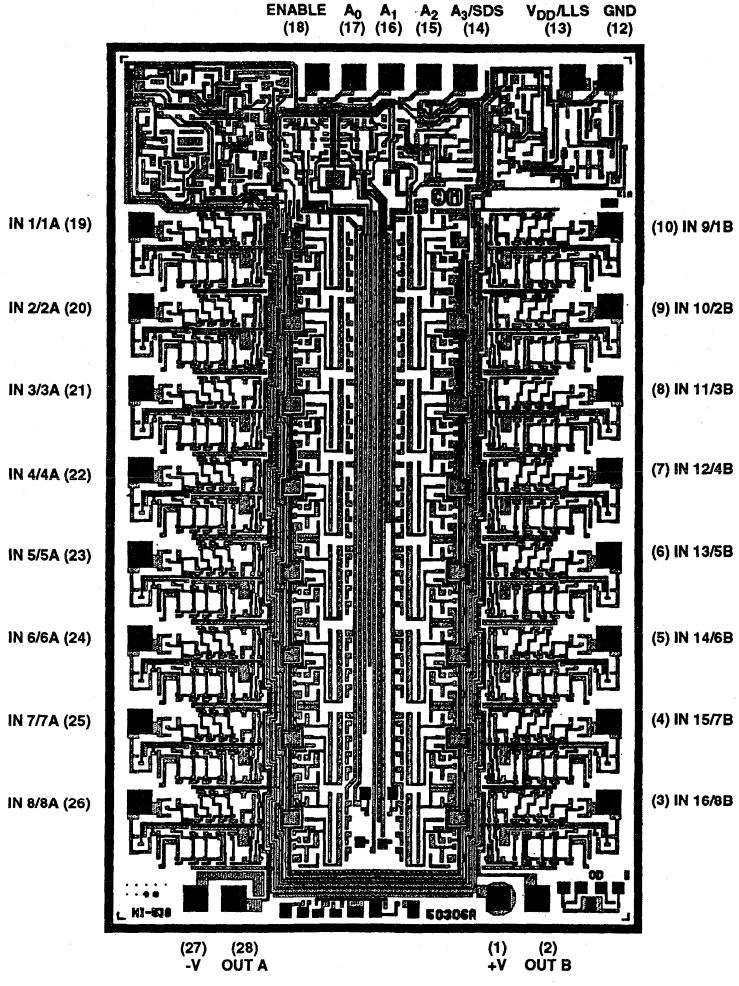
METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ± 1kÅ
Silox Thickness: 12kÅ ± 2kÅ

WORST CASE CURRENT DENSITY: $1.64 \times 10^5 A/cm^2$

Metallization Mask Layout

HI-516



HARRIS SEMICONDUCTOR

HI-518

8 Channel/Differential 4 Channel CMOS High Speed Analog Multiplexer

December 1993

Features

- Access Time (Typical) 130ns
- Settling Time 250ns (0.1%)
- Low Leakage (Typical)
  - $I_{S(OFF)}$ 10pA
  - $I_{D(OFF)}$ 15pA
- Low Capacitance (Max)
  - $C_{S(OFF)}$ 5pF
  - $C_{D(OFF)}$ 10pF
- Off Isolation at 500kHz 45dB (Min)
- Low Charge Injection Error 25mV
- Single Ended to Differential Selectable (SDS)
- Logic Level Selectable (LLS)

Applications

- Data Acquisition Systems
- Precision Instrumentation
- Industrial Control

Description

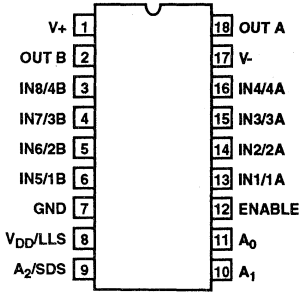
The HI-518 is a monolithic dielectrically isolated, high speed, high performance CMOS analog multiplexer. It offers unique built-in channel selection decoding plus an inhibit input for disabling all channels. The dual function of address input A_2 enables the HI-518 to be user programmed either as a single ended 8-channel multiplexer by connecting 'out A' to 'out B' and using A_2 as a digital address input, or as a 4-channel differential multiplexer by connecting A_2 to the V- supply. The substrate leakages and parasitic capacitances are reduced substantially by using the Harris Dielectric Isolation process to achieve optimum performance in both high and low level signal applications. The low output leakage current (I_{DOFF} < 100pA at +25°C) and fast settling (t_{SETTLE} = 800ns to 0.01%) characteristics of the device make it an ideal choice for high speed data acquisition systems, precision instrumentation, and industrial process control.

Ordering Information

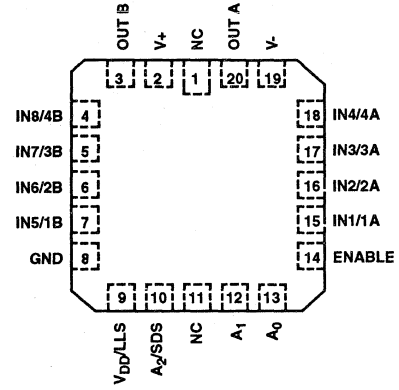
PART NUMBER	TEMP. RANGE	PACKAGE
HI3-0518-5	0°C to +75°C	18 Lead Plastic DIP
HI1-0518-5	0°C to +75°C	18 Lead Ceramic DIP
HI1-0518-2	-55°C to +125°C	18 Lead Ceramic DIP
HI1-0518-8	-55°C to +125°C	18 Lead Ceramic DIP
HI4P0518-5	0°C to +75°C	20 Lead Plastic PLCC
HI4-0518-8	-55°C to +125°C	20 Lead Ceramic LCC
HI1-0518-9	-40°C to +85°C	18 Lead Ceramic DIP
HI3-0518-9	-40°C to +85°C	18 Lead Plastic DIP
HI4P-0518-9	-40°C to +85°C	20 Lead Plastic LCC
HI9P-0518-5	0°C to +75°C	18 Lead SOIC
HI9P-0518-9	-40°C to +85°C	18 Lead SOIC

Pinouts

HI-518 (CDIP, PDIP)
TOP VIEW



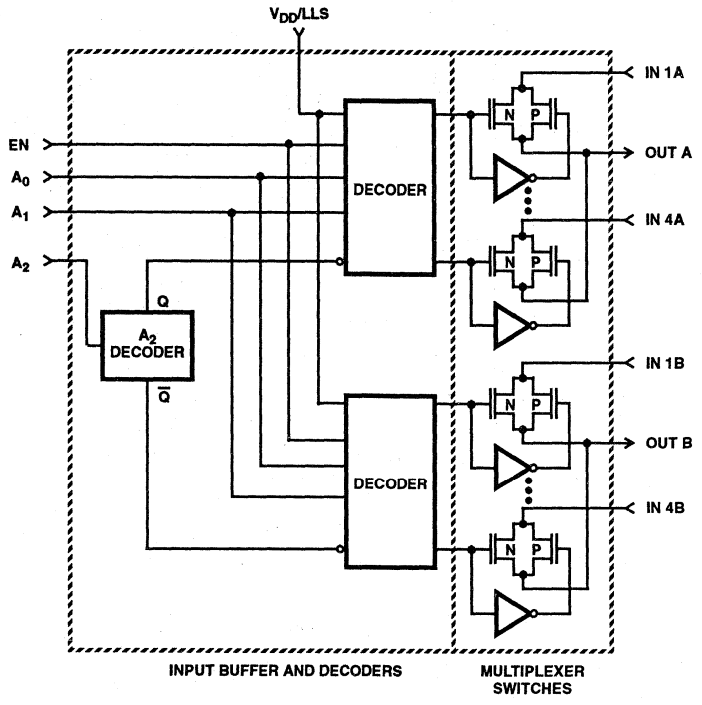
HI-518 (LCC, PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3147

Functional Block Diagram



A_2 DECODE		
A_2	Q	$\overline{Q}$
H	H	L
L	L	H
V-	L	L

Absolute Maximum Ratings (Note 1)

V+ to V- 33V
Analog Input Voltage
$+V_{IN}$ ..... (V+) +2V
$-V_{IN}$ ..... (V-) -2V
Digital Input Voltage
TTL Levels Selected (V_{DD}/LLS Pin = GND or Open)
$+V_A$ ..... +6V
$-V_A$ ..... -6V
$+A_2$/SDS ..... (V+) +2V
$-A_2$/SDS ..... (V-) -2V
CMOS Levels Selected (V_{DD}/LLS Pin = V_{DD})
$+V_A$ ..... (V+) +2V
$-V_A$ ..... -2V
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	90°C/W	-
Plastic PLCC Package	80°C/W	-
Ceramic DIP Package	77°C/W	23°C/W
Ceramic LCC Package	65°C/W	12°C/W
SOIC Package	100°C/W	-

Junction Temperature
Ceramic DIP, Ceramic LCC ..... +175°C
Plastic DIP, Plastic PLCC, SOIC ..... +150°C
Operating Temperature Ranges
HI-518-2,-8 ..... -55°C to +125°C
HI-518-5 ..... 0°C to +75°C
HI-518-9 ..... -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 1), Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP	HI-518-2, -8			HI-518-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, t_A		+25°C	-	130	175	-	130	175	ns
		Full	-	-	225	-	-	225	ns
Break-Before-Make Delay, t_{OPEN}		+25°C	10	20	-	10	20	-	ns
Enable Delay (ON), $t_{ON(EN)}$		+25°C	-	120	175		120	175	ns
Enable Delay (OFF), $t_{OFF(EN)}$		+25°C	-	140	175		140	175	ns
Settling Time									
0.1%		+25°C	-	250	-	-	250	-	ns
0.01%		+25°C	-	800	-	-	800	-	ns
Charge Injection Error	Note 4	+25°C	-	-	25	-	-	25	mV
Off Isolation	Note 5	+25°C	45	-	-	45	-	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		+25°C	-	-	5	-	-	5	pF
Channel Output Capacitance, $C_{D(OFF)}$		+25°C	-	-	10	-	-	10	pF
Digital Input Capacitance, C_A		+25°C	-	-	5	-	-	5	pF
Input to Output Capacitance, $C_{DS(OFF)}$		+25°C	-	0.02		-	0.02	-	pF
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, V_{AL} (TTL)		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH} (TTL)		Full	2.4	-	-	2.4	-	-	V
Input Low Threshold, V_{AL} (CMOS)		Full		-	$0.3V_{DD}$	-	-	$0.3V_{DD}$	V
Input High Threshold, V_{AH} (CMOS)		Full	$0.7V_{DD}$	-	-	$0.7V_{DD}$	-	-	V
Input Leakage Current, I_{AH} (High)		Full	-	-	1	-	-	1	µA
Input Leakage Current, I_{AL} (Low)		Full	-	-	20	-	-	20	µA

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4V, V_{AL} (Logic Level Low) = +0.8V; V_{DD}/LLS = GND. (Note 1), Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP	HI-518-2, -8			HI-518-5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_{IN}	Note 2	Full	-14		+14	-15	-	+15	V
On Resistance, R_{ON}	Note 3	+25°C	-	480	750	-	480	750	Ω
		Full	-	-	1,000	-	-	1,000	Ω
Off Input Leakage Current, $I_{S(OFF)}$		+25°C	-	0.01	-	-	0.01	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$		+25°C	-	0.015	-	-	0.015	-	nA
		Full	-	-	50	-	-	50	nA
On Channel Leakage Current, $I_{D(ON)}$		+25°C	-	0.015	-	-	0.015	-	nA
		Full	-	-	50	-	-	50	nA
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, P_D		Full	-	-	450	-	-	540	mW
I+, Current	Note 6	Full	-	-	15	-	-	18	mA
I-, Current	Note 6	Full	-	-	15	-	-	18	mA

NOTES:

1. V_{DD}/LLS pin = open or grounded for TTL compatibility. V_{DD}/LLS pin = V_{DD} for CMOS compatibility.
2. At temperatures above +90°C, care must be taken to assure V_{IN} remains at least 1.0V below the V_{SUPPLY} for proper operation.
3. V_{IN} = ±10V, I_{OUT} = -100µA.
4. V_{IN} = 0V, C_L = 100pF, enable input pulse = 3V, f = 500kHz.
5. C_L = 40pF, R_L = 1k. Due to the pin to pin capacitance between IN 8/4B and OUT B, channel 8/4B exhibits 60dB of OFF isolation under the above test conditions.
6. V_{EN} = +2.4V.

TRUTH TABLE HI-518 Used as an 8-Channel Multiplexer or 4-Channel Differential Multiplexer

USE A_2 AS DIGITAL ADDRESS INPUT				ON CHANNEL TO	
ENABLE	A_2	A_1	A_0	OUT A	OUT B
L	X	X	X	None	None
H	L	L	L	1A	None
H	L	L	H	2A	None
H	L	H	L	3A	None
H	L	H	H	4A	None
H	H	L	L	None	1B
H	H	L	H	None	2B
H	H	H	L	None	3B
H	H	H	H	None	4B

TRUTH TABLE HI-518 Used as a Differential 4-Channel Multiplexer

A_2 CONNECT TO V- SUPPLY			ON CHANNEL TO	
ENABLE	A_1	A_0	OUT A	OUT B
L	X	X	None	None
H	L	L	1A	1B
H	L	H	2A	2B
H	H	L	3A	3B
H	H	H	4A	4B

Test Circuits

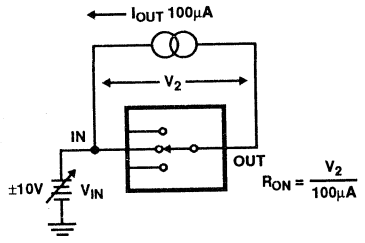


FIGURE 1. ON RESISTANCE vs INPUT SIGNAL LEVEL

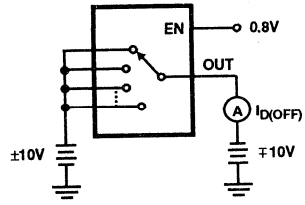


FIGURE 2. $I_{D(OFF)}$ (NOTE 1)

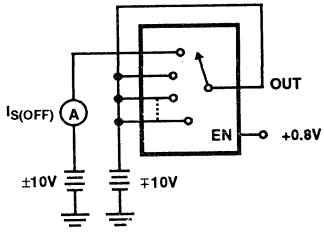


FIGURE 3. $I_{S(OFF)}$ (NOTE 1)

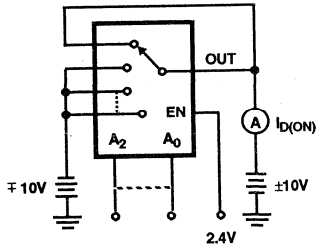


FIGURE 4. $I_{D(ON)}$ (NOTE 1)

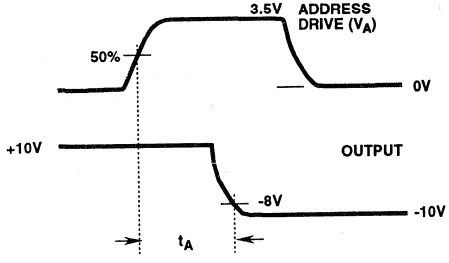


FIGURE 5A.

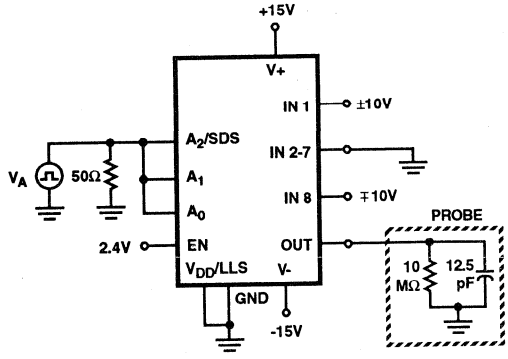


FIGURE 5B.

FIGURE 5. ACCESS TIME

NOTE:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V)

Test Circuits (Continued)

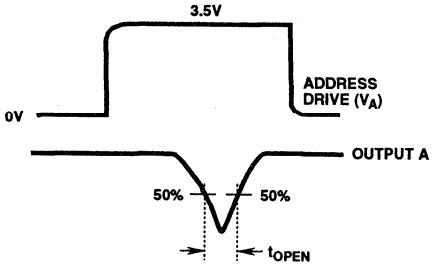


FIGURE 6A.

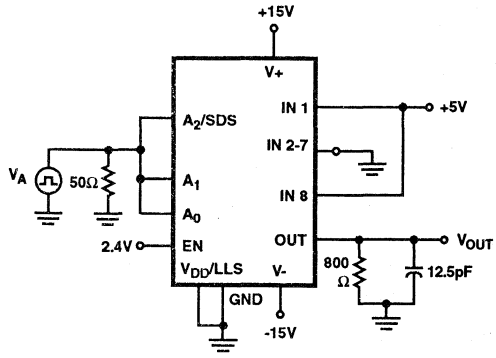


FIGURE 6B.

FIGURE 6. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

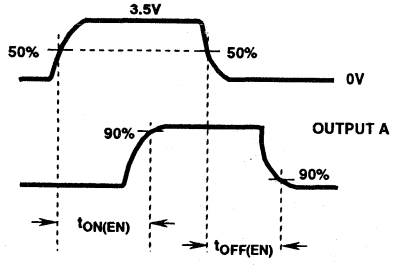


FIGURE 7A.

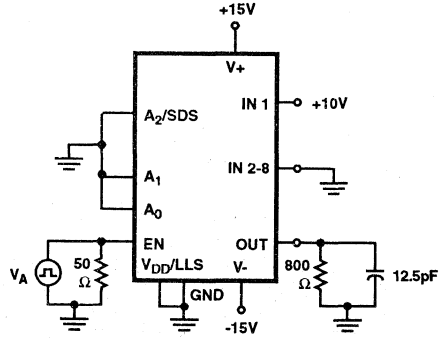


FIGURE 7B.

FIGURE 7. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$

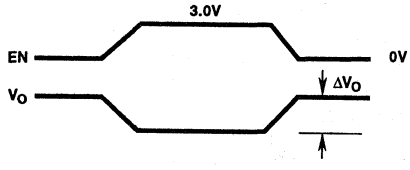


FIGURE 8A.

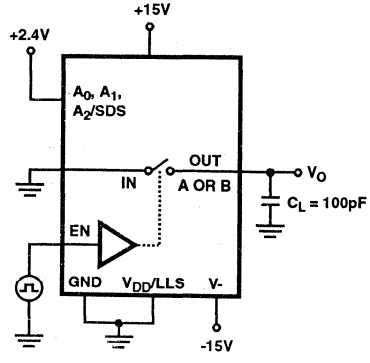


FIGURE 8B.

ΔV_O is the measured voltage error due to charge injection. The error voltage in coulombs is $Q = C_L \times \Delta V_O$

FIGURE 8. CHARGE INJECTION TEST CIRCUIT

Die Characteristics

DIE DIMENSIONS:
89 x 93 mils

METALLIZATION:
Type: Al Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ±1.0kÅ
Silox Thickness: 12kÅ ± 2.0kÅ

WORST CASE CURRENT DENSITY: $1.43 \times 10^5 A/cm^2$

TRANSISTOR COUNT: 356

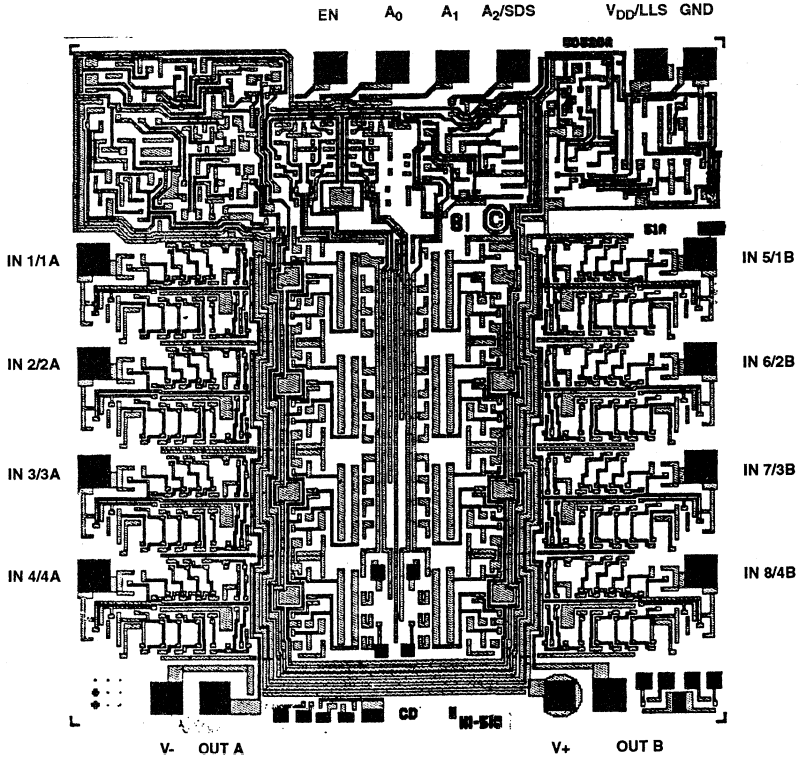
PROCESS: CMOS-DI

SUBSTRATE POTENTIAL*: $-V_{SUPPLY}$

* The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential

Metallization Mask Layout

HI-518



HARRIS SEMICONDUCTOR

HI-524

4 Channel Wideband and Video Multiplexer

December 1993

Features

- Crosstalk (10MHz) < -60dB
- Fast Access Time 150ns
- Fast Settling Time 200ns
- TTL Compatible

Applications

- Wideband Switching
- Radar
- TV Video
- ECM

Ordering Information

PART NUMBER	TEMP. RANGE	PACKAGE
HI1-0524-5	0°C to +75°C	18 Lead Ceramic DIP
HI1-0524-2	-55°C to +125°C	18 Lead Ceramic DIP
HI4P0524-5	0°C to +75°C	20 Lead PLCC
HI3-0524-5	0°C to +75°C	18 Lead Plastic DIP
HI1-0524-8	-55°C to +125°C	18 Lead Ceramic DIP
HI4-0524-8	-55°C to +125°C	20 Lead LCC
HI1-0524/883	-55°C to +125°C	18 Lead Ceramic DIP
HI4-0524/883	-55°C to +125°C	20 Lead LCC

Description

The HI-524 is a four channel CMOS analog multiplexer designed to process single-ended signals with bandwidths up to 10MHz. The chip includes a 1 of 4 decoder for channel selection and an enable input to inhibit all channels (chip select).

Three CMOS transmission gates are used in each channel, as compared to the single gate in more conventional CMOS multiplexers. This provides a double barrier to the unwanted coupling of signals from each input to the output. In addition, Dielectric Isolation (DI) processing helps to insure the Crosstalk is less than -60dB at 10MHz.

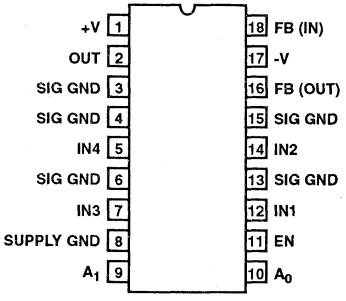
The HI-524 is designed to operate into a wideband buffer amplifier such as the Harris HA-2541. The multiplexer chip includes two "ON" switches in series, for use as a feedback element with the amplifier. This feedback resistance matches and tracks the channel R_{ON} resistance, to minimize the amplifier V_{OS} and its variation with temperature.

The HI-524 is well suited to the rapid switching of video and other wideband signals in telemetry, instrumentation, radar and video systems.

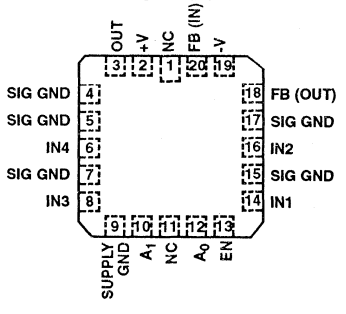
For MIL-STD-883 compliant parts, request the HI-524/883 data sheet.

Pinouts

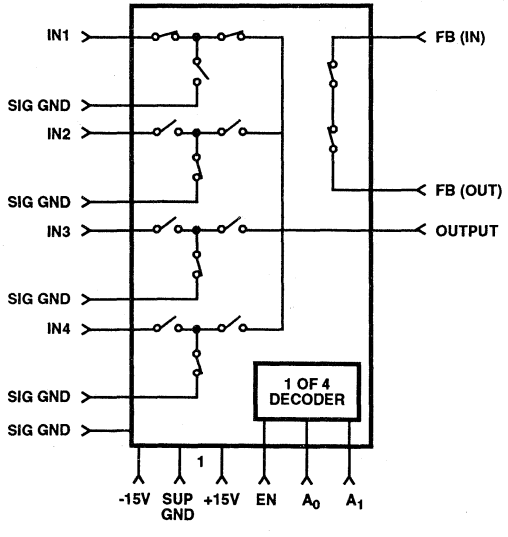
(CDIP, PDIP)
TOP VIEW



(LCC, PLCC)
TOP VIEW



Functional Diagram



10 MULTIPLEXERS

File Number 3148

Absolute Maximum Ratings

Voltage Between Supplies 33V
Digital Input Voltage
$+V_A$ ..... +6V
$-V_A$ ..... -6V
Analog Input Voltage
$+V_{IN}$ ..... $+V_{SUPPLY}$ +2.0V
$-V_{IN}$ ..... $-V_{SUPPLY}$ -2.0V
Either Supply to Ground 16.5V
Storage Temperature
(CDIP, CLCC) ..... -65°C to +150°C
(PLCC) ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	80°C/W	24°C/W
LCC Package	75°C/W	20°C/W
Plastic DIP Package	90°C/W	-
PLCC Package	80°C/W	-

Operating Temperature Range
HI-524-2, -8 ..... -55°C to +125°C
HI-524-5 ..... 0°C to +75°C
Junction Temperature ..... +175°C
(CDIP, CLCC) ..... +175°C
(PLCC, PDIP) ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4v, V_{AL} = (Logic Level Low) = +0.5V; V_{EN} = +2.4V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP	HI-524-2/-8			HI-524-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
SWITCHING CHARACTERISTICS									
Access Time, t_A	(Note 5)	+25°C	-	150	300	-	150	300	ns
Break-Before-Make Delay, t_{OPEN}	(Note 5)	+25°C	-	20	-	-	20	-	ns
Enable Delay (ON), R_L = 500Ω, $t_{ON\ (EN)}$		+25°C	-	180	300	-	180	-	ns
Enable Delay (OFF), R_L = 500Ω, $t_{OFF\ (EN)}$		+25°C	-	180	250	-	180	-	ns
Settling Time									
(0.1%)	(Note 5)	+25°C	-	200	-	-	200	-	ns
(0.01%)		+25°C	-	600	-	-	600	-	ns
Crosstalk	(Note 6)	+25°C	-	-65	-	-	-65	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		+25°C	-	4	-	-	4	-	pF
Channel Output Capacitance, $C_{D(OFF)}$		+25°C	-	10	-	-	10	-	pF
Digital Input Capacitance, C_A		+25°C	-	5	-	-	5	-	pF
DIGITAL INPUT SPECIFICATIONS									
Input Low Threshold (TTL), V_{AL}		Full	-	-	0.8	-	-	0.8	V
Input High Threshold (TTL), V_{AH}		Full	2.4	-	-	2.4	-	-	V
Input Leakage Current (High), I_{AH}		Full	-	0.05	1	-	0.05	1	µA
Current (Low), A_L		Full	-	-	25	-	-	25	µA
ANALOG CHANNEL SPECIFICATIONS									
Analog Signal Range, V_{IN}		Full	-10	-	+10	-10	-	+10	V
On Resistance, R_{ON}	(Note 2)	+25°C	-	700	-	-	700	-	Ω
		Full	-	-	1.5	-	-	1.5	KΩ
Off Input Leakage Current, $I_{S\ (OFF)}$	(Note 3)	+25°C	-	0.2	-	-	0.2	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D\ (OFF)}$	(Note 3)	+25°C	-	0.2	-	-	0.2	-	nA
		Full	-	-	50	-	-	50	nA
On Channel Leakage Current, $I_{D\ (ON)}$	(Note 3)	+25°C	-	0.7	-	-	0.7	-	nA
		Full	-	-	50	-	-	50	nA
3dB Bandwidth	(Note 4)	+25°C	-	8	-	-	8	-	MHz

Electrical Specifications Supplies = +15V, -15V; V_{AH} (Logic Level High) = +2.4v, V_{AL} = (Logic Level Low) = +0.5V; V_{EN} = +2.4V, Unless Otherwise Specified **(Continued)**

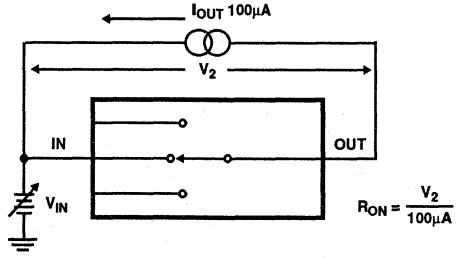
PARAMETER	TEST CONDITIONS	TEMP	HI-524-2/-8			HI-524-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY CHARACTERISTICS									
Power Dissipation, P_D		Full	-	-	750	-	-	750	mW
Current, I+	(Note 7)	Full	-	-	25	-	-	25	mA
Current, I-	(Note 7)	Full	-	-	25	-	-	25	mA

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. V_{IN} = 0V; I_{OUT} = 100µA (See Test Circuit 1).
3. V_O = ±10V; V_{IN} = ±10V. (See Test Circuits 2, 3, 4)
4. MUX output is buffered with HA-5033 amplifier.
5. 6V Step, ±3V to ±3V, See Test Circuit 5.
6. V_{IN} = 10MHz, $3V_{P-P}$ on one channel, with any other channel selected. (worst case is channel 3 selected with input on channel 4). MUX output is buffered with HA-2541 as shown in Applications section. Terminate all channels with 75Ω.
7. Supply currents vary less than 0.5mA for switching rates from DC to 2MHz.

Performance Curves and Test Circuits

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified



TEST CIRCUIT 1. ON RESISTANCE

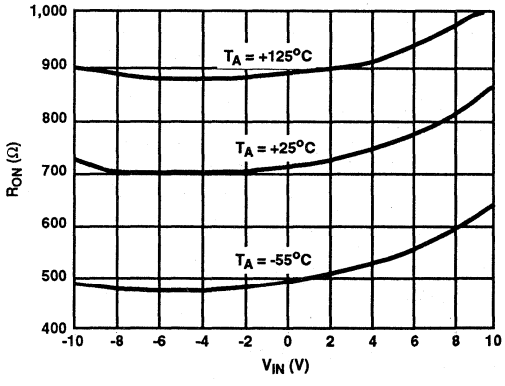


FIGURE 1. ON RESISTANCE vs ANALOG INPUT VOLTAGE

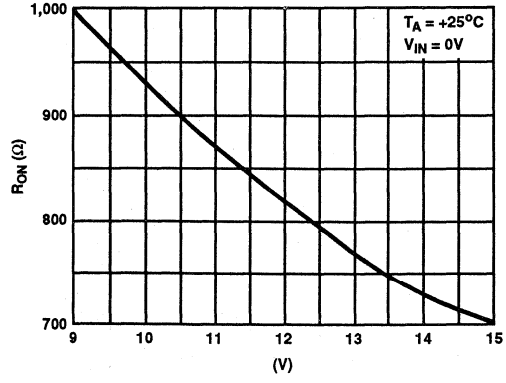


FIGURE 2. ON RESISTANCE vs SUPPLY VOLTAGE

Performance Curves and Test Circuits

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified **(Continued)**

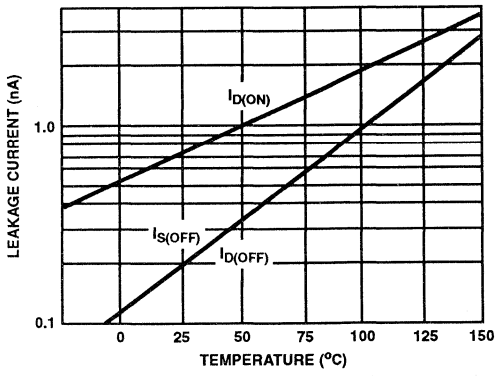
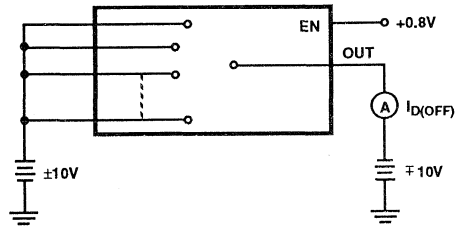
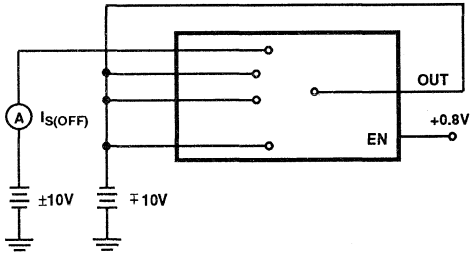


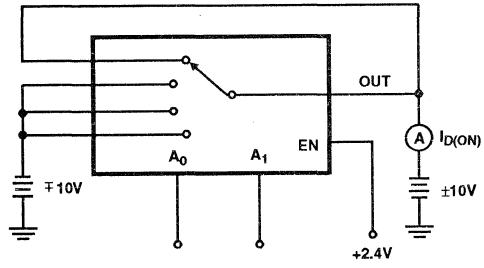
FIGURE 3. LEAKAGE CURRENT vs TEMPERATURE



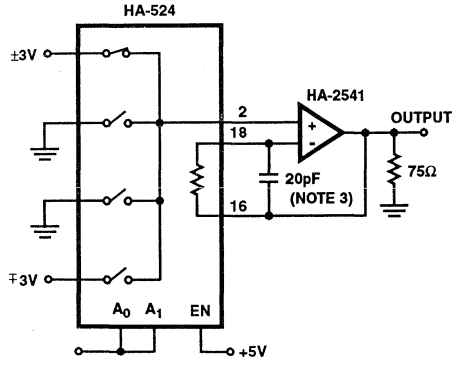
TEST CIRCUIT 2. LEAKAGE CURRENT (NOTE 1)



TEST CIRCUIT 3. LEAKAGE CURRENT (NOTE 1)



TEST CIRCUIT 4. LEAKAGE CURRENT (NOTE 1)



TEST CIRCUIT 5. SETTLING TIME, ACCESS TIME, BREAK-BEFORE-MAKE DELAY (NOTE 2)

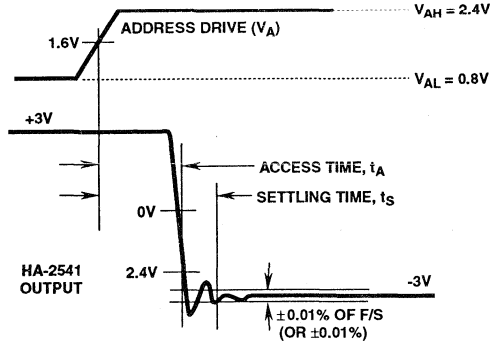


FIGURE 4. POWER SUPPLY CURRENT vs TEMPERATURE

NOTE:

1. Two measurements per channel: ±10V and ∓10V. (Two measurements per device for $I_{D(OFF)}$ ±10V and ∓10V)
2. This test requires channel inputs 1 and 4 at the same level.
3. Capacitor value may be selected to optimize AC performance.

Performance Curves and Test Circuits

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = 2.4V, V_{AL} = 0.8V, Unless Otherwise Specified **(Continued)**

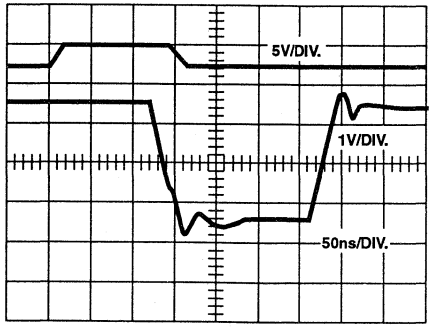


FIGURE 5. ACCESS TIME

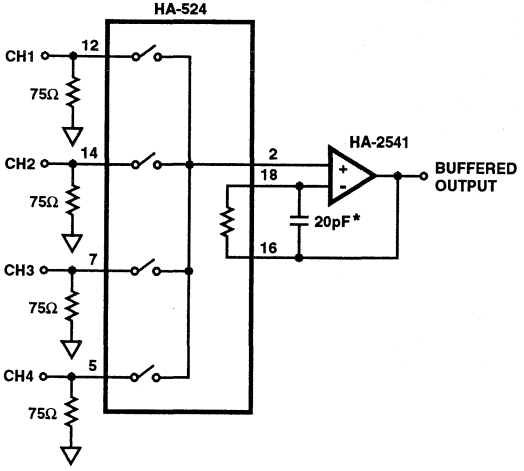
TABLE 1. TRUTH TABLE

A_1	A_0	EN	ON CHANNEL
X	X	L	None
L	L	H	1*
L	H	H	2
H	L	H	3
H	H	H	4

*Channel 1 is shown selected in the Functional Diagram

Typical Applications

Often it is desirable to buffer the HI-524 output, to avoid loading errors due to the channel "ON" resistance:



* Capacitor value may be selected to optimize AC performance.

The buffer amplifier should offer sufficient bandwidth and slew rate to avoid degradation of the anticipated signals. For video switching, the HA-5033 and HA-2542 offer good performance plus ±100mA output current for driving coaxial cables. For general wideband applications, the HA-2541 offers the convenience of unity gain stability plus 90ns settling (to ±0.1%) and ±10V output swing. Also, the HI-524 includes a feedback resistance for use with the HA-2541. This resistance matches and tracks the channel "ON" resistance, to minimize offset voltage due to the buffer's bias currents.

Note that the on-chip feedback element between pins 16 and 18 includes two switches in series, to simulate a channel resistance. These switches open for V_{EN} = Low. This allows two or more HI-524's to operate into one HA-2541, with their feedback elements connected in parallel. Thus, only the selected multiplexer provides feedback, and the amplifier remains stable.

All HI-524 DIP package pins labeled 'SIG GND' (pins 3,4, 6,13,15) should be externally connected to signal ground for best crosstalk performance.

Bypass capacitors (0.1µF to 1.0µF) are recommended from each HI-524 supply pin to power ground (pins 1 and 17 to pin 8 DIP package). Locate the buffer amplifier near the HI-524 so the two capacitors may bypass both devices.

If an analog input 1V or greater is present when supplies are off, a low resistance is seen from that input to a supply line. (For example, the resistance is approximately 160Ω for an input of -3V.) Current flow may be blocked by a diode in each supply line, or limited by a resistor in series with each channel. The best solution, of course, is to arrange that no digital or analog inputs are present when the power supplies are off.

Metallization Topology

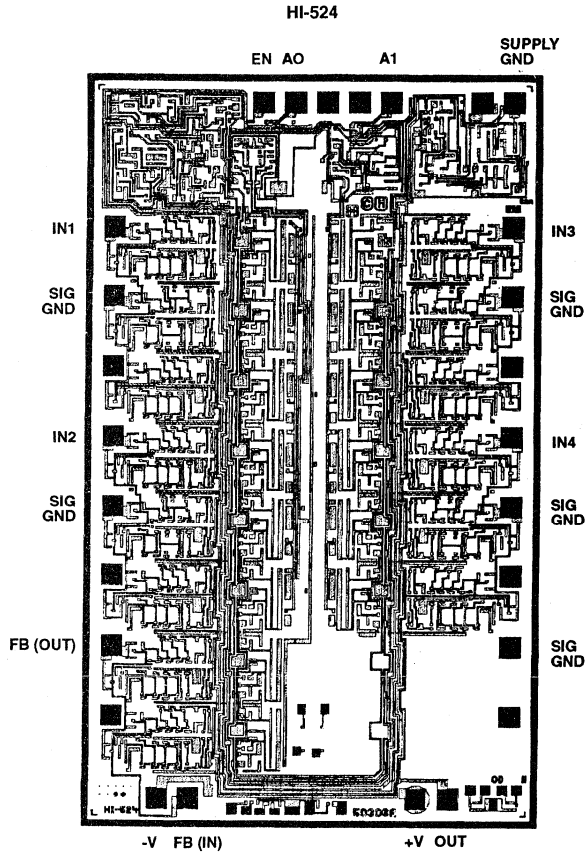
DIE DIMENSIONS:
2250µm x 3720µm x 485µm ±25µm

METALLIZATION:
Type: Cu AL
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ± 1kÅ
Silox Thickness: 12kÅ ± 2kÅ

WORST CASE CURRENT DENSITY: $1.58 \times 10^5 \, A/cm^2$

Metallization Mask Layout



HARRIS SEMICONDUCTOR

HI-539

Monolithic, 4 Channel, Low Level, Differential Multiplexer

December 1993

Features

- **Differential Performance, Typical:**
  - Low ΔR_{ON}, +125°C 5.5Ω
  - Low $\Delta I_{D(ON)}$, +125°C 0.6nA
  - Low Δ(Charge Injection) 0.1pC
  - Low Crosstalk ..... -124dB
- **Settling Time, ±0.01%** **900ns**
- **Wide Supply Range** ..... **±5V to ±18V**
- **Break-Before-Make Switching**
- **No Latch-Up**

Applications

- **Low Level Data Acquisition**
- **Precision Instrumentation**
- **Test Systems**

Description

The Harris HI-539 is a monolithic, four channel, differential multiplexer. Two digital inputs are provided for channel selection, plus an Enable input to disconnect all channels.

Performance is guaranteed for each channel over the voltage range ±10V, but is optimized for low level differential signals. Leakage current, for example, which varies slightly with input voltage, has its distribution centered at zero input volts.

In most monolithic multiplexers, the net differential offset due to thermal effects becomes significant for low level signals. This problem is minimized in the HI-539 by symmetrical placement of critical circuitry with respect to the few heat producing devices.

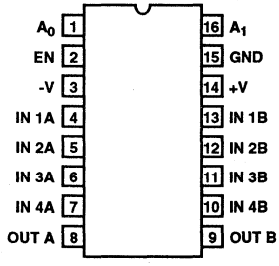
Supply voltages are ±15V and power consumption is only 2.5mW.

Ordering Information

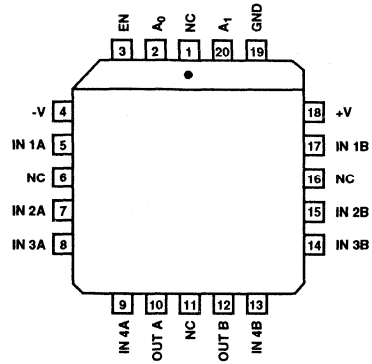
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI4P0539-5	0°C to +75°C	20 Lead PLCC
HI1-0539-2	-55°C to +125°C	16 Lead Ceramic DIP
HI3-0539-5	0°C to +75°C	16 Lead Plastic DIP
HI1-0539-4	-25°C to +85°C	16 Lead Ceramic DIP
HI1-0539-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-0539-8	-55°C to +125°C	16 Lead Ceramic DIP

Pinouts

HI1-539 (CDIP)
HI3-539 (PDIP)
TOP VIEW



HI4P539 (PLCC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3149**

Absolute Maximum Ratings

Voltage Between Supply Pins (+V, -V) 40V
Voltage From Either Supply to GND 20V
Analog Input Voltage, V_{IN} . . . . . $-V \le V_{IN} \le +V$
Digital Input Voltage . . . . . $-V \le V_A \le +V$
Current (Source or Drain) 20mA
Lead Temperature (Soldering 10s) . . . . . +300°C
Storage Temperature Range . . . . . -65°C to +150°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	78°C/W	23°C/W
Plastic DIP Package	100°C/W	-
Plastic PLCC Package	80°C/W	-

Operating Temperature Range
HI-539-2, -8 . . . . . -55°C to +125°C
HI-539-4 . . . . . -25°C to +85°C
HI-539-5 . . . . . 0°C to +75°C
Junction Temperature
Ceramic DIP . . . . . +175°C
Plastic DIP, Plastic PLCC . . . . . +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = ±15V. V_{EN} = +4.0V. V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V. See the "Performance Curves". Selected parameters are defined in "Definitions", Unless Otherwise Specified.

PARAMETER	TEST CONDITION	TEMP	HI-539-2, -4, -8, TYP	HI-539-2, -4, -8, MAX (MIN)	HI-539 -5 TYP	HI-539 -5 MAX (MIN)	UNITS
SWITCHING CHARACTERISTICS							
Access Time, T_A		+25°C	250	750	250	750	ns
		Full	-	1,000	-	1,000	ns
Break-Before-Make Delay, T_{OPEN}		+25°C	85	(30)	85	(30)	ns
		Full	-	(30)	-	(30)	ns
Enable Delay On, $T_{ON(EN)}$		+25°C	250	750	250	750	ns
		Full	-	1,000	-	1,000	ns
Enable Delay Off, $T_{OFF(EN)}$		+25°C	160	650	160	650	ns
		Full	-	900	-	900	ns
Settling Time, to ±0.01%		+25°C	0.9	-	0.9	-	µs
Charge Injection (Output)		Full	3	-	3	-	pC
Δ Charge Injection (Output)		Full	0.1	-	0.1	-	pC
Charge Injection (Input)		Full	10	-	10	-	pC
Differential Crosstalk	Note 3	+25°C	124	-	124	-	dB
Single Ended Crosstalk	Note 3	+25°C	100	-	100	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		Full	5	-	5	-	pF
Channel Output Capacitance, $C_{D(OFF)}$		Full	7	-	7	-	pF
Channel On Output Capacitance, $C_{D(ON)}$		Full	17	-	17	-	pF
Input to Output Capacitance, C_{DS}	Note 4	Full	0.08	-	0.08	-	pF
Digital Input Capacitance, C_A		Full	3	-	3	-	pF
DIGITAL INPUT CHARACTERISTICS							
Input Low Threshold, V_{AL}		Full	-	0.8	-	0.8	V
Input High Threshold, V_{AH}		Full	-	(4.0)	-	(4.0)	V
Input Leakage Current (High), I_{AH}		Full	-	1	-	1	µA
Input Leakage Current (Low), I_{AL}		Full	-	1	-	1	µA
ANALOG CHANNEL CHARACTERISTICS							
Analog Signal Range, V_{IN}		Full	-	(-10)/+10	-	(-10)/+10	V
On Resistance, R_{ON}	V_{IN} = 0V	+25°C	650	850	650	850	Ω
	V_{IN} = ±10V	+25°C	700	900	700	900	Ω
	V_{IN} = 0V	Full	950	1.3k	800	1k	Ω
	V_{IN} = ±10V	Full	1.1k	1.4k	900	1.1k	Ω

Electrical Specifications Supplies = ±15V. V_{EN} = +4.0V. V_{AH} (Logic Level High) = +4.0V, V_{AL} (Logic Level Low) = +0.8V. See the "Performance Curves". Selected parameters are defined in "Definitions", Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITION	TEMP	HI-539-2, -4, -8, TYP	HI-539-2, -4, -8, MAX (MIN)	HI-539 -5 TYP	HI-539 -5 MAX (MIN)	UNITS
(Side A-Side B), ΔR_{ON}	V_{IN} = 0V	+25°C	4.0	24	4.0	24	Ω
	V_{IN} = ±10V	+25°C	4.5	27	4.5	27	Ω
	V_{IN} = 0V	Full	4.75	28	4.0	24	Ω
	V_{IN} = ±10V	Full	5.5	33	4.5	27	Ω
Off Input Leakage Current, $I_{S(OFF)}$	Condition 0V (Note 1)	+25°C	30	-	30	-	pA
	Condition ±10V (Note 1)	+25°C	100	-	100	-	pA
	Condition 0V (Note 1)	Full	2	10	0.2	1	nA
	Condition ±10V (Note 1)	Full	5	25	0.5	2.5	nA
(Side A-Side B), $\Delta I_{S(OFF)}$	Condition 0V	+25°C	3	-	3	-	pA
	Condition ±10V	+25°C	10	-	10	-	pA
	Condition 0V	Full	0.2	2	0.02	0.2	nA
	Condition ±10V	Full	0.5	5	0.05	0.5	nA
Off Output Leakage Current, $I_{D(OFF)}$	Condition 0V (Note 1)	+25°C	30	-	30	-	pA
	Condition ±10V (Note 1)	+25°C	100	-	100	-	pA
	Condition 0V (Note 1)	Full	2	10	0.2	1	nA
	Condition ±10V (Note 1)	Full	5	25	0.5	2.5	nA
(Side A-Side B), $\Delta I_{D(OFF)}$	Condition 0V	+25°C	3	-	3	-	pA
	Condition ±10V	+25°C	10	-	10	-	pA
	Condition 0V	Full	0.2	2	0.02	0.2	nA
	Condition ±10V	Full	0.5	5	0.05	0.5	nA
On Channel Leakage Current, $I_{D(ON)}$	Condition 0V (Note 1)	+25°C	50	-	50	-	pA
	Condition ±10V (Note 1)	+25°C	150	-	150	-	pA
	Condition 0V (Note 1)	Full	5	25	0.5	2.5	nA
	Condition ±10V (Note 1)	Full	6	40	0.8	4.0	nA
(Side A-Side B), $\Delta I_{D(ON)}$	Condition 0V	+25°C	10	-	10	-	pA
	Condition ±10V	+25°C	30	-	30	-	pA
	Condition 0V	Full	0.5	5	0.05	0.5	nA
	Condition ±10V	Full	0.6	6	0.08	0.8	nA
Differential Offset Voltage, ΔV_{OS}	Note 2	+25°C	0.02	-	0.02	-	µV
		Full	0.70	-	0.08	-	µV
POWER REQUIREMENTS							
Power Dissipation, P_D		+25°C	2.3	-	2.3	-	mW
		Full	-	45	-	45	mW
Current, I+		+25°C	0.150	-	0.150	-	mA
		Full	-	2.0	-	2.0	mA
Current, I-		+25°C	0.001	-	0.001	-	mA
		Full	-	1.0	-	1.0	mA
Supply Voltage Range, ±V		Full	±15	(±5)/±18	±15	(±5)/ ±18	V

NOTES:

1. See Figures 2B, 2C, 2D. The condition ±10V means:
   $I_{S(OFF)}$ and $I_{D(OFF)}$:
   (V_S = +10V, V_D = -10V), then
   (V_S = -10V, V_D = +10V)
   $I_{D(ON)}$: (+10V, then -10V)
2. ΔV_{OS} (Exclusive of thermocouple effects) = R_{ON} $\Delta I_{D(ON)}$ + $I_{D(ON)}$ ΔR_{ON}. See Applications section for discussion of additional V_{OS} error.
3. V_{IN} = 1kHz, $15V_{P-P}$ on all but the selected channel. See Figure 7.
4. Calculated from typical Single-Ended Crosstalk performance.

Performance Curves Unless Otherwise Specified T_A = +25°C, +V = +15V, -V = -15V, V_{AH} = +4V and V_{AL} = +0.8V.

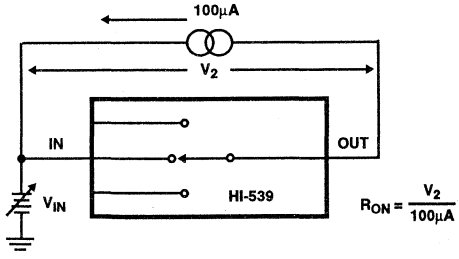


FIGURE 1A. ON RESISTANCE TEST CIRCUIT

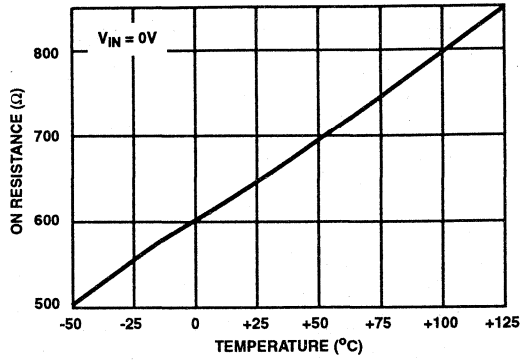


FIGURE 1B. ON RESISTANCE vs TEMPERATURE

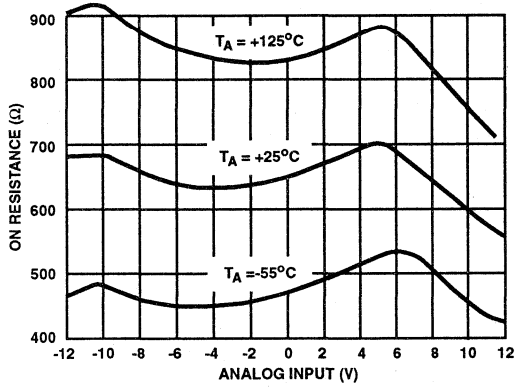


FIGURE 1C. ON RESISTANCE vs ANALOG INPUT VOLTAGE

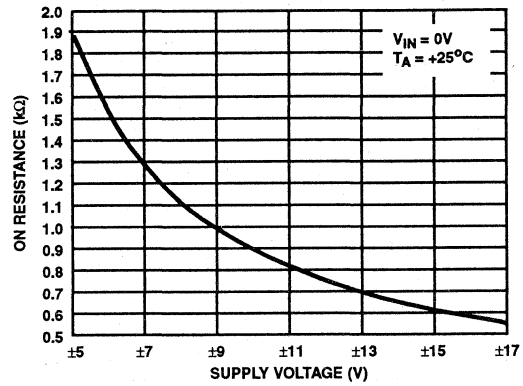


FIGURE 1D. ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

Performance Curves (Continued)

Unless Otherwise Specified T_A = +25°C, +V = +15V, -V = -15V, V_{AH} = +4V and V_{AL} = +0.8V.

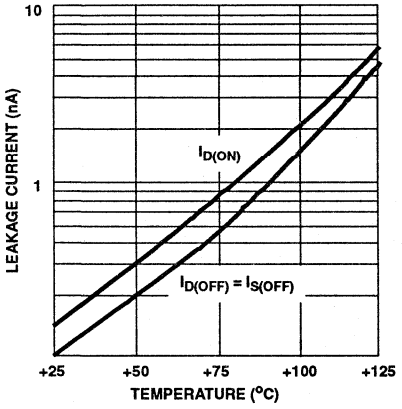
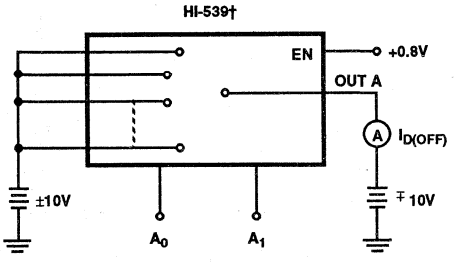
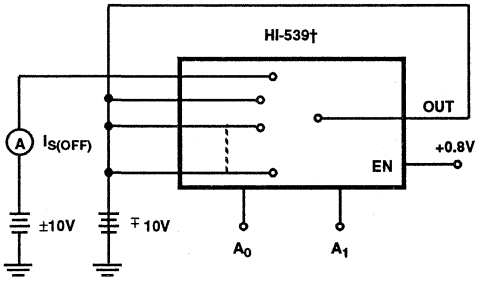


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE



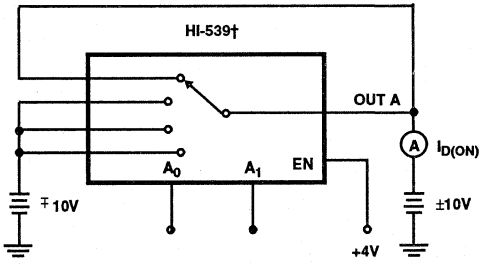
†Similar Connection For Side "B"

FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT (NOTE 1)



†Similar Connection For Side "B"

FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT (NOTE 1)



†Similar Connection For Side "B"

FIGURE 2D. $I_{D(ON)}$ TEST CIRCUIT (NOTE 1)

FIGURE 2. LEAKAGE CURRENT

NOTE:

1. Three measurements = +10V/-10V, -10V/+10V, and 0V

Performance Curves Unless Otherwise Specified T_A = +25°C, +V = +15V, -V = -15V, V_{AH} = +4V and V_{AL} = +0.8V. **(Continued)**

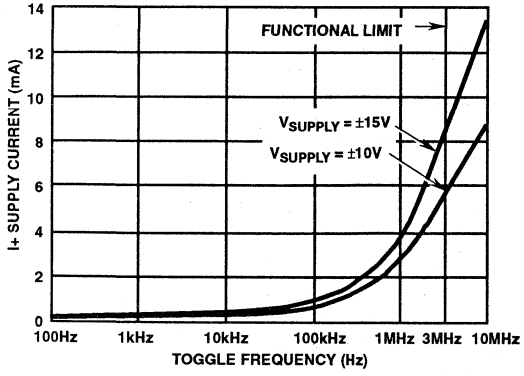
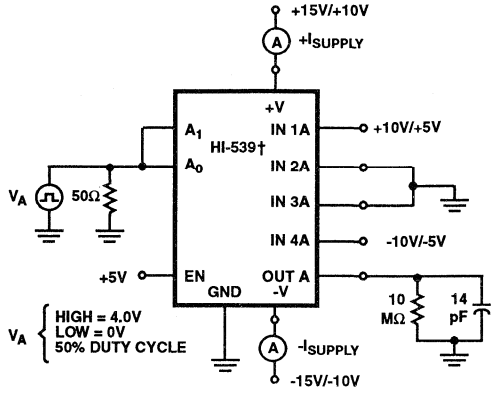


FIGURE 3A. SUPPLY CURRENT vs TOGGLE FREQUENCY



†Similar Connection For Side "B"

FIGURE 3B. SUPPLY CURRENT TEST CIRCUIT

FIGURE 3. SUPPLY CURRENT

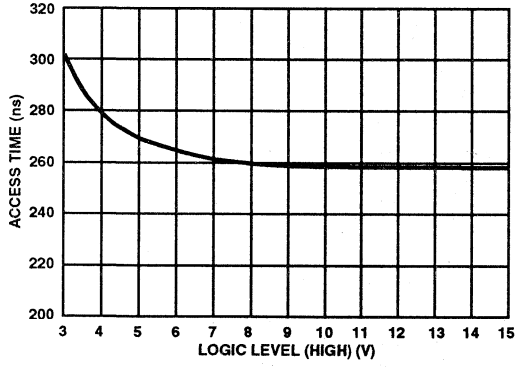


FIGURE 4A. ACCESS TIME vs LOGIC LEVEL (HIGH)

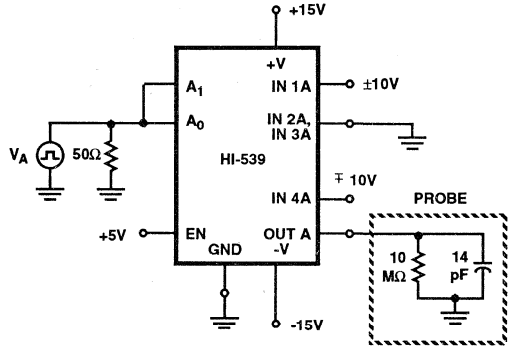


FIGURE 4B. ACCESS TIME TEST CIRCUIT

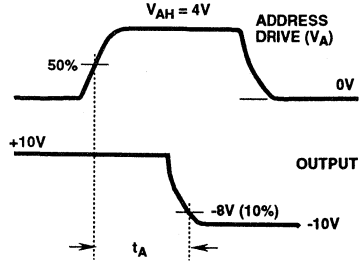


FIGURE 4C. ACCESS TIME MEASUREMENT

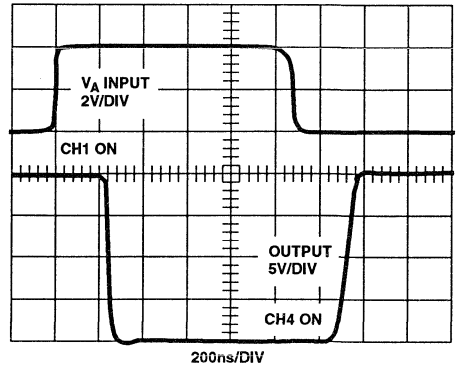


FIGURE 4D. ACCESS TIME WAVEFORMS

FIGURE 4. ACCESS TIME

Performance Curves Unless Otherwise Specified T_A = +25°C, +V = +15V, -V = -15V, V_{AH} = +4V and V_{AL} = +0.8V. **(Continued)**

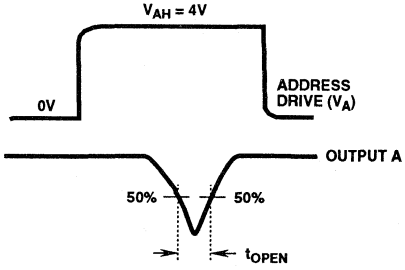
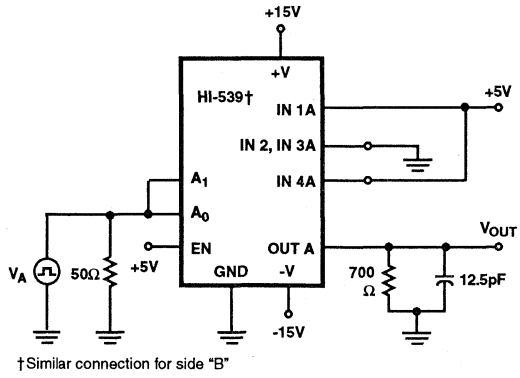


FIGURE 5A. t_{OPEN} MEASUREMENT



†Similar connection for side "B"

FIGURE 5B. t_{OPEN} TEST CIRCUIT

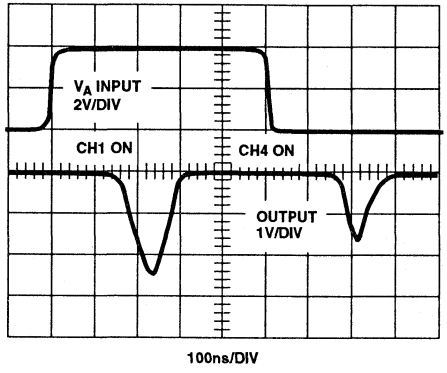
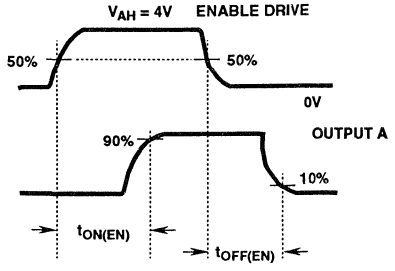


FIGURE 5C. t_{OPEN} WAVEFORMS

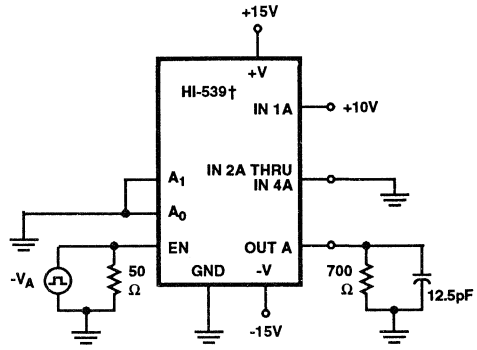
FIGURE 5. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

Performance Curves Unless Otherwise Specified T_A = +25°C, +V = +15V, -V = -15V, V_{AH} = +4V and V_{AL} = +0.8V. **(Continued)**



†Similar connection for side "B"

FIGURE 6A. $t_{ON(EN)}$, $t_{OFF(EN)}$ MEASUREMENT



†Similar connection for side "B"

FIGURE 6B. $t_{ON(EN)}$, $t_{OFF(EN)}$ TEST CIRCUIT

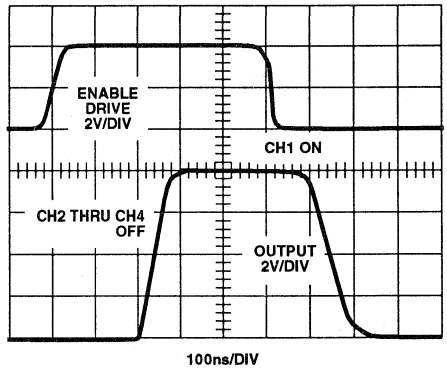
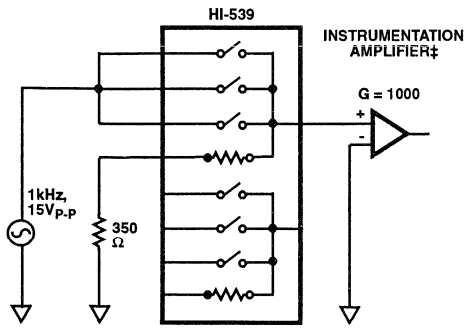


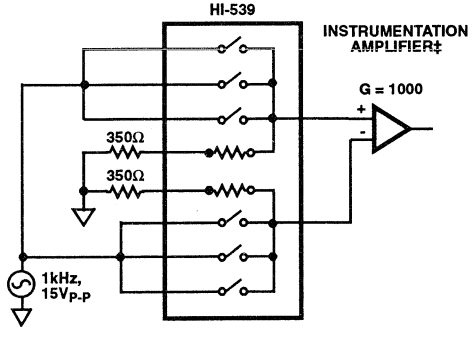
FIGURE 6C. $t_{ON(EN)}$, $t_{OFF(EN)}$ WAVEFORMS

FIGURE 6. ENABLE DELAY $t_{ON(EN)}$, $t_{OFF(EN)}$



‡AD606 or BB3630, for example

FIGURE 7A. SINGLE-ENDED CROSSTALK TEST CIRCUIT



‡AD606 or BB3630, for example

FIGURE 7B. DIFFERENTIAL CROSSTALK TEST CIRCUIT

FIGURE 7. CROSSTALK

Applications

General

The HI-539 accepts inputs in the range -15V to +15V, with performance guaranteed over the ±10V range. At these higher levels of analog input voltage it is comparable to the HI-509, and is plug-in compatible with that device (as well as the HI-509A). However, as mentioned earlier, the HI-539 was designed to introduce minimum error when switching low level inputs.

Special care is required in working with these low level signals. The main concern with signals below 100mV is that noise, offset voltage, and other aberrations can represent a large percentage error. A shielded differential signal path is essential to maintain a noise level below $50\mu V_{RMS}$.

Low Level Signal Transmission

The transmission cable carrying the transducer signal is critical in a low level system. It should be as short as practical and rigidly supported. Signal conductors should be tightly twisted for minimum enclosed area to guard against pickup of electromagnetic interference, and the twisted pair should be shielded against capacitively coupled (electrostatic) interference. A braided wire shield may be satisfactory, but a lapped foil shield is better since it allows only one tenth as much leakage capacitance to ground per foot. A key requirement for the transmission cable is that it presents a balanced line to sources of noise interference. This means an equal series impedance in each conductor plus an equally distributed impedance from each conductor to ground. The result should be signals equal in magnitude but opposite in phase at any transverse plane. Noise will be coupled in phase to both conductors, and may be rejected as common mode voltage by a differential amplifier connected to the multiplexer output.

Coaxial cable is not suitable for low level signals because the two conductors (center and shield) are unbalanced. Also, ground loops are produced if the shield is grounded at both ends by standard BNC connectors. If coax must be used, carry the signal on the center conductors of two equal-length cables whose shields are terminated only at the transducer end. As a general rule, terminate (ground) the shield at one end only, preferably at the end with greatest noise interference. This is usually the transducer end for both high and low level signals.

Watch Small ΔV Errors

Printed circuit traces and short lengths of wire can add substantial error to a signal even after it has traveled hundreds of feet and arrived on a circuit board. Here, the small voltage drops due to current flow through connections of a few milliohms must be considered, especially to meet an accuracy requirement of 12-bits or more.

Table 1 is a useful collection of data for calculating the effect of these short connections. (Proximity to a ground plane will lower the values of inductance.)

As an example, suppose the HI-539 is feeding a 12-bit converter system with an allowable error of $\pm 1/2$ LSB (±1.22mV). If the interface logic draws 100mA from the 5V supply, this current will produce 1.28mV across 6 inches of #24 wire; more than the error budget. Obviously, this digital current must not be routed through any portion of the analog ground return network.

TABLE 1.

WIRE GAGE	EQUIVALENT WIDTH OF P.C. CONDUCTOR (2 oz. Cu)	DC RESISTANCE PER FOOT	INDUCTANCE PER FOOT	IMPEDANCE PER FOOT	
				60Hz	10kHz
18	0.47"	0.0064Ω	0.36μH	0.0064Ω	0.0235Ω
20	0.30"	0.0102Ω	0.37μH	0.0102Ω	0.0254Ω
22	0.19"	0.0161Ω	0.37μH	0.0161Ω	0.0288Ω
24	0.12"	0.0257Ω	0.40μH	0.0257Ω	0.0345Ω
26	0.075"	0.041Ω	0.42μH	0.041Ω	0.0488Ω
28	0.047"	0.066Ω	0.45μH	0.066Ω	0.0718Ω
30	0.029"	0.105Ω	0.49μH	0.105Ω	0.110Ω
32	0.018"	0.168Ω	0.53μH	0.168Ω	0.171Ω

Provide Path For I_{BIAS}

The input bias current for any DC-coupled amplifier must have an external path back to the amplifier's power supply. No such path exists in Figure 8A, and consequently the amplifier output will remain in saturation.

A single large resistor (1MΩ to 10MΩ) from either signal line to power supply common will provide the required path, but a resistor on each line is necessary to preserve accuracy. A single pair of these bias current resistors on the HI-539 output may be used if their loading effect can be tolerated (each forms a voltage divider with R_{ON}). Otherwise, a resistor pair on each input channel of the multiplexer is required.

The use of bias current resistors is acceptable only if one is confident that the sum of signal plus common-mode voltage will remain within the input range of the multiplexer/amplifier combination.

Another solution is to simply run a third wire from the low side of the signal source, as in Figure 8B. This wire assures a low common-mode voltage as well as providing the path for bias currents. Making the connection near the multiplexer will save wire, but it will also unbalance the line and reduce the amplifier's common-mode rejection.

Differential Offset, ΔV_{OS}

There are two major sources of ΔV_{OS}. That part due to the expression ($R_{ON}\,\Delta I_{D(ON)} + I_{D(ON)}\,\Delta R_{ON}$) becomes significant with increasing temperature, as shown in the Electrical Specifications tables. The other source of offset is the thermocouple effects due to dissimilar materials in the signal path. These include silicon, aluminum, tin, nickel-iron and (often) gold, just to exit the package.

For the thermocouple effects in the package alone, the constraint on ΔV_{OS} may be stated in terms of a limit on the difference in temperature for package pins leading to any channel of the HI-539. For example, a difference of 0.13°C produces a 5μV offset. Obviously, this ΔT effect can dominate the ΔV_{OS} parameter at any temperature unless care is taken in mounting the HI-539 package.

Temperature gradients across the HI-539 package should be held to a minimum in critical applications. Locate the HI-539 far from heat producing components, with any air currents flowing lengthwise across the package.

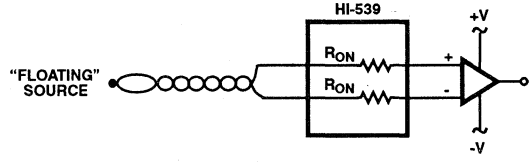


FIGURE 8A.

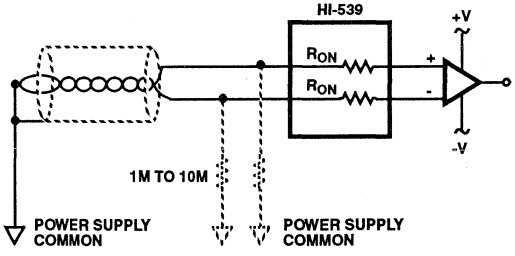


FIGURE 8B.

The amplifier in Figure 8A is unusable because its bias currents cannot return to the power supply. Figure 8B shows two alternative paths for these bias currents: either a pair of resistors, or (better) a third wire from the low side of the signal source.

Die Characteristics

DIE DIMENSIONS:
92 mils x 100 mils

METALLIZATION:
Type: Al Cu
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ± 1kÅ
Silox Thickness: 12kÅ ± 2.0kÅ

WORST CASE CURRENT DENSITY:
$2.54 \times 10^5 A/cm^2$ at 20mA

TRANSISTOR COUNT: 236

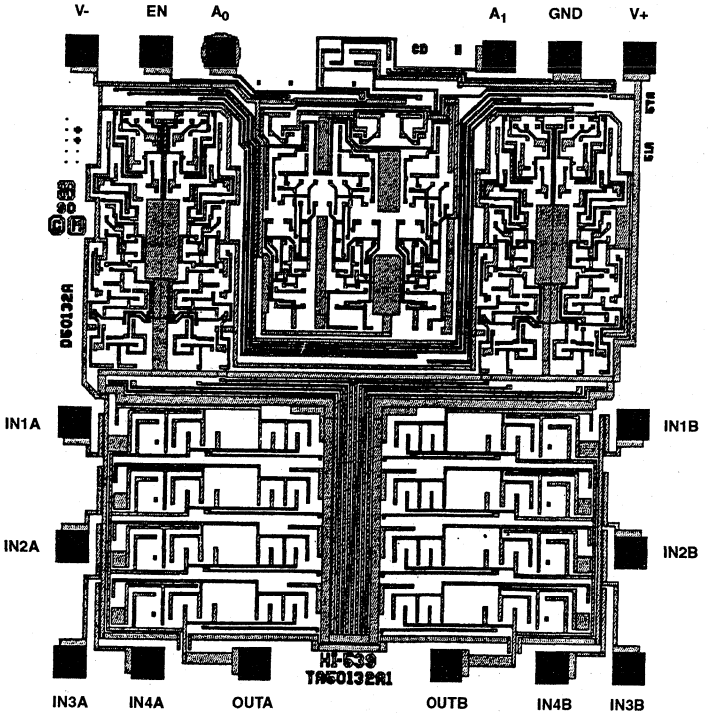
PROCESS: CMOS-DI

SUBSTRATE POTENTIAL*: $-V_{SUPPLY}$

* The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential

Metallization Mask Layout

HI-539



HARRIS SEMICONDUCTOR

HI-546, HI-547 HI-548, HI-549

Single 16 and 8, Differential 8 and 4 Channel CMOS Analog MUXs with Active Overvoltage Protection

December 1993

Features

- Analog Overvoltage Protection.....$70V_{P-P}$
- No Channel Interaction During Overvoltage
- Guaranteed R_{ON} Matching
- 44V Maximum Power Supply
- Break-Before-Make Switching
- Analog Signal Range.....±15V
- Access Time (Typical) 500ns
- Standby Power (Typical) 7.5mW

Applications

- Data Acquisition
- Industrial Controls
- Telemetry

Description

The HI-546, HI-547, HI-548 and HI-549 are analog multiplexers with active overvoltage protection and guaranteed RON matching. Analog input levels may greatly exceed either power supply without damaging the device or disturbing the signal path of other channels. Active protection circuitry assures that signal fidelity is maintained even under fault conditions that would destroy other multiplexers.

Analog inputs can withstand constant $70V_{P-P}$ levels with ±15V supplies. Digital inputs will also sustain continuous faults up to 4V greater than either supply. In addition, signal sources are protected from short circuiting should multiplexer supply loss occur. Each input presents 1KΩ of resistance under this condition. These features make the HI-546, HI-547, HI-548 and HI-549 ideal for use in systems where the analog inputs originate from external equipment or separately powered circuitry. All devices are fabricated with 44V Dielectrically Isolated CMOS technology. The HI-546 is a single 16 channel, the HI-547 is an 8 channel differential, the HI-548 is a single 8 channel and the HI-549 is a 4 channel differential device. If input overvoltage protection is not needed the HI-506/507/508/509 multiplexers are recommended. For further information see Application Notes 520 and 521. The HI-546 and HI-547 devices are available in a 28 lead Plastic or Ceramic DIP and a 28 pad Ceramic LCC package. The HI-548/549 devices are available in a 16 lead Plastic or Ceramic DIP and a 20 pad Ceramic LCC package.

The HI-546, HI-547, HI-548 and HI-549 are offered in industrial/commercial and military grades. Additional Hi-Rel screening including 160 hour Burn-In is specified by the "-8" suffix. For Mil-Std-883 compliant parts, request the HI-546/883, HI-547/883, HI-548/883 and HI-549/883 datasheets.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0546-4	-25°C to +85°C	28 Lead Ceramic DIP
HI1-0546-5	0°C to +75°C	28 Lead Ceramic DIP
HI1-0546-2	-55°C to +125°C	28 Lead Ceramic DIP
HI1-0546/883	-55°C to +125°C	28 Lead Ceramic DIP
HI3-0546-5	0°C to +75°C	28 Lead Plastic DIP
HI3-0546-9	-40°C to +85°C	28 Lead Plastic DIP
HI4-0546/883	-55°C to +125°C	28 Lead Ceramic LCC
HI4P0546-5	0°C to +75°C	28 Lead PLCC
HI9P0546-5	0°C to +75°C	28 Lead Plastic SOIC
HI9P0546-9	-40°C to +85°C	28 Lead Plastic SOIC
HI1-0547-2	-55°C to +125°C	28 Lead Ceramic DIP
HI1-0547-4	-25°C to +85°C	28 Lead Ceramic DIP

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0547-5	0°C to +75°C	28 Lead Ceramic DIP
HI1-0547-9	-40°C to +85°C	28 Lead Ceramic DIP
HI1-0547/883	-55°C to +125°C	28 Lead Ceramic DIP
HI3-0547-5	0°C to +75°C	28 Lead Plastic DIP
HI3-0547-9	-40°C to +85°C	28 Lead Plastic DIP
HI4-0547/883	-55°C to +125°C	28 Lead Ceramic LCC
HI4P0547-5	0°C to +75°C	28 Lead PLCC
HI9P0547-5	0°Cto +75°C	28 Lead Plastic SOIC
HI9P0547-9	-40°C to +85°C	28 Lead Plastic SOIC

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3150**

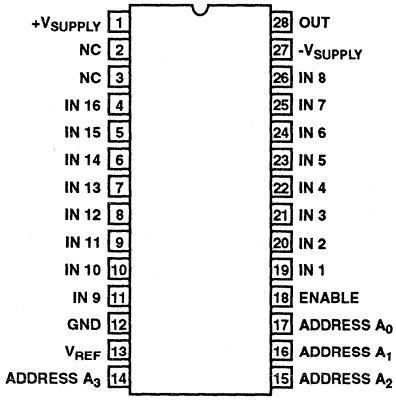
Ordering Information (Continued)

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0548-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0548-4	-25°C to +85°C	16 Lead Ceramic DIP
HI1-0548-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-0548/883	-55°C to +125°C	16 Lead Ceramic DIP
HI3-0548-5	0°C to +75°C	16 Lead Plastic DIP
HI3-0548-9	-40°C to +85°C	16 Lead Plastic DIP
HI4-0548/883	-55°C to +125°C	20 Lead Ceramic LCC
HI4P0548-5	0°C to +75°C	20 Lead Plastic LCC
HI9P0548-5	0°C to +75°C	16 Lead Plastic SOIC
HI9P0548-9	-40°C to +85°C	16 Pin SOIC (W)

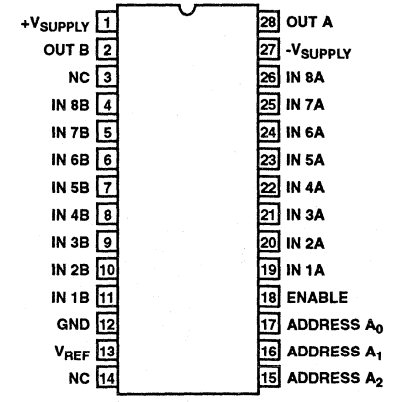
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-0549-2	-55°C to +125°C	16 Lead Ceramic DIP
HI1-0549-4	-25°C to +85°C	16 Lead Ceramic DIP
HI1-0549-5	0°C to +75°C	16 Lead Ceramic DIP
HI1-0549/883	-55°C to +125°C	16 Lead Ceramic DIP
HI3-0549-5	0°C to +75°C	16 Lead Plastic DIP
HI3-0549-9	-40°C to +85°C	16 Lead Plastic DIP
HI4-0549/883	-55°C to +125°C	20 Lead Ceramic LCC
HI4P0549-5	0°C to +75°C	20 Lead Plastic LCC
HI9P0549-5	0°C to +75°C	20 Lead Plastic SOIC
HI9P0549-9	-40°C to +85°C	16 Pin SOIC (W)

Pinouts

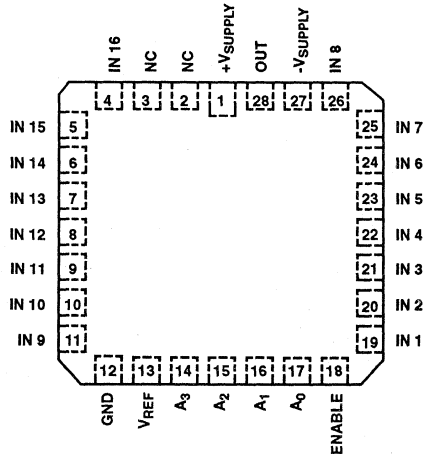
HI1-0546 (CDIP), HI3-0546 (PDIP), HI9P0546 (SOIC)
TOP VIEW



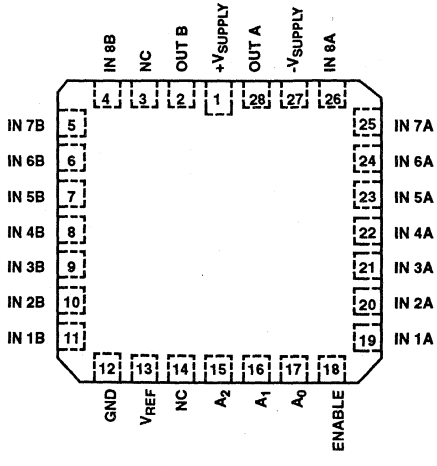
HI1-0547 (CDIP), HI3-0547 (PDIP), HI9P0547 (SOIC)
TOP VIEW



HI4P0546 (PLCC)
TOP VIEW

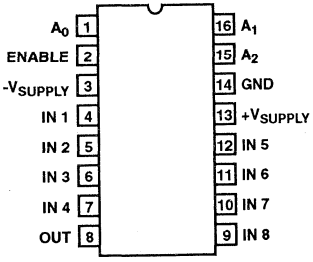


HI4P0547 (PLCC)
TOP VIEW

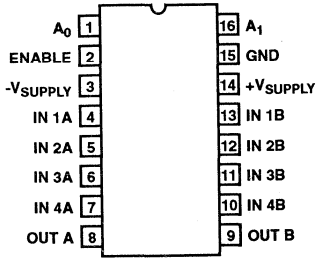


Pinouts (Continued)

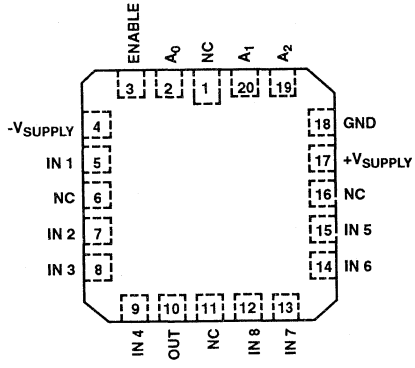
HI1-0548 (CDIP)
HI3-0548 (PDIP)
HI9P0548 (SOIC)
TOP VIEW



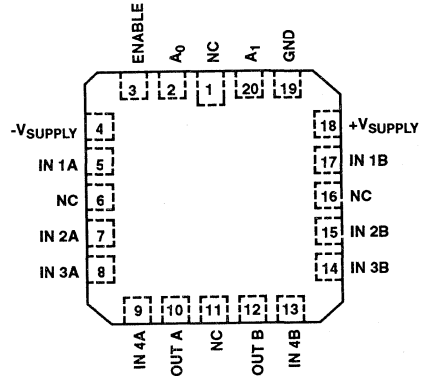
HI1-0549 (CDIP)
HI3-0549 (PDIP)
HI9P0549 (SOIC)
TOP VIEW



HI4P0548 (PLCC)
TOP VIEW

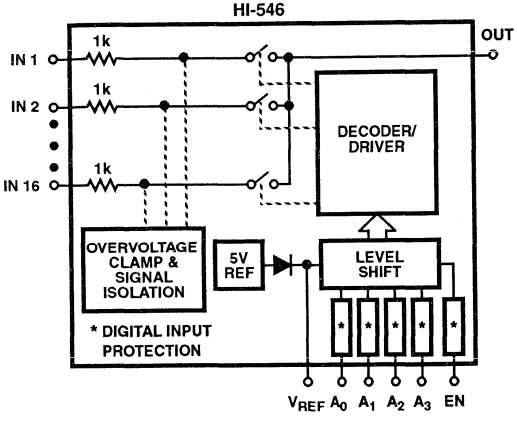


HI4-0549 (LCC)
HI4P0549 (PLCC)
TOP VIEW

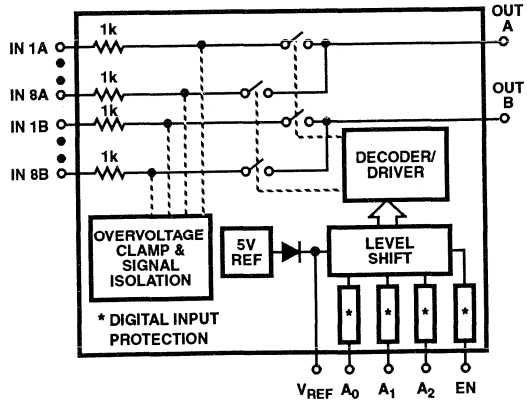


Functional Diagrams

HI-546

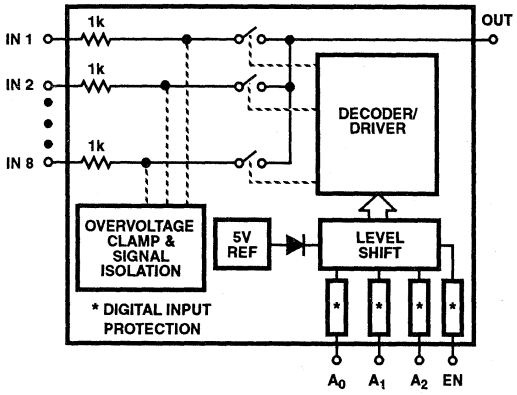


HI-547

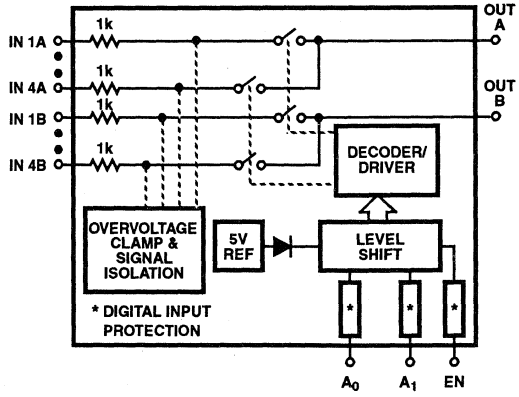


Functional Diagrams (Continued)

HI-548

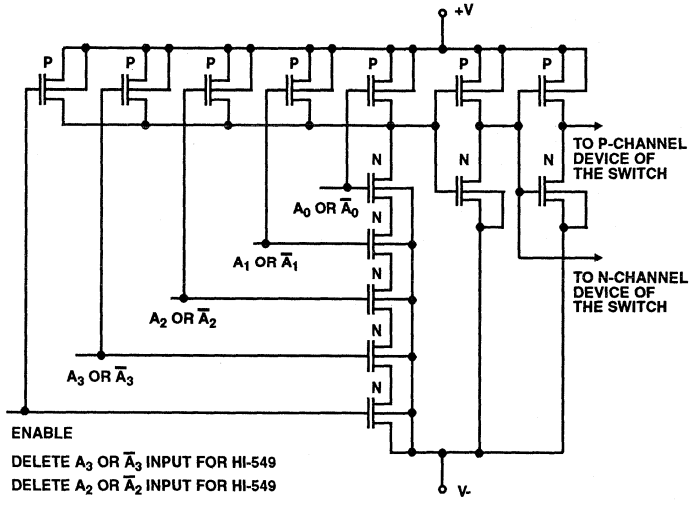


HI-549

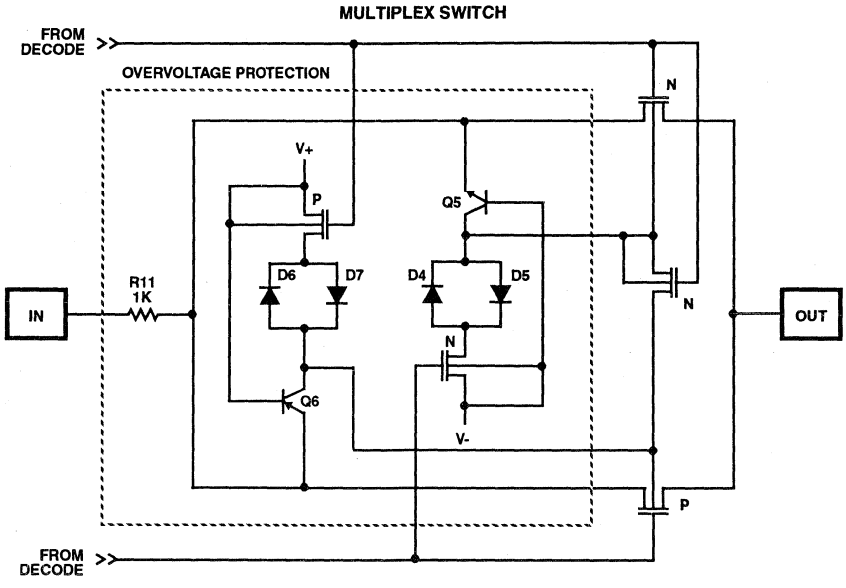


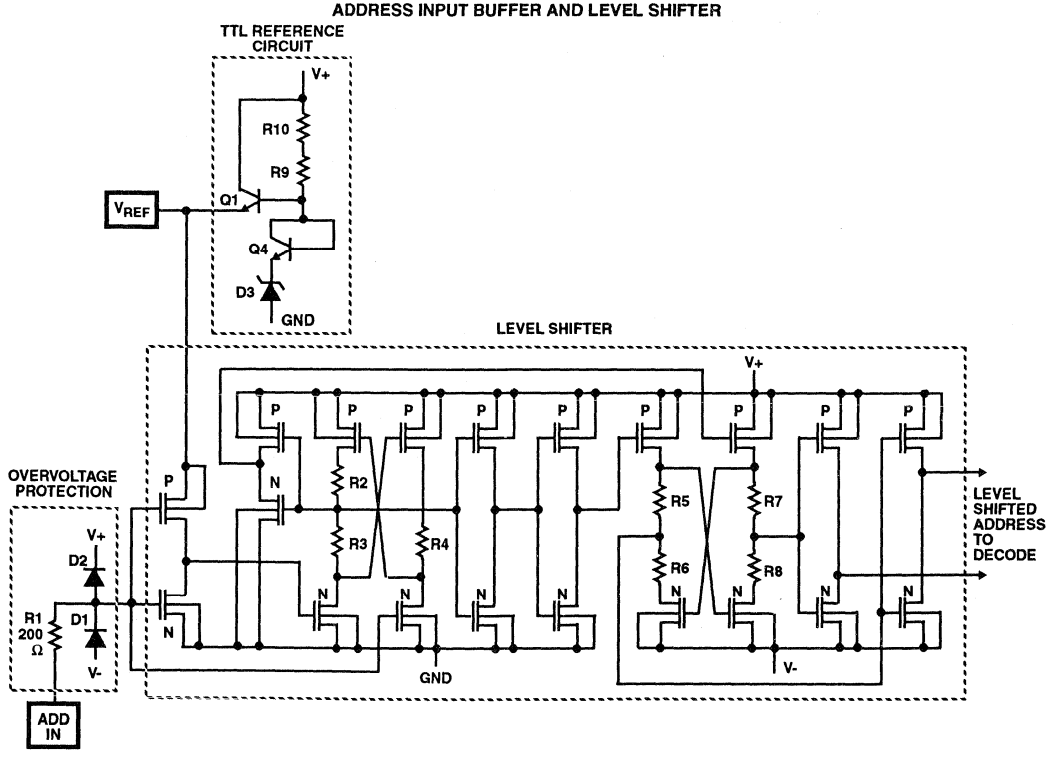
Schematic Diagrams

ADDRESS DECODER



Schematic Diagrams (Continued)





Absolute Maximum Ratings

$V_{SUPPLY(+)}$ to $V_{SUPPLY(-)}$ ..... +44V
$V_{SUPPLY(+)}$ to GND ..... +22V
$V_{SUPPLY(-)}$ to GND ..... -25V
Digital Input Overvoltage
$+V_{EN}$, $+V_A$ ..... $+V_{SUPPLY}$ +4V
$-V_{EN}$, $-V_A$ ..... $-V_{SUPPLY}$ -4V
or 20mA, whichever occurs first
Analog Signal Overvoltage (Note 6)
$+V_S$ ..... $+V_{SUPPLY}$ +20V
$-V_S$ ..... $-V_{SUPPLY}$ -20V
Continuous Current, S or D 20mA
Peak Current, S or D 40mA
(Pulsed at 1ms, 10% duty cycle max)
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic Packages		
16 Lead DIP	80°C/W	24°C/W
28 Lead DIP	55°C/W	20°C/W
20 Lead LCC	75°C/W	20°C/W
28 Lead LCC	60°C/W	11°C/W
Plastic DIP Packages		
28 Lead	60°C/W	-
16 Lead	100°C/W	-
Plastic PLCC Packages		
28 Lead	70°C/W	-
20 Lead	80°C/W	-
SOIC		
28 Lead	70°C/W	-
16 Lead	100°C/W	-

Operating Temperature Ranges
HI-546/547/548/549-2 ..... -55°C to +125°C
HI-546/547/548/549-4 ..... -25°C to +85°C
HI-546/547/548/549-5, -7 ..... 0°C to +75°C
HI-546/547/548/549-9 ..... -40°C to +85°C
Junction Temperature
Ceramic Package ..... +175°C
Plastic Package ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4V; V_{AL} (Logic Level Low) = +0.8V; Unless Otherwise Specified. For Test Conditions, Consult Performance Curves.

PARAMETER	TEST CONDITION	TEMP	HI-54X-2 MIN	HI-54X-2 TYP	HI-54X-2 MAX	HI-54X-4, -5, -9 MIN	HI-54X-4, -5, -9 TYP	HI-54X-4, -5, -9 MAX	UNITS
SWITCHING CHARACTERISTICS									
Access Time, t_A		+25°C	-	0.5	-	-	0.5	-	µs
		Full	-	-	1.0	-	-	1.0	µs
Break-Before Make Delay, t_{OPEN}		+25°C	25	80	-	25	80	-	ns
Enable Delay (ON), $t_{ON(EN)}$		+25°C	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Enable Delay (OFF), $t_{OFF(EN)}$		+25°C	-	300	500	-	300	-	ns
		Full	-	-	1000	-	-	1000	ns
Settling Time (0.1%)		+25°C	-	1.2	-	-	1.2	-	µs
(0.01%)		+25°C	-	3.5	-	-	3.5	-	µs
"Off Isolation"	Note 5	+25°C	50	68	-	50	68	-	dB
Channel Input Capacitance, $C_{S(OFF)}$		+25°C	-	5	-	-	5	-	pF
Channel Output Capacitance $C_{D(OFF)}$									
HI-546		+25°C	-	52	-	-	52	-	pF
HI-547		+25°C	-	30	-	-	30	-	pF
HI-548		+25°C	-	25	-	-	25	-	pF
HI-549		+25°C	-	12	-	-	12	-	pF
Input to Output Capacitance, $C_{DS(OFF)}$		+25°C	-	0.1	-	-	0.1	-	pF

Electrical Specifications Supplies = +15V, -15V; V_{REF} Pin = Open; V_{AH} (Logic Level High) = +4V; V_{AL} (Logic Level Low) = +0.8V; Unless Otherwise Specified. For Test Conditions, Consult Performance Curves. **(Continued)**

PARAMETER	TEST CONDITION	TEMP	HI-54X-2			HI-54X-4, -5, -9			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUT CHARACTERISTICS									
Input Low Threshold, TTL Drive, V_{AL}		Full	-	-	0.8	-	-	0.8	V
Input High Threshold, V_{AH}	Note 7	Full	4.0	-	-	4.0	-	-	V
MOS Drive (HI-546/547 Only), V_{AL}	Note 8	+25°C	-	-	0.8	-	-	0.8	V
MOS Drive (HI-546/547 Only), V_{AH}	Note 8	+25°C	6.0	-	-	6.0	-	-	V
Input Leakage Current (High or Low), I_A	Note 4	Full	-	-	1.0	-	-	1.0	µA
ANALOG CHANNEL CHARACTERISTICS									
Analog Signal Range, V_S		Full	-15	-	+15	-15	-	+15	V
On Resistance, R_{ON},	Note 1	+25°C	-	1.2	1.5	-	1.5	1.8	kΩ
		Full	-	1.5	1.8	-	1.8	2.0	kΩ
ΔR_{ON}, (Any Two Channels)		+25°C	-	-	7.0	-	-	7.0	%
Off Input Leakage Current, $I_{S(OFF)}$	Note 2	+25°C	-	0.03	-	-	0.03	-	nA
		Full	-	-	50	-	-	50	nA
Off Output Leakage Current, $I_{D(OFF)}$	Note 2	+25°C	-	0.1	-	-	0.1	-	nA
HI-546		Full	-	-	300	-	-	300	nA
HI-547		Full	-	-	200	-	-	200	nA
HI-548		Full	-	-	200	-	-	200	nA
HI-549		Full	-	-	100	-	-	100	nA
With Input Overvoltage Applied, $I_{D(OFF)}$	Note 3	+25°C	-	4.0	-	-	4.0	-	nA
		Full	-	-	2.0	-	-	-	µA
On Channel Leakage Current, $I_{D(ON)}$	Note 2	+25°C	-	0.1	-	-	0.1	-	nA
HI-546		Full	-	-	300	-	-	300	nA
HI-547		Full	-	-	200	-	-	200	nA
HI-548		Full	-	-	200	-	-	200	nA
HI-549		Full	-	-	100	-	-	100	nA
Differential Off Output Leakage Current (HI-547, HI-549 Only), I_{DIFF}		Full	-	-	50	-	-	50	nA
POWER REQUIREMENTS									
Power Dissipation, P_D		Full	-	7.5	-	-	7.5	-	mW
Current, I+	Note 6	Full	-	0.5	2.0	-	0.5	2.0	mA
Current, I-	Note 6	Full	-	0.02	1.0	-	0.02	1.0	mA

NOTES:

1. $V_{OUT} = \pm 10V$, $I_{OUT} = \mp 100\mu A$.
2. 10nA is the practical lower limit for high speed measurement in the production test environments.
3. Analog Overvoltage = ±33V.
4. Digital input leakage is primarily due to the clamp diodes (see Schematic). Typical leakage is less than 1nA at +25°C.
5. $V_{EN} = 0.8V$, $R_L = 1K$, $C_L = 15pF$, $V_S = 7V_{RMS}$, f = 100kHz.
6. V_{EN}, $V_A = 0V$ or 4.0V.
7. To drive from DTL/TTLCircuits, 1kΩ pull-up resistors to $+5.0V_{SUPPLY}$ are recommended.
8. $V_{REF} = +10V$.

Performance Curves $T_A = +25°C$, $V_{SUPPLY} = \pm15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$, V_{REF} = Open, Unless Otherwise Specified

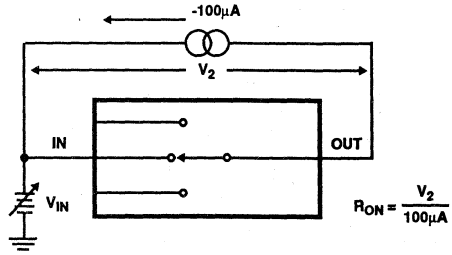


FIGURE 1A. ON RESISTANCE TEST CIRCUIT

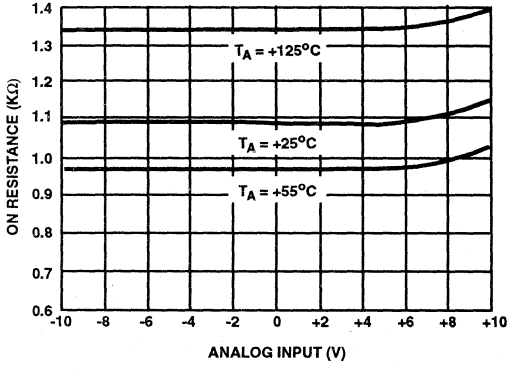


FIGURE 1B. ON RESISTANCE vs ANALOG INPUT VOLTAGE

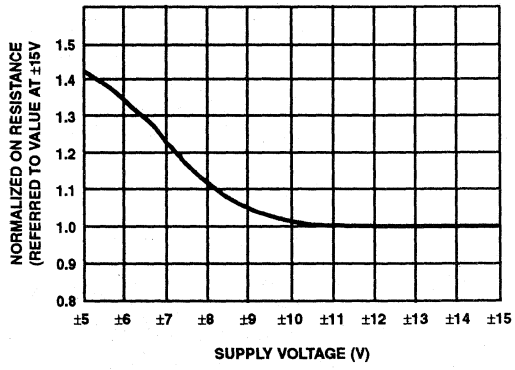


FIGURE 1C. NORMALIZED ON RESISTANCE vs SUPPLY VOLTAGE

FIGURE 1. ON RESISTANCE

Performance Curves T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified (Continued)

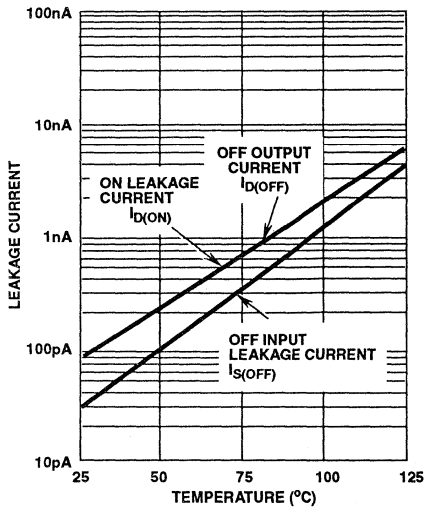


FIGURE 2A. LEAKAGE CURRENT vs TEMPERATURE

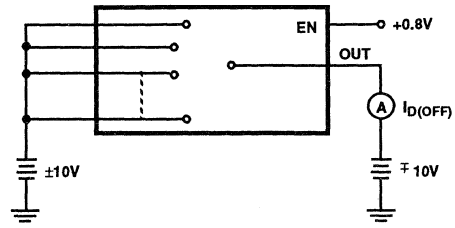


FIGURE 2B. $I_{D(OFF)}$ TEST CIRCUIT

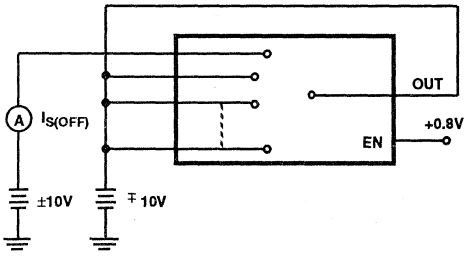


FIGURE 2C. $I_{S(OFF)}$ TEST CIRCUIT

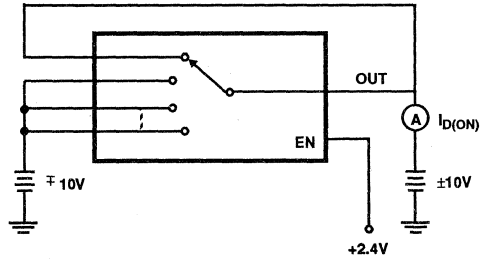


FIGURE 2D. $I_{D(ON)}$ TEST CIRCUIT

FIGURE 2. LEAKAGE CURRENT

NOTE:

1. Two measurements per channel: +10V/-10V and -10V/+10V. (Two measurements per device for $I_{D(OFF)}$: +10V/-10V and -10V/+10V)

Performance Curves (Continued)

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified

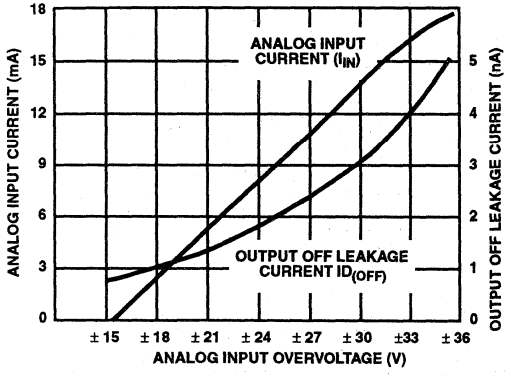


FIGURE 3A. ANALOG INPUT CURRENT AND OUTPUT OFF LEAKAGE CURRENT vs ANALOG INPUT OVERVOLTAGE

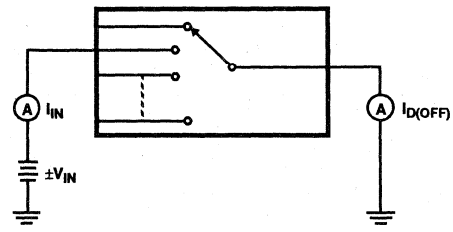


FIGURE 3B. ANALOG INPUT OVERVOLTAGE TEST CIRCUIT

FIGURE 3. ANALOG INPUT OVERVOLTAGE CHARACTERISTICS

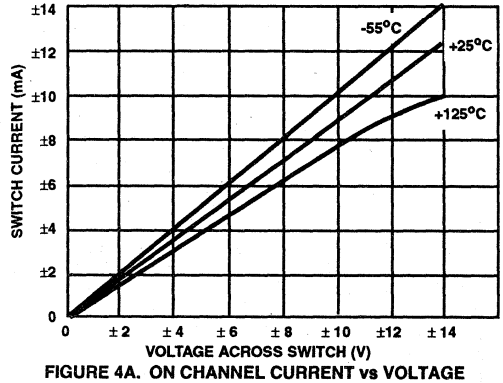


FIGURE 4A. ON CHANNEL CURRENT vs VOLTAGE

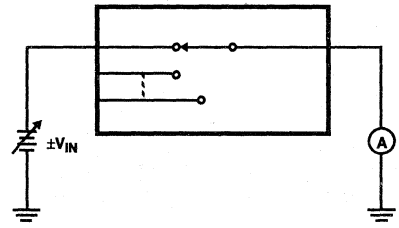


FIGURE 4B. ON CHANNEL CURRENT TEST CIRCUIT

FIGURE 4. ON CHANNEL CURRENT

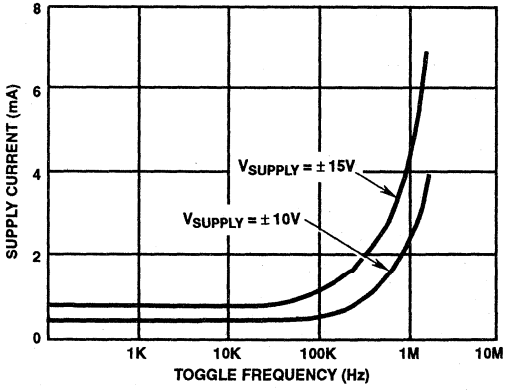
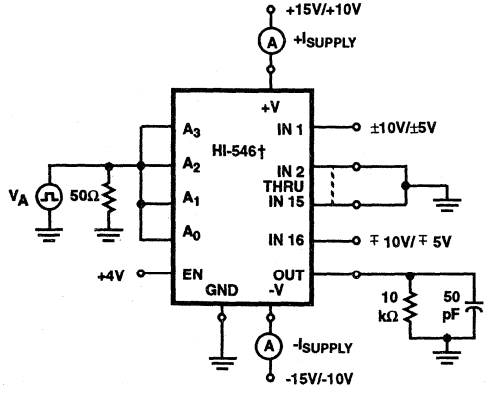


FIGURE 5A. SUPPLY CURRENT vs TOGGLE FREQUENCY



†Similar connection for HI-547/HI-548/HI-549

FIGURE 5B. SUPPLY CURRENT vs TOGGLE FREQUENCY

FIGURE 5. SUPPLY CURRENT

Performance Curves (Continued)

T_A = +25°C, V_{SUPPLY} = ±15V, V_{AH} = +4V, V_{AL} = 0.8V, V_{REF} = Open, Unless Otherwise Specified

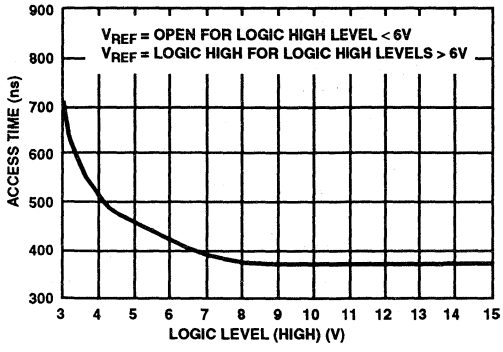
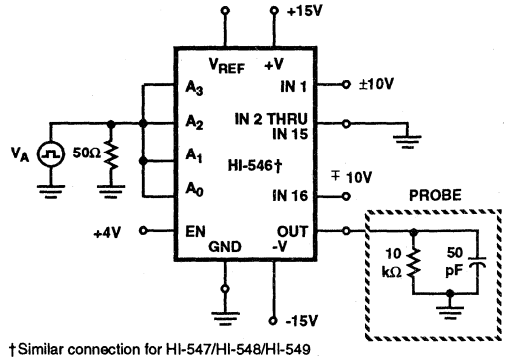


FIGURE 6A. ACCESS TIME vs LOGIC LEVEL (HIGH)



†Similar connection for HI-547/HI-548/HI-549

FIGURE 6B. ACCESS TIME TEST CIRCUIT

FIGURE 6. ACCESS TIME

Switching Waveforms

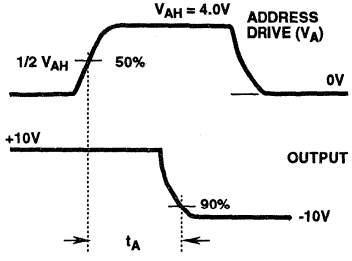


FIGURE 7A. ACCESS TIME MEASUREMENT

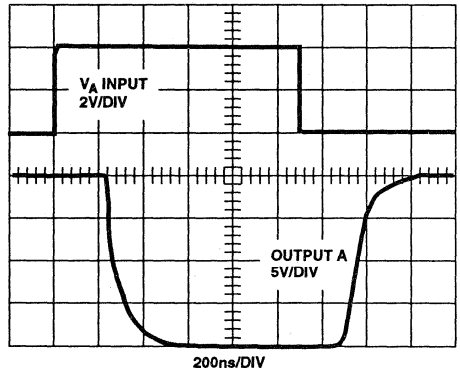
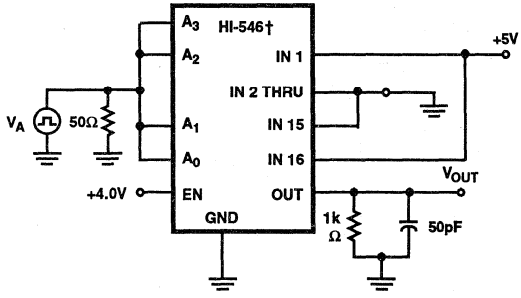


FIGURE 7B. ACCESS TIME WAVEFORMS

FIGURE 7. ACCESS TIME †

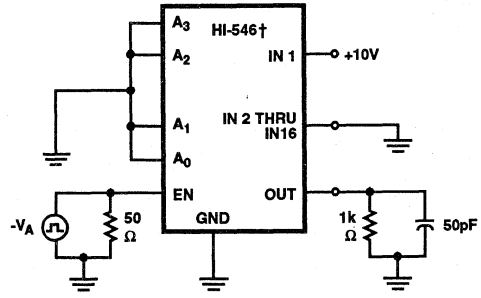
†Refer to Figure 6B for Test Circuit

Switching Waveforms (Continued)



†Similar connection for HI-547/HI-548/HI-549

FIGURE 8A. BREAK-BEFORE-MAKE DELAY TEST CIRCUIT



†Similar connection for HI-547/HI-548/HI-549

FIGURE 9A. ENABLE DELAY TEST CIRCUIT

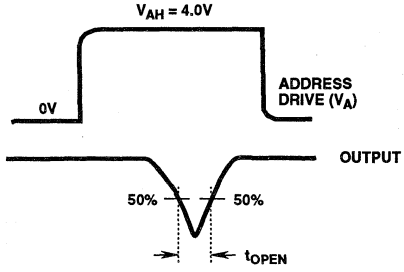


FIGURE 8B. BREAK-BEFORE-MAKE DELAY MEASUREMENT

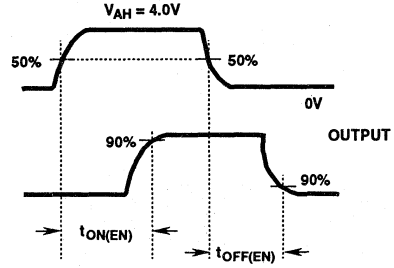


FIGURE 9B. ENABLE DELAY MEASUREMENTS

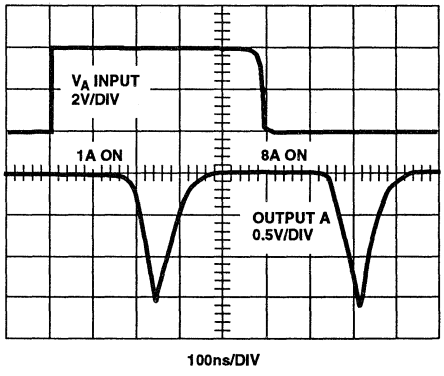


FIGURE 8C. BREAK-BEFORE-MAKE DELAY WAVEFORMS

FIGURE 8. BREAK-BEFORE-MAKE DELAY (t_{OPEN})

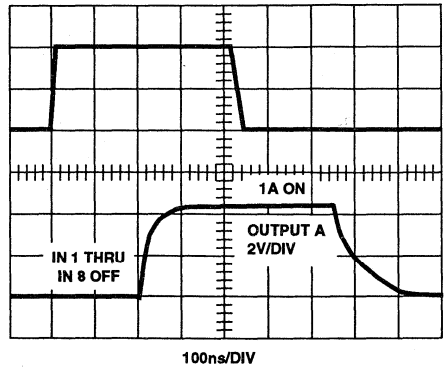


FIGURE 9C. ENABLE DELAY WAVEFORMS

FIGURE 9. ENABLE DELAY ($t_{ON(EN)}$, $t_{OFF(EN)}$)

Truth Tables

HI-546

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	None
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-547

A_2	A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-548

A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	L	None
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-549

A_1	A_0	EN	"ON" CHANNEL PAIR
X	X	L	None
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

Die Characteristics

DIE DIMENSIONS:
83.9 mils x 159 mils x 19 mils

METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ± 1kÅ
Silox Thickness: 12kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.4 \times 10^5 A/cm^2$

TRANSISTOR COUNT:
HI-546: 485
HI-547: 485

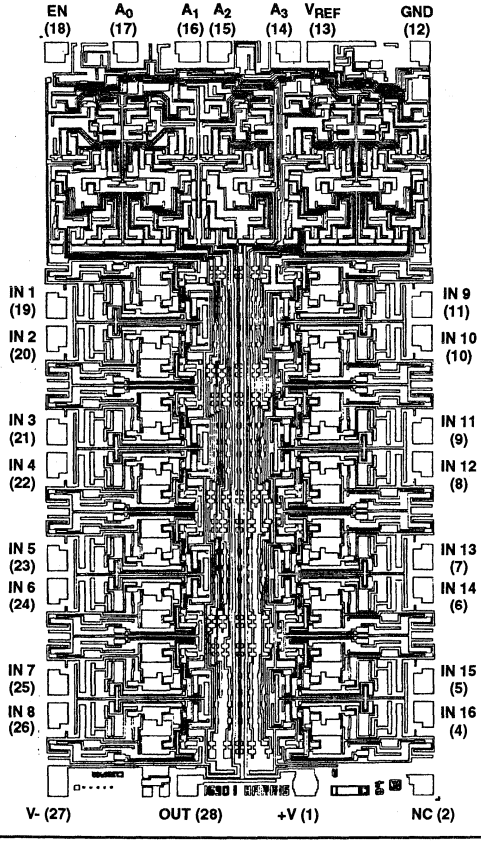
PROCESS: CMOS-DI

SUBSTRATE POTENTIAL †: $-V_{SUPPLY}$

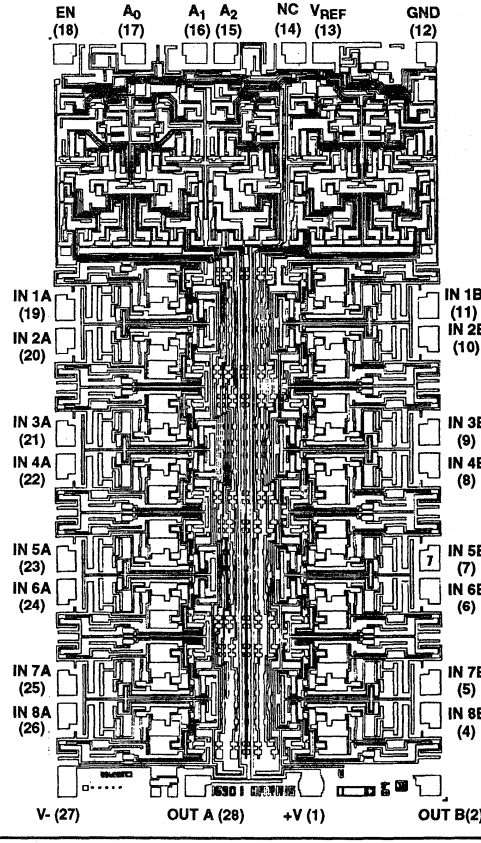
† The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layout

HI-546



HI-547



Die Characteristics

DIE DIMENSIONS:
83 mils x 108 mils x 19 mils

METALLIZATION:
Type: CuAl
Thickness: 16kÅ ± 2kÅ

GLASSIVATION:
Type: Nitride Over Silox
Nitride Thickness: 3.5kÅ ± 1kÅ
Silox Thickness: 12kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$1.4 \times 10^5 A/cm^2$

TRANSISTOR COUNT:
HI-548: 253
HI-549: 253

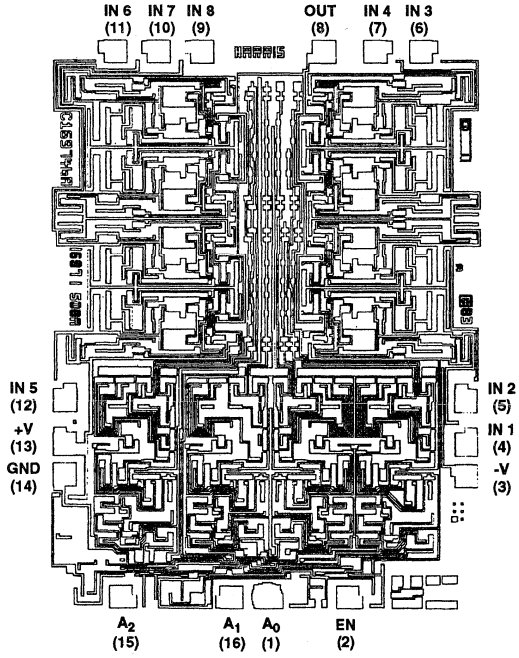
PROCESS: CMOS-DI

SUBSTRATE POTENTIAL†: $-V_{SUPPLY}$

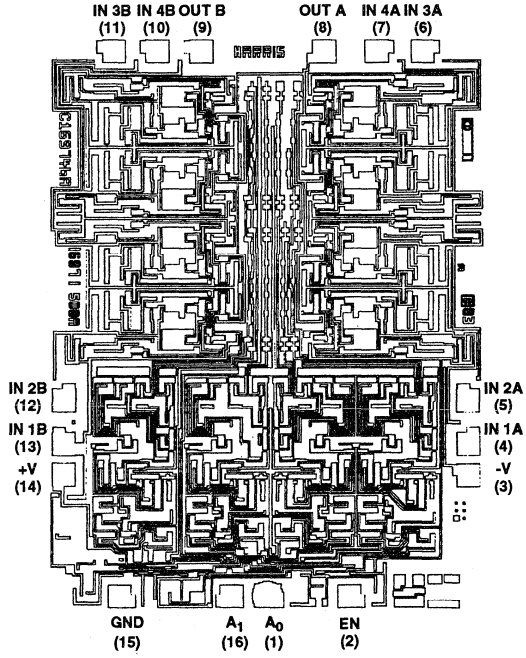
† The substrate appears resistive to the $-V_{SUPPLY}$ terminal, therefore it may be left floating (Insulating Die Mount) or it may be mounted on a conductor at $-V_{SUPPLY}$ potential.

Metallization Mask Layout

HI-548



HI-549



DATA ACQUISITION 11

COMMUNICATION INTERFACE

NOTE: Bold Type Designates a New Product from Harris.

HARRIS SEMICONDUCTOR HIN230 thru HIN241

ADVANCE INFORMATION

December 1993

+5V Powered RS-232 Transmitters/Receivers

Features

- **Meets All RS-232C and V.28 Specifications**
- **Requires Only Single +5V Power Supply**
  - **(+5V and +12V - HIN231 and HIN239)**
- **Onboard Voltage Doubler/Inverter**
- **Low Power Consumption**
- **Low Power Shutdown Function**
- **Tri-State TTL/CMOS Receiver Outputs**
- **Multiple Drivers**
  - **±10V Output Swing for +5V Input**
  - **300Ω Power-Off Source Impedance**
  - **Output Current Limiting**
  - **TTL/CMOS Compatible**
  - **30V/μs Maximum Slew Rate**
- **Multiple Receivers**
  - **±30V Input Voltage Range**
  - **3kΩ to 7kΩ Input Impedance**
  - **0.5V Hysteresis to Improve Noise Rejection**

Description

The HIN230-HIN241 family of RS-232 transmitters/receivers interface circuits meet all EIA RS-232C and V.28 specifications, and are particularly suited for those applications where ±12V is not available. They require a single +5V power supply (except HIN231 and HIN239) and features onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply. The family of devices offer a wide variety of RS232 transmitter/receiver combinations to accommodate various applications (see Selection Table).

The drivers feature true TTL/CMOS input compatibility, slew-rate-limited output, and 300Ω power-off source impedance. The receivers can handle up to +30V, and have a 3kΩ to 7kΩ input impedance. The receivers also feature hysteresis to greatly improve noise rejection.

Applications

- **Any System Requiring RS-232 Communications Port**
  - **Computer - Portable, Mainframe, Laptops**
  - **Peripheral - Printers and Terminals**
  - **Portable Instrumentation**
  - **Modems**

Selection Table

PART NUMBER	POWER SUPPLY VOLTAGE	NUMBER OF RS-232 DRIVERS	NUMBER OF RS-232 RECEIVERS	EXTERNAL COMPONENTS	LOW POWER SHUTDOWN /TTL TRI-STATE	NO. OF LEADS
HIN230	+5V	5	0	4 Capacitors	YES/NO	20
HIN231	+5V and +7.5V to 13.2V	2	2	2 Capacitors	NO/NO	16
HIN232	+5V	2	2	4 Capacitors	NO/NO	16
HIN234	+5V	4	0	4 Capacitors	NO/NO	16
HIN236	+5V	4	3	4 Capacitors	YES/YES	24
HIN237	+5V	5	3	4 Capacitors	NO/NO	24
HIN238	5V	4	4	4 Capacitors	NO/NO	24
HIN239	+5V and +7.5V to 13.2V	3	5	2 Capacitors	NO/YES	24
HIN240	+5V	5	5	4 Capacitors	YES/YES	44
HIN241	+5V	4	5	4 Capacitors	YES/YES	28

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIN230CB	0°C to +70°C	20 Lead SOIC
HIN230IB	-40°C to +85°C	20 Lead SOIC
HIN230BY		Die
HIN231CB	0°C to +70°C	16 Lead SOIC (W)
HIN231IB	-40°C to +85°C	16 Lead SOIC (W)
HIN231BY		Die
HIN232CP	0°C to +70°C	16 Lead Plastic DIP
HIN232CB	0°C to +70°C	16 Lead SOIC (W)
HIN232IP	-40°C to +85°C	16 Lead Plastic DIP
HIN232IJ	-40°C to +85°C	16 Lead Ceramic DIP
HIN232IB	-40°C to +85°C	16 Lead SOIC (W)
HIN232MJ	-55°C to +125°C	16 Lead Ceramic DIP
HIN232BY		Die
HIN234CB	0°C to +70°C	16 Lead SOIC (W)
HIN234IB	-40°C to +85°C	16 Lead SOIC (W)
HIN234BY		Die
HIN236CP	0°C to +70°C	24 Lead Plastic DIP
HIN236CB	0°C to +70°C	24 Lead SOIC
HIN236IP	-40°C to +85°C	24 Lead Plastic DIP
HIN236IB	-40°C to +85°C	24 Lead SOIC
HIN236BY		Die

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HIN237CP	0°C to +70°C	24 Lead Plastic DIP
HIN237CB	0°C to +70°C	24 Lead SOIC
HIN237IP	-40°C to +85°C	24 Lead Plastic DIP
HIN237IB	-40°C to +85°C	24 Lead SOIC
HIN237BY		Die
HIN238CP	0°C to +70°C	24 Lead Plastic DIP
HIN238CB	0°C to +70°C	24 Lead SOIC
HIN238IP	-40°C to +85°C	24 Lead Plastic DIP
HIN238IB	-40°C to +85°C	24 Lead SOIC
HIN238BY		Die
HIN239CP	0°C to +70°C	24 Lead Plastic DIP
HIN239CB	0°C to +70°C	24 Lead SOIC
HIN239IP	-40°C to +85°C	24 Lead Plastic DIP
HIN239IB	-40°C to +85°C	24 Lead SOIC
HIN239BY		Die
HIN240CN	0°C to +70°C	44 Lead MQFP
HIN240IN	-40°C to +85°C	44 Lead MQFP
HIN241CB	0°C to +70°C	28 Lead SOIC
HIN241IB	-40°C to +85°C	28 Lead SOIC
HIN241CA	0°C to +70°C	28 Lead SSOP
HIN241IA	-40°C to +85°C	28 Lead SSOP

Pin Description

PIN	FUNCTION
V_{CC}	Power Supply Input 5V ±10%
V+	Internally generated positive supply (+10V nominal), HIN231 and HIN239 requires +7.5V to +13.2V.
V-	Internally generated negative supply (-10V nominal).
GND	Ground lead. Connect to 0V.
C+	External capacitor (+ terminal) is connected to this lead.
C-	External capacitor (- terminal) is connected to this lead.
C2+	External capacitor (+ terminal) is connected to this lead.
C2-	External capacitor (- terminal) is connected to this lead.
T_{IN}	Transmitter Inputs. These leads accept TTL/CMOS levels. An internal 400KΩ pull-up resistor to V_{CC} is connected to each lead.
T_{OUT}	Transmitter Outputs. These are RS-232 levels (nominally ±10V).
R_{IN}	Receiver Inputs. These inputs accept RS-232 input levels. An internal 5KΩ pull-down resistor to GND is connected to each input.
R_{OUT}	Receiver Outputs. These are TTL/CMOS levels.
$\overline{EN}$	Enable input. This is an active low input which enables the receiver outputs. With EN = 5V, the outputs are placed in a high impedance state.
SD	Shutdown Input. With SD = 5V, the charge pump is disabled, the receiver outputs are in a high impedance state and the transmitters are shut off.
NC	No Connect. No connections are made to these leads.

Absolute Maximum Ratings

V_{CC} to Ground ..... (GND -0.3V) <V_{CC} < 6V
V+ to Ground ..... (V_{CC} -0.3V) <V+ < 12V
V- to Ground ..... -12V < V- < (GND +0.3V)
Input Voltages
$T1_{IN}$, $T2_{IN}$ ..... (V- -0.3V) < V_{IN} < (V+ +0.3V)
$R1_{IN}$, $R2_{IN}$ ..... ±30V
Output Voltages
$T1_{OUT}$, $T2_{OUT}$ ..... (V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
$R1_{OUT}$, $R2_{OU}T$ ..... (GND -0.3V) < V_{RXOUT} < (V+ +0.3V)
Short Circuit Duration
$T1_{OUT}$, $T2_{OUT}$ ..... Continuous
$R1_{OUT}$, $R2_{OUT}$ ..... Continuous

Thermal Information

Continuous Total Power Dissipation (T_A = +25°C)

Package	θ_{JA}	θ_{JC}
Plastic DIP 16 Lead	100°C/W	-
Plastic DIP 24 Lead	75°C/W	-
Plastic SOIC 16 Lead (W)	100°C/W	-
Plastic SOIC 24 Lead	85°C/W	-
Plastic SOIC 28 Lead	80°C/W	-
Plastic SSOP 28 Lead	100°C/W	-
Plastic MQFP 44 Lead	80°C/W	-
16 Lead CERDIP	80°C/W	24°C/W

Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
Operating Temperature Range
HIN-XXXCX ..... 0°C to +70°C
HIN-XXXIX ..... -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, T_A = Operating Temperature Range

PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Output Voltage Swing, T_{OUT}	Transmitter Outputs, 3kΩ to Ground	±5	±9	±10	V
Power Supply Current, I_{CC}	No Load, T_A = +25°C, HIN232-233	-	5	10	mA
	HIN230, HIN234-238, HIN240-241	-	7	15	mA
	HIN231, HIN239	-	0.4	1	mA
Shutdown Supply Current, I_{CC}(SD)			1	10	µA
Input Logic Low, T_{IN}, $\overline{EN}$, V_{IL}	T_{IN}, $\overline{EN}$, Shutdown	-	-	0.8	V
Input Logic High, V_{IH}	T_{IN}	2.0	-	-	V
	$\overline{EN}$, Shutdown	2.4	-	-	V
Logic Pullup Current, I_P	$T1_{IN}$, $T2_{IN}$ = 0V	-	15	200	µA
RS-232 Input Voltage Range, V_{IN}		-30	-	+30	V
Receiver Input Impedance, R_{IN}	V_{IN} = ±3V	3.0	5.0	7.0	kΩ
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5.0V, T_A = +25°C	0.8	1.2	-	V
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5.0V, T_A = +25°C	-	1.7	2.4	V
Receiver Input Hysteresis, V_{HYST}		0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 1.6mA H/N (231-232 I_{OUT} = 3.2mA)	-	0.1	0.4	V
TTL/CMOS Receiver Output voltage High, V_{OH}	I_{OUT} = -1.0mA	3.5	4.6	-	V
Output Enable Time, t_{EN}	HIN236, 239, 240, 241		400		ns
Output Disable Time, t_{DIS}	HIN236, 239, 240, 241		250		ns
Propagation Delay, t_{PD}	RS-232 to TTL	-	0.5	-	µs
Instantaneous Slew Rate, SR	C_L = 10pF, R_L = 3kΩ, T_A = +25°C (Note 1)	-	-	30	V/µs
Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V	-	3	-	V/µs
Output Resistance, R_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V	300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	$T1_{OUT}$ or $T2_{OUT}$ shorted to GND	-	±10	-	mA

NOTE: 1. Guaranteed by design.

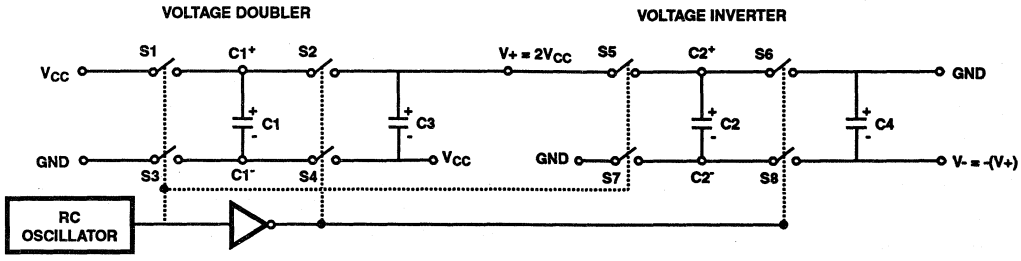


FIGURE 1. CHARGE PUMP

Detailed Description

The HIN230 thru HIN241 family of RS-232 transmitters/receivers are powered by a single +5V power supply (except HIN-231 and HIN239), feature low power consumption, and meet all EIA RS232C and V.28 specifications. The circuit is divided into three sections: the charge pump, transmitter, and receiver.

Charge Pump

An equivalent circuit of the charge pump is illustrated in Figure 1. The charge pump contains two sections: the voltage doubler and the voltage inverter. Each section is driven by a two phase, internally generated clock to generate +10V and -10V. The nominal clock frequency is 16kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C3 equal to twice V_{CC}. At the same time, C2 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The charge pump accepts input voltages up to 5.5V. The output impedance of the voltage doubler section (V+) is approximately 200Ω, and the output impedance of the voltage inverter section (V-) is approximately 450Ω. A typical application uses 1µF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the ouput impedance of the voltage doubler and inverter, increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.

During shutdown mode (HIN230, 235, 236, 240 and 241), SHUTDOWN control line set to logic "1", the charge pump is turned off, V+ is pulled down to V_{CC}, V- is pulled up to GND, and the supply current is reduced to less than 10µA. The transmitter outputs are disabled and the receiver outputs are placed in the high impedance state.

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ -0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specifications of ±5V minimum with the worst case conditions of: all transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/µs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with ±2V applied to the outputs and V_{CC} = 0V.

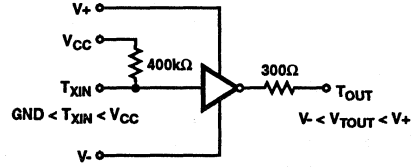


FIGURE 2. TRANSMITTER

Receivers

The receiver inputs accept up to ±30V while presenting the required 3kΩ to 7kΩ input impedance even it the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specifications. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis to improve noise rejection. The receiver Enable line $\overline{EN}$, when set to logic "1", (HIN235, 236, 239, 240, and 241) disables the receiver outputs, placing them in the high impedance mode. The receiver outputs are also placed in the high impedance state when in shutdown mode.

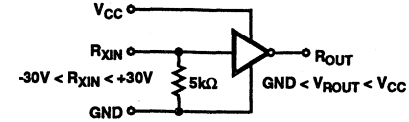


FIGURE 3. RECEIVER

HARRIS SEMICONDUCTOR

ICL232

+5V Powered Dual RS-232 Transmitter/Receiver

December 1993

Features

- Meets All RS-232C Specifications
- Requires Only Single +5V Power Supply
- Onboard Voltage Doubler/Inverter
- Low Power Consumption
- 2 Drivers
  - ±9V Output Swing for +5V Input
  - 300Ω Power-off Source Impedance
  - Output Current Limiting
  - TTL/CMOS Compatible
  - 30V/μs Maximum Slew Rate
- 2 Receivers
  - ±30V Input Voltage Range
  - 3kΩ to 7kΩ Input Impedance
  - 0.5V Hysteresis to Improve Noise Rejection
- All Critical Parameters are Guaranteed Over the Entire Commercial, Industrial and Military Temperature Ranges

Applications

- Any System Requiring RS-232 Communications Port
  - Computer - Portable and Mainframe
  - Peripheral - Printers and Terminals
  - Portable Instrumentation
  - Modems
  - Dataloggers

Description

The ICL232 is a dual RS-232 transmitter/receiver interface circuit that meets all EIA RS-232C specifications. It requires a single +5V power supply, and features two onboard charge pump voltage converters which generate +10V and -10V supplies from the 5V supply.

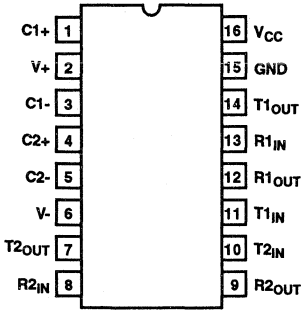
The drivers feature true TTL/CMOS input compatibility, slew-rate-limited output, and 300Ω power-off source impedance. The receivers can handle up to +30V, and have a 3kΩ to 7kΩ input impedance. The receivers also have hysteresis to improve noise rejection.

Ordering Information

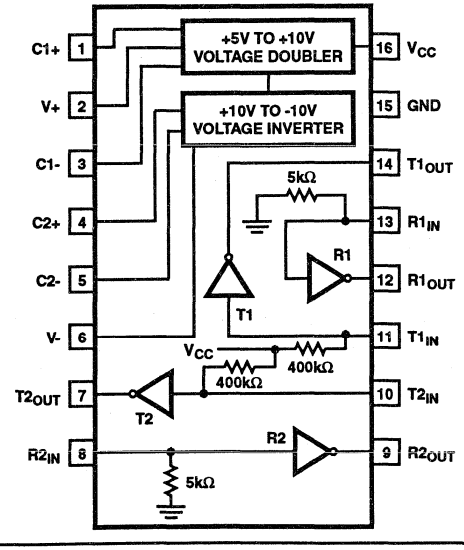
PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICL232CPE	0°C to +70°C	16 Lead Plastic DIP
ICL232CJE	0°C to +70°C	16 Lead Ceramic DIP
ICL232CBE	0°C to +70°C	16 Lead SOIC (W)
ICL232IPE	-40°C to +85°C	16 Lead Plastic DIP
ICL232IJE	-40°C to +85°C	16 Lead Ceramic DIP
ICL232IBE	-40°C to +85°C	16 Lead SOIC (W)
ICL232MJE	-55°C to + 125°C	16 Lead Ceramic DIP

Pinouts

ICL232
(PDIP, CDIP, SOIC)
TOP VIEW



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3020.2

Absolute Maximum Ratings

V_{CC} to Ground ..... (GND -0.3V) <V_{CC} < 6V
V+ to Ground ..... (V_{CC} -0.3V) <V+ < 12V
V- to Ground ..... -12V < V- < (GND +0.3V)
Input Voltages
$T1_{IN}$, $T2_{IN}$ ..... (V- -0.3V) < V_{IN} < (V+ +0.3V)
$R1_{IN}$, $R2_{IN}$ ..... ±30V
Output Voltages
$T1_{OUT}$, $T2_{OUT}$ ..... (V- -0.3V) < V_{TXOUT} < (V+ +0.3V)
$R1_{OUT}$, $R2_{OUT}$ ..... (GND -0.3V) < V_{RXOUT} < (V_{CC} +0.3V)
Short Circuit Duration
$T1_{OUT}$, $T2_{OUT}$ ..... Continuous
$R1_{OUT}$, $R2_{OUT}$ ..... Continuous
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	80°C/W	24°C/W
Plastic DIP Package	100°C/W	-
SOIC Package	100°C/W	-

Maximum Power Dissipation 250mW
Operating Temperature Range
ICL232C ..... 0°C to +70°C
ICL232I ..... -40°C to +85°C
ICL232M ..... -55°C to +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Test Conditions: V_{CC} = +5V ±10%, T_A = Operating Temperature Range. Test Circuit as in Figure 8 Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Transmitter Output Voltage Swing, T_{OUT}	$T1_{OUT}$ and $T2_{OUT}$ loaded with 3kΩ to Ground	±5	±9	±10	V
Power Supply Current, I_{CC}	Outputs Unloaded, T_A = +25°C	-	5	10	mA
T_{IN}, Input Logic Low, V_{IL}		-	-	0.8	V
T_{IN}, Input Logic High, V_{IH}		2.0	-	-	V
Logic Pullup Current, I_P	$T1_{IN}$, $T2_{IN}$ = 0V	-	15	200	µA
RS-232 Input Voltage Range, V_{IN}		-30	-	+30	V
Receiver Input Impedance, R_{IN}	V_{IN} = ±3V	3.0	5.0	7.0	kΩ
Receiver Input Low Threshold, V_{IN} (H-L)	V_{CC} = 5.0V, T_A = +25°C	0.8	1.2	-	V
Receiver Input High Threshold, V_{IN} (L-H)	V_{CC} = 5.0V, T_A = +25°C	-	1.7	2.4	V
Receiver Input Hysteresis, V_{HYST}		0.2	0.5	1.0	V
TTL/CMOS Receiver Output Voltage Low, V_{OL}	I_{OUT} = 3.2mA	-	0.1	0.4	V
TTL/CMOS Receiver Output Voltage High, V_{OH}	I_{OUT} = -1.0mA	3.5	4.6	-	V
Propagation Delay, t_{PD}	RS-232 to TTL	-	0.5	-	µs
Instantaneous Slew Rate, SR	C_L = 10pF, R_L = 3kΩ, T_A = +25°C (Notes 1, 2)	-	-	30	V/µs
Transition Region Slew Rate, SR_T	R_L = 3kΩ, C_L = 2500pF Measured from +3V to -3V or -3V to +3V	-	3	-	V/µs
Output Resistance, R_{OUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V	300	-	-	Ω
RS-232 Output Short Circuit Current, I_{SC}	$T1_{OUT}$ or $T2_{OUT}$ shorted to GND	-	±10	-	mA

NOTES:

1. Guaranteed by design.
2. See Figure 4 for definition.

Typical Performance Curves

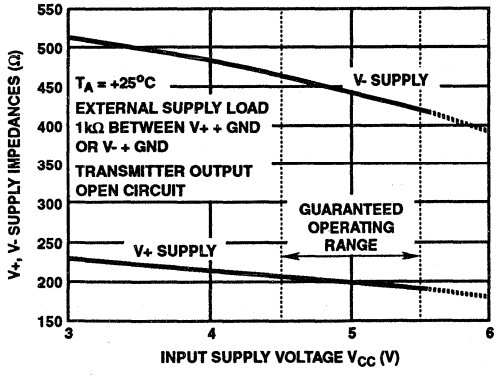


FIGURE 1. V+, V- OUTPUT IMPEDANCES vs V_{CC}

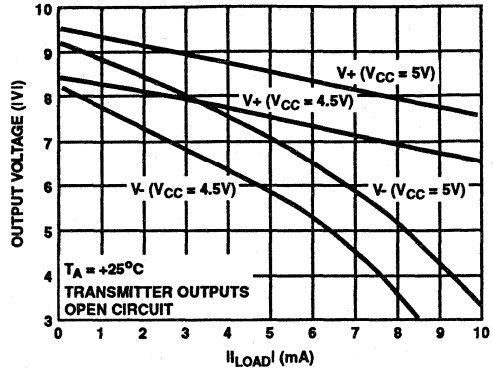


FIGURE 2. V+, V- OUTPUT VOLTAGES vs LOAD CURRENT

Pin Descriptions

PLASTIC DIP, CERAMIC DIP	SOIC	PIN NAME	DESCRIPTION
1	1	C1+	External capacitor "+" for internal voltage doubler.
2	2	V+	Internally generated +10V (typical) supply.
3	3	C1-	External capacitor "-" for internal voltage doubler.
4	4	C2+	External capacitor "+" internal voltage inverter.
5	5	C2-	External capacitor "-" internal voltage inverter.
6	6	V-	Internally generated -10V (typical) supply.
7	7	$T2_{OUT}$	RS-232 Transmitter 2 output ±10V (typical).
8	8	$R2_{IN}$	RS-232 Receiver 2 input, with internal 5K pulldown resistor to GND.
9	9	R2out	Receiver 2 TTL/CMOS output.
10	10	$T2_{IN}$	Transmitter 2 TTL/CMOS input, with internal 400K pullup resistor to V_{CC}.
11	11	$T1_{IN}$	Transmitter 1 TTL/CMOS input, with internal 400K pullup resistor to V_{CC}.
12	12	$R1_{OUT}$	Receiver 1 TTL/CMOS output.
13	13	$R1_{IN}$	RS-232 Receiver 1 input, with internal 5K pulldown resistor to GND.
14	14	$T1_{OUT}$	RS-232 Transmitter 1 output ±10V (typical).
15	15	GND	Supply Ground.
16	16	VCC	Positive Power Supply +5V ±10%

Detailed Description

The ICL232 is a dual RS-232 transmitter/receiver powered by a single +5V power supply which meets all EIA RS232C specifications and features low power consumption. The functional diagram illustrates the major elements of the ICL232. The circuit is divided into three sections: a voltage doubler/inverter, dual transmitters, and dual receivers.

Voltage Converter

An equivalent circuit of the dual charge pump is illustrated in Figure 3.

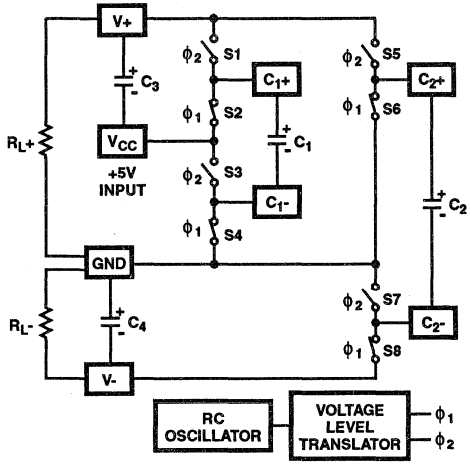
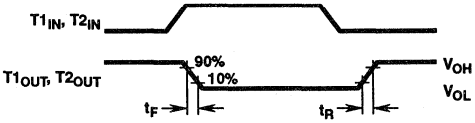


FIGURE 3. DUAL CHARGE PUMP

The voltage quadrupler contains two charge pumps which use two phases of an internally generated clock to generate +10V and -10V. The nominal clock frequency is 16kHz. During phase one of the clock, capacitor C1 is charged to V_{CC}. During phase two, the voltage on C1 is added to V_{CC}, producing a signal across C2 equal to twice V_{CC}. At the same time, C3 is also charged to $2V_{CC}$, and then during phase one, it is inverted with respect to ground to produce a signal across C4 equal to $-2V_{CC}$. The voltage converter accepts input voltages up to 5.5V. The output impedance of the doubler (V+) is approximately 200Ω, and the output impedance of the inverter (V-) is approximately 450Ω. Typical graphs are presented which show the voltage converters output vs input voltage and output voltages vs load characteristics. The test circuit (Figure 8) uses 1µF capacitors for C1-C4, however, the value is not critical. Increasing the values of C1 and C2 will lower the output impedance of the voltage doubler and inverter, and increasing the values of the reservoir capacitors, C3 and C4, lowers the ripple on the V+ and V- supplies.



Instantaneous Slew Rate (SR) $= \frac{(0.8)(V_{OH} - V_{OL})}{t_R}$ or $\frac{(0.8)(V_{OL} - V_{OH})}{t_F}$

FIGURE 4. SLEW RATE DEFINITION

Transmitters

The transmitters are TTL/CMOS compatible inverters which translate the inputs to RS-232 outputs. The input logic threshold is about 26% of V_{CC}, or 1.3V for V_{CC} = 5V. A logic 1 at the input results in a voltage of between -5V and V- at the output, and a logic 0 results in a voltage between +5V and (V+ -0.6V). Each transmitter input has an internal 400kΩ pullup resistor so any unused input can be left unconnected and its output remains in its low state. The output voltage swing meets the RS-232C specification of ±5V minimum with the worst case conditions of: both transmitters driving 3kΩ minimum load impedance, V_{CC} = 4.5V, and maximum allowable operating temperature. The transmitters have an internally limited output slew rate which is less than 30V/µs. The outputs are short circuit protected and can be shorted to ground indefinitely. The powered down output impedance is a minimum of 300Ω with ±2V applied to the outputs and V_{CC} = 0V.

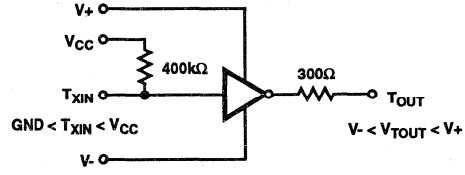


FIGURE 5. TRANSMITTER

Receivers

The receiver inputs accept up to ±30V while presenting the required 3kΩ to 7kΩ input impedance even it the power is off (V_{CC} = 0V). The receivers have a typical input threshold of 1.3V which is within the ±3V limits, known as the transition region, of the RS-232 specification. The receiver output is 0V to V_{CC}. The output will be low whenever the input is greater than 2.4V and high whenever the input is floating or driven between +0.8V and -30V. The receivers feature 0.5V hysteresis to improve noise rejection.

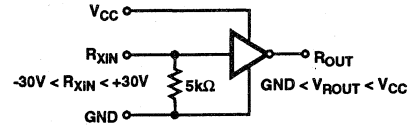
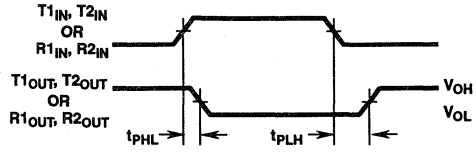


FIGURE 6. RECEIVER



Average Propagation Delay $= \frac{t_{PHL} + t_{PLH}}{2}$

FIGURE 7. PROPAGATION DELAY DEFINITION

Test Circuits

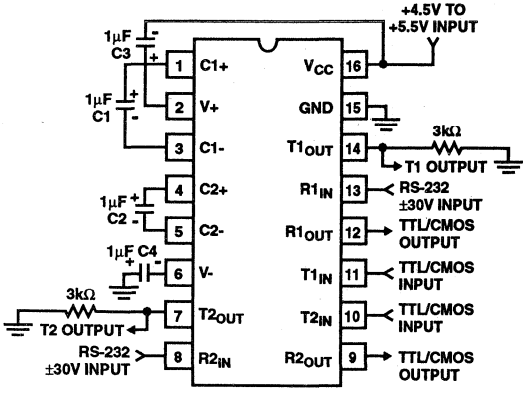


FIGURE 8. GENERAL TEST CIRCUIT

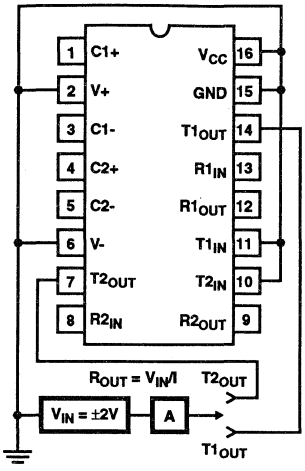


FIGURE 9. POWER-OFF SOURCE RESISTANCE CONFIGURATION

Applications

The ICL232 may be used for all RS-232 data terminal and communication links. It is particularly useful in applications where ±12V power supplies are not available for conventional RS-232 interface circuits. The applications presented represent typical interface configurations.

A simple duplex RS-232 port with CTS/RTS handshaking is illustrated in Figure 10. Fixed output signals such as DTR (data terminal ready) and DSRS (data signaling rate select) is generated by driving them through a 5kΩ resistor connected to V+.

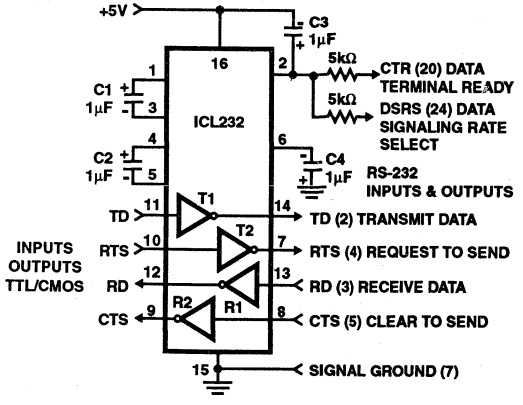


FIGURE 10. SIMPLE DUPLEX RS-232 PORT WITH CTS/RTS HANDSHAKING

In applications requiring four RS-232 inputs and outputs (Figure 11), note that each circuit requires two charge pump capacitors (C1 and C2) but can share common reservoir capacitors (C3 and C4). The benefit of sharing common reservoir capacitors is the elimination of two capacitors and the reduction of the charge pump source impedance which effectively increases the output swing of the transmitters.

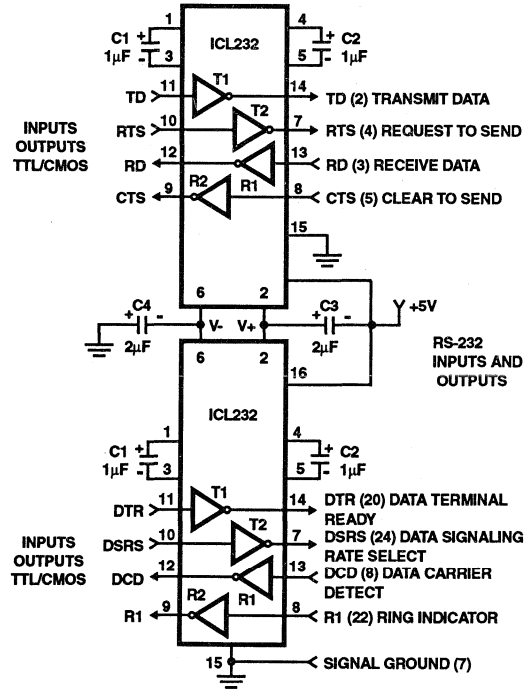


FIGURE 11. COMBINING TWO ICL232s FOR 4 PAIRS OF RS-232 INPUTS AND OUTPUTS

DATA ACQUISITION 12

DISPLAY DRIVERS

HARRIS SEMICONDUCTOR

CA3161

BCD to Seven Segment Decoder/Driver

December 1993

Features

- **TTL Compatible Input Logic Levels**
- **25mA (Typ) Constant Current Segment Outputs**
- **Eliminates Need for Output Current Limiting Resistors**
- **Pin Compatible with Other Industry Standard Decoders**
- **Low Standby Power Dissipation 18mW (Typ)**

Description

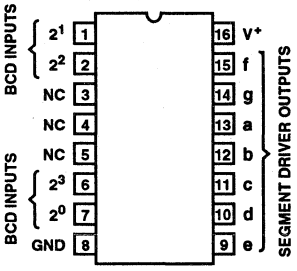
The CA3161E is a monolithic integrated circuit that performs the BCD to seven segment decoding function and features constant current segment drivers. When used with the CA3162E A/D Converter the CA3161E provides a complete digital readout system with a minimum number of external parts.

The CA3161 is supplied in the 16 lead dual in line plastic package (E suffix).

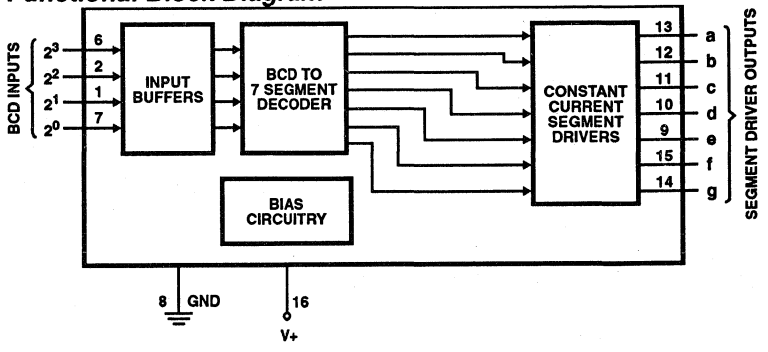
Ordering Information

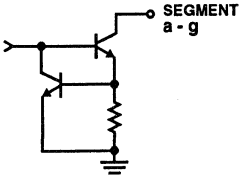
PART NUMBER	TEMPERATURE RANGE	PACKAGE
CA3161E	0°C to +70°C	16 Lead Plastic DIP

Pinout

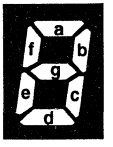


Functional Block Diagram





SEGMENT DRIVER



SEGMENT IDENTIFICATION

12 DISPLAY DRIVERS

File Number **1079.2**

Absolute Maximum Ratings

DC V_{SUPPLY} (Between Terminals 1 and 10) . . . . . +7.0V
Input Voltage (Terminals 1, 2, 6, 7) . . . . . +5.5V
Output Voltage
  Output "Off" . . . . . +7V
  Output "On" (Note 1) . . . . . +10V
Device Dissipation
  Up To T_A = +55°C 1W
  Above T_A = +55°C . . . . . Derate Linearly at 10.5mW/°C
Ambient Temperature Range
  Operating . . . . . 0°C to +75°C
  Storage . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +265°C

Thermal Information

Thermal Resistance	θ_{JA}
Plastic DIP Package	100°C/W
Junction Temperature	+150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

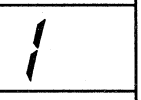
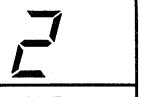
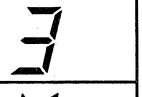
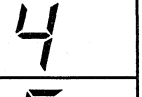
Electrical Specifications T_A = +25°C

PARAMETERS		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
V_{SUPPLY} Operating Range, V^+		4.5	5	5.5	V
Supply Current, I^+ (All Inputs High)		-	3.5	8	mA
Output Current Low (V_O = 2V)		18	25	32	mA
Output Current High (V_O = 5.5V)		-	-	250	µA
Input Voltage High (Logic "1" Level)		2	-	-	V
Input Voltage Low (Logic "0" Level)		-	-	0.8	V
Input Current High (Logic "1")	2V	-30	-	-	µA
Input Current Low (Logic "0")	0V	-40	-	-	µA
Propagation Delay Time	t_{PHL}	-	2.6	-	µs
	t_{PLH}	-	1.4	-	µs

NOTE:

1. This is the maximum output voltage for any single output. The output voltage must be consistent with the maximum dissipation and derating curve for worst case conditions. Example: All segments "ON", 100% duty cycle.

TRUTH TABLE

BINARY STATE	INPUTS				OUTPUTS							DISPLAY
	2^3	2^2	2^1	2^0	a	b	c	d	e	f	g	
0	L	L	L	L	L	L	L	L	L	L	H	
1	L	L	L	H	H	L	L	H	H	H	H	
2	L	L	H	L	L	L	H	L	L	H	L	
3	L	L	H	H	L	L	L	L	H	H	L	
4	L	H	L	L	H	L	L	H	H	L	L	
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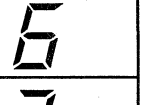
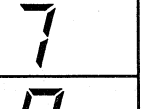
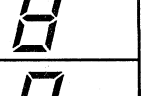
6	L	H	H	L	L	H	L	L	L	L	L	
7	L	H	H	H	L	L	L	H	H	H	H	
8	H	L	L	L	L	L	L	L	L	L	L	
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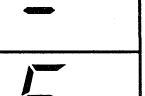
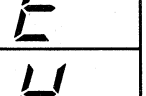
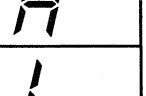
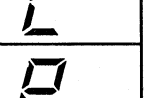
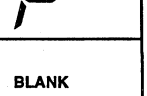
10	H	L	H	L	H	H	H	H	H	H	L	
11	H	L	H	H	L	H	H	L	L	L	L	
12	H	H	L	L	H	L	L	H	L	L	L	
13	H	H	L	H	H	H	H	L	L	L	H	
14	H	H	H	L	L	L	H	H	L	L	L	
15	H	H	H	H	H	H	H	H	H	H	H	BLANK

HARRIS SEMICONDUCTOR

ICM7211, ICM7212

4-Digit ICM7211 (LCD) and ICM7212 (LED) Display Drive

December 1993

Features ICM7211 (LCD)

- **Four Digit Non-Multiplexed 7 Segment LCD Display Outputs With Backplane Driver**
- **Complete Onboard RC Oscillator to Generate Backplane Frequency**
- **Backplane Input/Output Allows Simple Synchronization of Slave-Devices to a Master**
- **ICM7211 Devices Provide Separate Digit Select Inputs to Accept Multiplexed BCD Input (Pinout and Functionally Compatible With Siliconix DF411)**
- **ICM7211M Devices Provide Data and Digit Address Latches Controlled by Chip Select Inputs to Provide a Direct High Speed Processor Interface**
- **ICM7211 Decodes Binary to Hexadecimal; ICM7211A Decodes Binary to Code B (0-9, Dash, E, H, L, P, Blank)**
- **ICM7211A Available in Surface Mount Package**

Features ICM7212AM (LED)

- **28 Current-Limited Segment Outputs Provide 4-Digit Non-Multiplexed Direct LED Drive at >5mA Per Segment**
- **Brightness Input Allows Direct Control of LED Segment Current With a Single Potentiometer or Digitally as a Display Enable**
- **ICM7212AM Device Provides Same Input Configuration and Output Decoding Options as the ICM7211AM**

Description

The ICM7211 (LCD) and ICM7212 (LED) devices constitute a family of non-multiplexed four-digit seven-segment CMOS display decoder-drivers.

The ICM7211 devices are configured to drive conventional LCD displays by providing a complete RC oscillator, divider chain, backplane driver, and 28 segment outputs.

The ICM7212 devices are configured to drive common-anode LED displays, providing 28 current-controlled, low leakage, open-drain n-channel outputs. These devices provide a BRighTness input, which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

These devices are available with multiplexed or microprocessor input configurations. The multiplexed versions provide four data inputs and four Digit Select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226, and ICL7135. The microprocessor versions provide data input latches and Digit Address latches under control of high-speed Chip Select inputs. These devices simplify the task of implementing a cost-effective alphanumeric seven-segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices will provide two different decoder configurations. The basic device will decode the four bit binary inputs into a seven-segment alphanumeric hexadecimal output. The "A" versions will provide the "Code B" output code, i.e., 0-9, dash, E, H, L, P, blank. Either device will correctly decode true BCD to seven-segment decimal outputs.

Devices in the ICM7211 and ICM7212 family are packaged in a standard 40 lead plastic dual-in-line and 44 lead plastic MQFP packages and all inputs are fully protected against static discharge.

Ordering Information

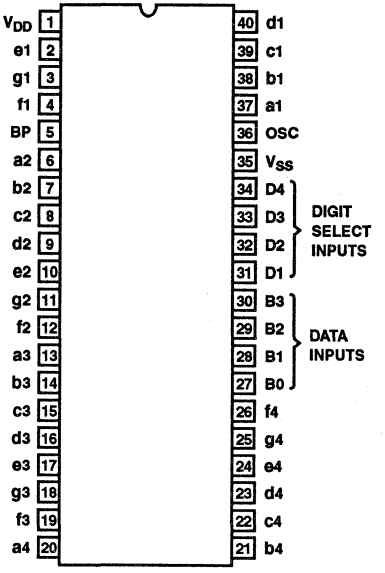
PART NUMBER	DISPLAY TYPE	DISPLAY DECODING	INPUT INTERFACING	DISPLAY DRIVE TYPE	TEMPERATURE RANGE	PACKAGE
ICM7211IPL	LCD	Hexadecimal	Multiplexed	Direct Drive	-40°C to +85°C	40 Lead Plastic DIP
ICM7211MIPL	LCD	Hexadecimal	Microprocessor	Direct Drive	-40°C to +85°C	40 Lead Plastic DIP
ICM7211AIPL	LCD	Code B	Multiplexed	Direct Drive	-40°C to +85°C	40 Lead Plastic DIP
ICM7211AMIPL	LCD	Code B	Microprocessor	Direct Drive	-40°C to +85°C	40 Lead Plastic DIP
ICM7211AIM44	LCD	Code B	Multiplexed	Direct Drive	-40°C to +85°C	44 Lead MQFP Flatpack
ICM7211AMIM44	LCD	Code B	Microprocessor	Direct Drive	-40°C to +85°C	44 Lead MQFP Flatpack
ICM7212AMIPL	LED	Code B	Microprocessor	Common Anode	-40°C to +85°C	40 Lead Plastic DIP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

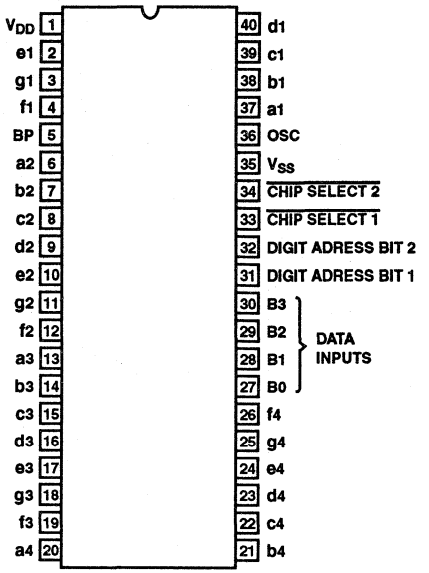
File Number **3158**

Pinouts

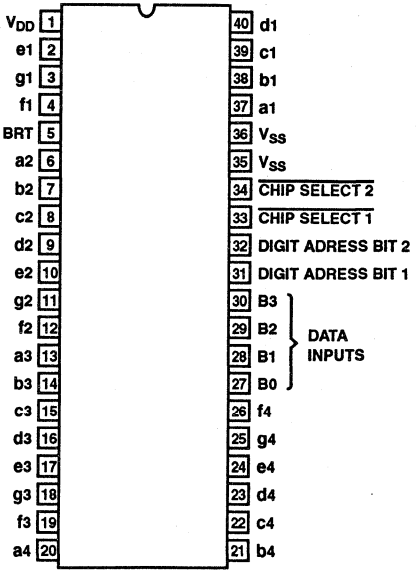
ICM7211, ICM7211A
(PDIP)
TOP VIEW



ICM7211M, ICM7211AM
(PDIP)
TOP VIEW

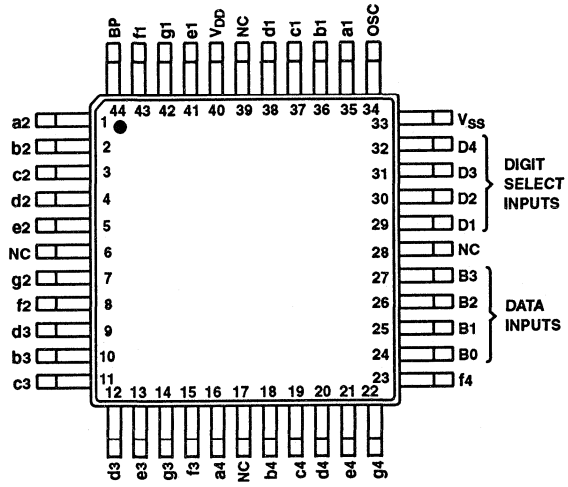


ICM7212AM
(PDIP)
TOP VIEW

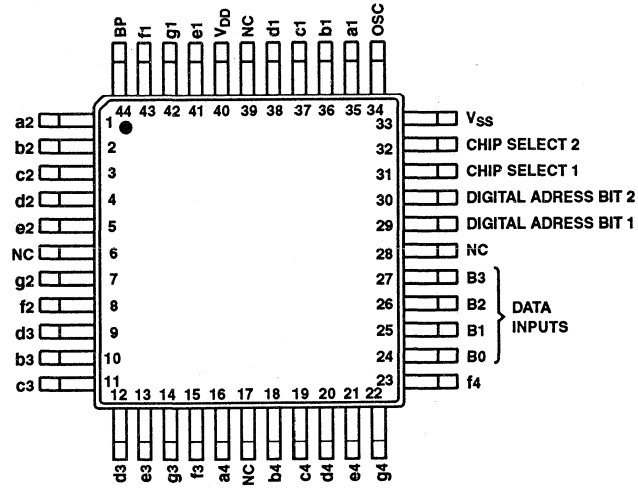


Pinouts (Continued)

ICM7211A
(PLASTIC FLATPACK)
TOP VIEW

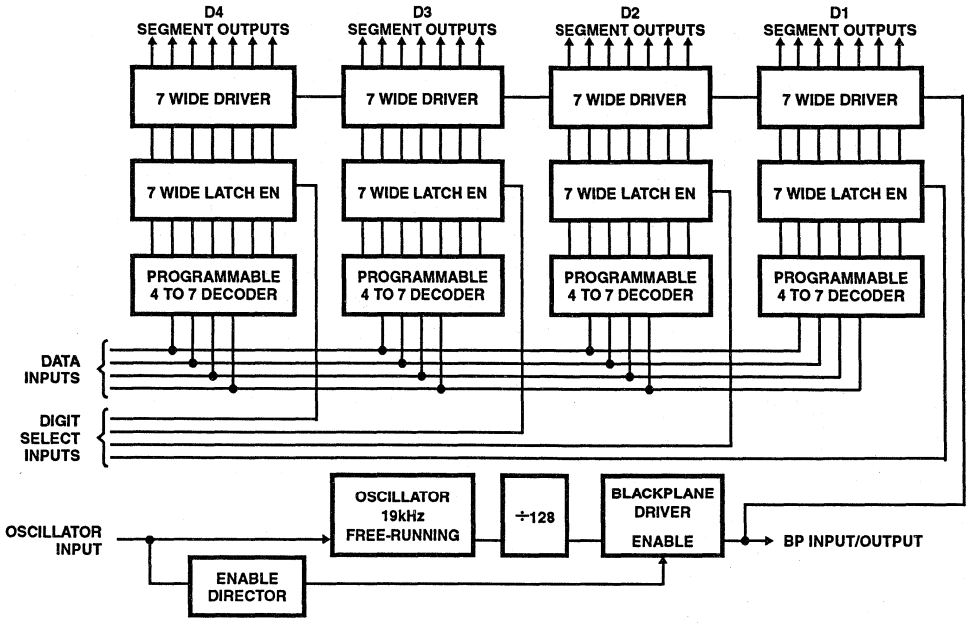


ICM7211AM
(PLASTIC FLATPACK)
TOP VIEW

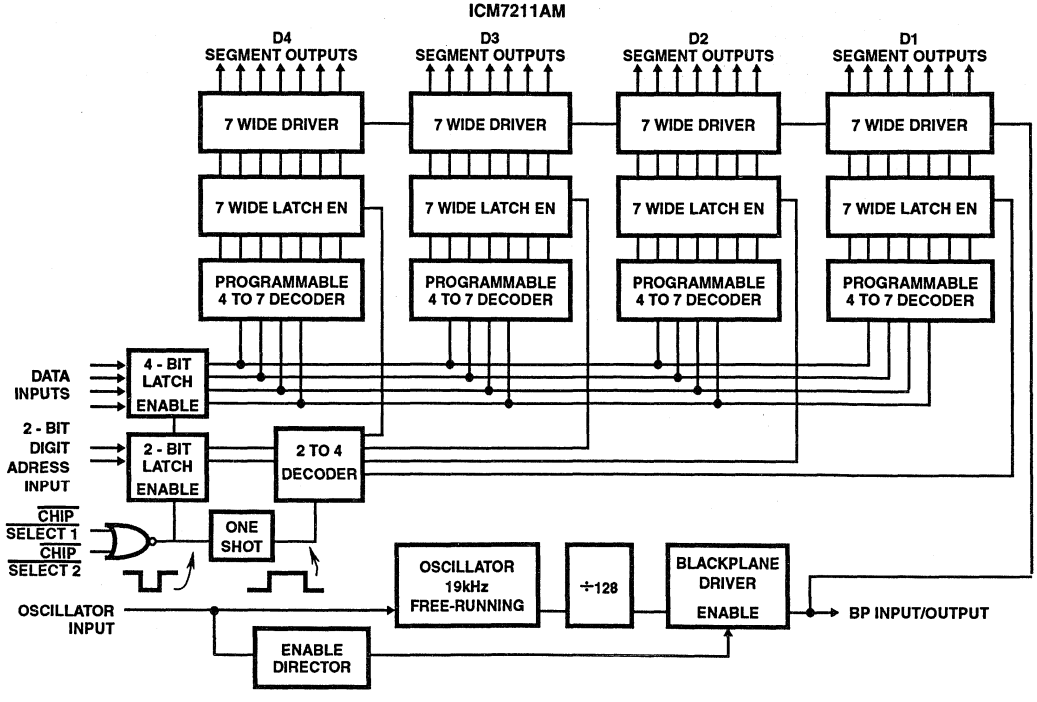


Functional Block Diagrams

ICM7211A

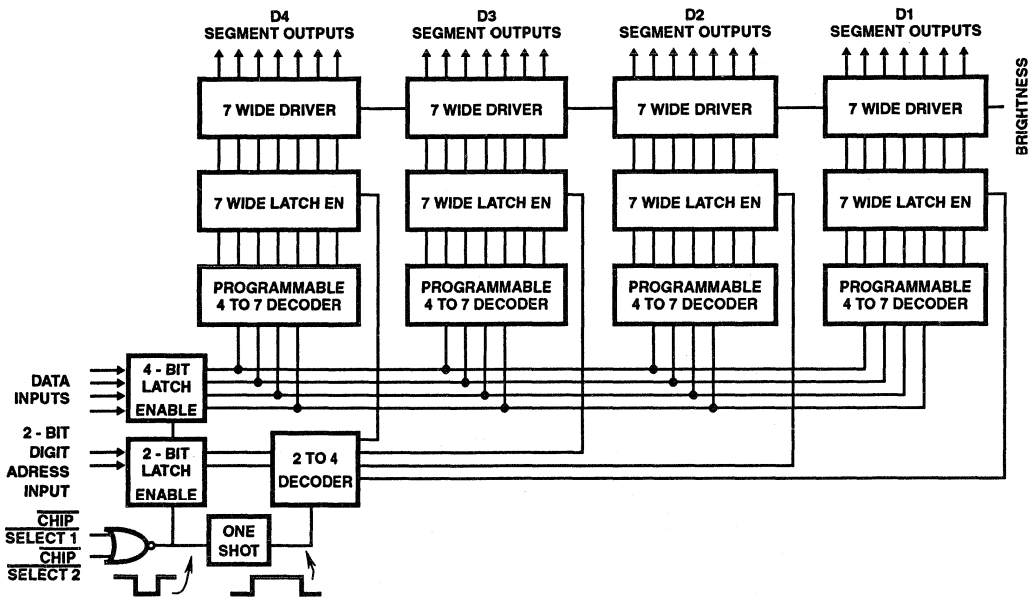


ICM7211AM



Functional Block Diagrams (Continued)

ICM7212AM



Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) 6.5V
Input Voltage (Any Terminal) (Note 1) ....V_{SS} - 0.3V to V_{DD} + 0.3V
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (Soldering, 10s) ..... +300°C
Junction Temperature ..... +150°C

Thermal Information

Thermal Resistance	θ_{JA}
Plastic DIP Package	50°C/W
Plastic MQFP Package	80°C/W
Operating Temperature Range	-40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ICM7211 CHARACTERISTICS (LCD) V_{DD} = 5V 10%, T_A = +25°C, V_{SS} = 0V Unless Otherwise Specified.					
Operating Supply Voltage Range (V_{DD} - V_{SS}), V_{SUPPLY}		3	5	6	V
Operating Current, I_{DD}	Test circuit, Display blank	-	10	50	µA
Oscillator Input Current, I_{OSCI}	Pin 36	-	±2	±10	µA
Segment Rise/Fall Time, t_R, t_F	C_L = 200pF	-	0.5	-	µs
Backplane Rise/Fall Time, t_R, t_F	C_L = 5000pF	-	1.5	-	µs
Oscillator Frequency, f_{OSC}	Pin 36 Floating	-	19	-	kHz
Backplane Frequency, f_{BP}	Pin 36 Floating	-	150	-	Hz
ICM7212 CHARACTERISTICS (Common Anode LED)					
Operating Supply Voltage Range (V_{DD} - V_{SS}), V_{SUPPLY}		4	5	6	V
Operating Current Display Off, I_{STBY}	Pin 5 (Brightness), Pins 27-34 V_{SS}	-	10	50	µA
Operating Current, I_{DD}	Pin 5 at V_{DD}, Display all 8's	-	200	-	mA
Segment Leakage Current, I_{SLK}	Segment Off	-	±0.01	±1	µA
Segment On Current, I_{SEG}	Segment On, V_O = +3V	5	8	-	mA
INPUT CHARACTERISTICS (ICM7211 and ICM7212)					
Logical "1" Input Voltage, V_{IH}		4	-	-	V
Logical "0" Input Voltage, V_{IL}		-	-	1	V
Input Leakage Current, I_{ILK}	Pins 27-34	-	±0.01	±1	µA
Input Capacitance, C_{IN}	Pins 27-34	-	5		pF
BP/Brightness Input Leakage, I_{BPLK}	Measured at Pin 5 with Pin 36 at V_{SS}	-	±0.01	±1	µA
BP/Brightness Input Capacitance, C_{BPI}	All Devices	-	200	-	pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION					
Digit Select Active Pulse Width, t_{WH}	Refer to Timing Diagrams	1	-	-	µs
Data Setup Time, t_{DS}		500	-	-	ns
Data Hold Time, t_{DH}		200	-	-	ns
Inter-Digit Select Time, t_{IDS}		2	-	-	µs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE					
Chip Select Active Pulse Width, t_{WL}	Other Chip Select either held active, or both driven together	200	-	-	ns
Data Setup Time, t_{DS}		100	-	-	ns
Data Hold Time, t_{DH}		10	0	-	ns
Inter-Chip Select Time, t_{ICS}		2	-	-	µs

NOTES:

1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211 and ICM7212 be turned on first.

Input Definitions In this table, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified under Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITIONS	FUNCTION	
B0	27	V_{DD} = Logical One V_{SS} = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V_{DD} = Logical One V_{SS} = Logical Zero	Twos	
B2	29	V_{DD} = Logical One V_{SS} = Logical Zero	Fours	
B3	30	V_{DD} = Logical One V_{SS} = Logical Zero	Eights (Most Significant)	
OSC (LCD Devices Only)	36	Floating or with external capacitor to V_{DD}	Oscillator Input	
		V_{SS}	Disables BP output devices, allowing segments to be synchronized to an external signal input at the BP terminal (Pin 5)	

ICM7211 Multiplexed-Binary Input Configuration

INPUT	TERMINAL	CONDITIONS	FUNCTION
D1	31	V_{DD} = Inactive V_{SS} = Active	D1 Digit Select (Least Significant)
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 Digit Select (Most Significant)

ICM7211M/ICM7212M Microprocessor Interface Input Configuration

INPUT	DESCRIPTION	TERMINAL	CONDITIONS	FUNCTION
DA1	Digit Address Bit 1 (LSB)	31	V_{DD} = Logical One V_{SS} = Logical Zero	DA1 & DA2 serve as a two bit Digit Address Input DA2, DA1 = 00 selects D4 DA2, DA1 = 01 selects D3 DA2, DA1 = 10 selects D2 DA2, DA1 = 11 selects D1
DA2	Digit Address Bit 2 (MSB)	32	V_{DD} = Logical One V_{SS} = Logical Zero	
$\overline{CS1}$	Chip Select 1	33	V_{DD} = Inactive V_{SS} = Active	When both $\overline{CS1}$ and $\overline{CS2}$ are taken low, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of either Chip Select, the data is decoded and written into the output latches.
$\overline{CS2}$	Chip Select 2	34	V_{DD} = Inactive V_{SS} = Active	

Timing Diagrams

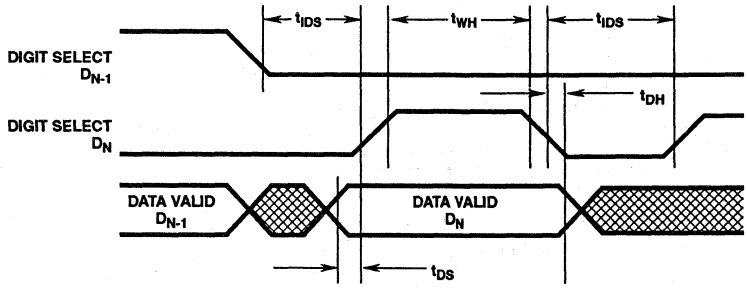


FIGURE 1. MULTIPLEXED INPUT

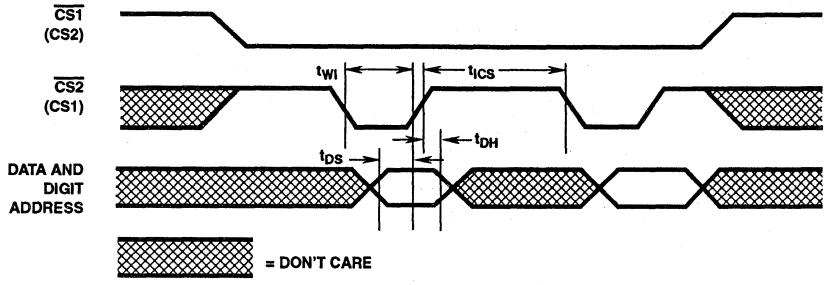


FIGURE 2. MICROPROCESSOR INTERFACE INPUT

Typical Performance Curves

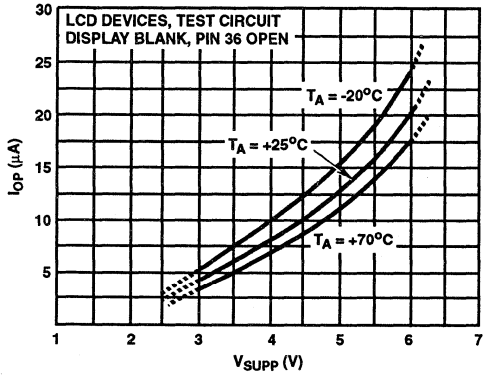


FIGURE 3. ICM7211 OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

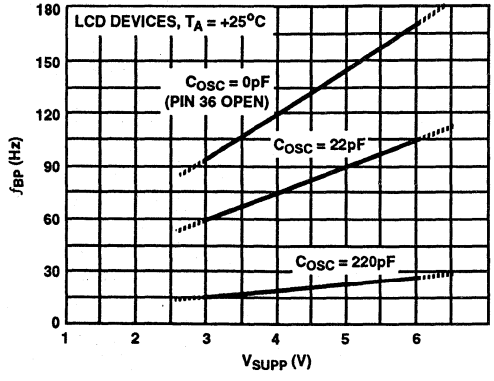


FIGURE 4. ICM7211 BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

Typical Performance Curves (Continued)

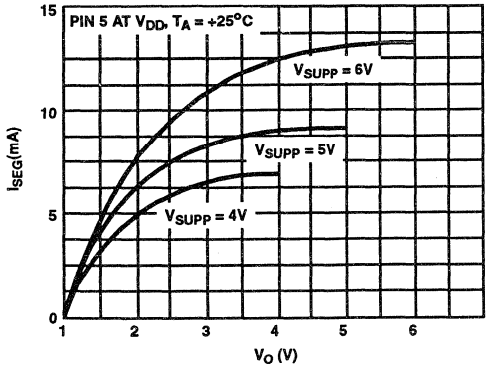


FIGURE 5. ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

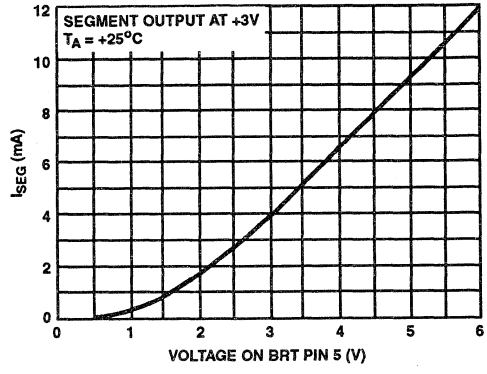


FIGURE 6. ICM7212 LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE

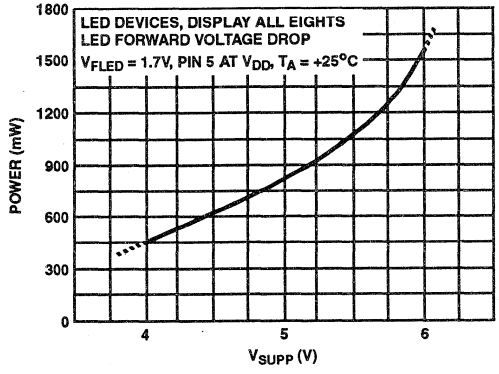


FIGURE 7. ICM7212 OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE

Description Of Operation

LCD Devices

The LCD devices in the family (ICM7211, ICM7211A, ICM7211M, ICM7211AM) provide outputs suitable for driving conventional four-digit, seven-segment LCD displays. These devices include 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n-channel and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any DC component, which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the OSCillator input (pin 36) to V_{SS}. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device, or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device represents a load of approximately 200pF (comparable to one additional segment). Thus the limitation of the number of devices that can be slaved to one master device backplane driver is the additional load represented by the

larger backplane of displays of more than four digits. A good rule of thumb to observe in order to minimize power consumption is to keep the backplane rise and fall times less than about 5µs. The backplane output driver should handle the backplane to a display of 16 one-half inch characters. It is recommended, if more than four devices are to be slaved together, the backplane signal be derived externally and all the ICM7211 devices be slaved to it. This external signal should be capable of driving very large capacitive loads with short (1 - 2µs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz although this may be too fast for optimum display response at lower display temperatures, depending on the display type.

The onboard oscillator is designed to free run at approximately 19kHz at microampere current levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running; the oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal and V_{DD}.

The oscillator may also be overdriven if desired, although care must be taken to ensure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a D.C. component to the display). This can be done by driving the OSCillator input between the positive supply and a level out of the range where the backplane disable is sensed (about one fifth of the supply voltage above V_{SS}). Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

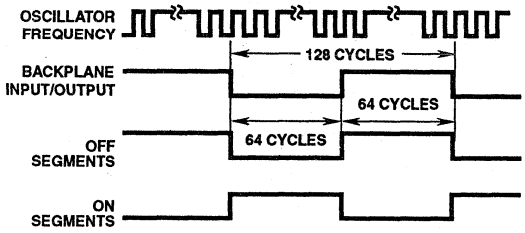


FIGURE 8. DISPLAY WAVEFORMS

LED Devices

The LED device in the family (ICM7212AM) provides outputs suitable for directly driving four-digit, seven-segment common-anode LED displays. These devices include 28 individual segment drivers, each consisting of a low-leakage, current-controlled, open-drain, n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the BRtrighTness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Figure 9. The potentiometer should be a high value (100kΩ to 1MΩ) to minimize power consumption, which can be significant when the display is off.

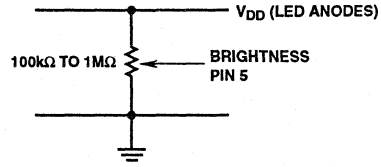


FIGURE 9. BRIGHTNESS CONTROL

The BRighTness input may also be operated digitally as a display enable; when high, the display is fully on, and low fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two voltages at the BRighTness input.

Note that the LED device has two connections for V_{SS}; both of these pins should be connected. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1W at +25°C, derated linearly above +35°C to 500mW at +70°C (-15mW/°C above +35°C). Power dissipation for the device is given by:

$$P = (V_{SUPP} - V_{FLED})(I_{SEG})(n_{SEG})$$

where V_{FLED} is the LED forward voltage drop, I_{SEG} is segment current, and n_{SEG} is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the BRighTness input to keep power dissipation within the limits described above.

Input Configurations and Output Codes

The standard devices in the ICM7211 and ICM7212 family accept a four-bit true binary (i.e., positive level = logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM7211 and ICM7211M devices decode this binary input into a seven- segment alphanumeric hexadecimal output, while the ICM7211A, ICM7211AM, and ICM7212AM decode the binary input into seven-segment alphanumeric "Code B" output, i.e. 0-9, dash, E, H, L, P, blank. These codes are shown explicitly in Table 1. Either decoder option will

correctly decode true BCD to a seven-segment decimal output.

TABLE 1. OUTPUT CODES

BINARY				HEXADECIMAL ICM7211 ICM7211M	CODE B ICM7211A ICM7212AM
B3	B2	B1	BO		
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

These devices are actually mask-programmable to provide any 16 combinations of the seven segment outputs decoded from the four input bits. For large quantity orders custom decoder options can be arranged. Contact the factory for details.

The ICM7211 and ICM7211A devices are designed to accept multiplexed binary or BCD input. These devices provide four separate digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30.

The ICM7211M, ICM7211AM, and ICM7212AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the two-bit digit address (DA1 pin 31, DA2 pin 32) are written into input buffer latches when both chip select inputs ($\overline{CS1}$ pin 33, $\overline{CS2}$ pin 34) are taken low. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the digit address latches.

An address of 00 writes into D4, DA2 = 0, DA1 = 1 writes into D3, DA2 = 1, DA1 = 0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Figure 2, and the chip select pulse widths and data setup and hold times are specified under Operating Characteristics.

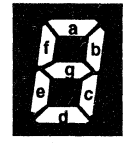


FIGURE 10. SEGMENT ASSIGNMENT

Test Circuit

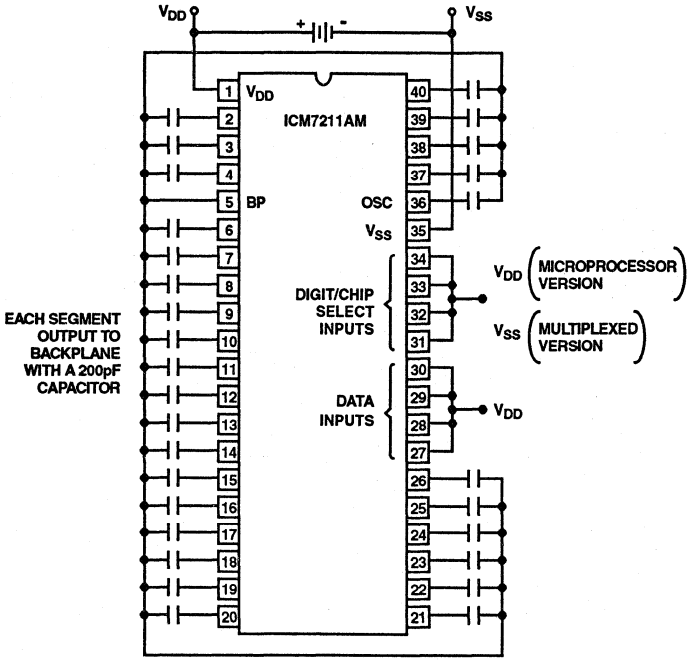


FIGURE 11.

Typical Applications

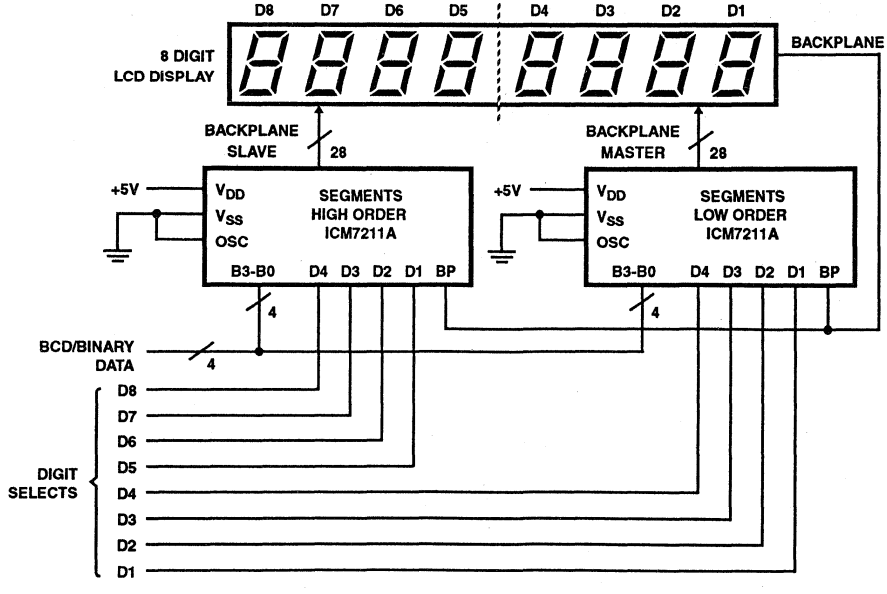


FIGURE 12. GANGED ICM7211's DRIVING 8-DIGIT LCD DISPLAY

Typical Applications (Continued)

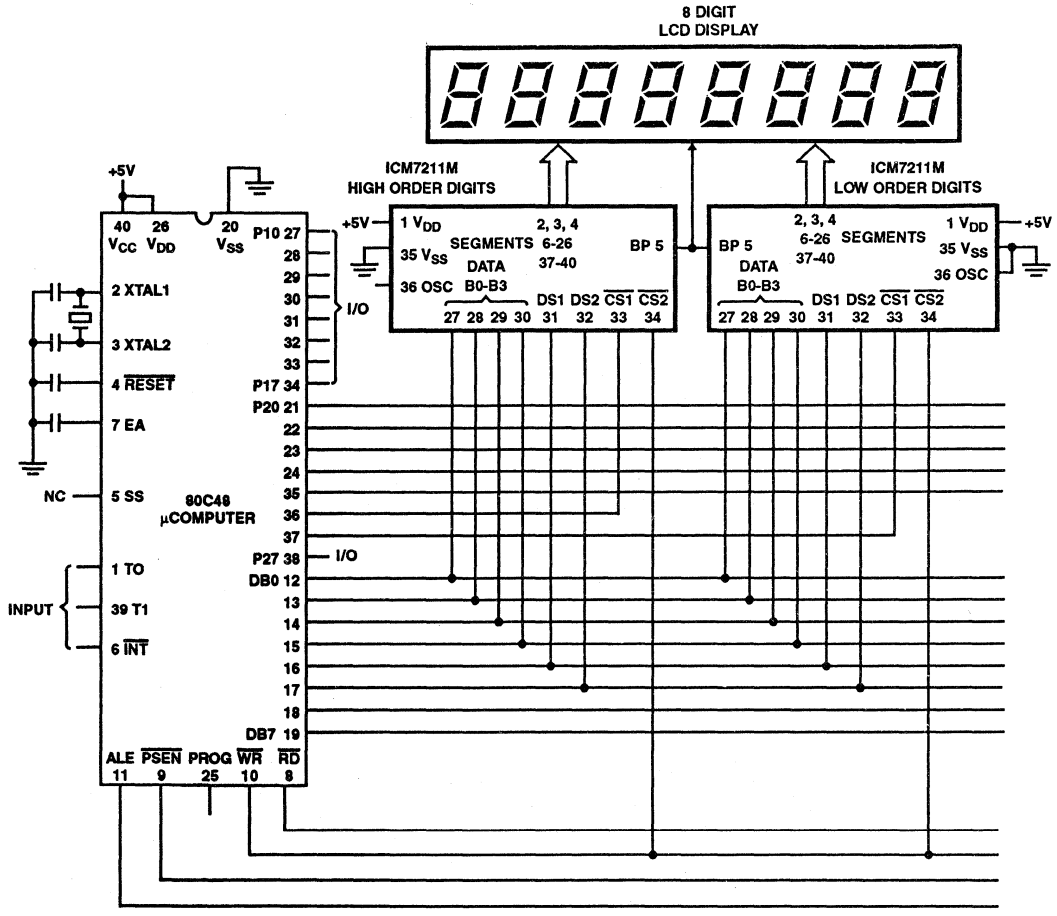


FIGURE 13. 80C48 MICROPROCESSOR INTERFACE

HARRIS SEMICONDUCTOR

ICM7228

8-Digit µP Compatible LED Display Decoder Driver

December 1993

Features

- Improved 2nd Source to Maxim ICM7218
- Fast Write Access Time of 200ns
- Multiple Microprocessor Compatible Versions
- Hexadecimal, Code B and No Decode Modes
- Individual Segment Control with "No Decode" Feature
- Digit and Segment Drivers On-Chip
- Non-Overlapping Digits Drive
- Common Anode and Common Cathode LED Versions
- Low Power CMOS Architecture
- Single 5V Supply

Applications

- Instrumentation
- Test Equipment
- Hand Held Instruments
- Bargraph Displays
- Numeric and Non-Numeric Panel Displays
- High and Low Temperature Environments where LCD Display Integrity is Compromised

Description

The Harris ICM7228 display driver interfaces microprocessors to an 8 digit, 7 segment, numeric LED display. Included on chip are two types of 7 segment decoder, multiplex scan circuitry, LED display segment drivers, LED display digit drivers and an 8-byte static memory as display RAM.

Data can be written to the ICM7228A and ICM7228B's display RAM in sequential 8 digit update or in single digit update format. Data is written to the ICM7228C and ICM7228D display RAM in parallel random access format. The ICM7228A and ICM7228C drive common anode displays. The ICM7228B and ICM7228D drive common cathode displays. All versions can display the RAM data as either Hexadecimal or Code B format. The ICM7228A and ICM7228B incorporate a No Decode mode allowing each bit of each digit's RAM word to drive individual display segments resulting in independent control of all display segments. As a result, bargraph and other irregular display segments and formats can be driven directly by this chip.

The Harris ICM7228 is an alternative to both the Maxim ICM7218 and the Harris ICM7218 display drivers. Notice that the ICM7228A/B has an additional single digit access mode. This could make the Harris ICM7218A/B software incompatible with ICM7228A/B operation.

Ordering Information

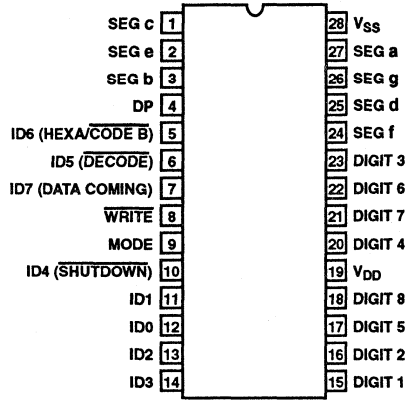
PART NUMBER	DATA ENTRY PROTOCOL	DISPLAY TYPE	TEMP. RANGE	PACKAGE
ICM7228AIPI	Sequential	Common Anode	-40°C to +85°C	28 Lead Plastic DIP
ICM7228BIPI	Sequential	Common Cathode	-40°C to +85°C	28 Lead Plastic DIP
ICM7228CIPI	Random	Common Anode	-40°C to +85°C	28 Lead Plastic DIP
ICM7228DIPI	Random	Common Cathode	-40°C to +85°C	28 Lead Plastic DIP
ICM7228AIJI	Sequential	Common Anode	-40°C to +85°C	28 Lead Ceramic DIP
ICM7228BIJI	Sequential	Common Cathode	-40°C to +85°C	28 Lead Ceramic DIP
ICM7228CIJI	Random	Common Anode	-40°C to +85°C	28 Lead Ceramic DIP
ICM7228DIJI	Random	Common Cathode	-40°C to +85°C	28 Lead Ceramic DIP
ICM7228AIBI	Sequential	Common Anode	-40°C to +85°C	28 Lead SOIC
ICM7228BIBI	Sequential	Common Cathode	-40°C to +85°C	28 Lead SOIC
ICM7228CIBI	Random	Common Anode	-40°C to +85°C	28 Lead SOIC
ICM7228DIBI	Random	Common Cathode	-40°C to +85°C	28 Lead SOIC
ICM7228AMJI	Sequential	Common Anode	-55°C to +125°C	28 Lead Ceramic DIP
ICM7228BMJI	Sequential	Common Cathode	-55°C to +125°C	28 Lead Ceramic DIP
ICM7228CMJI	Random	Common Anode	-55°C to +125°C	28 Lead Ceramic DIP
ICM7228DMJI	Random	Common Cathode	-55°C to +125°C	28 Lead Ceramic DIP
ICM7228AMJI883B	Sequential	Common Anode	-55°C to +125°C	28 Lead Ceramic DIP
ICM7228BMJI883B	Sequential	Common Cathode	-55°C to +125°C	28 Lead Ceramic DIP
ICM7228CMJI883B	Random	Common Anode	-55°C to +125°C	28 Lead Ceramic DIP
ICM7228DMJI883B	Random	Common Cathode	-55°C to +125°C	28 Lead Ceramic DIP

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

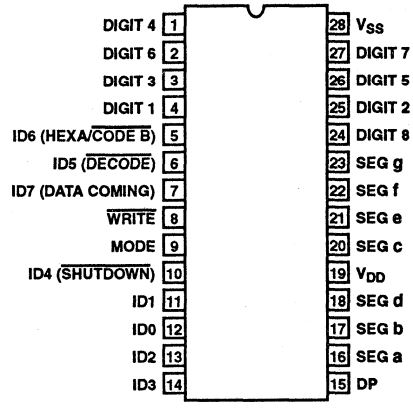
File Number 3160

Pinouts

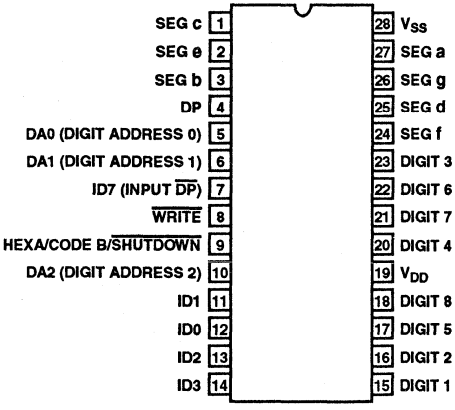
ICM7228A
(CDIP, PCIP SOIC)
COMMON ANODE
TOP VIEW



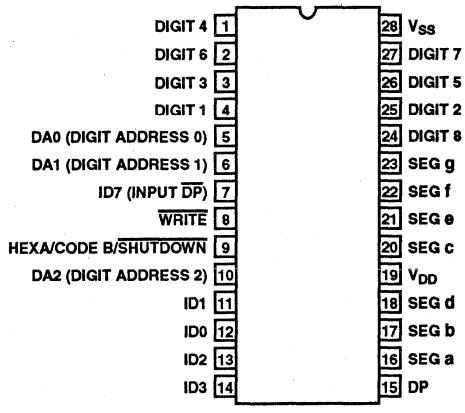
ICM7228B
(CDIP, PCIP SOIC)
COMMON CATHODE
TOP VIEW



ICM7228C
(CDIP, PCIP SOIC)
COMMON ANODE
TOP VIEW

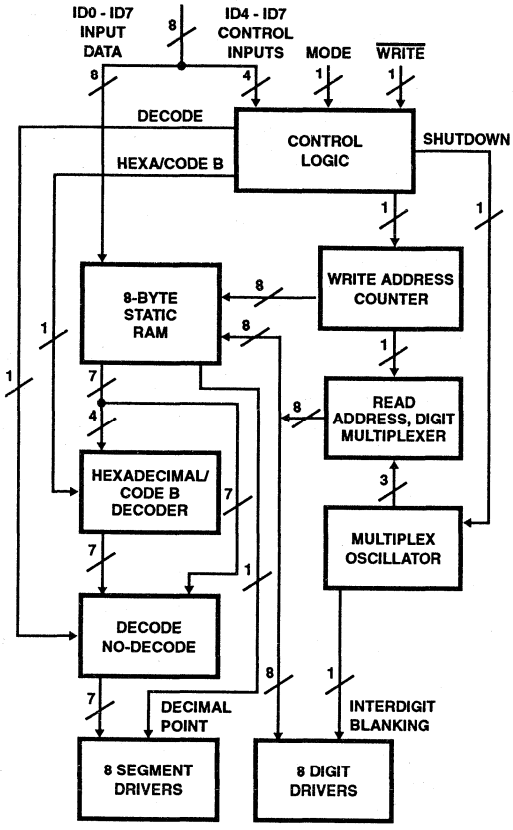


ICM7228D
(CDIP, PCIP SOIC)
COMMON CATHODE
TOP VIEW

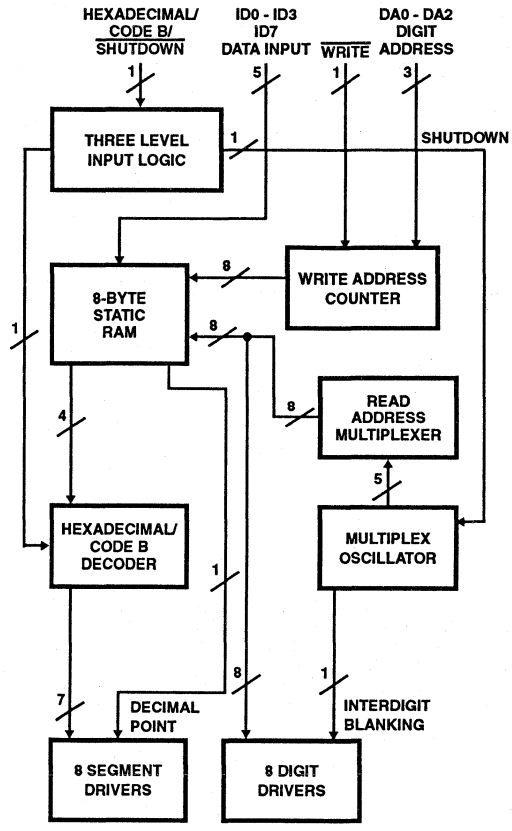


Functional Block Diagram

ICM7228A, ICM7228B



ICM7228C, ICM7228D



Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) 6V
Digit Output Current 500mA
Segment Output Current 100mA
Input Voltage (Note 1) (Any Terminal) .. (V_{SS} - 0.3V) < V_{IN} < (V_{DD} + 0.3V)
Storage Temperature Range ..... -65°C < T_S < +160°C
Lead Temperature (Soldering 10s) ..... +300°C
Junction Temperature
IPI, IJI, IBI Suffix ..... +150°C
MIJI Suffix ..... +175°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	55°C/W	20°C/W
Plastic DIP Package	60°C/W	-
SOIC Package	70°C/W	-

Operating Temperature Range
IPI, IJI, IBI Suffix ..... -40°C < T_A < +85°C
MIJI Suffix ..... -55°C < T_A < +125°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = +5.0V ± 10%, V_{SS} = 0V, Unless Otherwise Specified

INDUSTRIAL TEMPERATURE RANGE, IPI, IJI, LBI DEVICES

PARAMETER	TEST CONDITIONS	T_A = +25°C			-40°C ≤ T_A ≤ +85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Range, V_{SUPPLY}	Operating	4	-	6	4	-	6	V
	Power Down Mode	2	-	-	2	-	-	
Quiescent Supply Current, I_Q	Shutdown, ICM7228A, IMC7228B	-	1	100	-	1	100	µA
	Shutdown, 7228C, 7228D	-	2.5	100	-	2.5	100	
Operating Supply Current, I_{DD}	Common Anode, ICM7228A/C Segments = ON Outputs = OPEN	-	200	450	-	200	450	µA
	Common Anode, ICM7228A/C Segments = OFF Outputs = OPEN	-	100	450	-	100	450	
	Common Cathode, ICM7228B/D Segments = ON Outputs = OPEN	-	250	450	-	250	450	
	Common Cathode, ICM7228B/D Segments = OFF Outputs = OPEN	-	175	450	-	175	450	
Digit Drive Current, I_{DIG}	Common Anode, ICM7228A/C V_{OUT} = V_{DD} - 2.0V	200	-	-	175	-	-	mA
	Common Cathode, ICM7228B/D V_{OUT} = V_{SS} + 1.0V	50	-	-	40	-	-	
Digit Leakage Current, I_{DLK}	Shutdown Mode, V_{OUT} = 2.0V Common Anode, ICM7228A/C	-	1	100	-	1	100	µA
	Shutdown Mode, V_{OUT} = 5.0V Common Cathode, 7228B/D	-	1	100	-	1	100	
Peak Segment Drive Current, I_{SEG}	Common Anode, ICM7228A/C V_{OUT} = V_{SS} + 1.0V	20	25	-	20	-	-	mA
	Common Cathode, 7228B/D V_{OUT} = V_{DD} - 2.0V	10	12	-	10	-	-	
Segment Leakage Current, I_{SLK}	Shutdown Mode, V_{OUT} = V_{DD} Common Anode, ICM7228A/C	-	1	50	-	1	50	µA
	Shutdown Mode, V_{OUT} = V_{SS} Common Cathode, ICM7228B/D	-	1	50	-	1	50	
Input Leakage Current, I_{IL}	All Inputs except Pin 9 ICM7228C, ICM7228D V_{IN} = V_{SS}	-	-	1	-	-	1	µA
	All Inputs except Pin 9 ICM7228C, ICM7228D V_{IN} = 5.0V	-	-	-1	-	-	-1	
Display Scan Rate, f_{MUX}	Per Digit	-	390	-	-	390	-	Hz
Inter-Digit Blanking Time, t_{IDB}		2	10	-	2	-	-	µs

Electrical Specifications V_{DD} = +5.0V ± 10%, V_{SS} = 0V, Unless Otherwise Specified

INDUSTRIAL TEMPERATURE RANGE, IPI, IJI, LBI DEVICES (Continued)

PARAMETER	TEST CONDITIONS	T_A = +25°C			-40°C ≤ T_A ≤ +85°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Logical "1" Input Voltage, V_{INH}	Three Level Input: Pin 9 ICM7228C, ICM7228D Hexadecimal V_{DD} = 5V	4.2	-	-	4.2	-	-	V
Floating Input, V_{INF}	Three Level Input: Pin 9 ICM7228C, ICM7228D Code B V_{DD} = 5V	2.0	-	3.0	2.0	-	3.0	V
Logical "0" Input Voltage, V_{INL}	Three Level Input: Pin 9 ICM7228C, ICM7228D Shutdown V_{DD} = 5V	-	-	0.8	-	-	0.8	V
Three Level Input Impedance, Z_{IN}	V_{CC} = 5V Pin 9 of ICM7228C and ICM7228D	50	-	-	50	-	-	kΩ
Logical "1" Input Voltage, V_{IH}	All Inputs except Pin 9 of ICM7228C, ICM7228D V_{DD} = 5V	2.0	-	-	2.0	-	-	V
Logical "0" Input Voltage, V_{IL}	All Inputs except Pin 9 of ICM7228C, ICM7228D V_{DD} = 5V	-	-	0.8	-	-	0.8	V
SWITCHING SPECIFICATIONS V_{DD} = +5.0V ± 10%, V_{SS} = 0V, V_{IL} = +0.4V, V_{IH} = +2.4V								
Write Pulsewidth (Low), t_{WL}		200	100	-	250	-	-	ns
Write Pulsewidth (High), t_{WH}		850	540	-	1200	-	-	ns
Mode Hold Time, t_{MH}	ICM7228A, ICM7228B	0	-65	-	0	-	-	ns
Mode Setup Time, t_{MS}	ICM7228A, ICM7228B	250	150	-	250	-	-	ns
Data Setup Time, t_{DS}		250	160	-	250	-	-	ns
Data Hold Time, t_{DH}		0	-60	-	0	-	-	ns
Digit Address Setup Time, t_{AS}	ICM7228C, ICM7228D	250	110	-	250	-	-	ns
Digit Address Hold Time, t_{AH}	ICM7228C, ICM7228D	0	-60	-	0	-	-	ns

Electrical Specifications V_{DD} = +5.0V ± 10%, V_{SS} = 0V, Unless Otherwise Specified

MILITARY TEMPERATURE RANGE, MIJI, DEVICES

PARAMETER	TEST CONDITIONS	T_A = +25°C			-55°C ≤ T_A ≤ +125°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage Range, V_{SUPPLY}	Operating	4	-	6	4	-	6	V
	Power Down Mode	2	-	-	2	-	-	V
Quiescent Supply Current, I_Q	Shutdown, ICM7228A, IMC7228B	-	1	100	-	1	100	µA
	Shutdown, 7228C, 7228D	-	2.5	100	-	2.5	100	µA
Operating Supply Current, I_{DD}	Common Anode, ICM7228A/C Segments = ON Outputs = OPEN	-	200	450	-	200	550	µA
	Common Anode, ICM7228A/C Segments = OFF Outputs = OPEN	-	100	450	-	100	450	µA
	Common Cathode, ICM7228B/D Segments = ON Outputs = OPEN	-	250	450	-	250	550	µA
	Common Cathode, ICM7228B/D Segments = OFF Outputs = OPEN	-	175	450	-	175	450	µA
Digit Drive Current, I_{DIG}	Common Anode, V_{DD} = 5V V_{OUT} = V_{DD} - 2.0V	200	-	-	170	-	-	mA
	Common Cathode, V_{DD} = 5V V_{OUT} = V_{SS} + 1.0V	50	-	-	35	-	-	mA

Electrical Specifications V_{DD} = +5.0V ± 10%, V_{SS} = 0V, Unless Otherwise Specified

MILITARY TEMPERATURE RANGE, MIJI, DEVICES (Continued)

PARAMETER	TEST CONDITIONS	T_A = +25°C			-55°C ≤ T_A ≤ +125°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Digit Leakage Current, I_{DLK}	Shutdown Mode, V_{OUT} = 2.0V Common Anode, ICM7228A/C	-	1	100	-	1	100	µA
	Shutdown Mode, V_{OUT} = 5.0V Common Cathode, 7228B/D	-	1	100	-	1	100	µA
Peak Segment Drive Current, I_{SEG}	Common Anode, ICM7228A/C $V_{OUT} = V_{SS}$ + 1.0V, V_{DD} = 5V	20	25	-	20	25	-	mA
	Common Cathode, 7228B/D $V_{OUT} = V_{DD}$ - 2.0V, V_{DD} = 5V	10	12	-	10	12	-	mA
Segment Leakage Current, I_{SLK}	Shutdown Mode, $V_{OUT} = V_{DD}$ Common Anode, ICM7228A/C	-	1	50	-	1	50	µA
	Shutdown Mode, $V_{OUT} = V_{SS}$ Common Cathode, ICM7228B/D	-	1	50	-	1	50	µA
Input Leakage Current, I_{IL}	All Inputs except Pin 9 ICM7228C, ICM7228D $V_{IN} = V_{SS}$	-	-	1	-	-	1	µA
	All Inputs except Pin 9 ICM7228C, ICM7228D V_{IN} = 5.0V	-	-	-1	-	-	-1	µA
Display Scan Rate, f_{MUX}	Per Digit	-	390	-	-	390		Hz
Inter-Digit Blanking Time, t_{IDB}		2	10	-	2	10		µs
Logical "1" Input Voltage, V_{INH}	Three Level Input: Pin 9 ICM7228C, ICM7228D Hexadecimal V_{DD} = 5V	4.2	-	-	4.2	-		V
Floating Input, V_{INF}	Three Level Input: Pin 9 ICM7228C, ICM7228D Code B V_{DD} = 5V	2.0	-	3.0	2.4	-	3.0	V
Logical "0" Input Voltage, V_{INL}	Three Level Input: Pin 9 ICM7228C, ICM7228D Shutdown V_{DD} = 5V	-	-	0.8	-	-	0.4	V
Three Level Input Impedance, Z_{IN}	V_{CC} = 5V Pin 9 of ICM7228C and ICM7228D	50	-	-	50	-	-	kΩ
Logical "1" Input Voltage, V_{IH}	All Inputs except Pin 9 of ICM7228C, ICM7228D V_{DD} = 5V	2.0	-	-	2.0	-	-	V
Logical "0" Input Voltage, V_{IL}	All Inputs except Pin 9 of ICM7228C, ICM7228D V_{DD} = 5V	-	-	0.8	-	-	0.8	V
SWITCHING SPECIFICATIONS (V_{DD} = +5.0V ± 10%, V_{SS} = 0V, V_{IL} = +0.4V, V_{IH} = +2.4V)								
Write Pulsewidth (Low), t_{WL}		200	100	-	250	115	-	ns
Write Pulsewidth (High), t_{WH}		850	540	-	1200	840	-	ns
Mode Hold Time, t_{MH}	ICM7228A, ICM7228B	0	-65	-	0	-65	-	ns
Mode Setup Time, t_{MS}	ICM7228A, ICM7228B	250	150	-	250	165	-	ns
Data Setup Time, t_{DS}		250	160	-	250	160	-	ns
Data Hold Time, t_{DH}		0	-60	-	0	-60	-	ns
Digit Address Setup Time, t_{AS}	ICM7228C, ICM7228D	250	110	-	250	100	-	ns
Digit Address Hold Time, t_{AH}	ICM7228C, ICM7228D	0	-60	-	0	-60	-	ns

NOTES:

1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater then V_{DD} or less then V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs row sources operating on a different power supply be applied to the device before its own supply is established, and when using multiple supply systems the supply to the ICM7228 should be turned on first.

Timing Diagrams

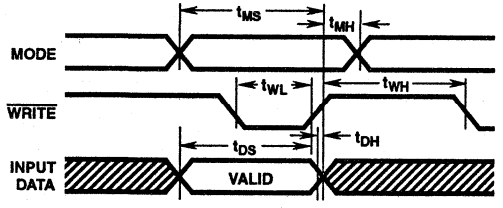


FIGURE 1. ICM7228A/B WRITE CYCLE

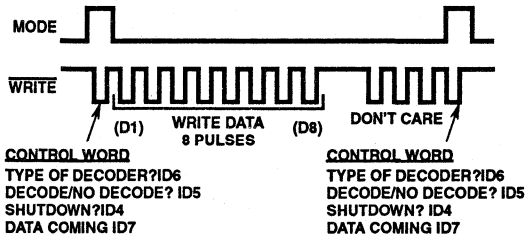


FIGURE 2. ICM7228A/B SEQUENTIAL 8 DIGIT RAM UPDATE

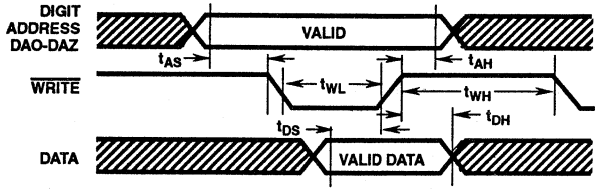


FIGURE 3. ICM7228C/D WRITE CYCLE

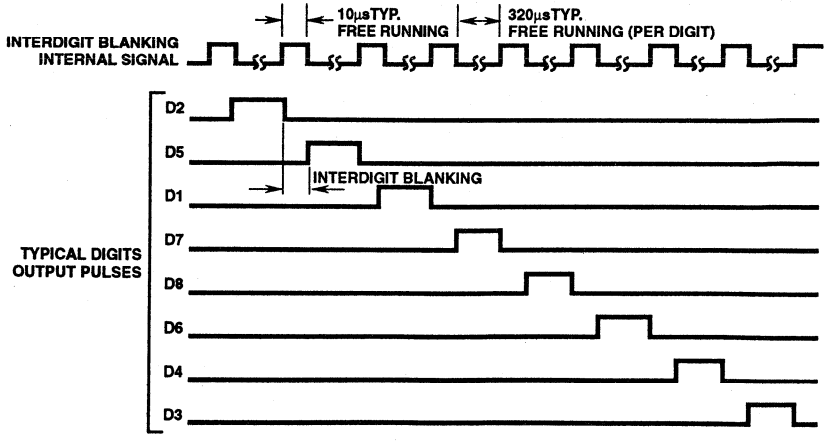


FIGURE 4. DISPLAY DIGITS MULTIPLEX (COMMON ANODE DISPLAY)

Typical Performance Curves

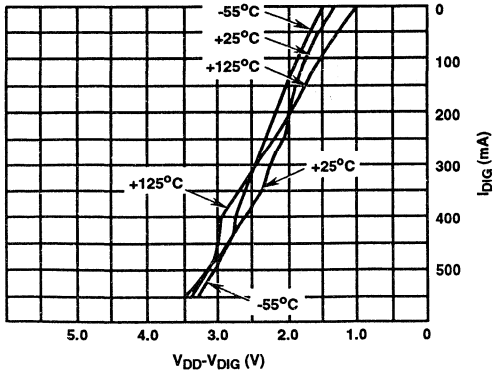


FIGURE 5. COMMON ANODE DIGIT DRIVER I_{DIG} vs (V_{DD} - V_{DIG})

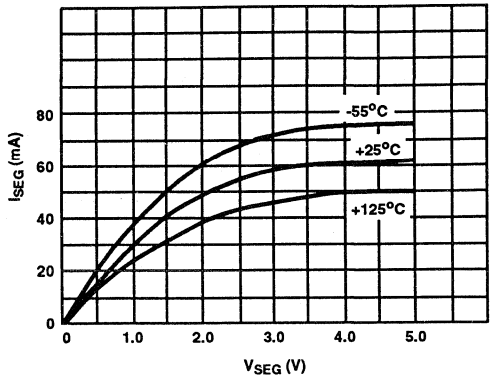


FIGURE 6. COMMON ANODE SEGMENT DRIVER I_{SEG} vs V_{SEG}

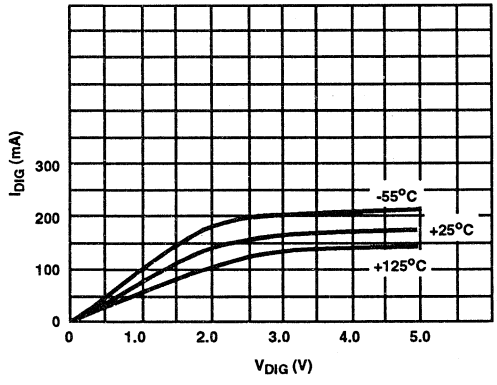


FIGURE 7. COMMON CATHODE DIGIT DRIVER I_{DIG} vs V_{DIG}

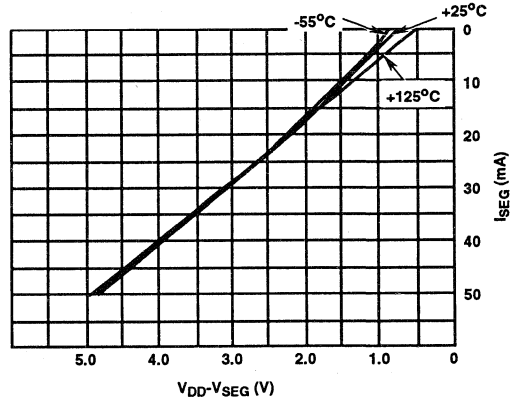


FIGURE 8. COMMON CATHODE SEGMENT DRIVER I_{SEG} vs (V_{DD} - V_{SEG})

TABLE 1. ICM7228A PIN ASSIGNMENTS AND DESCRIPTIONS

PIN NO.	NAME	FUNCTION	DESCRIPTION
1	SEG c	Output	LED Display Segments c, e, b and Decimal Point Drive Lines.
2	SEG e		
3	SEG b		
4	DP		
5	ID6, (HEXA/$\overline{\text{CODE B}}$)	Input	When "MODE" Low: Display Data Input, Bit 7. When "MODE" High: Control Bit, Decoding Scheme Selection: High, Hexadecimal Decoding; Low, Code B Decoding.
6	ID5, ($\overline{\text{DECODE}}$)	Input	When "MODE" Low: Display Data Input, Bit 6. When "MODE" High: Control Bit, Decode/No Decode Selection: High, No Decode; Low, Decode.
7	ID7, (DATA COMING)	Input	When "MODE" Low: Display Data Input, Bit 8, Decimal Point Data. When "MODE" High: Control Bit, Sequential Data Update Select: High, Data Coming; Low, No Data Coming.
8	$\overline{\text{WRITE}}$	Input	Data Input Will Be Written to Control Register or Display RAM on Rising Edge of WRITE.
9	MODE	Input	Selects Data to Be Loaded to Control Register or Display RAM: High, Loads Control Register; Low, Loads Display RAM.
10	ID4, ($\overline{\text{SHUTDOWN}}$)	Input	When "MODE" Low: Display Data Input, Bit 5. When "MODE" High: Control Bit, Low Power Mode Select: High, Normal Operation; Low, Oscillator and Display Disabled.
11	ID1	Input	When "MODE" Low: Display Data Input, Bit 2. When "MODE" High and "ID7 (DATA COMING)" Low: Digit Address, Bit 2, Single Digit Update Mode.
12	ID0	Input	When "MODE" Low: Display Data Input, Bit 1. When "MODE" High and "ID7 (DATA COMING)" Low: Digit Address, LSB, Single Digit Update Mode.
13	ID2	Input	When "MODE" Low: Display Data Input, Bit 3. When "MODE" High and "ID7 (DATA COMING)" Low: Digit Address, MSB, Single Digit Update Mode.
14	ID3	Input	When "MODE" Low: Display Data Input, Bit 4. When "MODE" High: RAM Bank Select (Decode Modes Only): High, RAM Bank A; Low, RAM Bank B
15	DIGIT 1	Output	LED Display Digits 1, 2, 5 and 8 Drive Lines.
16	DIGIT 2		
17	DIGIT 5		
18	DIGIT 8		
19	V_{DD}	Supply	Device Positive Power Supply Rail.
20	DIGIT 4	Output	LED Display Digits 4, 7, 6 and 3 Drive Lines.
21	DIGIT 7		
22	DIGIT 6		
23	DIGIT 3		
24	SEG f	Output	LED Display Segments f, d, g and a Drive Lines.
25	SEG d		
26	SEG g		
27	SEG a		
28	V_{SS}	Supply	Device Ground or Negative Power Supply Rail.

TABLE 2. ICM7228B PIN ASSIGNMENTS AND DESCRIPTIONS

PIN NO.	NAME	FUNCTION	DESCRIPTION
1	DIGIT 4	Output	LED Display Digits 4, 6, 3 and 1 Drive Lines.
2	DIGIT 6		
3	DIGIT 3		
4	DIGIT 1		
5	ID6, (HEXA/$\overline{\text{CODE B}}$)	Input	When "MODE" Low: Display Data Input, Bit 7. When "MODE" High: Control Bit, Decoding Scheme Selection: High, Hexadecimal Decoding; Low, Code B Decoding.
6	ID5, ($\overline{\text{DECODE}}$)	Input	When "MODE" Low: Display Data Input, Bit 6. When "MODE" High: Control Bit, Decode/No Decode Selection: High, No Decode; Low, Decode.
7	ID7, (DATA COMING)	Input	When "MODE" Low: Display Data Input, Bit 8, Decimal Point Data. When "MODE" High: Control Bit, Sequential Data Update Select: High, Data Coming; Low, No Data Coming.
8	$\overline{\text{WRITE}}$	Input	Data Input Will Be Written to Control Register or Display RAM on Rising Edge of WRITE.
9	MODE	Input	Selects Data to Be Loaded to Control Register or Display RAM: High, Loads Control Register; Low, Loads Display RAM.
10	ID4, ($\overline{\text{SHUTDOWN}}$)	Input	When "MODE" Low: Display Data Input, Bit 5. When "MODE" High: Control Bit, Low Power Mode Select: High, Normal Operation; Low, Oscillator and Display Disabled.
11	ID1	Input	When "MODE" Low: Display Data Input, Bit 2. When "MODE" High and "ID7 (DATA COMING)" Low: Digit Address, Bit 2, Single Digit Update Mode.
12	ID0	Input	When "MODE" Low: Display Data Input, Bit 1. When "MODE" High and "ID7 (DATA COMING)" Low: Digit Address, LSB, Single Digit Update Mode.
13	ID2	Input	When "MODE" Low: Display Data Input, Bit 3. When "MODE" High and "ID7 (DATA COMING)" Low: Digit Address, MSB, Single Digit Update Mode.
14	ID3	Input	When "MODE" Low: Display Data Input, Bit 4. When "MODE" High: RAM Bank Select (Decode Modes Only): High, RAM Bank A; Low, RAM Bank B.
15	DP	Output	LED Display Decimal Point and Segments a, b, and d Drive Lines
16	SEG a		
17	SEG b		
18	SEG d		
19	V_{DD}	Supply	Device Positive Power Supply Rail.
20	SEG c	Output	LED Display Segments c, e, f and g Drive Lines.
21	SEG e		
22	SEG f		
23	SEG g		
24	DIGIT 8	Output	LED Display Digits 8, 2, 5 and 7 Drive Lines.
25	DIGIT 2		
26	DIGIT 5		
27	DIGIT 7		
28	V_{SS}	Supply	Device Ground or Negative Power Supply Rail.

TABLE 3. ICM7228C PIN ASSIGNMENTS AND DESCRIPTIONS

PIN NO.	NAME	FUNCTION	DESCRIPTION
1	SEG c	Output	LED Display Segments c, e, band Decimal Point Drive Lines.
2	SEG e		
3	SEG b		
4	DP		
5	DA0	Input	Digit Address Input, Bit 1 LSB.
6	DA1	Input	Digit Address Input, Bit 2.
7	ID7, (INPUT $\overline{DP}$)	Input	Display Decimal Point Data Input, Negative True.
8	$\overline{WRITE}$	Input	Data Input Will Be Written to Display RAM on Rising Edge of $\overline{WRITE}$.
9	HEXA/CODE B/ SHUTDOWN	Input	Three Level Input. Display Function Control: High, Hexadecimal Decoding; Float, Code B Decoding; Low, Oscillator, and Display Disabled.
10	DA2	Input	Digit Address Input, Bit 3, MSB.
11	ID1	Input	Display Data Inputs.
12	ID0		
13	ID2		
14	ID3		
15	DIGIT 1	Output	LED Display Digits 1, 2, 5 and 8 Drive Lines.
16	DIGIT 2		
17	DIGIT 5		
18	DIGIT 8		
19	V_{DD}	Supply	Device Positive Power Supply Rail.
20	DIGIT 4	Output	LED Display Digits 4, 7, 6 and 3 Drive Lines.
21	DIGIT 7		
22	DIGIT 6		
23	DIGIT 3		
24	SEG f	Output	LED Display Segments f, d, g and a Drive Lines.
25	SEG d		
26	SEG g		
27	SEG a		
28	V_{SS}	Supply	Device Ground or Negative Power Supply Rail.

TABLE 4. ICM7228D PIN ASSIGNMENTS AND DESCRIPTIONS

PIN NO.	NAME	FUNCTION	DESCRIPTION
1	DIGIT 4	Output	LED Display Digits 4, 6, 3 and 1 Drive Lines.
2	DIGIT 6		
3	DIGIT 3		
4	DIGIT 1		
5	DA0	Input	Digit Address Input, Bit 1 LSB.
6	DA1	Input	Digit Address Input, Bit 2.
7	ID7, (INPUT $\overline{DP}$)	Input	Display Decimal Point Data Input, Negative True.
8	$\overline{WRITE}$	Input	Data Input Will Be Written to Display RAM on Rising Edge of $\overline{WRITE}$.
9	HEXA/CODE B/ SHUTDOWN	Input	Three Level Input. Display Function Control: High, Hexadecimal Decoding; Float, Code B Decoding; Low, Oscillator and Display Disabled.
10	DA2	Input	Digit Address Input, Bit 3, MSB.
11	ID1	Input	Display Data Inputs.
12	ID0		
13	ID2		
14	ID3		
15	DP	Output	LED Display Decimal Point and Segments a, b, and d Drive Lines.
16	SEG a		
17	SEG b		
18	SEG d		
19	V_{DD}	Supply	Device Positive Power Supply Rail.
20	SEG c	Output	LED Display Segments c, e, f and g Drive Lines.
21	SEG e		
22	SEG f		
23	SEG g		
24	DIGIT 8	Output	LED Display Digits 8, 2, 5 and 7 Drive Lines.
25	DIGIT 2		
26	DIGIT 5		
27	DIGIT 7		
28	V_{SS}	Supply	Device Ground or Negative Power Supply Rail.

Detailed Description

System Interfacing and Data Entry Modes, ICM7228A and ICM7228B

The ICM7228A/B devices are compatible with the architectures of most microprocessor systems. Their fast switching characteristics makes it possible to access them as a memory mapped I/O device with no wait state necessary in most microcontroller systems. All the ICM7228A/B inputs, including MODE, feature a 250ns minimum setup and 0ns hold time with a 200ns minimum $\overline{\text{WRITE}}$ pulse. Input logic levels are TTL and CMOS compatible. Figure 9 shows a generic method of driving the ICM7228A/B from a microprocessor bus. To the microprocessor, each device appears to be 2 separate I/O locations; the Control Register and the Display RAM. Selection between the two is accomplished by the MODE input driven by address line A0. Input data is placed on the ID0 - ID7 lines. The $\overline{\text{WRITE}}$ input acts as both a device select and write cycle timing pulse. See Figure 1 and Switching Specifications Table for write cycle timing parameters.

The ICM7228A/B have three data entry modes: Control Register update without RAM update, sequential 8 digit update and single digit update. In all three modes a control word is first written by pulsing the $\overline{\text{WRITE}}$ input while the MODE input is high, thereby latching data into the Control Register. The logic level of individual bits in the Control Register select Shutdown, Decode/No Decode, Hex/Code B, RAM bank A/B and Display RAM digit address as shown in Tables 1 and 2.

The ICM7228A/B Display RAM is divided into 2 banks, called bank A and B. When using the Hexadecimal or code B display modes, these RAM banks can be selected separately. This allows two separate sets of display data to be stored and displayed alternately. Notice that the RAM bank selection is not possible in No-Decode mode, this is because the display data in the No-Decode mode has 8-bits, but in Decoded schemes (Hex/Code B) is only 4-bits (ID0 - ID3 data). It should also be mentioned that the decimal point is independent of selected bank, a turned on decimal point will remain on for either bank. Selection of the RAM banks is controlled by ID3 input. The ID3 logic level (during Control Register update) selects which bank of the internal RAM to be written to and/or displayed.

Control Register Update without RAM Update

The Control Register can be updated without changing the display data by a single pulse on the $\overline{\text{WRITE}}$ input, with MODE high and DATA COMING low. If the display is being decoded (Hex/Code B), then the value of ID3 determines which RAM bank will be selected and displayed for all eight digits.

Sequential 8 Digit Update

The logic state of DATA COMING (ID7) is also latched during a Control Register update. If the latched value of DATA COMING (ID7) is high, the display becomes blanked and a sequential 8 digit update is initiated. Display data can now be written into RAM with 8 successive $\overline{\text{WRITE}}$ pulses, starting with digit 1 and ending with digit 8 (See Figure 2). After all 8 RAM locations have been written to, the display turns on again and the new data is displayed. Additional write pulses are ignored until a new Control Register update is performed. All 8 digits are displayed in the format (Hex/Code B or No Decode) specified by the control word that preceded the 8 digit update. If a decoding scheme (Hex/Code B) is to be used, the value of ID3 during the control word update determines which RAM bank will be written to.

Single Digit Update

In this mode each digit data in the display RAM can be updated individually without changing the other display data. First, with MODE input high, a control word is written to the Control Register carrying the following information; DATA COMING (ID7) low, the desired display format data on ID4 - ID6, the RAM bank selected by ID3 (if decoding is selected) and the address of the digit to be updated on data lines ID0 - ID2 (See Table 5). A second write to the ICM7228A/B, this time with MODE input low, transfers the data at the ID0 - ID7

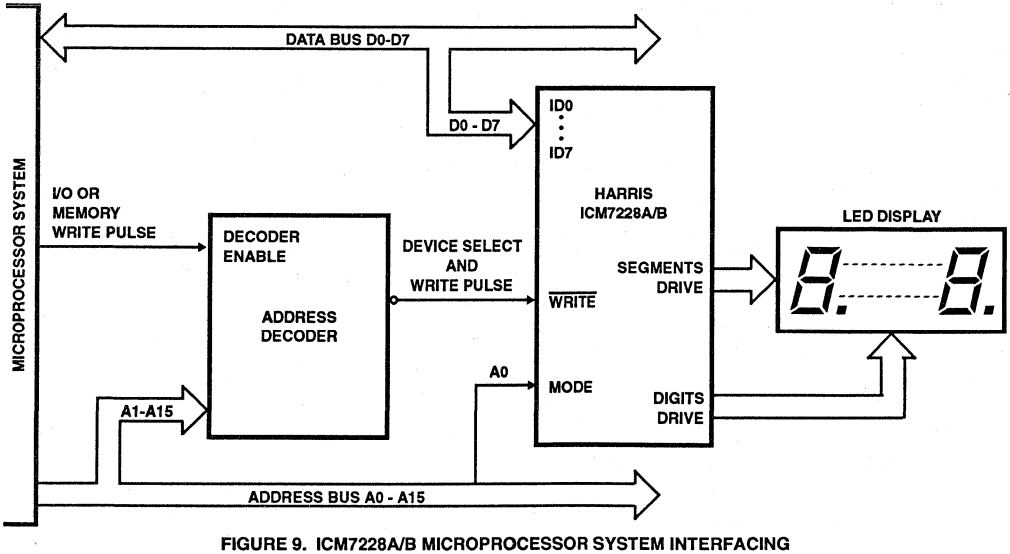


FIGURE 9. ICM7228A/B MICROPROCESSOR SYSTEM INTERFACING

inputs into the selected digit's RAM location. In single digit update mode, each individual digit's data can be specified independently for being displayed in Decoded or No-Decode mode. For those digits which decoding scheme (Hex/Code B) is selected, only one can be effective at a time. Whenever a control word is written, the specified decoding scheme will be applied to all those digits which selected to be displayed in Decoded mode.

TABLE 5. DIGITS ADDRESS, ICM7228A/B

INPUT DATA LINES			
1D2	ID2	ID0	SELECTED DIGIT
0	0	0	DIGIT1
0	0	1	DIGIT2
0	1	0	DIGIT3
0	1	1	DIGIT4
1	0	0	DIGIT5
1	0	1	DIGIT6
1	1	0	DIGIT7
1	1	1	DIGIT8

System Interfacing, ICM7228C and ICM7228D

The ICM7228C/D devices are directly compatible with the architecture of most microprocessor systems. Their fast switching characteristics make it possible to access them as a memory mapped I/O device with no wait state necessary in most microcontroller systems. All the ICM7228C/D inputs, excluding HEXA/CODE B/SHUTDOWN, feature a 250ns minimum setup and 0ns hold time with a 200ns minimum WRITE pulse. Input logic levels are TTL and CMOS compatible. Figure 10 shows a generic method of driving the ICM7228C/D from a microprocessor bus. To the microprocessor, the 8 bytes of the Display RAM appear to be 8 separate I/O locations. Loading the ICM7228C/D is quite similar to a standard memory write cycle. The address of the digit to be updated is placed on lines DA0 - DA2, the data to be written is placed on lines ID0 - ID3 and ID7, then a low pulse on WRITE input will transfer the data in. See Figure 3 and Switching Characteristics Table for write cycle timing parameters.

The ICM7228C/D devices do not have any control register, and also they do not provide the No Decode display format. Hexadecimal or Code B character selection and shutdown mode are directly controlled through the three level input at Pin 9, which is accordingly called HEXA/CODE B/SHUTDOWN. See Tables 3 and 4 for input and output definitions of the ICM7228C/D devices.

Display Formats

The ICM7228A and ICM7228B have three possible display formats; Hexadecimal, Code B and No Decode. Table 6 shows the character sets for the decode modes and their corresponding input code.

The display formats of the ICM7228A/B are selected by writing data to bits ID4, ID5 and ID6 of the Control Register (See Table 1 and 2 for input Definitions). Hexadecimal and Code B data is entered via ID0-ID3 and ID7 controls the decimal point.

TABLE 6. DISPLAY CHARACTER SETS

INPUT DATA CODE				DISPLAY CHARACTERS	
ID3	ID2	ID1	ID0	HEXADECIMAL	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5

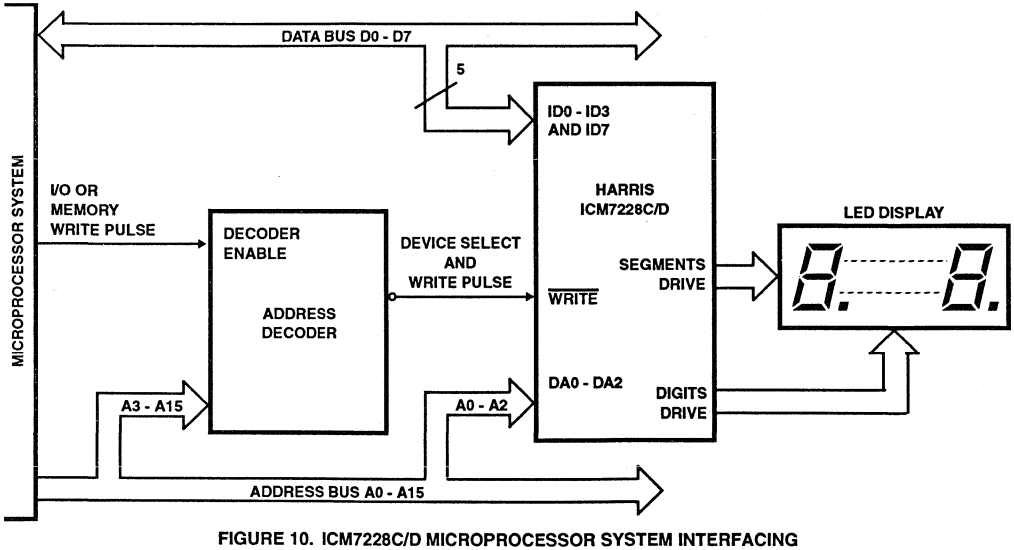


FIGURE 10. ICM7228C/D MICROPROCESSOR SYSTEM INTERFACING

TABLE 6. DISPLAY CHARACTER SETS (Continued)

INPUT DATA CODE			DISPLAY CHARACTERS		
ID3	ID2	ID1	ID0	HEXADECIMAL	CODE B
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(Blank)

FIGURE 10. DIGITS SEGMENT ASSIGNMENTS

The No Decode mode of the ICM7228A and ICM7228B allows the direct segment-by-segment control of all 64 segments driven by the device. In the No Decode mode, the input data directly control the outputs as shown in Table 7.

TABLE 7. NO DECODE SEGMENT LOCATIONS

DATA INPUT	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Controlled Segment	Decimal Point	a	b	c	e	g	f	d

An input high level turns on the respective segment, except for the decimal point, which is turned on by an input low level on ID7.

The No Decode mode can be used in different applications such as bar graph or status panel driving where each segment controls an individual LED.

The ICM7228C and ICM7228D have only the Hexadecimal and Code B character sets. The HEXA/CODE B/$\overline{\text{SHUTDOWN}}$ input, pin 9, requires a three level input. Pin 9 selects the Hexadecimal format when pulled high, the Code B format when floating or driven to mid-supply, and the shutdown mode when pulled low (See Tables 3 and 4). Table 6 also applies to the ICM7228C/D devices.

Shutdown and Display Banking

When shutdown, the ICM7228 enters a low power standby mode typically consuming only 1µA of supply current for the ICM7228A/B and 2.5µA for the ICM7228C/D. In this mode the ICM7228 turns off the multiplex scan oscillator as well as the digit and segment drivers. However, input data can still be entered when in the shutdown mode. Data is retained in memory even with the supply voltage as low as 2V.

The ICM7228A/B is shutdown by writing a control word with Shutdown (ID4) low. The ICM7228C/D is put into shutdown mode by driving pin 9, HEXA/CODE B/$\overline{\text{SHUTDOWN}}$, low.

The ICM7228 operating current with the display blanked is within 100µA - 200µA for all versions. All versions of the ICM7228 can be blanked by writing Hex FF to all digits and selecting Code B format. The ICM7228A and ICM7228B can also be blanked by selecting No Decode mode and writing Hex 80 to all digits (See Tables 6 and 7).

Common Anode Display Drivers, ICM7228A and ICM7228C

The common anode digit and segment driver output schematics are shown in Figure 12. The common anode digit driver output impedance is approximately 4Ω. This provides a nearly constant voltage to the display digits. Each digit has a minimum of 200mA drive capability. The N-channel segment driver's output impedance of 50Ω limits the segment current to approximately 25mA peak current per segment. Both the segment and digit outputs can directly drive the display, current limiting resistors are not required.

Individual segment current is not significantly affected by whether other segments are on or off. This is because the segment driver output impedance is much higher than that of the digit driver. This feature is important in bar graph applications where each bar graph element should have the same brightness, independent of the number of elements being turned on.

Common Cathode Display Drivers, ICM7228B and ICM7228D

The common cathode digit and segment driver output schematics are shown in Figure 13. The N-channel digit drivers have an output impedance of approximately 15Ω. Each digit has a minimum of 50mA drive capability. The segment drivers have an output impedance of approximately 100Ω with typically 10mA peak current drive for each segment. The common cathode display driver output currents are only $^1/_4$ of the common anode display driver currents. Therefore, the ICM7228A and ICM7228C common anode display drivers are recommended for those applications where high display brightness is desired. The ICM7228B and ICM7228D common cathode display drivers are suitable for driving bubble-lensed monolithic 7 segment displays. They can also drive individual LED displays up to 0.3 inches in height when high brightness is not required.

Display Multiplexing

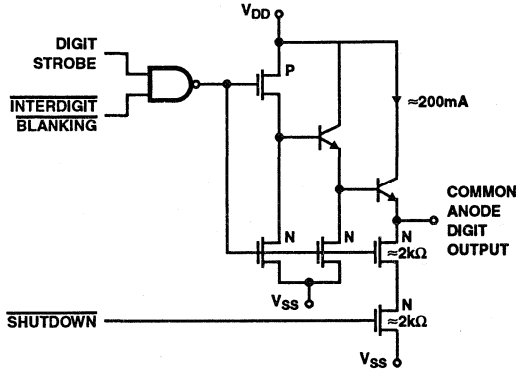
Each digit of the ICM7228 is on for approximately 320µs, with a multiplexing frequency of approximately 390Hz. The ICM7228 display drivers provide interdigit blanking. This ensures that the segment information of the previous digit is gone and the information of the next digit is stable before the next digit is driven on. This is necessary to eliminate display ghosting (a faint display of data from previous digit superimposed on the next digit). The interdigit blanking time is 10µs typical with a guaranteed 2µs minimum. The ICM7228 turns off both the digit drivers and the segment drivers during the interdigit blanking period. The digit multiplexing sequence is: D2, D5, D1, D7, D8, D6, D4 and D3. A typical digit's drive pulses are shown on Figure 4.

Due to the display multiplexing, the driving duty cycle for each digit is 12% (100 x $^1/_8$) This means the average current for each segment is $^1/_8$ of its peak current. This must be considered while designing and selecting the displays.

Driving Larger Displays

If very high display brightness is desired, the ICM7228 display driver outputs can be externally buffered. Figures 14 thru 16 show how to drive either common anode or common cathode displays using the ICM7228 and external driver circuit for higher current displays.

Another method of increasing display currents is to connect two digit outputs together and load the same data into both digits. This drives the display with the same peak current, but the average current doubles because each digit of the display is on for twice as long, i.e., $^1/_4$ duty cycle versus $^1/_8$.



NOTE: When SHUTDOWN goes low INTERDIGIT BLANKING also stays low.

FIGURE 12A. DIGIT DRIVER

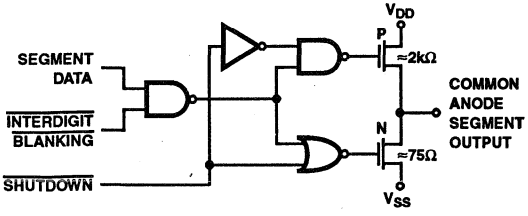
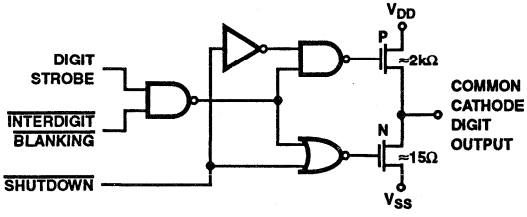
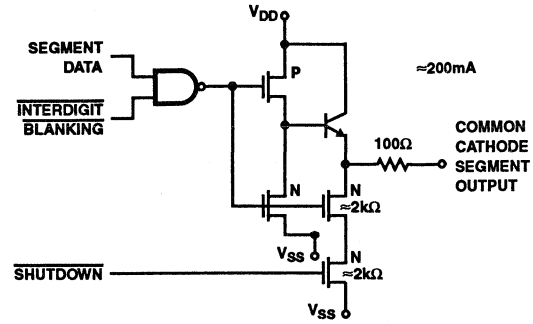


FIGURE 12B. SEGMENT DRIVER

FIGURE 12. COMMON ANODE DISPLAY DRIVERS



13A. DIGIT DRIVER



NOTE: When SHUTDOWN goes low INTERDIGIT BLANKING also stays low.

FIGURE 13B. SEGMENT DRIVER

FIGURE 13. COMMON CATHODE DISPLAY DRIVERS

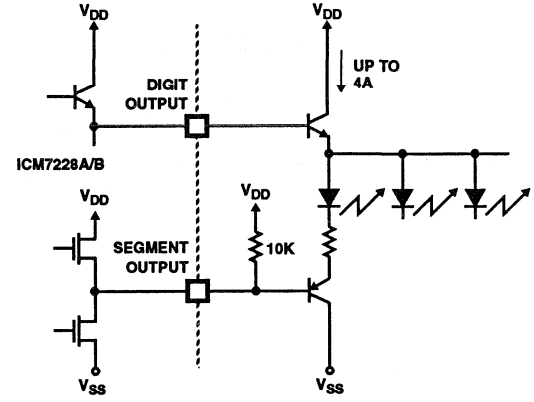


FIGURE 14. DRIVING HIGH CURRENT DISPLAY, COMMON ANODE ICM7228A/C TO COMMON ANODE DISPLAY

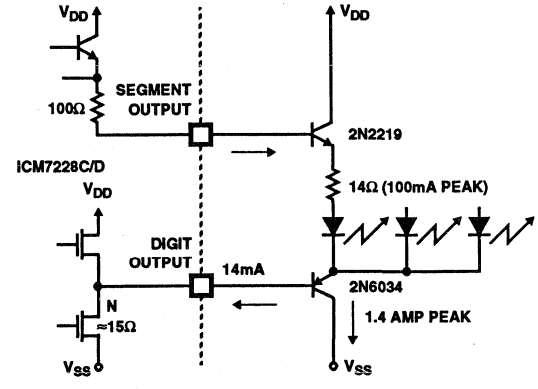


FIGURE 15. DRIVING HIGH CURRENT DISPLAY, COMMON CATHODE ICM7228B/D TO COMMON CATHODE DISPLAY

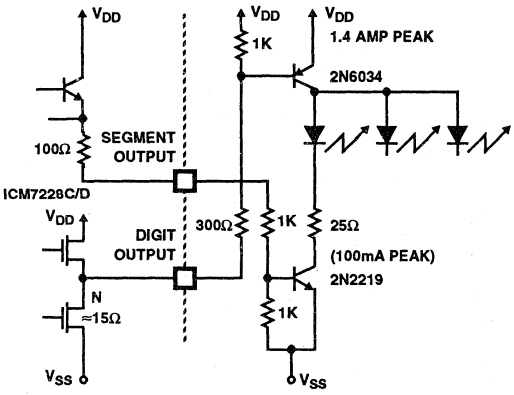


FIGURE 16. DRIVING HIGH CURRENT DISPLAY, COMMON CATHODE ICM7228B/D TO COMMON CATHODE DISPLAY

Three Level Input, ICM7228C and ICM7228D

As mentioned before, pin 9 is a three level input and controls three functions: Hexadecimal display decoding, Code B display decoding and shutdown mode. In many applications, pin 9 will be left open or permanently wired to one state. When pin 9 can not be permanently left in one state, the circuits illustrated in Figure 17 can be used to drive this three level input.

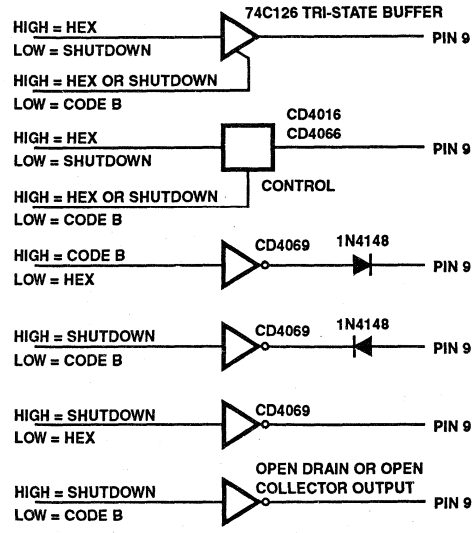


FIGURE 17. ICM7228C/D PIN 9 DRIVE CIRCUITS

Power Supply Bypassing

Connect a minimum of 47µF in parallel with 0.1µF capacitors between V_{DD} and V_{SS} of ICM7228. These capacitors should be placed in close proximity to the device to reduce the power supply ripple caused by the multiplexed LED display drive current pulses.

Test Circuits

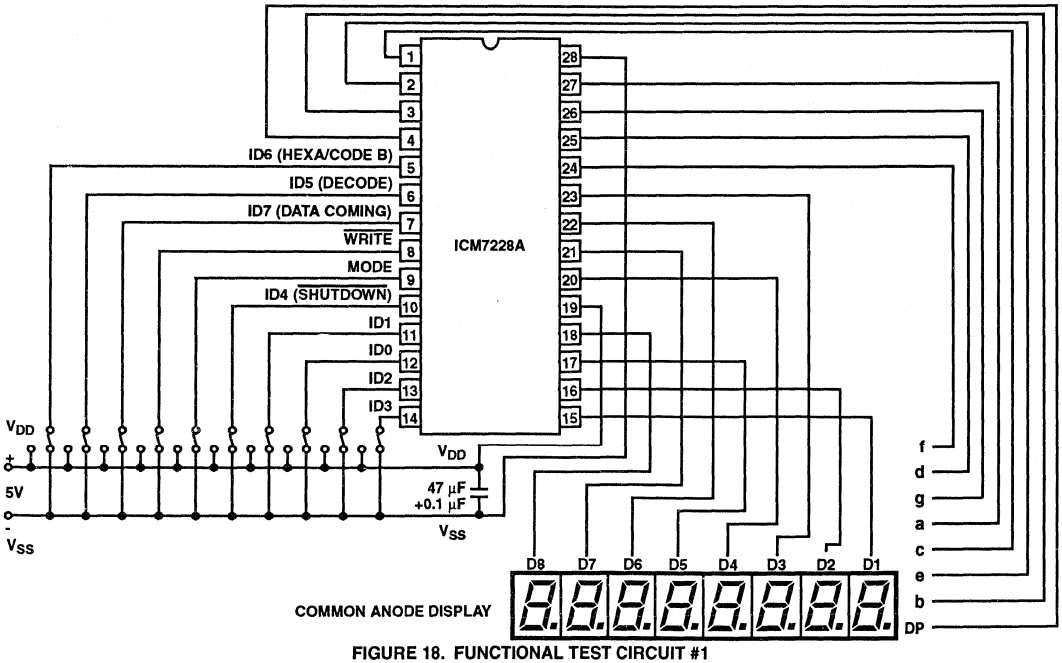


FIGURE 18. FUNCTIONAL TEST CIRCUIT #1

Test Circuits (Continued)

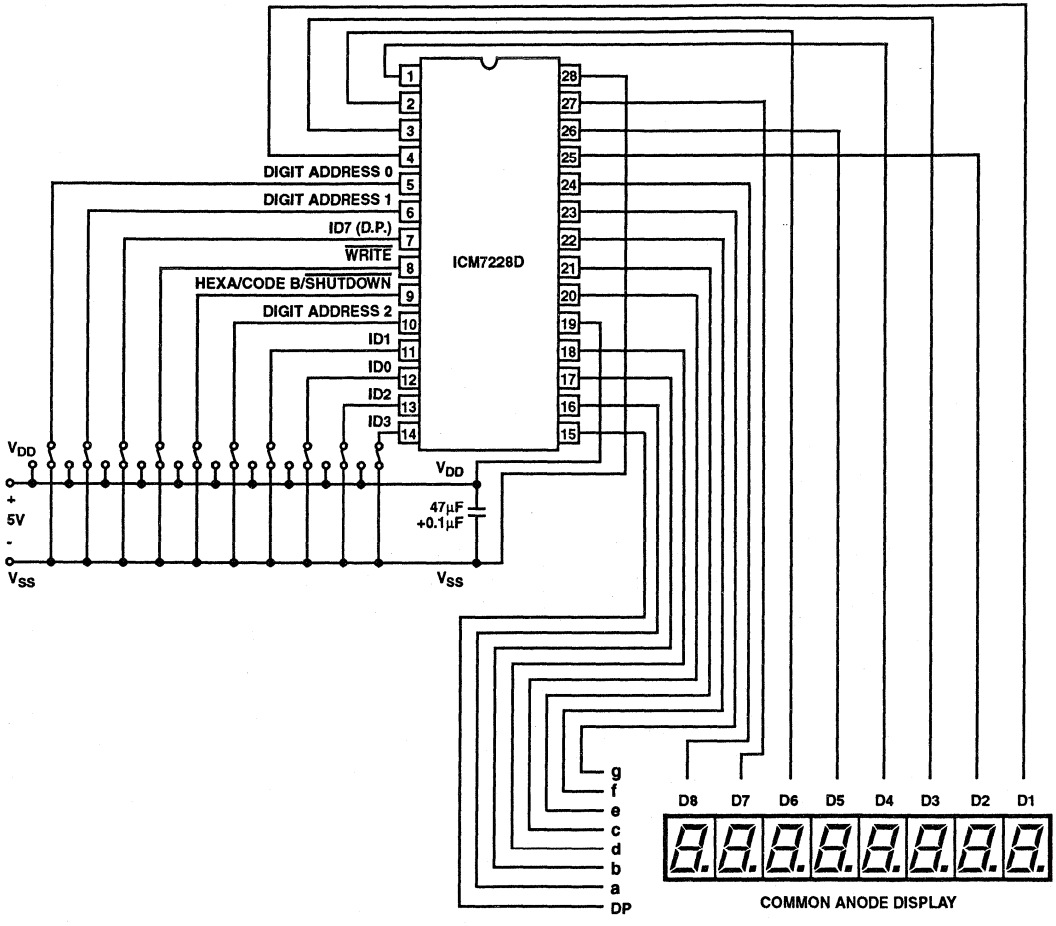


FIGURE 19. FUNCTIONAL TEST CIRCUIT #2

HARRIS SEMICONDUCTOR

ICM7231, ICM7232

Numeric/Alphanumeric Triplexed LCD Display Driver

December 1993

Features

- **ICM7231 Drives 8 Digits of 7 Segments with Two Independent Annunciators Per Digit Address and Data Input in Parallel Format**
- **ICM7232 Drives 10 Digits of 7 Segments with Two Independent Annunciators Per Digit Address and Data Input in Serial Format**
- **All Signals Required to Drive Rows and Columns of Triplexed LCD Display are Provided**
- **Display Voltage Independent of Power Supply**
- **On-Chip Oscillator Provides All Display Timing**
- **Total Power Consumption Typically 200μW, Maximum 500μW at 5V**
- **Low-Power Shutdown Mode Retains Data With 5μW Typical Power Consumption at 5V, 1μW at 2V**
- **Direct Interface to High-Speed Microprocessors**

Description

The ICM7231 and ICM7232 family of integrated circuits are designed to generate the voltage levels and switching waveforms required to drive triplexed liquid-crystal displays. These chips also include input buffer and digit address decoding circuitry allowing six bits of input data to be decoded into 64 independent combinations of the output segments of the selected digit.

The family is designed to interface to modern high performance microprocessors and microcomputers and ease system requirements for ROM space and CPU time needed to service a display.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE	NUMBER OF DIGITS	INPUT FORMAT
ICM7231 BFIJL	-25°C to +85°C	40 Lead Ceramic DIP	8 Digit	Parallel
ICM7231 BFIPL	-25°C to +85°C	40 Lead Plastic DIP	8 Digit	Parallel
ICM7232 AFIJL	-25°C to +85°C	40 Lead Ceramic DIP	10 Digit	Serial
ICM7232BFIPL	-25°C to +85°C	40 Lead Plastic DIP	10 Digit	Serial
ICM7232CRIPL	-25°C to +85°C	40 Lead Plastic DIP	10 Digit	Serial

NOTE:

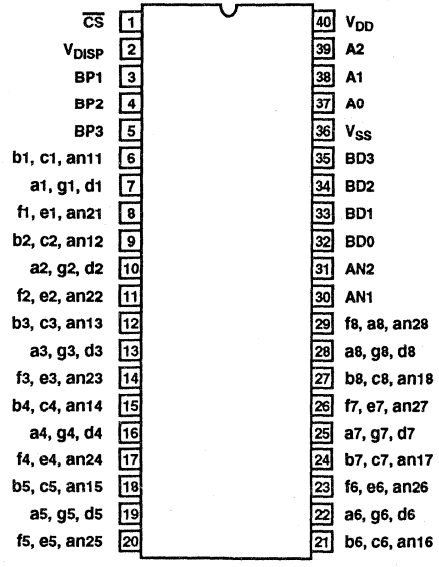
All versions intended for triplexed LCD displays.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

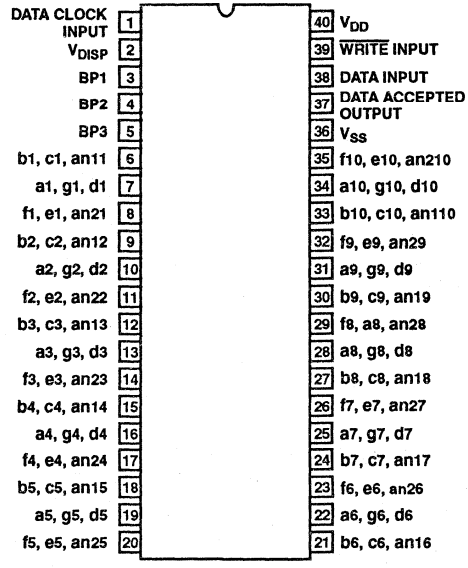
File Number **3161**

Pinouts

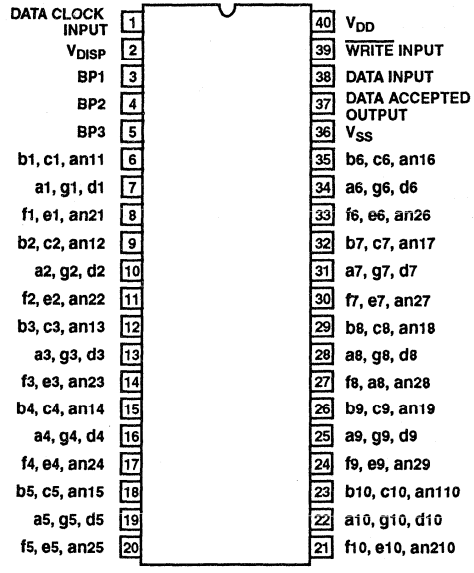
ICM7231BF
(PDIP)
TOP VIEW



ICM7232AF, BF
(PDIP)
TOP VIEW

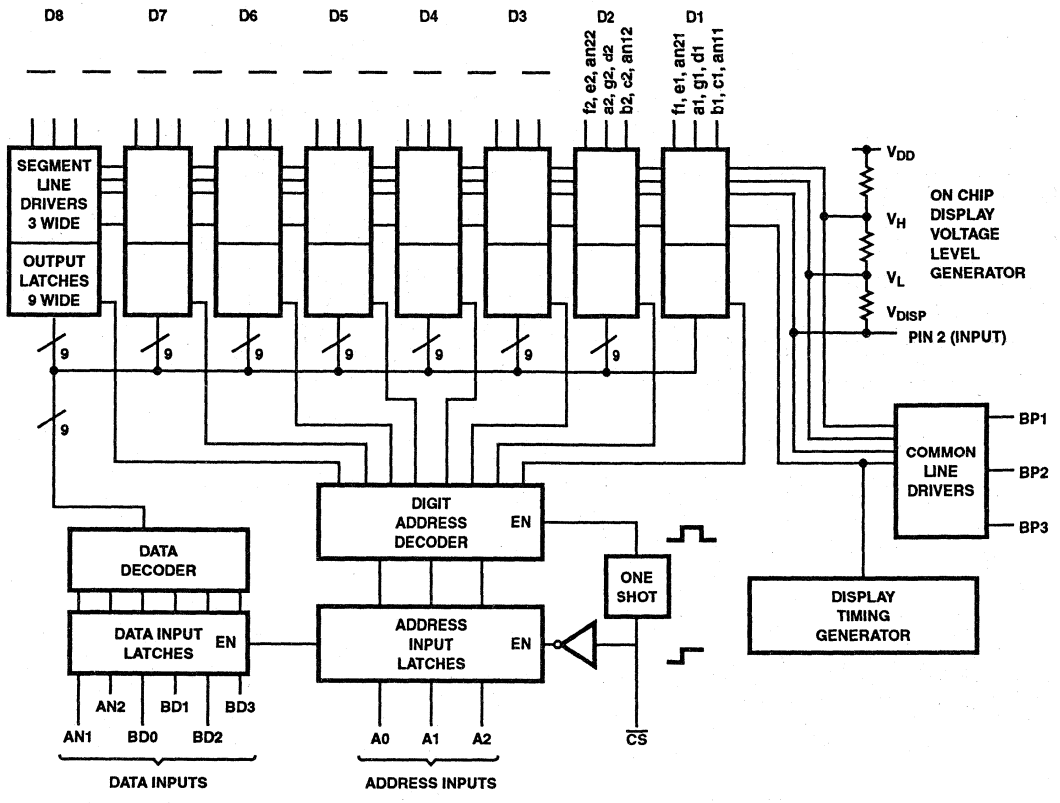


ICM7232CR
(PDIP)
TOP VIEW



Functional Block Diagrams

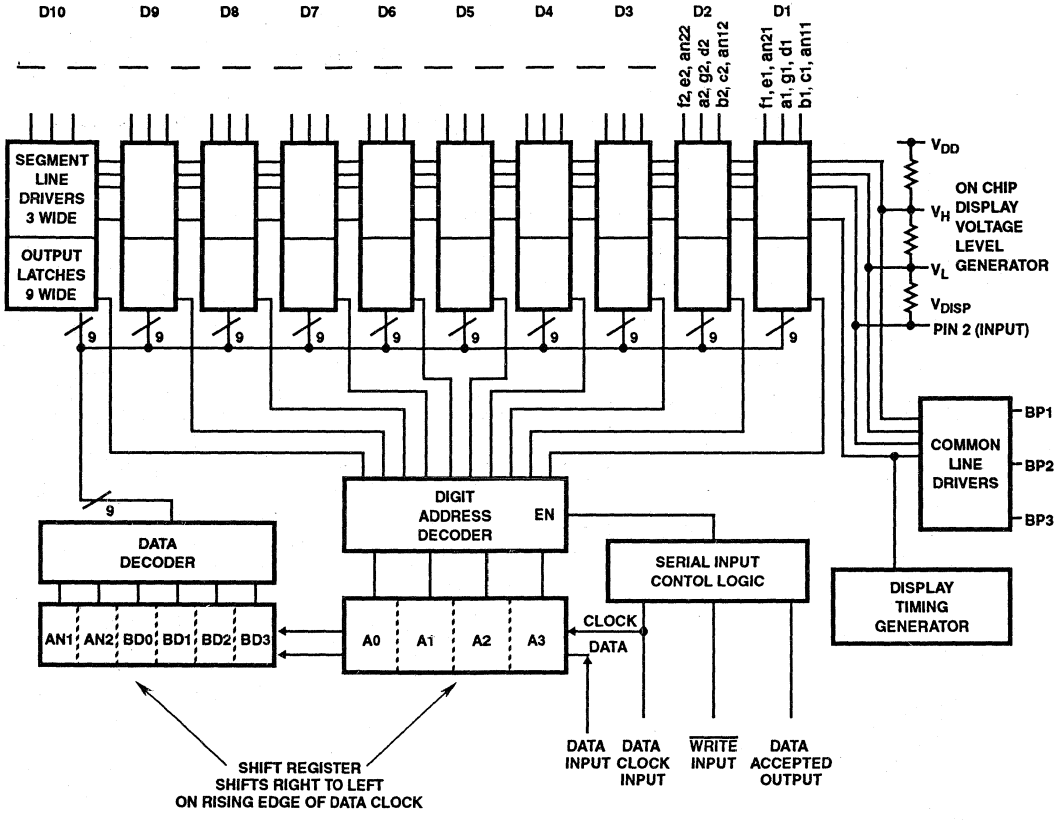
ICM7231



NOTE: See Figure 13 for display segment connections

Functional Block Diagrams (Continued)

ICM7232



NOTE: See Figures 13 and 14 for display segment connections.

Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) 6.5V
Input Voltage (Note 1) ..... V_{SS} - 0.3 ≤ V_{IN} ≤ 6.5
Display Voltage (Note 1) ..... 0.3 ≤ V_{DISP} ≤ +0.3
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP Package	50°C/W	-
Ceramic DIP Package	45°C/W	15°C/W

Operating Temperature Range ..... -25°C to +85°C
Junction Temperature
Ceramic ..... +175°C
Plastic ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V+ = 5V + 10%, V_{SS} = 0V, T_A = -25°C to +85°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage, V_{DD}		4.5	>4	5.5	V
Data Retention Supply Voltage, V_{DD}	Guaranteed Retention at 2V	2	1.6	-	V
Logic Supply Current, I_{DD}	Current from V_{DD} to Ground Excluding Display. V_{DISP} = 2V	-	30	100	µA
Shutdown Total Current, I_S	V_{DISP} Pin 2 Open	-	1	10	µA
Display Voltage Range, V_{DISP}	V_{SS} ≤ V_{DISP} ≤ V_{DD}	0		V_{DD}	V
Display Voltage Setup Current, I_{DISP}	V_{DISP} = 2V, Current from V_{DD} to V_{DISP} On-Chip	-	15	30	µA
Display Voltage Setup Resistor Value, R_{DISP}	One of Three Identical Resistors in String	40	75	-	kΩ
DC Component of Display Signals	(Sample Test Only)	-	1/4	1	% (V_{DD} - V_{DISP})
Display Frame Rate, f_{DISP}	See Figure 5	60	90	120	Hz
Input Low Level, V_{IL}	ICM7231, Pins 30 - 35, 37 - 39, 1 ICM7232, Pins 1, 38, 39 (Note 3)	-	-	0.8	V
Input High Level, V_{IH}		2.0	-	-	V
Input Leakage, I_{ILK}		-	0.1	1	µA
Input Capacitance, C_{IN}		-	5	-	pF
Output Low Level, V_{OL}	Pin 37, ICM7232, I_{OL} = 1mA,	-	-	0.4	V
Output High Level, V_{OH}	V_{DD} = 4.5V, I_{OH} = -500µA	4.1	-	-	V
Operating Temperature Range, T_{OP}	Industrial Range	-25	-	+85	°C

AC Specifications

V_{DD} = 5V + 10% V_{SS} = 0V, -25°C ≤ T_A ≤ +85°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PARALLEL INPUT (ICM7231) See Figure 1					
$\overline{\text{Chip Select}}$ Pulse Width, t_{CS}	(Note 2)	500	350	-	ns
Address/Data Setup Time, t_{DS}	(Note 2)	200	-	-	ns
Address/Data Hold Time, t_{DH}	(Note 2)	0	-20	-	ns
Inter-Chip Select Time, t_{ICS}	(Note 2)	3	-	-	µs
SERIAL INPUT (ICM7232) See Figures 2, 3					
Data Clock Low Time, $\overline{t_{CL}}$	(Note 2)	350	-	-	ns
Data Clock High Time, t_{CL}	(Note 2)	350	-	-	ns
Data Setup Time, t_{DS}	(Note 2)	200	-	-	ns
Data Hold Time, t_{DH}	(Note 2)	0	-20	-	ns
$\overline{\text{Write}}$ Pulse Width, t_{WP}	(Note 2)	500	350	-	ns
$\overline{\text{Write}}$ Pulse to Clock at Initialization, t_{WLL}	(Note 2)	1.5	-	-	µs
Data Accepted Low Output Delay, t_{ODL}	(Note 2)	-	200	400	ns
Data Accepted High Output Delay, t_{ODH}	(Note 2)	-	1.5	3	µs
Write Delay After Last Clock, t_{CWS}	(Note 2)	350	-	-	ns

Table of Features

TYPE NUMBER	OUTPUT CODE	ANNUNCIATOR LOCATIONS	INPUT	OUTPUT
ICM7231BF	Code B	Both Annunciators on BP3	Parallel Entry, 4-bit Data, 2-bit Annunciators, 3-bit Address	8 Digits plus 16 Annunciators
ICM7232AF	Hexadecimal	Both Annunciators on BP3	Serial Entry, 4-bit Data, 2-bit Annunciators, 4-bit Address	10 Digits plus 20 Annunciators
ICM7232BF	Code B			
ICM7232CR	Code B	1 Annunciator BP1 1 Annunciator BP3		

Terminal Definitions

TERMINAL	PIN NO.	DESCRIPTION	FUNCTION	
ICM7231 PARALLEL INPUT NUMERIC DISPLAY				
AN1	30	Annunciator 1 Control Bit	High = ON	
AN2	31	Annunciator 2 Control Bit	Low = OFF	See Table 3
BD0	32	Least Significant } 4-bit Binary Data Inputs	Input Data (See Table 1)	HIGH = Logical One (1) LOW = Logical Zero (0)
BD1	33			
BD2	34			
BD3	35	Most Significant		
A0	37	Least Significant } 3-bit Digit Address Inputs	Input Address (See Table 2)	
A1	38			
A2	39	Most Significant		
$\overline{CS}$	1	Data Input Strobe/Chip Select (Note 3)	Trailing (Positive going) edge latches data, causes data input to be decoded and sent out to addressed digit	
ICM7232 SERIAL DATA AND ADDRESS INPUT				
Data Input	38	Data+ Address Shift Register Input	HIGH = Logical One (1) LOW = Logical Zero (O)	
$\overline{WRITE}$ Input	39	Decode, Output, and Reset Strobe	When DATA ACCEPTED Output is LOW, positive going edge of $\overline{WRITE}$ causes data in shift register to be decoded and sent to addressed digit, then shift register and control logic to be reset. When DATA ACCEPTED Output is HIGH, positive going edge of $\overline{WRITE}$ triggers reset only.	
Data Clock Input	1	Data Shift Register and Control Logic Clock	Positive going edge advances data in shift register. ICM7232: Eleventh edge resets shift register and control logic.	
DATA ACCEPTED Output	37	Handshake Output	Output LOW when correct number of bits entered into shift register.	
ALL DEVICES				
Display Voltage V_{DISP}	2	Negative end of on-chip resistor string used to generate intermediate voltage levels for display. Shutdown Input.	Display voltage control. When open (or less than 1V from V_{DD}) chip is shutdown; oscillator stops, all display pins to V_{DD}.	
Common Line Driver Outputs	3,4,5		Drive display commons, or rows	
Segment Line Driver Outputs	6 - 29 6 - 35	(On ICM7231) (On ICM7232)	Drive display segments, or columns.	
V_{DD}	40	Chip Positive Supply		
V_{SS}	36	Chip Negative Supply		

NOTE:

1. Due to the SCR structure inherent in these devices, connecting any display terminal or the display voltage terminal to a voltage outside the power supply to the chip may cause destructive device latchup. The digital inputs should never be connected to a voltage less than -0.3V below ground, but maybe connected to voltages above V_{DD} but not more than 6.5V above V_{SS}.
2. For Design reference only, not 100% tested.
3. $\overline{CS}$ has a special "mid-level" sense circuit that establishes a test mode if it is held near 3V for several ms. Inadvertent triggering of this mode can be avoided by pulling it high when inactive, or ensuring frequent activity

Timing Diagrams

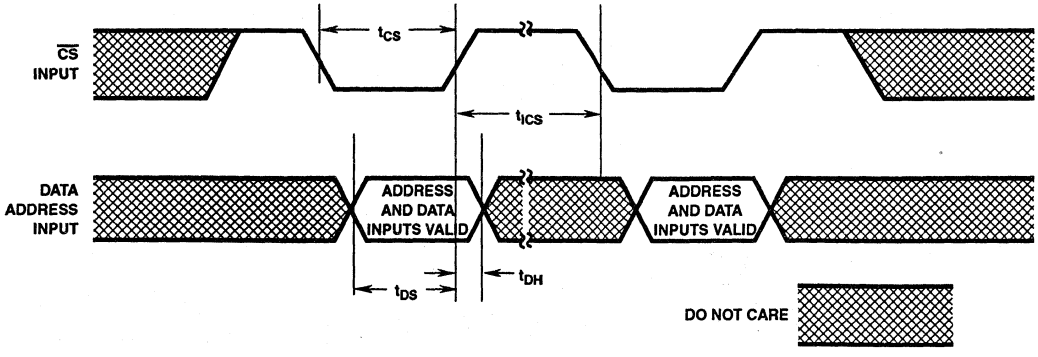


FIGURE 1. ICM7231 INPUT TIMING DIAGRAM

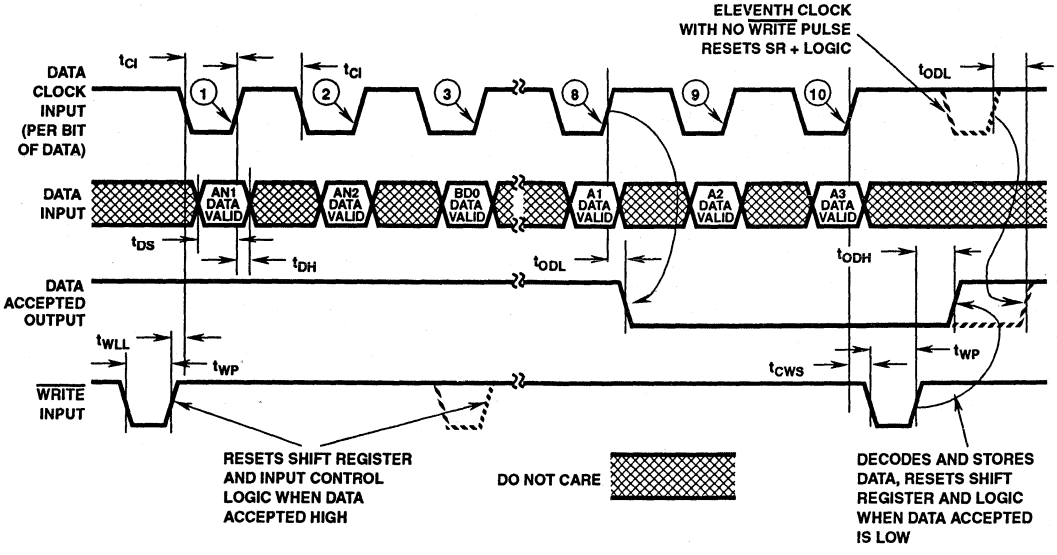


FIGURE 2. ICM7232 ONE DIGIT INPUT TIMING DIAGRAM, WRITING BOTH ANNUNCIATORS

Timing Diagrams

AN1 ENTER FIRST	AN2	BD0	BD1	BD2	BD3	A0	A1	A2	A3 ENTER LAST

ICM7232 WRITE ORDER

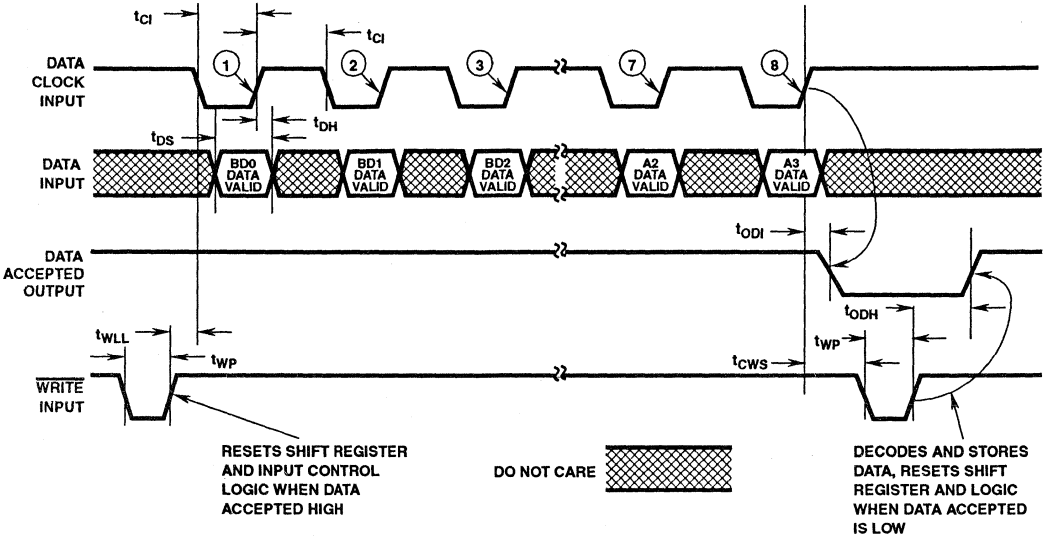


FIGURE 3. ICM7232 INPUT TIMING DIAGRAM, LEAVING BOTH ANNUNCIATORS OFF

ICM7231 Family Description

The ICM7231 drives displays with 8 seven-segment digits with two independent annunciators per digit, accepting six data bits and three digit address bits from parallel inputs controlled by a chip select input. The data bits are subdivided into four binary code bits and two annunciator control bits.

The ICM7232 drives 10 seven-segment digits with two independent annunciators per digit. To write into the display, six bits of data and four bits of digit address are clocked serially into a shift register, then decoded and written to the display.

Input levels are TTL compatible, and the DATA ACCEPTED output on the serial input devices will drive one LSTTL load. The intermediate voltage levels necessary to drive the display properly are generated by an on-chip resistor string, and the output of a totally self-contained on-chip oscillator is used to generate all display timing. All devices in this family have been fabricated using Harris' MAXCMOS® process and all inputs are protected against static discharge.

MAXCMOS® is a registered trademark of Harris Corporation.

Triplexed (1/3 Multiplexed) Liquid Crystal Displays

Figure 4 shows the connection diagram for a typical 7-segment display with two annunciators such as would be used with an ICM7231 or ICM7232 numeric display driver. Figure 5 shows the voltage waveforms of the common lines and one segment line, chosen for this example to be the "a, g, d" segment line. This line intersects with BP1 to form the "a" segment, BP2 to form the "g" segment and BP3 to form the "d" segment. Figure 5 also shows the waveform of the "a, g, d" segment line for four different ON/OFF combinations of the "a", "g" and "d" segments. Each intersection (segment or annunciator) acts as a capacitance from segment line to common line, shown schematically in Figure 6. Figure 7 shows the voltage across the "g" segment for the same four combinations of ON/OFF segments used in Figure 5.

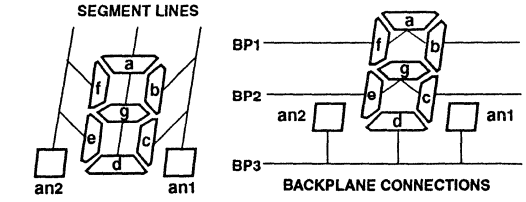
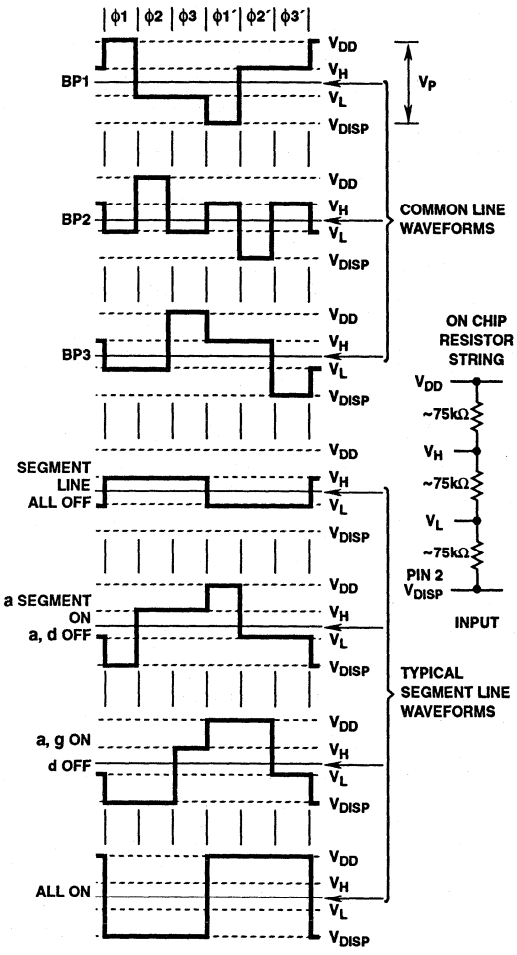


FIGURE 4. CONNECTION DIAGRAMS FOR TYPICAL 7-SEGMENT DISPLAYS



NOTES:

1. ϕ1, ϕ2, ϕ3, - BP High with Respect to Segment.
2. ϕ1′, ϕ2′, ϕ3′, - BP Low with Respect to Segment.
3. BP1 Active during ϕ1, and ϕ1′.
4. BP2 Active during ϕ2, and ϕ2′.
5. BP3 Active during ϕ3, and ϕ3′.

FIGURE 5. DISPLAY VOLTAGE WAVEFORMS

The degree of polarization of the liquid crystal material and thus the contrast of any intersection depends on the RMS voltage across the intersection capacitance. Note from Figure 7 that the RMS OFF voltage is always $V_P/3$ and that the RMS ON voltage is always $1.92\ V_P/3$.

For a $^1/_3$ multiplexed LCD, the ratio of RMS ON to OFF voltages is fixed at 1.92, achieving adequate display contrast with this ratio of applied RMS voltage makes some demands on the liquid crystal material used.

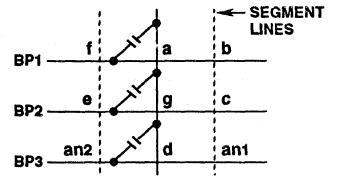
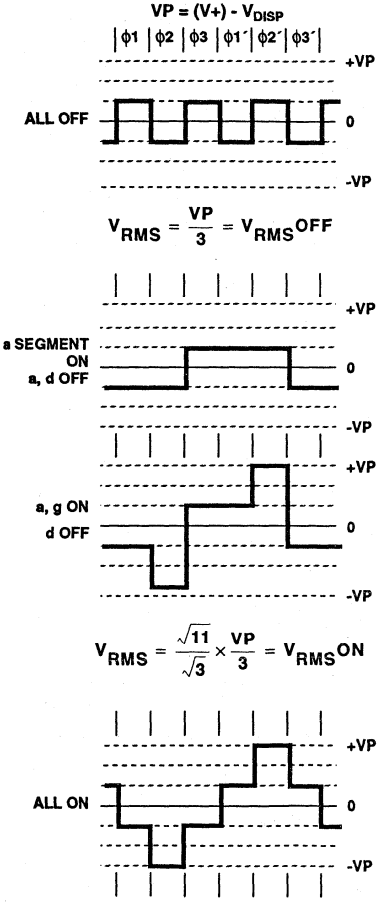


FIGURE 6. DISPLAY SCHEMATIC



$$\text{Voltage Contrast Ratio} = \frac{V_{RMS}ON}{V_{RMS}OFF} = \frac{\sqrt{11}}{\sqrt{3}} = 1.92$$

NOTES:

1. ϕ1, ϕ2, ϕ3, - BP High with Respect to Segment.
2. ϕ1′, ϕ2′, ϕ3′, - BP Low with Respect to Segment.
3. BP1 Active during ϕ1, and ϕ1′.
4. BP2 Active during ϕ2, and ϕ2′.
5. BP3 Active during ϕ3, and ϕ3′.

FIGURE 7. VOLTAGE WAVEFORMS ON SEGMENT g(V_G)

Figure 8 shows the curve of contrast versus applied RMS voltage for a liquid crystal material tailored for V_P = 3.1 V, a typical value for $^1/_3$ multiplexed displays in calculators. Note that the RMS OFF voltage $V_P/3 \approx 1V$ is just below the "threshold" voltage where contrast begins to increase. This places the RMS ON voltage at 2.1V, which provides about 85% contrast when viewed straight on.

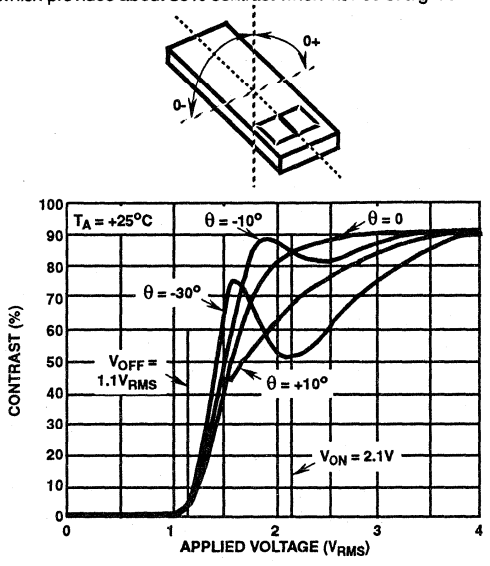


FIGURE 8. CONTRAST vs APPLIED RMS VOLTAGE

All members of the ICM7231 and ICM7232 family use an internal resistor string of three equal value resistors to generate the voltages used to drive the display. One end of the string is connected on the chip to V_{DD} and the other end (user input) is available at pin 2 (V_{DISP}) on each chip. This allows the display voltage input (V_{DISP}) to be optimized for the particular liquid crystal material used. Remember that $V_P = V_{DD} - V_{DISP}$ and should be three times the threshold voltage of the liquid crystal material used. Also it is very important that pin 2 never be driven below V_{SS}. This can cause device latchup and destruction of the chip.

Temperature Effects and Temperature Compensation

The performance of the LCD material is affected by temperature in two ways. The response time of the display to changes of applied RMS voltage gets longer as the display temperature drops. At very low temperatures (-20°C) some displays may take several seconds to change a new character after the new information appears at the outputs. However, for most applications above 0°C this will not be a problem with available multiplexed LCD materials, and for low-temperature applications, high-speed liquid crystal materials are available. At high temperature, the effect to consider deals with plastic materials used to make the polarizer.

Some polarizers become soft at high temperatures and permanently lose their polarizing ability, thereby seriously degrading display contrast. Some displays also use sealing materials unsuitable for high temperature use. Thus, when specifying displays the following must be kept in mind: liquid crystal material, polarizer, and seal materials.

A more important effect of temperature is the variation of threshold voltage. For typical liquid crystal materials suitable for multiplexing, the peak voltage has a temperature coefficient of -7 to -14mV/°C. This means that as temperature rises, the threshold voltage goes down. Assuming a fixed value for V_P when the threshold voltage drops below $V_P/3$ OFF segments begin to be visible. Figure 9 shows the temperature dependence of peak voltage for the same liquid crystal material of Figure 8.

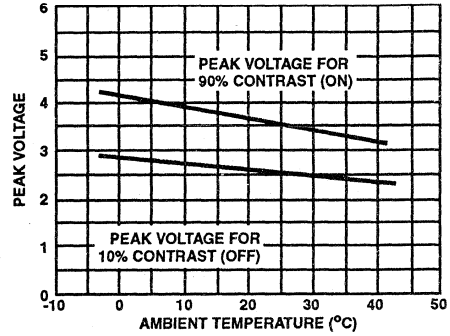


FIGURE 9. TEMPERATURE DEPENDENCE OF LC THRESHOLD

For applications where the display temperature does not vary widely, V_P may be set at a fixed voltage chosen to make the RMS OFF voltage, $V_P/3$, just below the threshold voltage at the highest temperature expected. This will prevent OFF segments turning ON at high temperature (this at the cost of reduced contrast for ON segments at low temperatures).

For applications where the display temperature may vary to wider extremes, the display voltage V_{DISP} (and thus V_P) may require temperature compensation to maintain sufficient contrast without OFF segments becoming visible.

Display Voltage and Temperature Compensation

These circuits allow control of the display peak voltage by bringing the bottom of the voltage divider resistor string out at pin 2. The simplest means for generating a display voltage suitable to a particular display is to connect a potentiometer from pin 2 to V_{SS} as shown in Figure 10. A potentiometer with a maximum value of 200kΩ should give sufficient range of adjustment to suit most displays. This method for generating display voltage should be used only in applications where the temperature of the chip and display won't vary more than ±5°C (±9°F), as the resistors on the chip have a positive temperature coefficient, which will tend to increase the display peak voltage with an increase in temperature. The display voltage also depends on the power supply voltage, leading to tighter tolerances for wider temperature ranges.

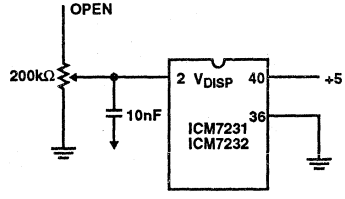


FIGURE 10. SIMPLE DISPLAY VOLTAGE ADJUSTMENT

Figure 11A shows another method of setting up a display voltage using five silicon diodes in series. These diodes, 1N914 or equivalent, will each have a forward drop of approximately 0.65V, with approximately 20µA flowing through them at room temperature. Thus, 5 diodes will give 3.25V, suitable for a 3V display using the material properties shown in Figures 4 and 5. For higher voltage displays, more diodes may be added. This circuit provides reasonable temperature compensation, as each diode has a negative temperature coefficient of -2mV/°C; five in series gives -10mV/°C, not far from optimum for the material described.

The disadvantage of the diodes in series is that only integral multiples of the diode voltage can be achieved. The diode voltage multiplier circuit shown in Figure 11B allows fine-tuning the display voltage by means of the potentiometer; it likewise provides temperature compensation since the temperature coefficient of the transistor base-emitter junction (about -2mV/°C) is also multipled. The transistor should have a beta of at least 100 with a collector current of 10µA. The inexpensive 2N2222 shown in the figure is a suitable device.

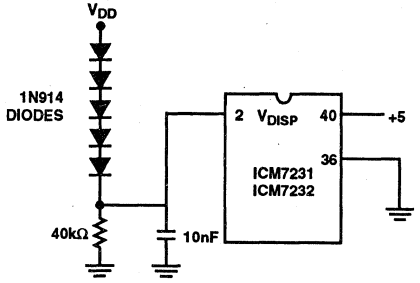


FIGURE 11A. STRING OF DIODES

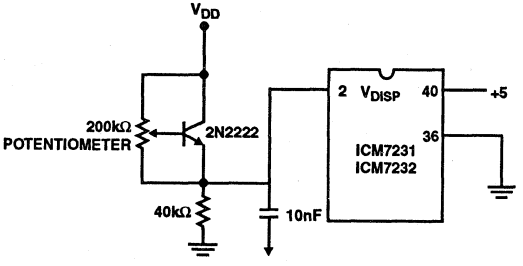


FIGURE 11B. TRANSISTOR-MULTIPLIER

FIGURE 11. DIODE-BASED TEMPERATURE COMPENSATION

For battery operation, where the display voltage is generally the same as the battery voltage (usually 3 - 4.5V), the chip may be operated at the display voltage, with V_{DISP} connected to V_{SS}. The inputs of the chip are designed such that they may be driven above V_{DD} without damaging the chip. This allows, for example, the chip and display to operate at a regulated 3V, and a microprocessor driving its inputs to operate with a less well controlled 5V supply. (The inputs should not be driven more than 6.5V above GND under any circumstances.) This also allows temperature compensation with the ICL7663S, as shown in Figure 12. This circuit allows independent adjustment of both voltage and temperature compensation.

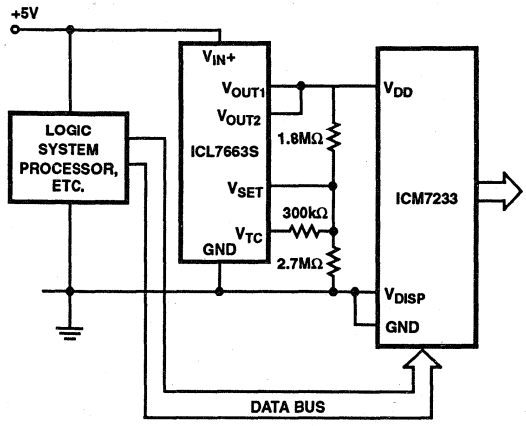


FIGURE 12. FLEXIBLE TEMPERATURE COMPENSATION

Description Of Operation

Parallel Input Of Data And Address (ICM7231)

The parallel input structure of the ICM7231 device is organized to allow simple, direct interfacing to all microprocessors, (see the Functional Block Diagram). In the ICM7231, address and data bits are written into the input latches on the rising edge of the Chip Select input.

The rising edge of the Chip Select also triggers an on-chip pulse which enables the address decoder and latches the decoded data into the addressed digit/character outputs. The timing requirements for the parallel input device are shown in Figure 1, with the values for setup, hold, and pulse width times shown in the AC Specifications section. Note that there is a minimum time between Chip Select pulses; this is to allow sufficient time for the on-chip enable pulse to decay, and ensures that new data doesn't appear at the decoder inputs before the decoded data is written to the outputs.

Serial Input Of Data And Address (ICM7232)

The ICM3232 trades six pins used as data inputs on the ICM7231 for six more segment lines, allowing two more 9-segment digits. This is done at the cost of ease in interfacing, and requires that data and address information be entered serially. Refer to Functional Block Diagram and timing diagrams, Figures 2 and 3. The interface consists of four pins: DATA Input, DATA CLOCK Input, $\overline{\text{WRITE}}$ Input and DATA ACCEPTED Output. The data present at the DATA Input is clocked into a shift register on the rising edge of the DATA CLOCK Input signal, and when the correct number of bits has been shifted into the shift register (8 in the ICM7232), the DATA ACCEPTED Output goes low. Following this, a low-going pulse at the $\overline{\text{WRITE}}$ input will trigger the chip to decode the data and store it in the output latches of the addressed digit/character. After the data is latched at the outputs, the shift register and the control logic are reset,

returning the DATA ACCEPTED Output high. After this occurs, a pulse at the WRITE input will not change the outputs, but will reset the control logic and shift register, assuring that each data bit will be entered into the correct position in the shift register depending on subsequent DATA CLOCK inputs.

The shift register and control logic will also be reset if too many DATA CLOCK INPUT edges are received; this prevents incorrect data from being decoded. In the ICM7232, the eleventh clock resets the shift register and control logic.

The recommended procedure for entering data is shown in the serial input timing diagram, Figure 2. First, when DATA ACCEPTED is high, send a WRITE pulse. This resets the shift register and control logic and initializes the chip for the data input sequence. Next clock in the appropriate number of correct data and address bits. The DATA ACCEPTED Output may be monitored if desired, to determine when the chip is ready to output the decoded data. When the correct number of bits has been entered, and the DATA ACCEPTED Output is low, a pulse at WRITE will cause the data to be decoded and stored in the latches of the addressed digit/character. The shift register and control logic are reset, causing DATA ACCEPTED to return high, and leaving the chip ready to accept data for the next digit/character.

Note that for the ICM7232 the eleventh clock resets the shift register and control logic, but the DATA ACCEPTED Output goes low after the eighth clock. This allows the user to abbreviate the data to eight bits, which will write the correct character to the 7-segment display, but will leave the annunciators off, as shown in Figure 3.

If only AN2 is to be turned on, nine bits are clocked in; if AN1 is to be turned on, all ten bits are used.

The DATA ACCEPTED Output will drive one low-power Schottky TTL input, and has equal current drive capability pulling high or low.

Note that in the serial Input devices, it is possible to address digits/characters which don't exist. As shown in Table 2 when an incorrect address is applied together with a WRITE pulse, none of the outputs will be changed.

Display Fonts and Output Codes

The standard versions of the ICM7231 and ICM7232 chips are programmed to drive a 7-segment display plus two annunciators per digit. See Table 3 for annunciator input controls.

The "A" and "B" suffix chips place both annunciators on BP3. The display connections for one digit of this display are shown in Figure 13. The "A" devices decode the input data into a hexadecimal 7-segment output, while the "B" devices supply Code B outputs (see Table 1).

The "C" devices place the left hand annunciator on BP1 and the right hand annunciator (usually a decimal point) on BP3. (See Figure 14). The "C" devices provide only a "Code B" output for the 7-segments.

TABLE 1. BINARY DATA DECODING ICM7231 AND ICM7232

CODE INPUT				DISPLAY OUTPUT	
BD3	BD2	BD1	BD0	HEX	CODE B
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	BLANK

TABLE 2. ADDRESS DECODING (ICM7231 AND ICM7232),

CODE INPUT				DISPLAY OUTPUT
ICM7232 ONLY A3	A2	A1	A0	DIGIT SELECTED
0	0	0	0	D1
0	0	0	1	D2
0	0	1	0	D3
0	0	1	1	D4
0	1	0	0	D5
0	1	0	1	D6
0	1	1	0	D7
0	1	1	1	D8
1	0	0	0	D9
1	0	0	1	D10
1	0	1	0	NONE
1	0	1	1	NONE
1	1	0	0	NONE
1	1	0	1	NONE
1	1	1	0	NONE
1	1	1	1	NONE

TABLE 3. ANNUNCIATOR DECODING

CODE INPUT		DISPLAY OUTPUT	
AN2	AN1	ICM7231A AND ICM7231B ICM7232A AND ICM7232B BOTH ANNUNCIATORS ON BP3	ICM7231C ICM7232C an2 ANNUNCIATOR BP1 an1 ANNUNCIATOR BP3
0	0	8	8
0	1	.8	8.
1	0	8.	'8
1	1	.8.	'8.

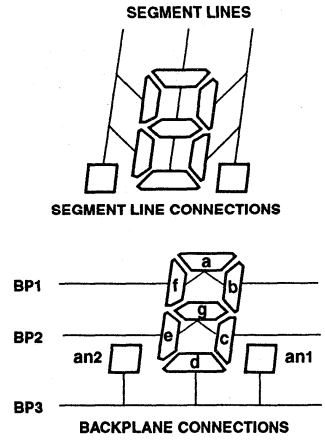
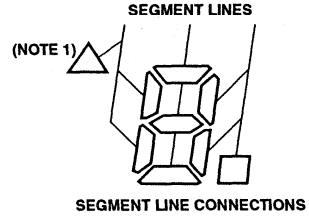
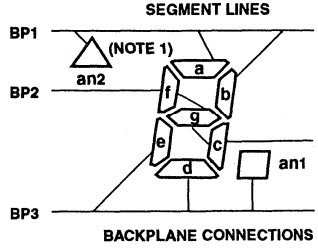


FIGURE 13. ICM7231 AND ICM7232 DISPLAY FONTS ("A" AND "B" SUFFIX VERSIONS)





NOTE:

1. Annunciators can be: STOP , GO , △ , ↑ -arrows that point to information printed around the display opening etc., whatever the designer display opening etc., whatever the designer chooses to incorporate in the liquid crystal display.

FIGURE 14. ICM7231 DISPLAY FONTS ("C" SUFFIX VERSIONS)

Compatible Displays

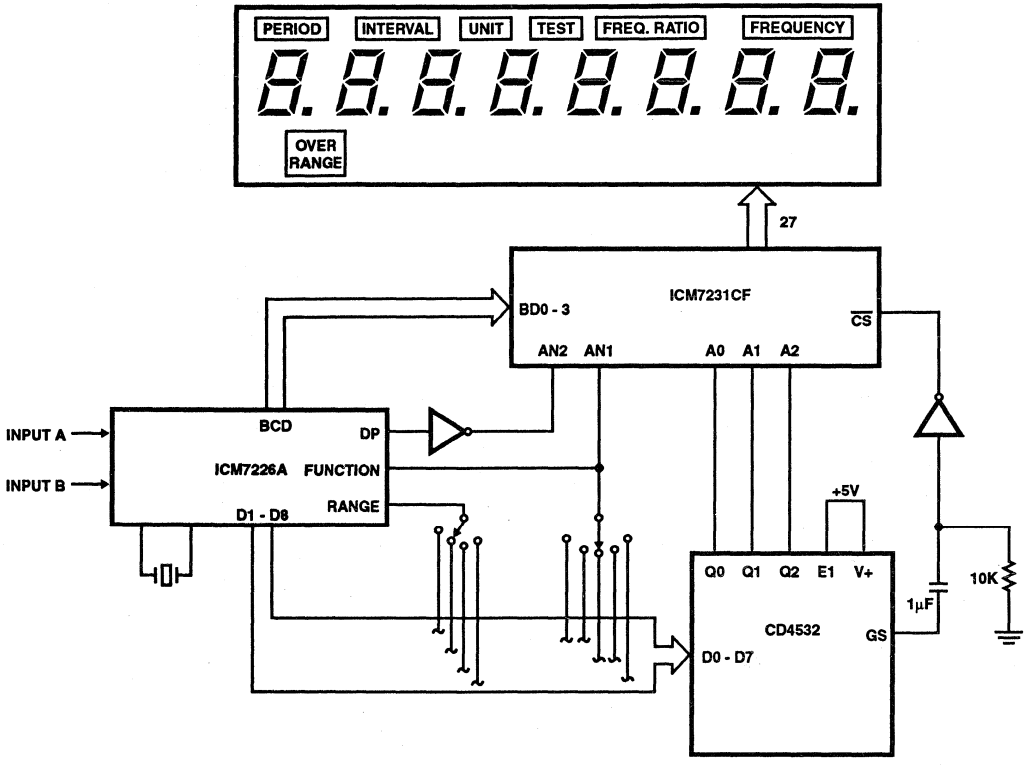
Compatible displays are manufactured by: G.E. Displays Inc., Beechwood, Ohio (216) 831-8100 (#356E3R99HJ)

Epson America Inc., Torrance CA
(Model Numbers LDB726/7/8).

Seiko Instruments USA Inc., Torrance CA
(Custom Displays)

Crystaloid, Hudson, OH

Typical Applications



NOTE: The annunciators show function and the decimal points indicate the range of the current operation. the system can be efficiently battery operated.

FIGURE 23. 10MHz FREQUENCY/PERIOD POINTER WITH LCD DISPLAY

Typical Applications (Continued)

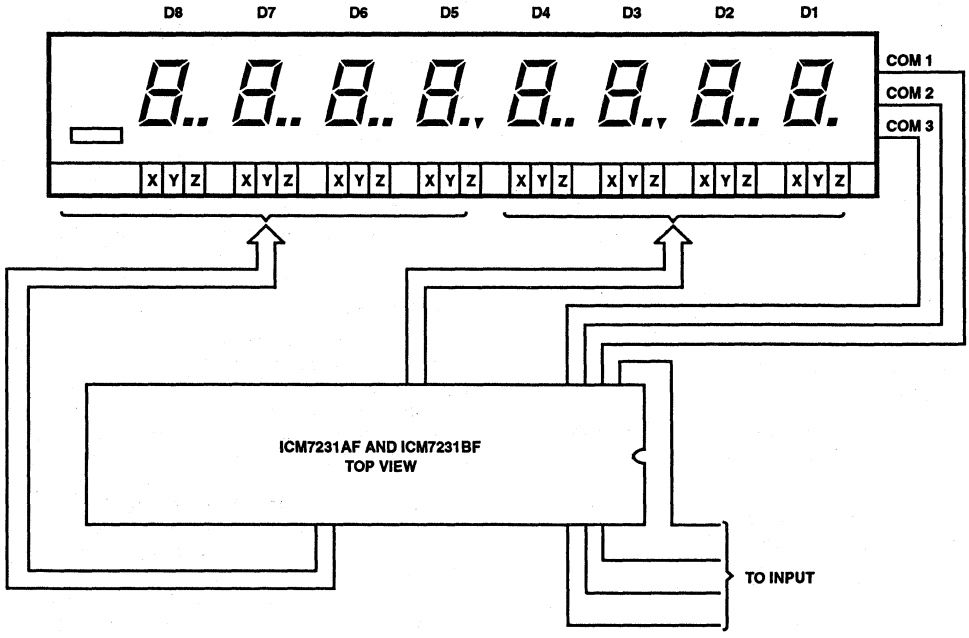


FIGURE 24. "FORWARD" PIN ORIENTATION AND DISPLAY CONNECTIONS

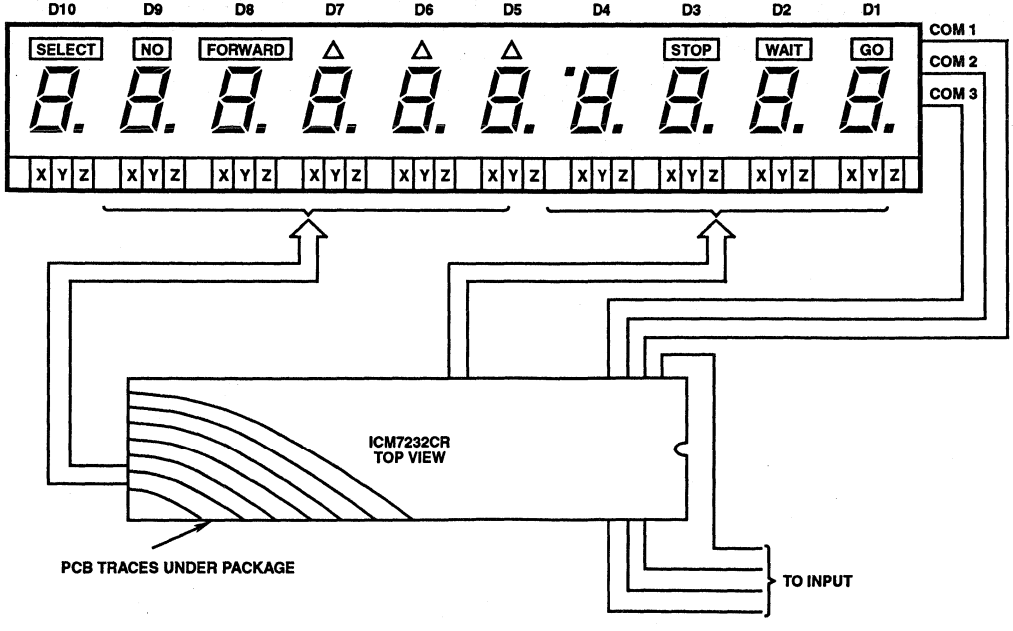


FIGURE 17. "REVERSE" PIN ORIENTATION AND DISPLAY CONNECTIONS

HARRIS SEMICONDUCTOR

ICM7243

8-Character μP-Compatible LED Display Decoder Driver

December 1993

Features

- 14-Segment and 16-Segment Fonts With Decimal Point
- Mask Programmable for Other Font-Sets Up to 64 Characters
- Microprocessor Compatible
- Directly Drives LED Common Cathode Displays
- Cascadable Without Additional Hardware
- Standby Feature Turns Display Off; Puts Chip In Low Power Mode
- Sequential Entry or Random Entry of Data Into Display
- Single +5V Operation
- Character and Segment Drivers, All MUX Scan Circuitry, 8 x 6 Static Memory and 64-Character ASCII Font Generator Included On-Chip

Ordering Information

NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7243AIJL	-25°C to +85°C	40 Lead Ceramic DIP
ICM7243AIPL	-25°C to +85°C	40 Lead Plastic DIP
ICM7243BIJL	-25°C to +85°C	40 Lead Ceramic DIP
ICM7243BIPL	-25°C to +85°C	40 Lead Plastic DIP

Description

The ICM7243 is an 8-character alphanumeric display driver and controller which provides all the circuitry required to interface a microprocessor or digital system to a 14-segment or 16-segment display. It is primarily intended for use in microprocessor systems, where it minimizes hardware and software overhead. Incorporated on-chip are a 64-character ASCII decoder, 8 x 6 memory, high power character and segment drivers, and the multiplex scan circuitry.

6-bit ASCII data to be displayed is written into the memory directly from the microprocessor data bus. Data location depends upon the selection of either **Sequential** (MODE = 1) or **Random** access mode (MODE = 0). In the **Sequential Access** mode the first entry is stored in the lowest location and displayed in the "left-most" character position. Each subsequent entry is automatically stored in the next higher location and displayed to the immediate "right" of the previous entry. A DISPlay FULL signal is provided after 8 entries; this signal can be used for cascading devices together. A $\overline{\text{CLeaR}}$ pin is provided to clear the memory and reset the location counter. The **Random Access** mode allows the processor to select the memory address and display digit for each input word.

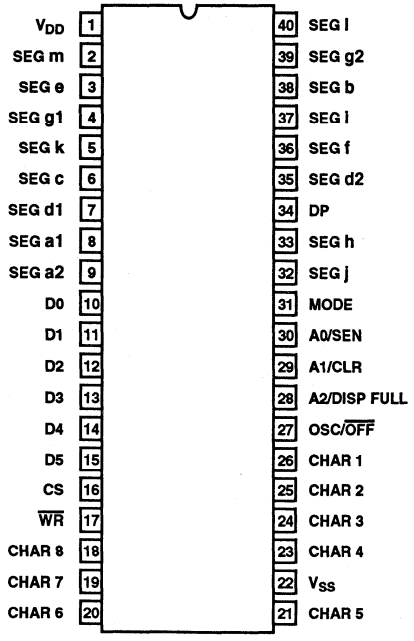
The character multiplex scan runs whenever data is not being entered. It scans the memory and CHARacter drivers, and ensures that the decoding from memory to display is done in the proper sequence. Intercharacter blanking is provided to avoid display ghosting.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

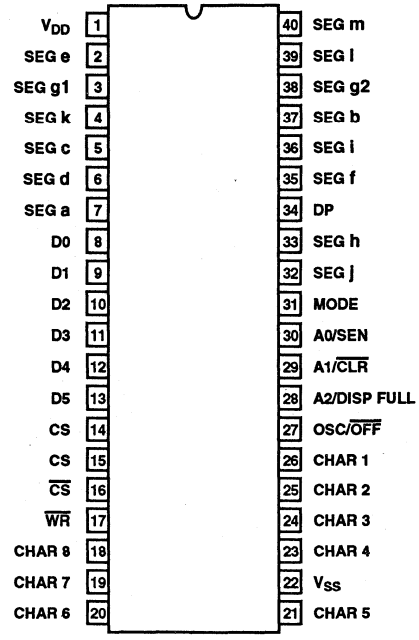
File Number **3162**

Pinouts

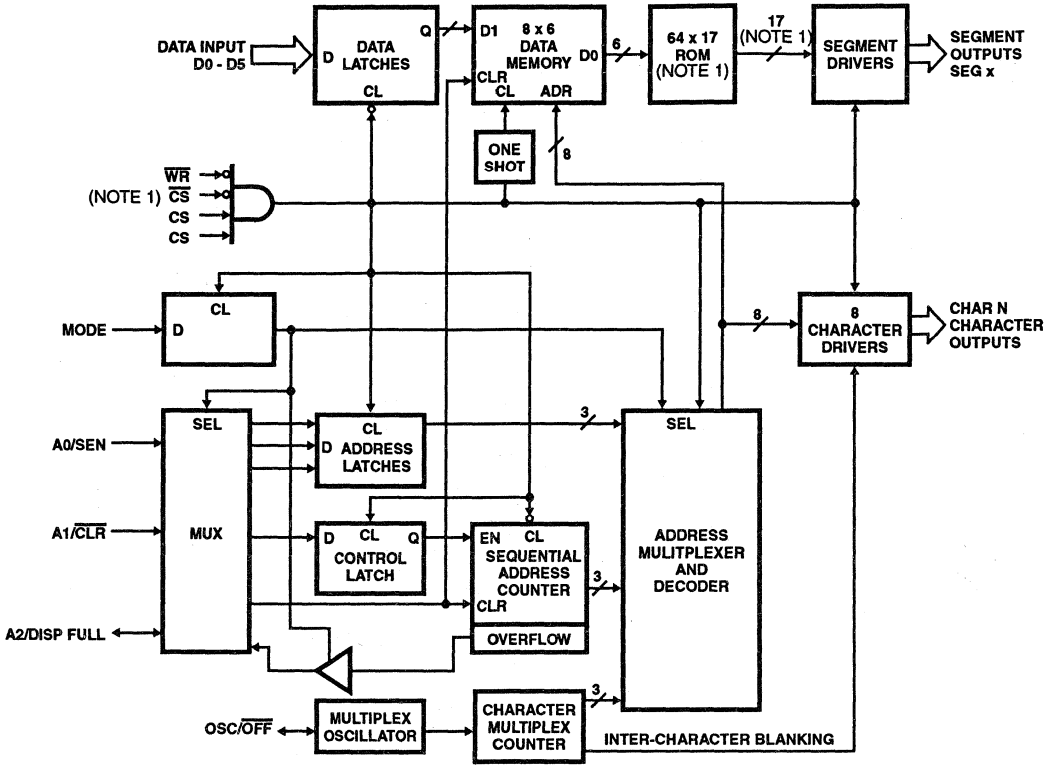
ICM7243A (16-SEGMENT CHARACTER) (PDIP)
TOP VIEW



ICM7243B (14-SEGMENT CHARACTER) (PDIP)
TOP VIEW



Functional Block Diagram



NOTE:

1. ICM7243A has only one CS and no $\overline{CS}$.
   ICM7243B has 15 Segments.

Absolute Maximum Ratings

Supply Voltage V_{DD} - V_{SS} ..... +6.0V
Input Voltage (Any Terminal) ..... V_{DD} +0.3V to V_{SS} -0.3V
CHARacter Output Current 300mA
SEGment Output Current 30mA
Storage Temperature Range ..... -55°C to +125°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic DIP	50°C/W	-
Ceramic DIP	45°C/W	15°C/W

Operating Temperature Range ..... -25°C to +85°C
Junction Temperature
Ceramic DIP Package ..... +175°C
Plastic DIP Package ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

V_{DD} = 5V, V_{SS} = 0V, T_A = 25°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{DD} - V_{SS}), V_{SUPP}		4.75	5.0	5.25	V
Operating Supply Current, I_{DD}	V_{SUPP} = 5.25V, 10 Segments ON, All 8 Characters	-	180	-	mA
Quiescent Supply Current, I_{STBY}	V_{SUPP} = 5.25V, OSC/$\overline{OFF}$ Pin < 0.5V, CS = V_{SS}	-	30	250	µA
Input High Voltage, V_{IH}		2	-	-	V
Input Low Voltage, V_{IL}		-	-	0.8	V
Input Current, I_{IN}		-10	-	+10	µA
CHARacter Drive Current, I_{CHAR}	V_{SUPP} = 5V, V_{OUT} = 1V	140	190	-	mA
CHARacter Leakage Current, I_{CHLK}		-	-	100	µA
SEGment Drive Current, I_{SEG}	V_{SUPP} = 5V, V_{OUT} = 2.5V	14	19	-	mA
SEGment Leakage Current, I_{SLK}		-	0.01	10	µA
DISPlay FULL Output Low, V_{OL}	I_{OL} = 1.6mA	-	-	0.4	V
DISPlay FULL Output High, V_{OH}	I_{IH} = 100µA	2.4	-	-	V
Display Scan Rate, f_{DS}		-	400	-	Hz

AC Electrical Specifications

Drive levels 0.4V and 2.4V, timing measured at 0.8V and 2.0V. V_{DD} = 5V, T_A = 25°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{WR}$, $\overline{CLeaR}$ Pulse Width Low, t_{WPl}		300	250	-	ns
$\overline{WR}$, $\overline{CLeaR}$ Pulse Width High (Note 1), t_{WPH}		-	250	-	ns
Data Hold Time, t_{DH}		0	-100	-	ns
Data Setup Time, t_{DS}		250	150	-	ns
Address Hold Time, t_{AH}		125	-	-	ns
Address Setup Time, t_{AS}		40	15	-	ns
CS, $\overline{CS}$ Setup Time, t_{CS}		0	-	-	ns
Pulse Transition Time, t_T		-	-	100	ns
SEN Setup Time, t_{SEN}		0	-25	-	ns
Display Full Delay, t_{WDF}		700	480	-	ns

Capacitance

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Capacitance, C_{IN}	(Note 2)	-	5	-	pF
Output Capacitance, C_O	(Note 2)	-	5	-	pF

NOTES:

1. In Sequential mode $\overline{WR}$ high must be ≥ T_{SEN} + T_{WDF}.
2. For design reference only, not tested.

Timing Waveforms

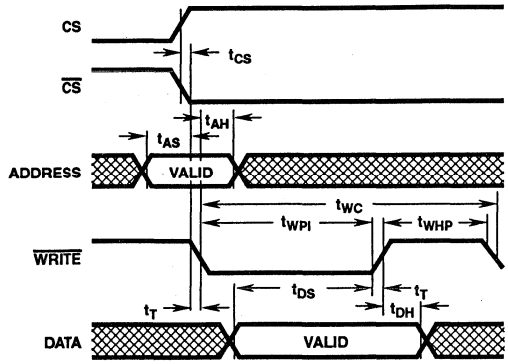


FIGURE 1. RANDOM ACCESS TIMING

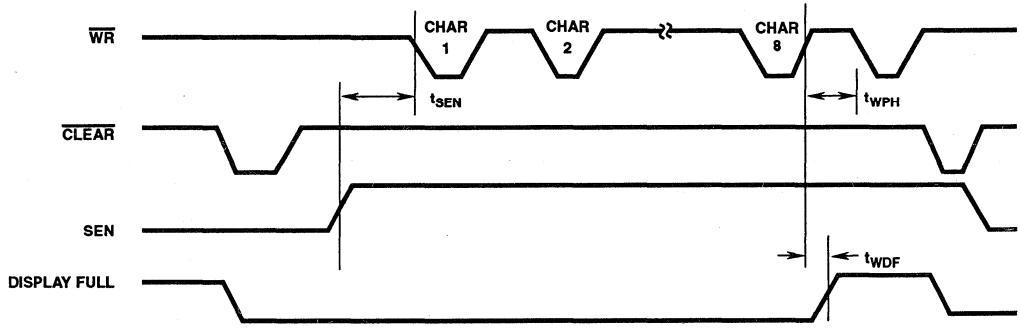


FIGURE 2. SEQUENTIAL ACCESS MODE TIMING (MODE = 1)

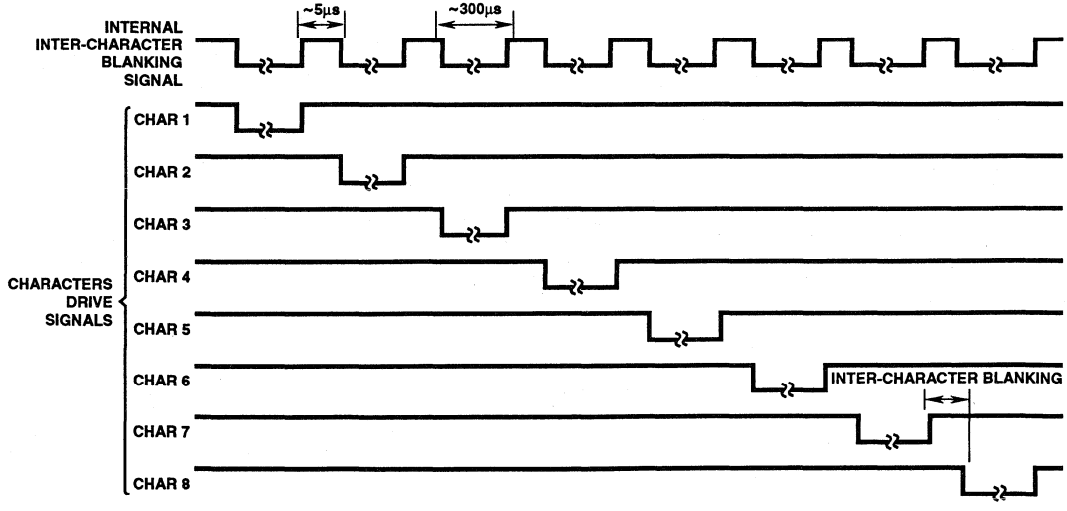


FIGURE 3. DISPLAY CHARACTERS MULTIPLEX TIMING DIAGRAM

Performance Curves

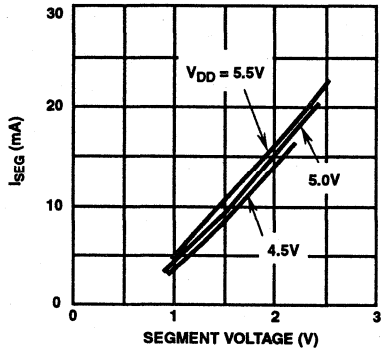


FIGURE 4. SEGMENT CURRENT vs OUTPUT VOLTAGE

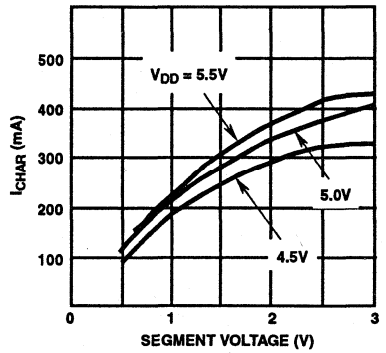


FIGURE 5. CHARACTER CURRENT VS OUPUT VOLTAGE

Pin Descriptions

SIGNAL	PIN	FUNCTION
ICM7243A(B)		
D0 - D5	10 - 15 (8 - 13)	Six-Bit ASCII Data input pins (active high).
CS, $\overline{CS}$	16 (14 - 16)	Chip Select from µP address decoder, etc.
$\overline{WR}$	17	WRite pulse input pin (active low). For an active high write pulse, CS can be used, and $\overline{WR}$ can be used as $\overline{CS}$.
MODE	31	Selects data entry MODE. High selects **Sequential Access (SA)** mode where first entry is displayed in "leftmost" character and subsequent entries appear to the "right". Low selects the **Random Access (RA)** mode where data is displayed on the character addressed via A0 - A2 Address pins.
A0/SEN	30	In **RA** mode it is the LSB of the character Address. In **SA** mode it is used for cascading devices for displays of more than 8 characters (active high enables device controller).
A1/$\overline{CLeaR}$	29	In **RA** mode this is the second bit of the address. In **SA** mode, a low input will CLeaR the Serial Address Counter, the Data Memory and the display.
A2/DISPlay FULL	28	In **RA** mode this is the MSB of the Address. In **SA** mode, the output goes high after eight entries, indicating DISPlay FULL.
OSC/$\overline{OFF}$	27	OSCillator input pin. Adding capacitance to V_{DD} will lower the internal oscillator frequency. An external oscillator can be applied to this pin. A low at this input sets the device into a (shutdown) mode, shutting OFF the display and oscillator but retaining data stored in memory.
SEG a - SEG m, DP	2 - 9, 32 - 40 (2 - 7), (32 - 40)	SEGment driver outputs.
CHARacter 1 - 8	18 - 21, 23 - 26	CHARacter driver outputs.

Test Circuit

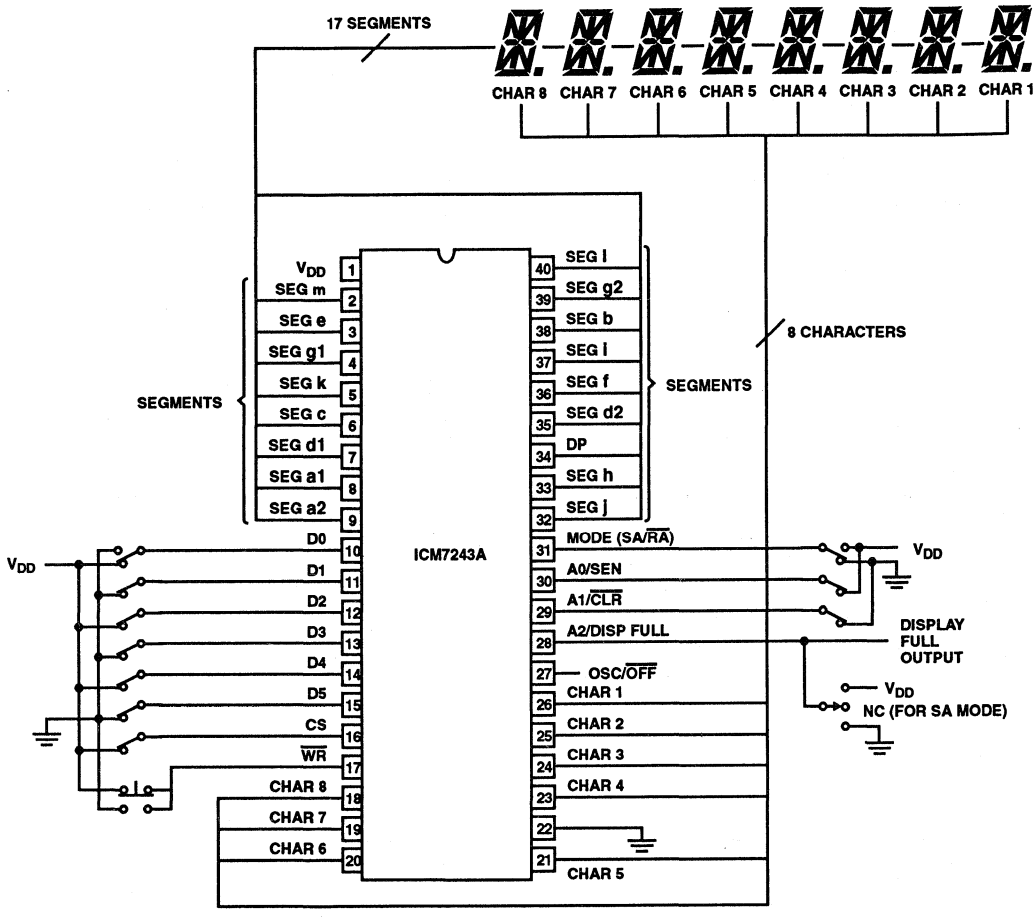


FIGURE 6.

Typical Applications

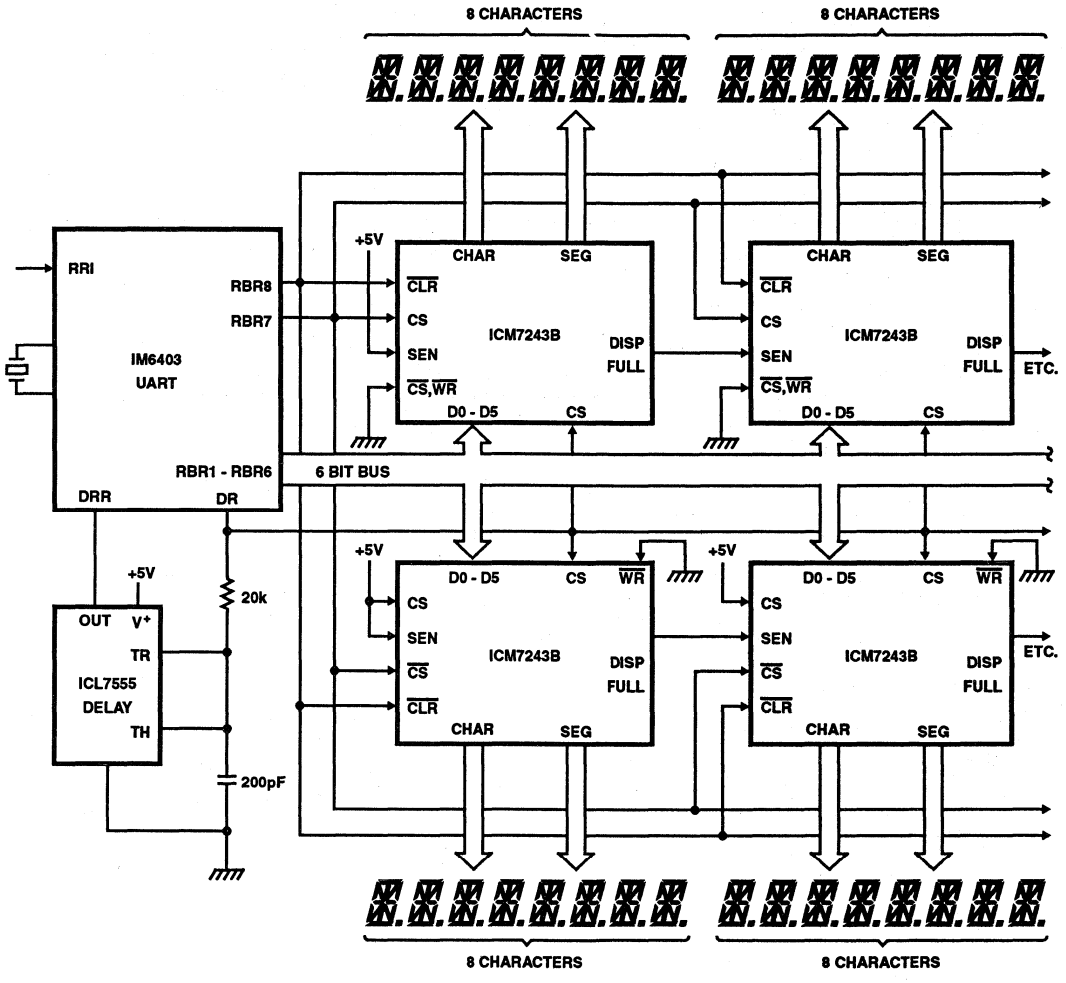
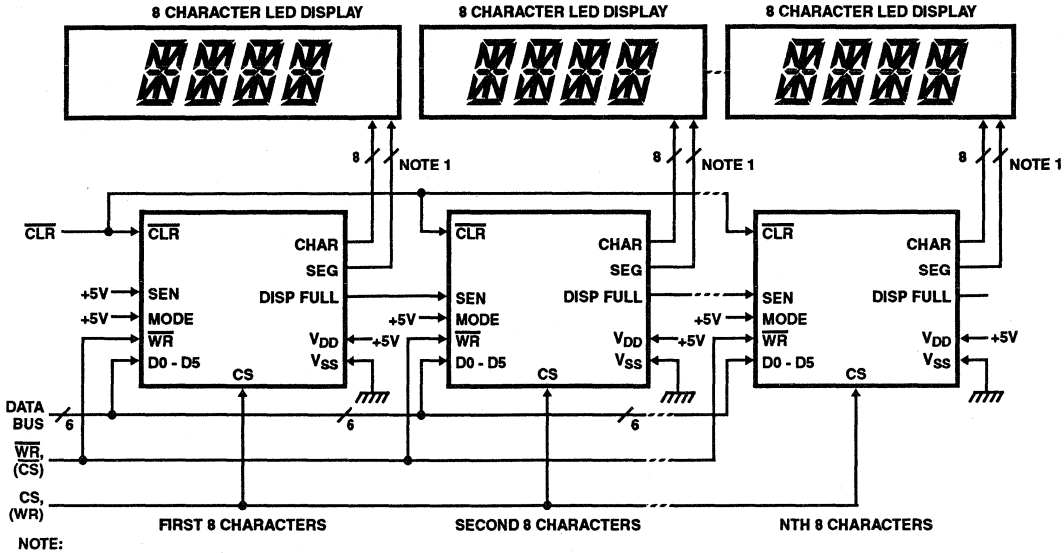


FIGURE 7. DRIVING TWO ROWS OF CHARACTERS FROM A SERIAL INPUT

Typical Applications (Continued)



NOTE:
1. 17 FOR ICM7243A, 15 FOR ICM7243B.

FIGURE 8. MULTICHARACTER DISPLAY USING SEQUENTIAL ACCESS MODE

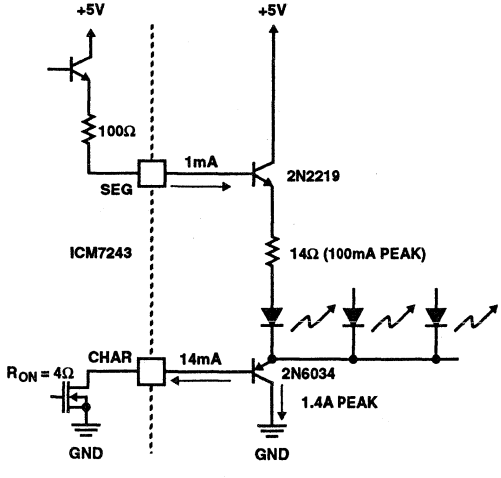


FIGURE 9A. COMMON CATHODE DISPLAY

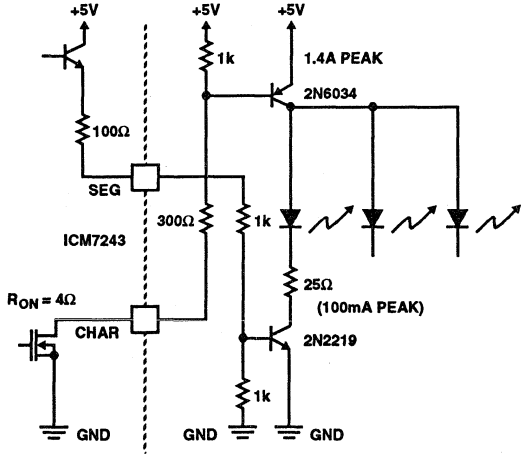


FIGURE 9B. COMMON ANODE DISPLAY

FIGURE 9. DRIVING LARGE DISPLAYS

Typical Applications (Continued)

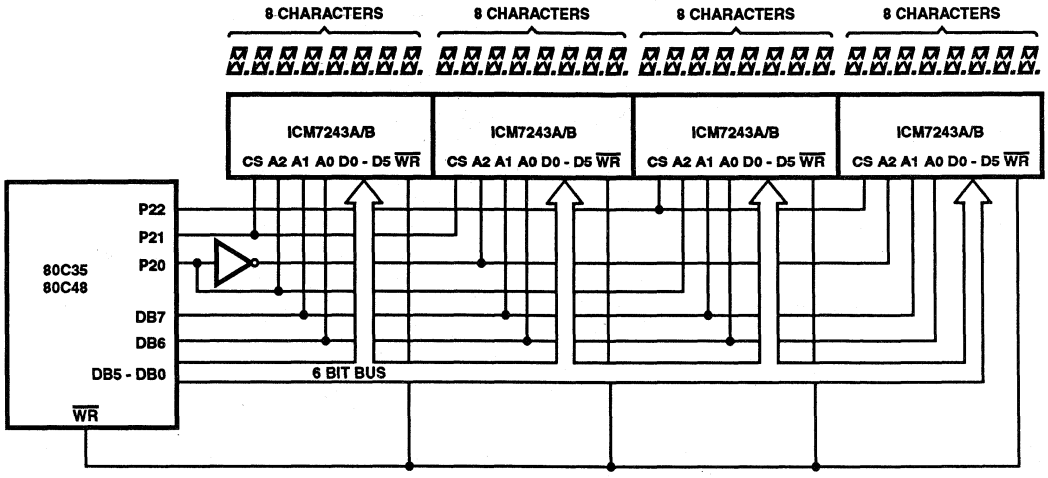
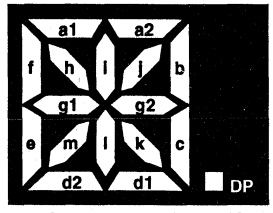


FIGURE 10. RANDOM ACCESS 32-CHARACTER DISPLAY IN A 80C48 SYSTEM

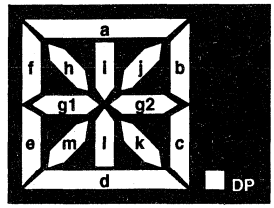
Display Font and Segment Assignments



D5, D4	0	0	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
	0	1	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	↑	_
	1	0		!	"	£	$	%	&	'	(	)	*	+	,	-	.	/
	1	1	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
		D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

FIGURE 11. ICM7232A 16-SEGMENT CHARACTER FONT WITH DECIMAL POINT

Display Font and Segment Assignments (Continued)



D5, D4	0	0	@	A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
	0	1	P	Q	R	S	T	U	V	W	X	Y	Z	[	\	]	↑	_
	1	0		!	"	#	$	%	&	'	(	)	*	+	,	-	.	/
	1	1	0	1	2	3	4	5	6	7	8	9	:	;	<	=	>	?
		D3	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
		D2	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
		D1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
		D0	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

NOTE: Segments a and d appear as 2 segments each, but both halves are driven together.

FIGURE 12. ICM7243B 14-SEGMENT CHARACTER FONT WITH DECIMAL POINT

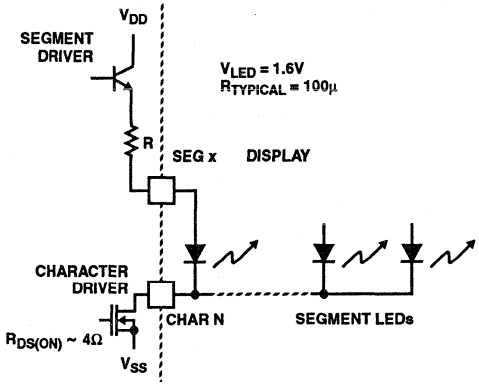


FIGURE 13. SEGMENT AND CHARACTER DRIVERS OUTPUT CIRCUIT

Detailed Description

$\overline{WR}$, $\overline{CS}$, CS - These pins are immediately functionally ANDed, so all actions described as occurring on an edge of $\overline{WR}$, with CS and $\overline{CS}$ enabled, will occur on the equivalent (last) enabling or (first) disabling edge of any of these inputs. The delays from CS pins are slightly (about 5ns) greater than from $\overline{WR}$ or $\overline{CS}$ due to the additional inverter required on the former.

MODE - The MODE pin input is latched on the falling edge of $\overline{WR}$ (or its equivalent, see above). The location (in Data Memory) where incoming data will be placed is determined either from the Address pins or the Sequential Address Counter. This is controlled by MODE input. MODE also controls the function of A0/SEN, A1/$\overline{CLR}$, and A2/DISPlay FULL lines.

Random Access Mode - When the internal mode latch is set for **Random Access (RA)** (MODE latched low), the Address input on A0, A1 and A2 will be latched by the falling edge of $\overline{WR}$ (or its equivalent). Subsequent changes on the Address lines will not affect device operation. This allows use of a multiplexed 6-bit bus controlling both address and data, with timing controlled by $\overline{WR}$.

Sequential Access Mode - If the internal latch is set for **Sequential Access (SA)**, (MODE latched high), the Serial ENable input or SEN will be latched on the falling edge of $\overline{WR}$ (or its equivalent). The $\overline{CLR}$ input is asynchronous, and will force-clear the Sequential Address Counter to address 000 (CHARacter 1), and set all Data Memory contents to 100000 (blank) at any time. The DISPlay FULL output will be active in **SA** mode to indicate the overflow status of the Sequential Address Counter. If this output is low, and SEN is (latched) high, the contents of the Counter will be used to establish the Data Memory location for the Data input. The Counter is then incremented on the rising edge of $\overline{WR}$. If SEN is low, or DISPlay FULL is high, no action will occur. This allows easy "daisy-chaining" of display drivers for multiple character displays in a **Sequential Access** mode.

Changing Modes - Care must be exercised in any application involving changing from one mode to another. The change will occur only on a falling edge of $\overline{WR}$ (or its equivalent). When changing mode from **Sequential Access** to **Random Access**, note that A2/DISPlay FULL will be an output until $\overline{WR}$ has fallen low, and an Address drive here could cause a conflict. When changing from **Random Access** to **Sequential Access**, A1/$\overline{CLR}$ should be high to avoid inadvertent clearing of the Data Memory and Sequential Address Counter. DISPlay FULL will become active immediately after the rising edge of $\overline{WR}$.

Data Entry - The input Data is latched on the rising edge of $\overline{WR}$ (or its equivalent) and then stored in the Data Memory location determined as described above. The six Data bits can be multiplexed with the Address information on the same lines in **Random Access** mode. Timing is controlled by the $\overline{WR}$ input.

OSC/OFF - The device includes a relaxation oscillator with an internal capacitor and a nominal frequency of 200kHz. By adding external capacitance to V_{DD} at the OSC/$\overline{OFF}$ pin, this frequency can be reduced as far as desired. Alternatively, an external signal can be injected on this pin. The oscillator (or external) frequency is pre-divided by 64, and then further divided by 8 in the Multiplex Counter, to drive the CHARacter drive lines (see Figure 3). An inter-character blanking signal is derived from the pre-divider. An additional comparator on the OSC/$\overline{OFF}$ input detects a level lower than the relaxation oscillator's range, and blanks the display, disables the DISPlay FULL output (if active), and clears the pre-divider and Multiplex Counter. This puts the circuit in a low-power-dissipation mode in which all outputs are effectively open circuits, except for parasitic diodes to the supply lines. Thus a display connected to the output may be driven by another circuit (including another ICM7243) without driver conflicts.

Display Output - The output of the Multiplex Counter is decoded and multiplexed into the address input of the Data Memory, except during $\overline{WR}$ operations (in Sequential Access mode, with SEN high and DISPlay FULL low), when it scans through the display data. The address decoder also drives the CHARacter outputs, except during the inter-character blanking interval (nominally about 5µs). Each CHARacter output lasts nominally about 300µs, and is repeated nominally every 2.5ms, i.e., at a 400Hz rate (times are based on internal oscillator without external capacitor).

The 6 bits read from the Data Memory are decoded in the ROM to the 17 (15 for ICM7243B) segment signals, which drive the SEGment outputs. Both CHARacter and SEGment outputs are disabled during $\overline{WR}$ operations (with SEN high and DISPlay FULL Low for **Sequential Access** mode). The outputs may also be disabled by pulling OSC/$\overline{OFF}$ low.

The decode pattern from 6 bits to 17 (15) segments is done by a ROM pattern according to the ASCII font shown. Custom decode patterns can be arranged, within these limitations, by consultation with the factory.

DATA ACQUISITION 13

COUNTERS WITH DISPLAY DRIVERS/ TIMEBASE GENERATORS

NOTE: Bold Type Designates a New Product from Harris.

HARRIS SEMICONDUCTOR

HA7210

December 1993

Low Power Crystal Oscillator

Features

- Single Supply Operation@ 32kHz .....2.0V to 7.0V
- Operating Frequency Range..... 10kHz to 10MHz
- Supply Current at 32kHz.....5μA
- Supply Current at 1MHz 130μA
- Drives 2 CMOS Loads
- Only Requires an External Crystal for Operation

Applications

- Battery Powered Circuits
- Remote Metering
- Embedded Microprocessors
- Palm Top/Notebook PC

Description

The HA7210 is a very low power crystal-controlled oscillator that can be externally programmed to operate between 10kHz and 10MHz. For normal operation it requires only the addition of a crystal. The part exhibits very high stability over a wide operating voltage and temperature range.

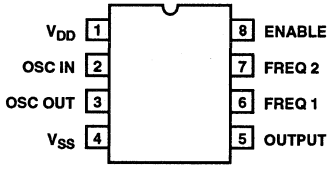
The HA7210 also features a disable mode that switches the output to a high impedance state. This feature is useful for minimizing power dissipation during standby and when multiple oscillator circuits are employed.

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA7210IP	-40°C to +85°C	8 Lead Plastic DIP
HA7210IB	-40°C to +85°C	8 Lead SOIC
HA7210Y	-40°C to +85°C	DIE

Pinout

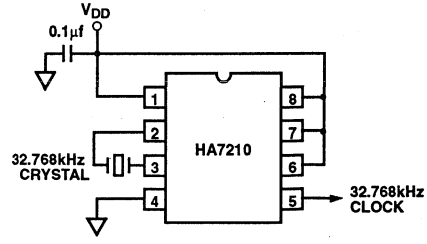
HA7210
TOP VIEW



FREQUENCY SELECTION TRUTH TABLE

ENABLE	FREQ 1	FREQ 2	OUTPUT RANGE
1	1	1	10kHz - 100kHz
1	1	0	100kHz - 1MHz
1	0	1	1MHz - 5MHz
1	0	0	5MHz - 10MHz+
0	X	X	High-Z

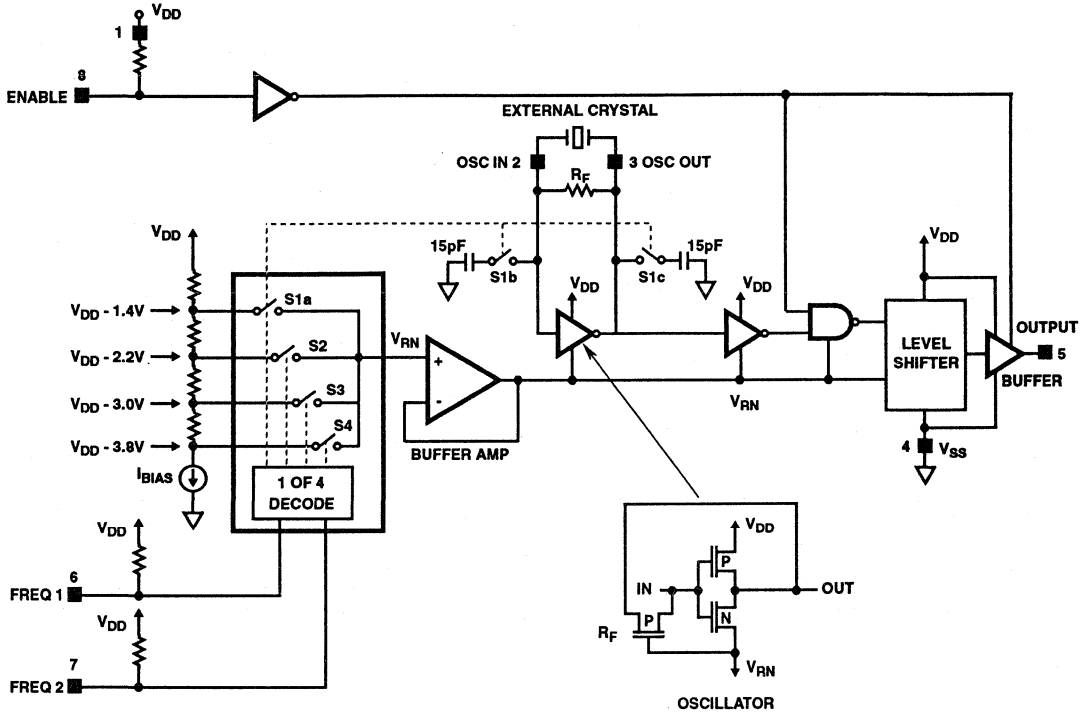
Typical Application Circuit



32.768kHz MICROPOWER CLOCK OSCILLATOR

File Number 3389.3

Simplified Block Diagram



ENABLE	FREQ 1	FREQ2	SWITCH	OUTPUT RANGE
1	1	1	S1a, b, c	10kHz - 100kHz
1	1	0	S2	100kHz - 1MHz
1	0	1	S3	1MHz - 5MHz
1	0	0	S4	5MHz - 10MHz+
0	X	X	X	High Impedance

Absolute Maximum Ratings

Supply Voltage 10.0V
Voltage (any pin) ..... V_{SS}-0.3V to V_{DD}+0.3V
Junction Temperature (Plastic Package) ..... +150°C
ESD Rating (Note 2) ..... >4000V
Lead Temperature (Soldering 10s) ..... +300°C

Operating Conditions

Operating Temperature (Note 3) ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
SOIC ..... 170°C/W
Plastic DIP ..... 150°C/W

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{SS} = GND, T_A = +25°C, Unless Otherwise Specified.

PARAMETER	V_{DD} = 5V			V_{DD} = 3V			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
V_{DD} Supply Range (f_{OSC} = 32kHz)	2	5	7	-	-	-	V
I_{DD} Supply Current							
f_{OSC} = 32kHz, EN = 0 Standby	-	5.0	9.0	-	-	-	µA
f_{OSC} = 32kHz, C_L = 10pF (Note 1), EN = 1, Freq1 = 1, Freq2 = 1	-	5.2	10.2	-	3.6	6.1	µA
f_{OSC} = 32kHz, C_L = 40pF, EN = 1, Freq1 = 1, Freq2 = 1	-	10	15	-	6.5	9	µA
f_{OSC} = 1MHz, C_L = 10pF (Note 1), EN = 1, Freq1 = 0, Freq2 = 1	-	130	200	-	90	180	µA
f_{OSC} = 1MHz, C_L = 40pF, EN = 1, Freq1 = 0, Freq2 = 1	-	270	350	-	180	270	µA
V_{OH} Output High Voltage (I_{OUT} = -1mA)	4.0	4.9	-	-	2.8	-	V
V_{OL} Output Low Voltage (I_{OUT} = 1mA)	-	0.07	0.4	-	0.1	-	V
I_{OH} Output High Current ($V_{OUT} \geq 4V$)	-	-10	-5	-	-	-	mA
I_{OL} Output Low Current ($V_{OUT} \leq 0.4V$)	5.0	10.0	-	-	-	-	mA
Tri-State Leakage Current							
(V_{OUT} = 0V, 5V, T_A = 25°C, -40°C)	-	0.1	-	-	-	-	nA
(V_{OUT} = 0V, 5V, T_A = 85°C)	-	10	-	-	-	-	nA
I_{IN} Enable, Freq1, Freq2 Input Current (V_{IN} = V_{SS} to V_{DD})	-	0.4	1.0	-	-	-	µA
V_{IH} Input High Voltage Enable, Freq1, Freq2	2.0	-	-	-	-	-	V
V_{IL} Input Low Voltage Enable, Freq1, Freq2	-	-	0.8	-	-	-	V
Enable Time (C_L = 18pF, R_L = 1kΩ)	-	800	-	-	-	-	ns
Disable Time (C_L = 18pF, R_L = 1kΩ)	-	90	-	-	-	-	ns
t_R Output Rise Time (10% - 90%, f_{OSC} = 32kHz, C_L = 40pF)	-	12	25	-	12	-	ns
t_F Output Fall Time (10% - 90%, f_{OSC} = 32kHz, C_L = 40pF)	-	12	25	-	14	-	ns
Duty Cycle (C_L = 40pF) f_{OSC} = 1MHz, Packaged Part Only (Note 4)	40	54	60	-	-	-	%
Duty Cycle (C_L = 40pF) f_{OSC} = 32kHz, (See Typical Curves)	-	41	-	-	44	-	%
Frequency Stability vs. Supply Voltage (f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF)	-	1	-	-	-	-	ppm/V
Frequency Stability vs. Temperature (f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF)	-	0.1	-	-	-	-	ppm/°C
Frequency Stability vs. Load (f_{OSC} = 32kHz, V_{DD} = 5V, C_L=10pF)	-	0.01	-	-	-	-	ppm/pF

NOTES:

1. Calculated using the equation $I_{DD} = I_{DD}$ (No Load) + (V_{DD}) (f_{OSC})(C_L)
2. Human body model.
3. This product is production tested at +25°C only.
4. Duty cycle will vary with supply voltage, oscillation frequency, and parasitic capacitance on the crystal pins.

Test Circuits

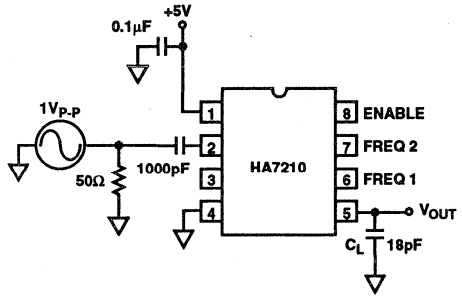


FIGURE 1

In production the HA7210 is tested with a 32kHz and a 1MHz crystal. However for characterization purposes data was taken using a sinewave generator as the frequency determining element, as shown in Figure 1. The $1V_{P-P}$ input is a smaller amplitude than what a typical crystal would generate so the transitions are slower. In general the Generator data will show a "worst case" number for I_{DD}, duty cycle, and rise/fall time. The Generator test method is useful for testing a variety of frequencies quickly and provides curves which can be used for understanding performance trends. Data for the HA7210 using crystals has also been taken. This data has been overlaid onto the generator data to provide a reference for comparison.

Theory of Operation

The HA7210 is a Pierce Oscillator optimized for low power consumption, requiring no external components except for a bypass capacitor and a Parallel Mode Crystal. The Simplified Block Diagram shows the Crystal attached to pins 2 and 3, the Oscillator input and output. The crystal drive circuitry is detailed showing the simple CMOS inverter stage and the P-channel device being used as biasing resistor R_F. The inverter will operate mostly in its linear region increasing the amplitude of the oscillation until limited by its transconductance and voltage rails, V_{DD} and V_{RN}. The inverter is self biasing using R_F to center the oscillating waveform at the input threshold. Do not interfere with this bias function with external loads or excessive leakage on pin 2. Nominal values for R_F are 17MΩ in the lowest frequency range to 7MΩ in the highest frequency range.

The HA7210 optimizes its power for 4 frequency ranges selected by digital inputs Freq1 and Freq2 as shown in the Block Diagram. Internal pull up resistors on Enable, Freq1 and Freq2 allow the user simply to leave one or all digital inputs not connected for a corresponding "1" state. All digital inputs may be left open for 10kHz to 100kHz operation.

A current source develops 4 selectable reference voltages through series resistors. The selected voltage, V_{RN}, is buffered and used as the negative supply rail for the oscillator section of the circuit. The use of a current source in the reference string allows for wide supply variation with minimal mance. The reduced operating voltage of the oscillator section reduces power consumption and limits transconductance and bandwidth to the frequency range selected. For frequencies at the edge of a range, the higher range may provide better performance.

The crystal oscillator waveform on pin 3 is squared up through a series of inverters to the output drive stage. The Enable function is implemented with a NAND gate in the inverter string, gating the signal to the level shifter and output stage. Also during Disable the output is set to a high impedance state useful for minimizing power during standby and when multiple oscillators are OR'd to a single node.

Design Considerations

The low power CMOS transistors are designed to consume power mostly during transitions. Keeping these transitions short requires a good decoupling capacitor as close as possible to the supply pins 1 and 4. A ceramic 0.1µF is recommended. Additional supply decoupling on the circuit board with 1µF to 10µF will further reduce overshoot, ringing and power consumption. The HA7210, when compared to a crystal and inverter alone, will speed clock transition times, reducing power consumption of all CMOS circuitry run from that clock.

Power consumption may be further reduced by minimizing the capacitance on moving nodes. The majority of the power will be used in the output stage driving the load. Minimizing the load and parasitic capacitance on the output, pin 5, will play the major role in minimizing supply current. A secondary source of wasted supply current is parasitic or crystal load capacitance on pins 2 and 3. The HA7210 is designed to work with most available crystals in its frequency range with no external components required. Two 15pF capacitors are internally switched onto pins 2 and 3 to compensate the oscillator in the 10kHz to 100kHz frequency range.

The supply current of the HA7210 may be approximately calculated from the equation:

$$I_{DD} = I_{DD}(\text{Disabled}) + V_{DD} \times F_{OSC} \times C_L$$

where: I_{DD} = Total supply current
V_{DD} = Total voltage from V_{DD} (pin1) to V_{SS} (pin4)
F_{OSC} = Frequency of Oscillation
C_L = Output (pin5) load capacitance

Example #1:

V_{DD} = 5V, F_{OSC} = 100kHz, C_L = 30pF
I_{DD}(Disabled) = 4.5µA (Figure 10)
I_{DD} = 4.5µA + (5V)(100kHz)(30pF) = 19.5µA
Measured I_{DD} = 20.3µA

Example #2:

V_{DD} = 5V, F_{OSC} = 5MHz, C_L = 30pF
I_{DD}(Disabled) = 75µA (Figure 9)
I_{DD} = 75µA + (5V)(5MHz)(30pF) = 825µA
Measured I_{DD} = 809µA

Crystal Selection

For general purpose applications, a Parallel Mode Crystal is a good choice for use with the HA7210. However for applications where a precision frequency is required, the designer needs to consider other factors.

Crystals are available in two types or modes of oscillation, Series and Parallel. Series Mode crystals are manufactured to operate at a specified frequency with zero load capacitance and appear as a near resistive impedance when oscillating. Parallel Mode crystals are manufactured to operate with a specific capacitive load in series, causing the crystal to operate at a more inductive impedance to cancel the load capacitor. Loading a crystal with a different capacitance will "pull" the frequency off its value.

The HA7210 has 4 operating frequency ranges. The higher three ranges do not add any loading capacitance to the oscillator circuit. In the lowest range, 10kHz to 100kHz, the HA7210 automatically switches in two 15pF capacitors onto OSC IN (pin2) and OSC OUT (pin3) to eliminate potential start-up problems. These capacitors create an effective crystal loading capacitor equal to the series combination of these two capacitors. For the HA7210, in the lowest range, the effective loading capacitance is 7.5pF. Therefore the choice for a crystal, in this range, should be a Parallel Mode crystal that requires a 7.5pF load.

In the higher 3 frequency ranges, the capacitance on pins 2 and 3 will be determined by package and layout parasitics, typically 4 to 5pF. Ideally the choice for crystal should be a Parallel Mode set for 2.5pF load. A crystal manufactured for a different load will be "pulled" from its nominal frequency (see Crystal Pullability).

Frequency Fine Tuning

Two Methods will be discussed for fine adjustment of the crystal frequency. The first and preferred method (Figure 2), provides better frequency accuracy and oscillator stability than method two (Figure 3). Method one also eliminates start-up problems sometimes encountered with 32kHz tuning fork crystals.

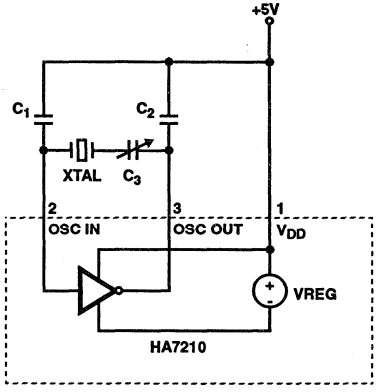


FIGURE 2

For best oscillator performance, two conditions must be met: the capacitive load must be matched to both the inverter and crystal to provide ideal conditions for oscillation, and the frequency of the oscillator must be adjustable to the desired frequency. In Method two these two goals can be at odds with each other; either the oscillator is trimmed to frequency by de-tuning the load circuit, or stability is increased at the expense of absolute frequency accuracy.

Method one allows these two conditions to be met independently. The two fixed capacitors, C_1 and C_2, provide the optimum load to the oscillator and crystal. C_3 adjusts the frequency at which the circuit oscillates without appreciably changing the load (and thus the stability) of the system. Once a value for C_3 has been determined for the particular type of crystal being used, it could be replaced with a fixed capacitor. For the most precise control over oscillator frequency, C_3 should remain adjustable.

This three capacitor tuning method will be more accurate and stable than method two and is recommended for 32kHz tuning fork crystals; without it they may leap into an overtone mode when power is initially applied.

Method two has been used for many years and may be preferred in applications where cost or space is critical. Note that in both cases the crystal loading capacitors are connected between the oscillator and V_{DD}; do not use V_{SS} as an AC ground. The Simplified Block Diagram shows that the oscillating inverter does not directly connect to V_{SS} but is referenced to V_{DD} and V_{RN}. Therefore V_{DD} is the best AC ground available.

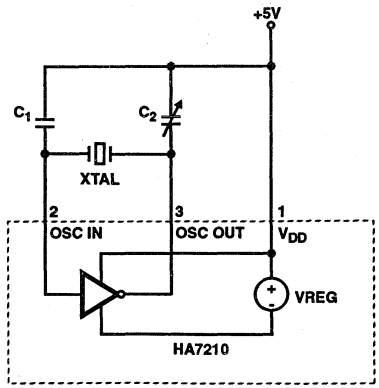


FIGURE 3

Typical values of the capacitors in Figure 2 are shown below. Some trial and error may be required before the best combination is determined. The values listed are total capacitance including parasitic or other sources. Remember that in the 10kHz to 100kHz frequency range setting the HA7210 switches in two internal 15pF capacitors.

CRYSTAL FREQUENCY	LOAD CAPS C1, C2	TRIMMER CAP C3
32kHz	33pF	5-50pF
1MHz	33pF	5-50pF
2MHz	25pF	5-50pF
4MHz	22pF	5-100pF

Crystal Pullability

Figure 4 shows the basic equivalent circuit for a crystal and its loading circuit.

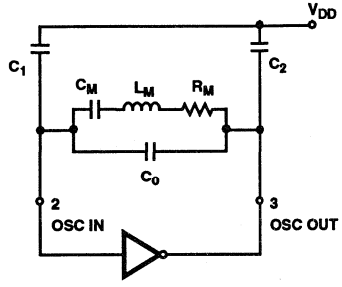


FIGURE 4

Where: C_M = Motional Capacitance
L_M = Motional Inductance
R_M = Motional Resistance
C_0 = Shunt Capacitance

$$C_{CL} = \frac{1}{\left(\frac{1}{C_1} + \frac{1}{C_2}\right)} = \text{Equivalent Crystal Load}$$

If loading capacitance is connected to a Series Mode Crystal, the new Parallel Mode frequency of resonance may be calculated with the following equation:

$$F_P = F_S\left[1 + \frac{C_M}{2(C_0 + C_{CL})}\right]$$

Where: F_P = Parallel Mode Resonant Frequency
F_S = Series Mode Resonant Frequency

In a similar way, the Series Mode resonant frequency may be calculated from a Parallel Mode crystal and then you may calculate how much the frequency will "pull" with a new load.

Layout Considerations

Due to the extremely low current (and therefore high impedance) the circuit board layout of the HA7210 must be given special attention. Stray capacitance should be minimized. Keep the oscillator traces on a single layer of the PCB. Avoid putting a ground plane above or below this layer. The traces between the crystal, the capacitors, and the HA7210 OSC pins should be as short as possible. Completely surround the oscillator components with a thick trace of V_{DD} to minimize coupling with any digital signals. The final assembly must be free from contaminants such as solder flux, moisture, or any other potential source of leakage. A good solder mask will help keep the traces free of moisture and contamination over time.

Further Reading

Al Little "HA7210 Low Power Oscillator: Micropower Clock Oscillator and Op Amps Provide System Shutdown for Battery Circuits". Harris Semiconductor Application Note AN9317.

S. S. Eaton "Timekeeping Advances Through COS/MOS Technology". Harris Semiconductor Application Note ICAN-6086.

E. A. Vittoz et. al. "High-Performance Crystal Oscillator circuits: Theory and Application". IEEE Journal of Solid-State Circuits, Vol. 23, No3, June 1988, pp774-783.

M. A. Unkrich et. al. "Conditions for Start-Up in Crystal Oscillators". IEEE Journal of Solid-State Circuits, Vol. 17, No1, Feb. 1982, pp87-90.

Marvin E. Frerking "Crystal Oscillator Design and Temperature Compensation". New York: Van Nostrand-Reinhold, 1978. Pierce Oscillators Discussed pp56-75.

Die Characteristics

DIE DIMENSIONS:
68 x 64 x 14 ± 1mils

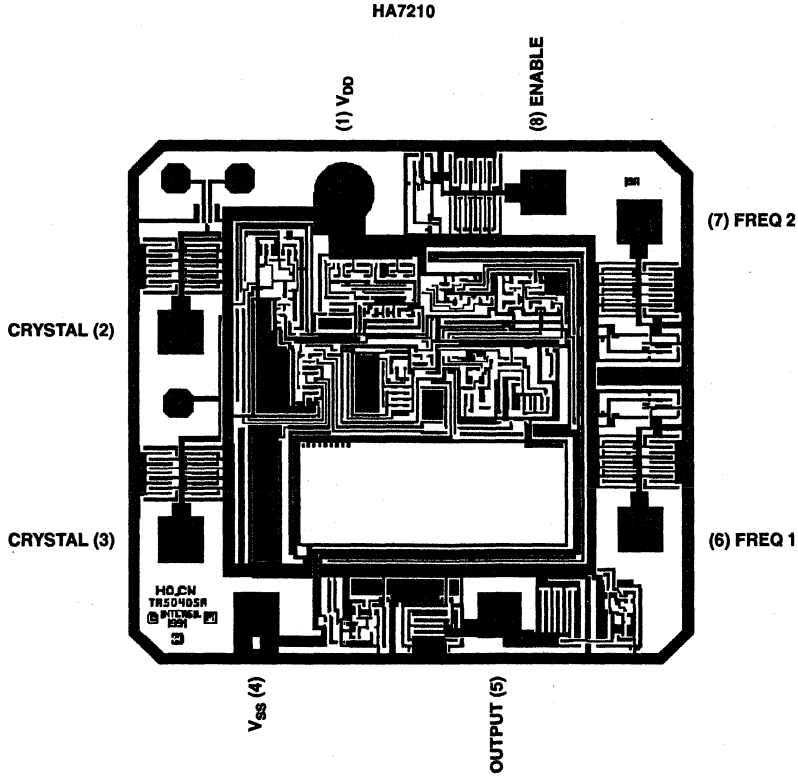
METALLIZATION:
Type: Si - Al
Thickness: 10kÅ ± 1kÅ

GLASSIVATION:
Type: Nitride (Si_3N_4) Over Silox (SiO_2, 3% Phos)
Silox Thickness: 7kÅ ± 1kÅ
Nitride Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Silver Epoxy - Plastic DIP and SOIC

SUBSTRATE POTENTIAL: V_{SS}

Metallization Mask Layout



Typical Performance Curves

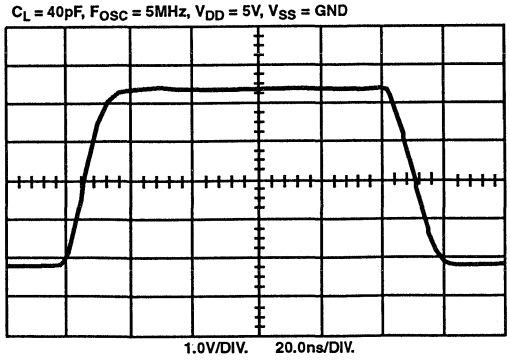


FIGURE 5. OUTPUT WAVEFORM (C_L = 40pF)

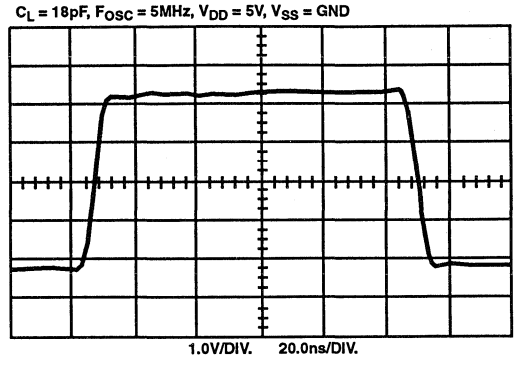


FIGURE 6. OUTPUT WAVEFORM (C_L = 18pF)

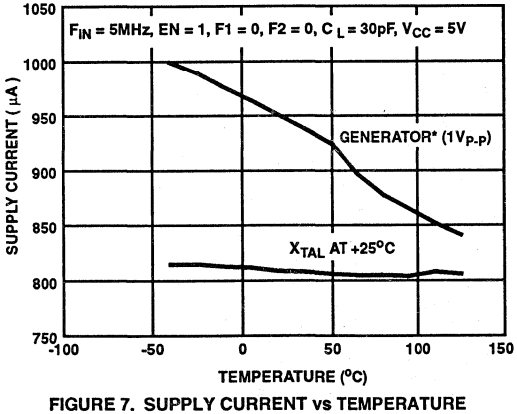


FIGURE 7. SUPPLY CURRENT vs TEMPERATURE

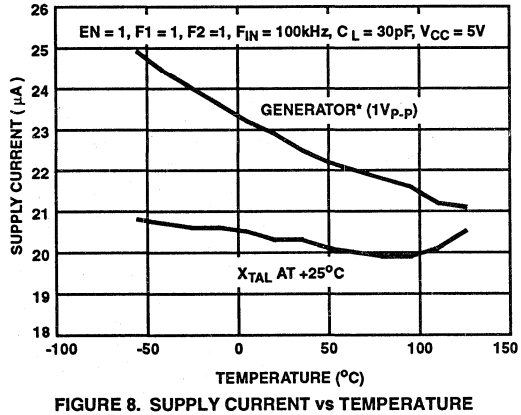


FIGURE 8. SUPPLY CURRENT vs TEMPERATURE

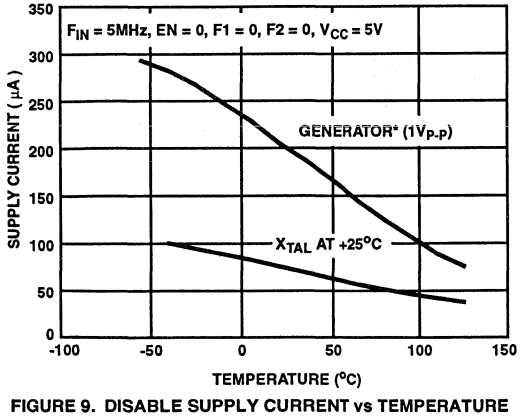


FIGURE 9. DISABLE SUPPLY CURRENT vs TEMPERATURE

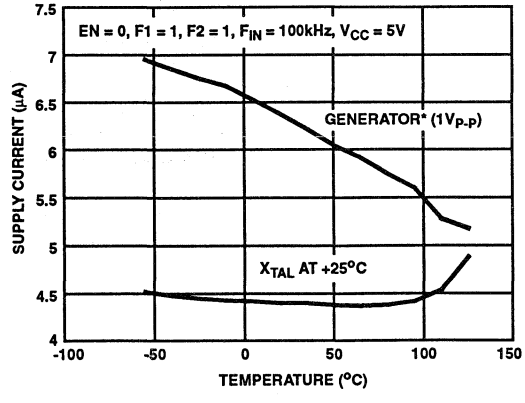


FIGURE 10. DISABLE SUPPLY CURRENT vs TEMPERATURE

* Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

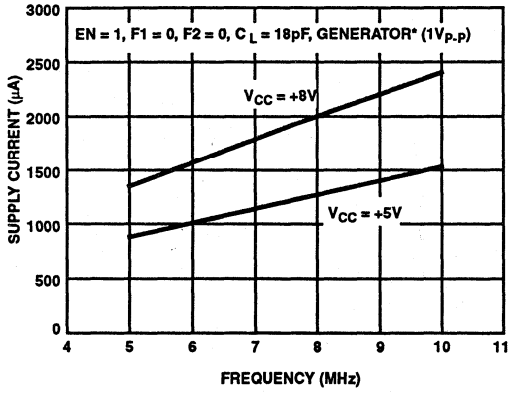


FIGURE 11. SUPPLY CURRENT vs FREQUENCY

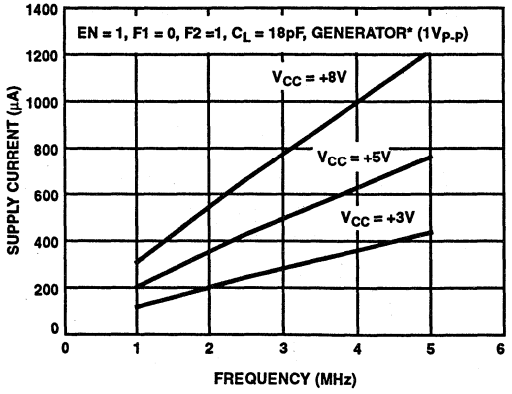


FIGURE 12. SUPPLY CURRENT vs FREQUENCY

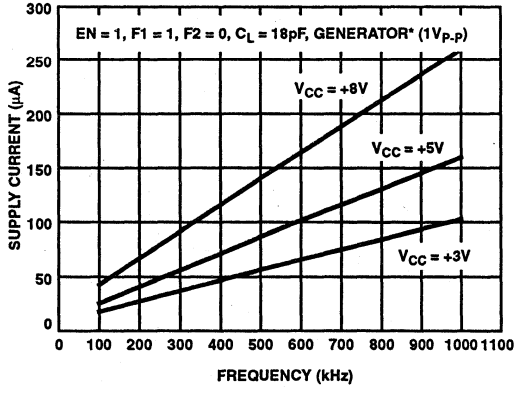


FIGURE 13. SUPPLY CURRENT vs FREQUENCY

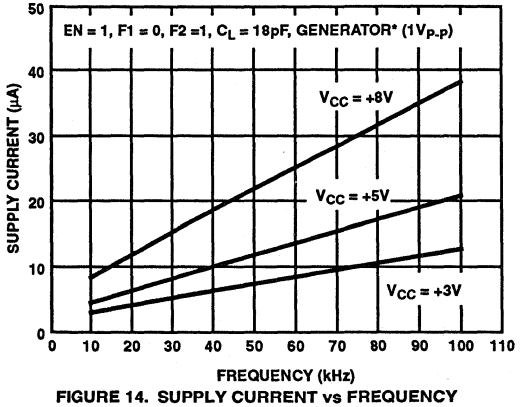


FIGURE 14. SUPPLY CURRENT vs FREQUENCY

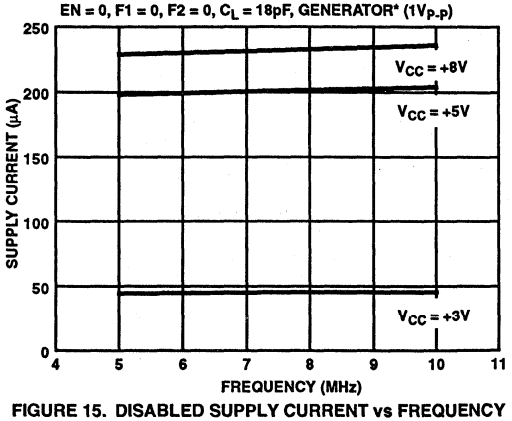


FIGURE 15. DISABLED SUPPLY CURRENT vs FREQUENCY

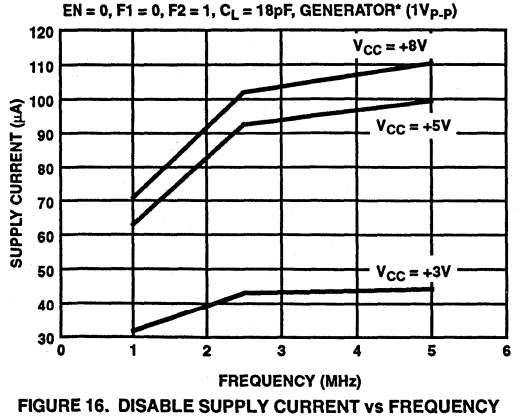


FIGURE 16. DISABLE SUPPLY CURRENT vs FREQUENCY

* Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

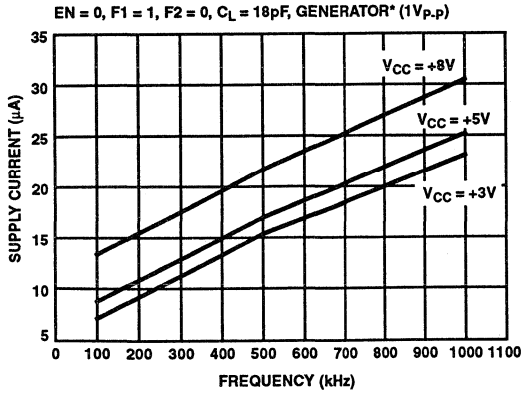


FIGURE 17. DISABLE SUPPLY CURRENT vs FREQUENCY

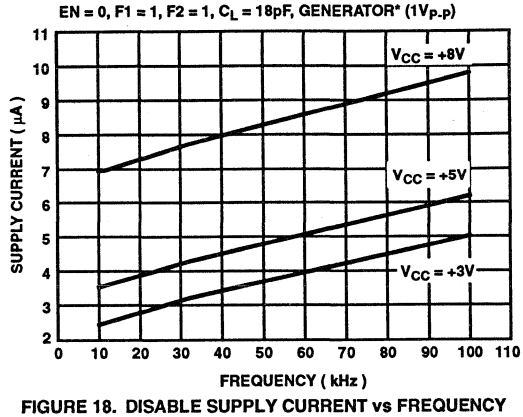


FIGURE 18. DISABLE SUPPLY CURRENT vs FREQUENCY

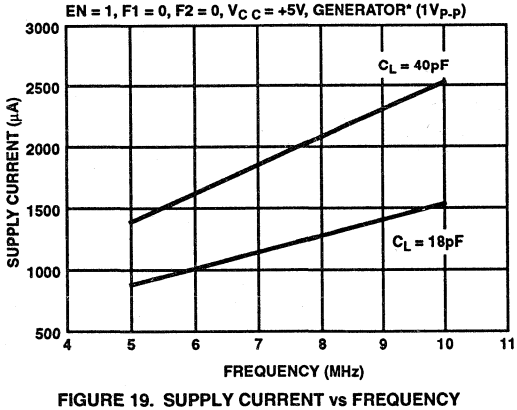


FIGURE 19. SUPPLY CURRENT vs FREQUENCY

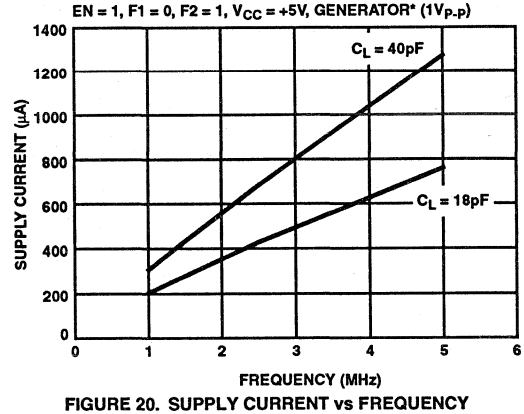


FIGURE 20. SUPPLY CURRENT vs FREQUENCY

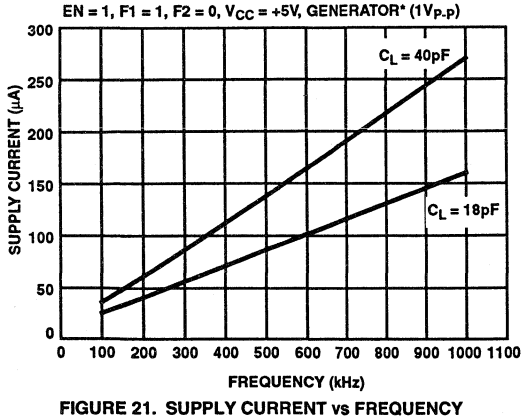


FIGURE 21. SUPPLY CURRENT vs FREQUENCY

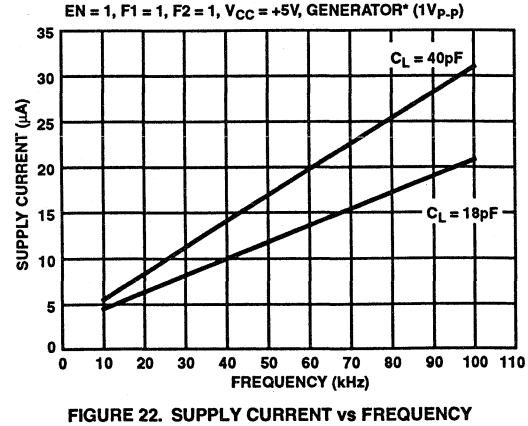


FIGURE 22. SUPPLY CURRENT vs FREQUENCY

* Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

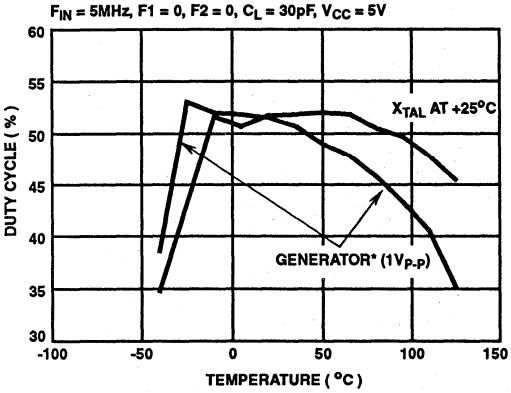


FIGURE 23. DUTY CYCLE vs TEMPERATURE

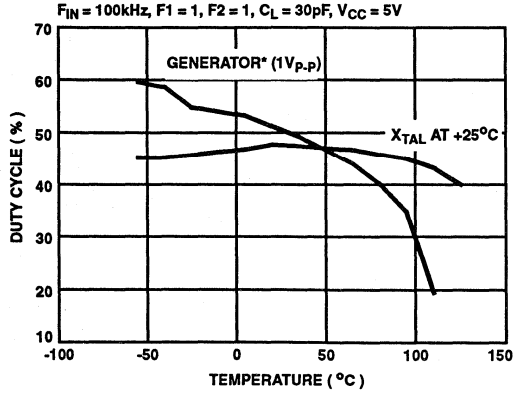


FIGURE 24. DUTY CYCLE vs TEMPERATURE

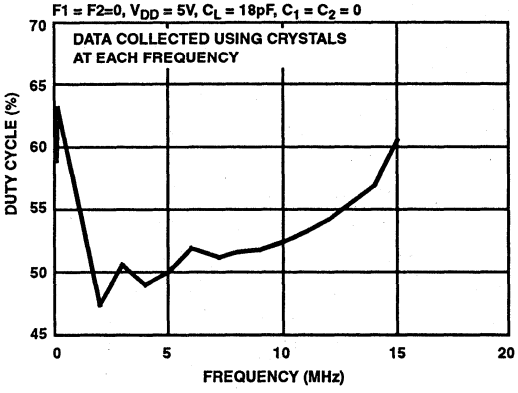


FIGURE 25. DUTY CYCLE vs FREQUENCY

F1 = 0, F2 = 0 RECOMMENDED FOR 5MHz TO 10MHz RANGE

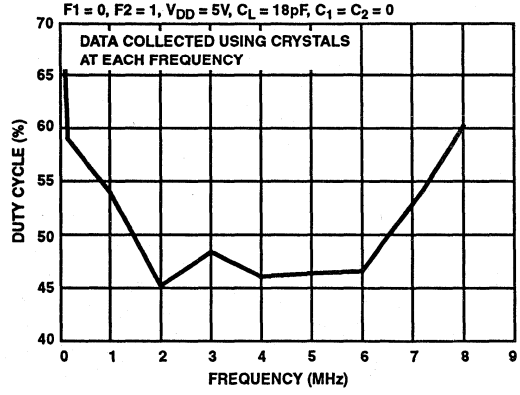


FIGURE 26. DUTY CYCLE vs FREQUENCY

F1 = 0, F2 = 1 RECOMMENDED FOR 1MHz TO 5MHz RANGE

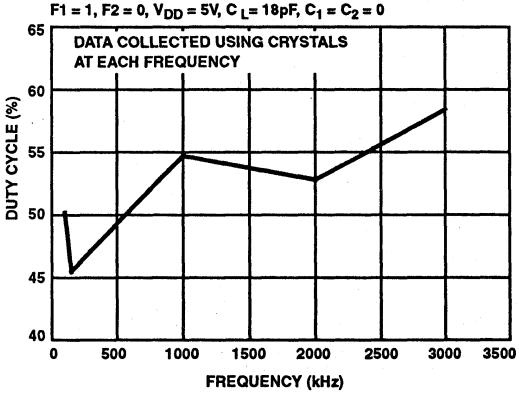


FIGURE 27. DUTY CYCLE vs FREQUENCY

F1 = 0, F2 = 0 RECOMMENDED FOR 100kHz TO 1MHz RANGE

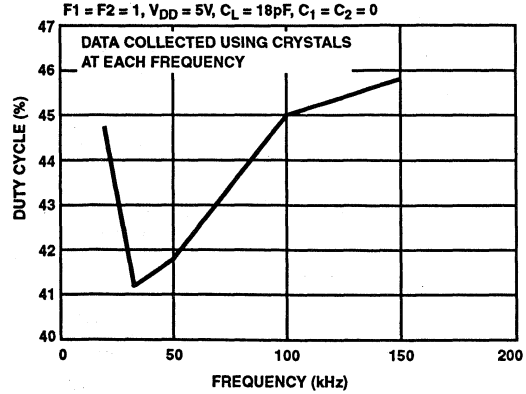


FIGURE 28. DUTY CYCLE vs FREQUENCY

F1 = 1, F2 = 1 RECOMMENDED FOR 10kHz TO 100kHz RANGE

* Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

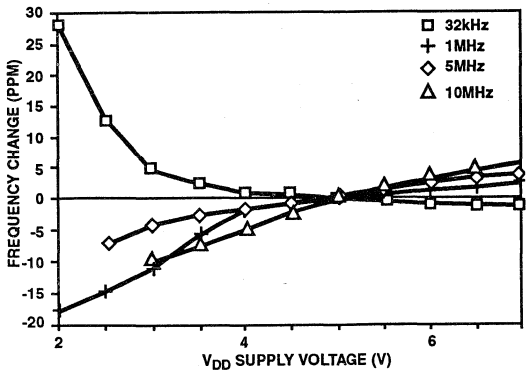


FIGURE 29. FREQUENCY CHANGE vs V_{DD}
Deviation from 5.0V Frequency

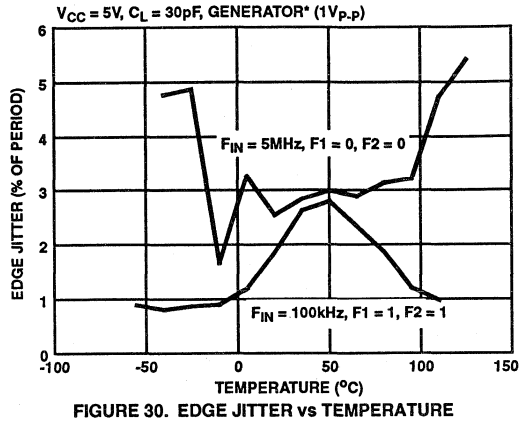


FIGURE 30. EDGE JITTER vs TEMPERATURE

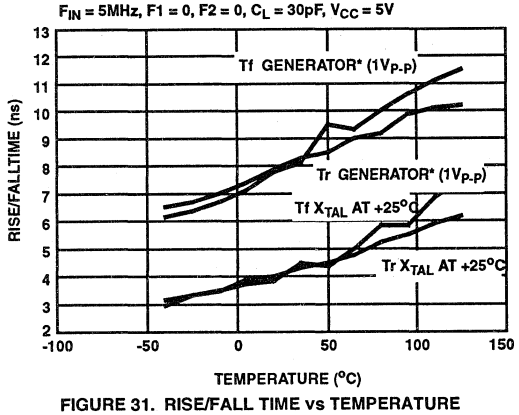


FIGURE 31. RISE/FALL TIME vs TEMPERATURE

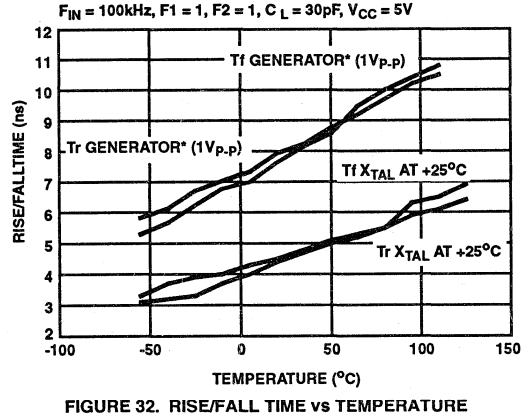


FIGURE 32. RISE/FALL TIME vs TEMPERATURE

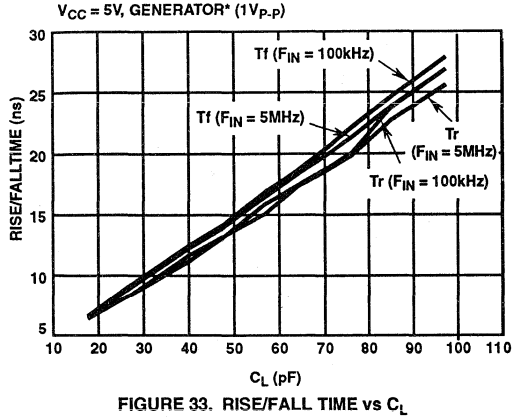


FIGURE 33. RISE/FALL TIME vs C_L

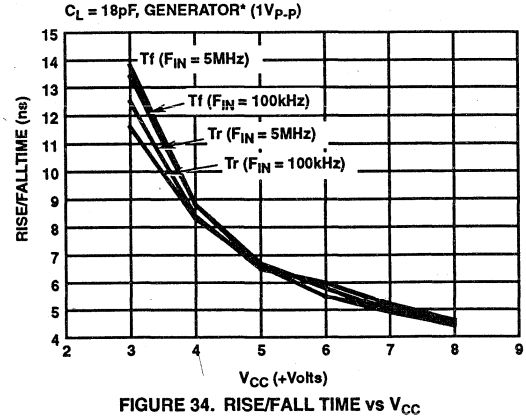


FIGURE 34. RISE/FALL TIME vs V_{CC}

* Refer to Test Circuit (Figure 1).

Typical Performance Curves (Continued)

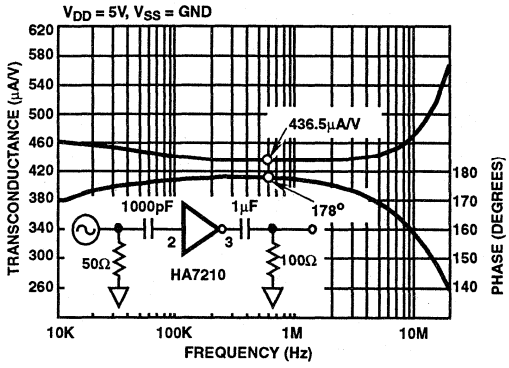


FIGURE 35. TRANSCONDUCTANCE vs FREQUENCY
F1 = 0, F2 = 0

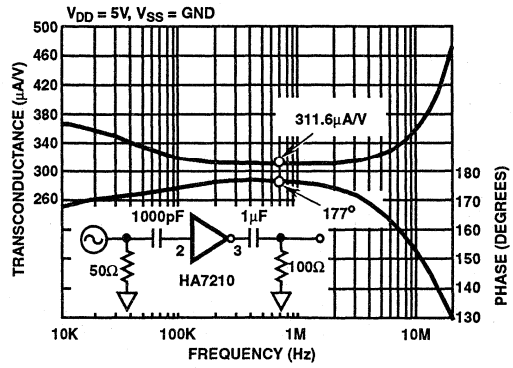


FIGURE 36. TRANSCONDUCTANCE vs FREQUENCY
F1 = 0, F2 = 1

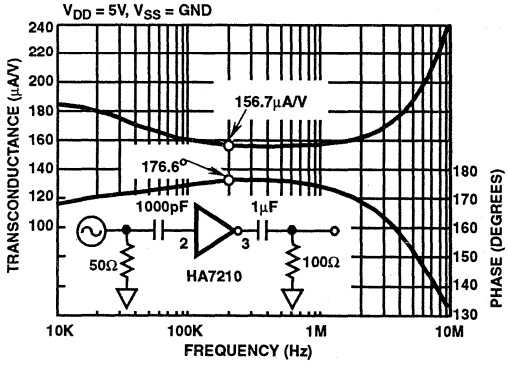


FIGURE 37. TRANSCONDUCTANCE vs FREQUENCY
F1 = 1, F2 = 0

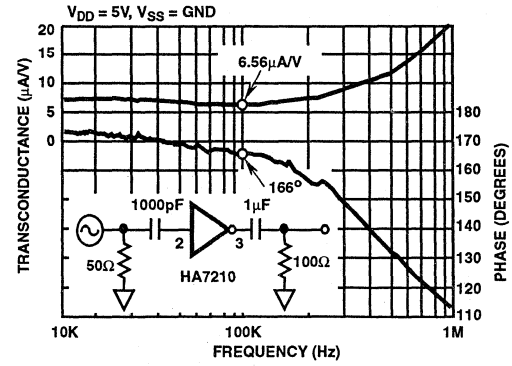


FIGURE 38. TRANSCONDUCTANCE vs FREQUENCY
F1 = 1, F2 = 1

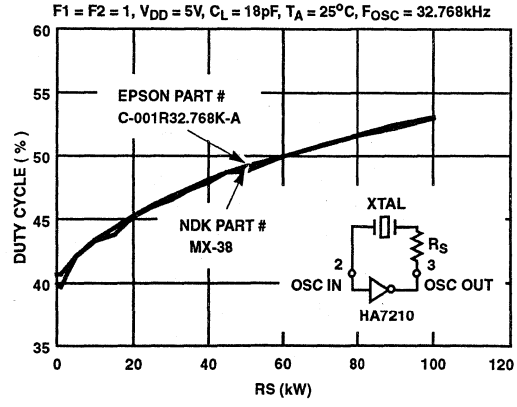


FIGURE 39. DUTY CYCLE vs R_S at 32kHz

NOTE: Figure 39 (Duty Cycle vs R_S at 32kHz) should only be used for 32kHz crystals. R_S may be used at other frequencies to adjust Duty Cycle but experimentation will be required to find an appropriate value. The R_S value will be proportional to the effective series resistance of the crystal being used.

HARRIS SEMICONDUCTOR

ICM7213

One Second/One Minute Timebase Generator

December 1993

Features

- Guaranteed 2V Operation
- Very Low Current Consumption: Typ. 100μA at 3V
- All Outputs TTL compatible
- On Chip Oscillator Feedback Resistor
- Oscillator Requires Only 3 External components: Fixed Capacitor, Trim Capacitor, and A Quartz Crystal
- Output Inhibit Function
- 4 Simultaneous Outputs: One Pulse/Sec, One Pulse/Min, 16Hz and Composite 1024 + 16 + 2Hz Outputs
- Test Speed-Up Provides Other Frequency Outputs

Description

The ICM7213 is a fully integrated micropower oscillator and frequency divider with four buffered outputs suitable for interfacing with most logic families. The power supply may be either a two battery stack (Ni-cad, alkaline, etc.) or a regular power supply greater than 2V. Depending upon the state of the WIDTH, INHIBIT, and TEST inputs, using a 4.194304MHz crystal will produce a variety of output frequencies including 2048Hz, 1024Hz, 34.133Hz, 16Hz, 1Hz, and $^1/_{60}$Hz (plus composites).

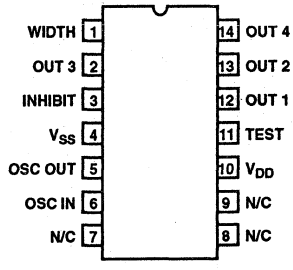
The ICM7213 utilizes a very high speed low power metal gate CMOS technology which uses 6.4V zeners between the drains and sources of each transistor and also across the supply terminals. Consequently, the ICM7213 is limited to a 6V maximum V_{SUPPLY}, although a simple dropping network can be used to extend the V_{SUPPLY} range well above 6V (See Figure 9).

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7213IPD	-25°C to +85°C	14 Lead Plastic DIP

Pinout

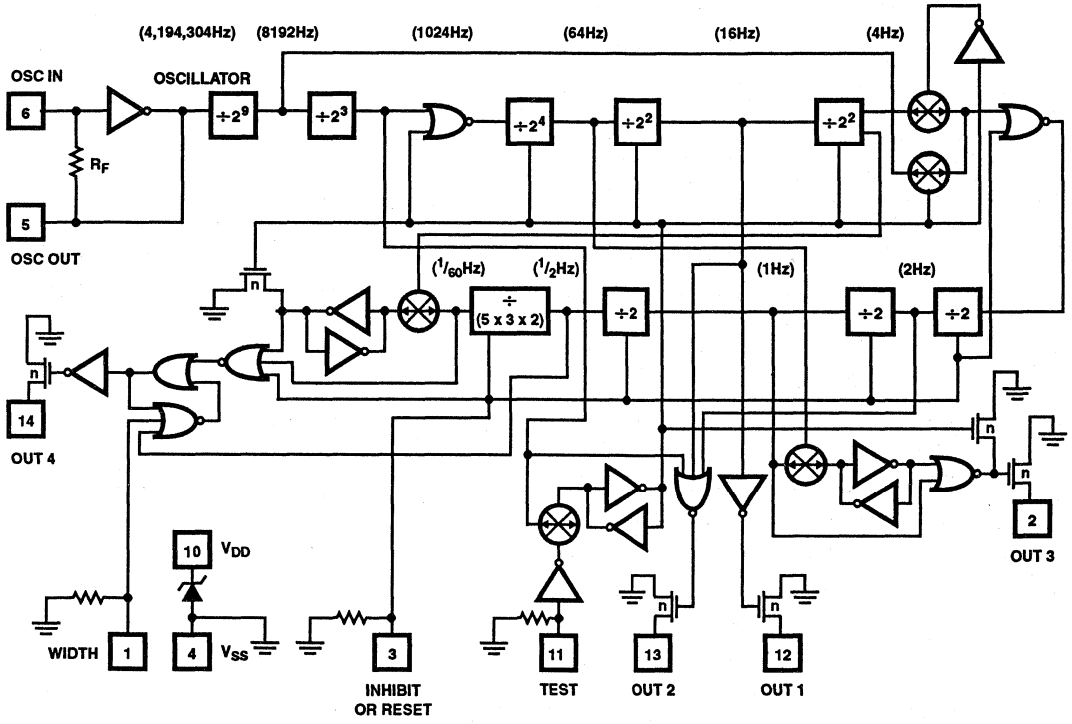
ICM7213
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3165

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) 6.0V
Output Current (Any output) 20mA
All Input and Oscillator Voltages ..... V_{SS} - 0.3V to V_{DD} + 0.3V
All Output Voltages ..... V_{SS} to 6.0V
Operating Temperature Range ..... -25°C to +85°C
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic Package ..... 145°C/W
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} - V_{SS} = 3.0V, f_{OSC} = 4.194304MHz, Test Circuit, T_A = 25°C Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current, I_{DD}		-	100	140	µA
Guaranteed Operating Supply Voltage Range (V_{DD} - V_{SS}), V_{SUPPLY}	-20°C < T_A < +85°C	2	-	4	V
Output Leakage Current, I_{OLK}	Any output, V_{OUT} = 6V	-	-	10	µA
Output Sat. Resistance, R_{OUT}	Any output, I_{OLK} = 2.5mA	-	120	200	Ω
Inhibit Input Current, I_I	Inhibit terminal connected to V_{DD}	-	10	40	µA
Test Point Input Current, I_{TP}	Test point terminal connected to V_{DD}	-	10	40	µA
Width Input Current, I_W	Width terminal connected to V_{DD}	-	10	40	µA
Oscillator Transconductance, g_M	V_{DD} = 2V	100	-	-	µS
Oscillator Frequency Range (Note 1), f_{OSC}		1	-	10	MHz
Oscillator Stability, f_{STAB}	2V < V_{DD} < 4V	-	1.0	-	ppm
Oscillator Start Time, t_S		-	0.1	-	s
	V_{DD} = 2.0V	-	0.2	-	s

NOTE:

1. The ICM7213 uses dynamic dividers for high frequency division. As with any dynamic system, information is stored on very small nodal capacitances instead of latches (static system), therefore there is a lower frequency of operation. Dynamic dividers are used to improve the high frequency performance while at the same time significantly decreasing power consumption. At low V_{SUPPLY}, operation at less than 1MHz is possible.

Output Definitions

(NOTE 1) INPUT STATES			PIN 12 OUT 1	PIN 13 OUT 2	PIN 2 OUT 3	PIN 14 OUT 4
TEST	INHIBIT	WIDTH				
L	L	L	16Hz ÷ 2^{18}	$\overline{1024 + 16 + 2}$Hz (÷ 2^{12} ÷ 2^{18} ÷ 2^{21}) composite	1Hz, 7.8ms ÷ 2^{22}	1/60Hz, 1s ÷ (2^{24} x 3 x 5)
L	L	H	16Hz ÷ 2^{18}	$\overline{1024 + 16 + 2}$Hz (÷ 2^{12} ÷ 2^{18} ÷ 2^{21}) composite	1Hz, 7.8ms ÷ 2^{22}	$^1/_{60}$Hz, 125ms
L	H	L	16Hz ÷ 2^{18}	$\overline{1024 + 16}$Hz (÷ 2^{12} ÷ 2^{18}) composite	OFF	OFF
L	H	H	16Hz ÷ 2^{18}	$\overline{1024 + 16}$Hz (÷ 2^{12} ÷ 2^{18}) composite	OFF	See Waveforms
H	L	L	ON	$\overline{4096 + 1024}$Hz (÷ 2^{10} ÷ 2^{12}) composite	2048Hz ÷ 2^{11}	34.133Hz, 50% D.C. ÷ (2^{13} x 5 x 3)
H	L	H	ON	$\overline{4096 + 1024}$Hz (÷ 2^{10} ÷ 2^{12}) composite	2048Hz ÷ 2^{11}	34.133Hz, 50% D.C. ÷ (2^{13} x 5 x 3)
H	H	L	ON	1024Hz ÷ 2^{12}	ON	OFF
H	H	H	ON	1024Hz ÷ 2^{12}	ON	OFF

NOTE:

1. When TEST and RESET are connected to ground, or left open, all outputs except for OUT 3 and OUT 4 have a 50% duty cycle.

Timing Waveforms

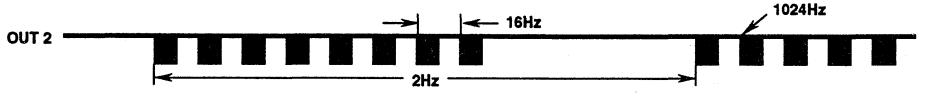


FIGURE 1. OUTPUT WAVEFORM

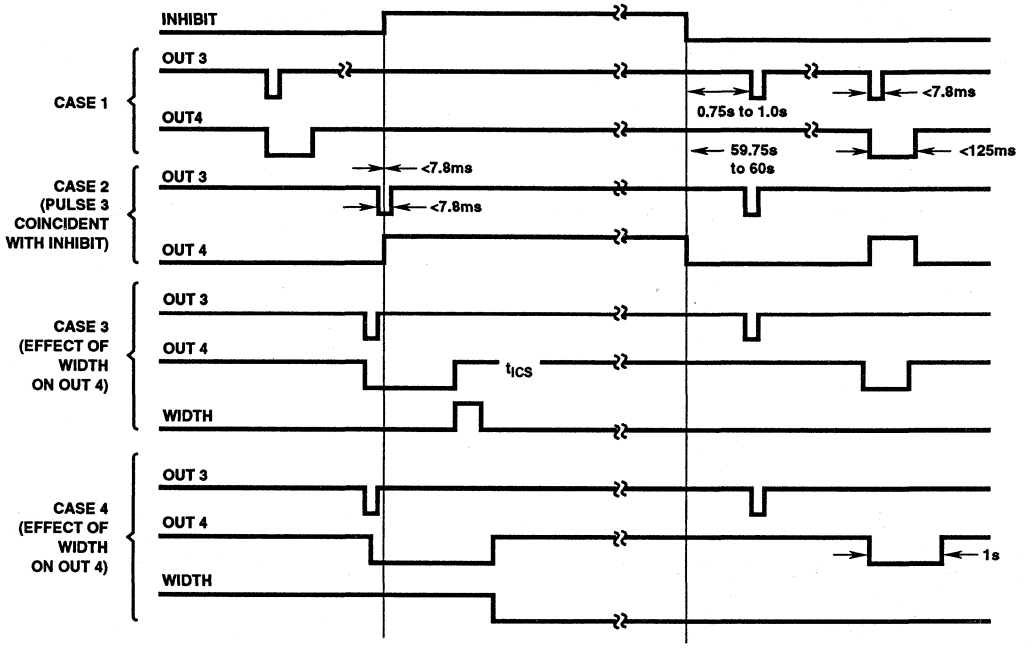


FIGURE 2. EFFECT OF THE INHIBIT (TEST CONNECTED TO V_{SS} OR LEFT OPEN)

Typical Performance Curves

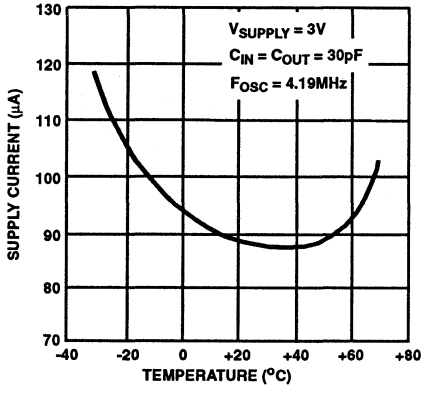


FIGURE 3. SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

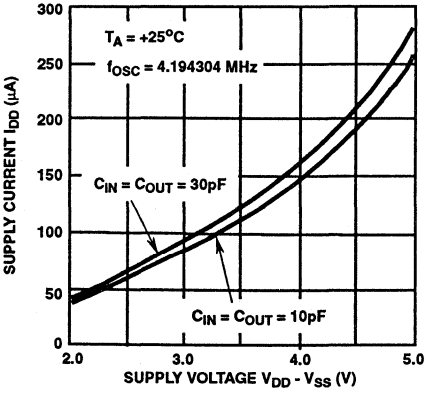


FIGURE 4. SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

Typical Performance Curves

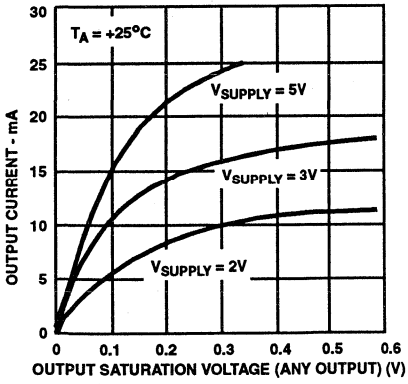


FIGURE 5. OUTPUT CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE

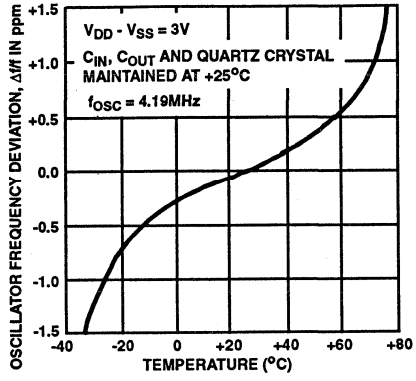


FIGURE 6. OSCILLATOR STABILITY AS A FUNCTION OF DEVICE TEMPERATURE

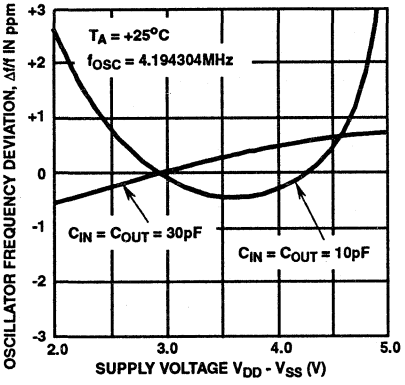


FIGURE 7. OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE

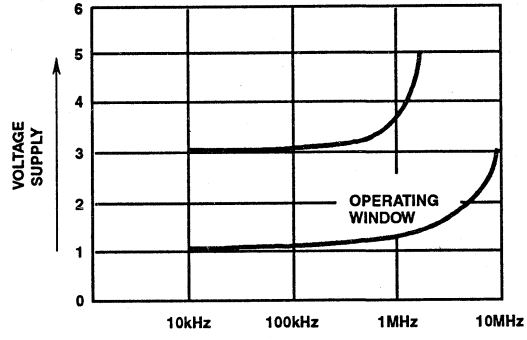
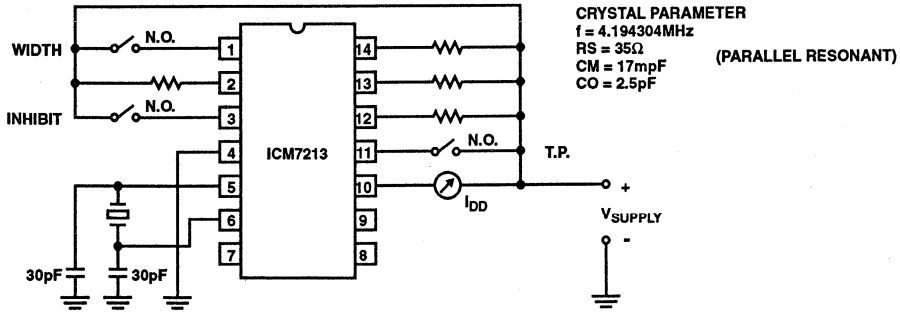


FIGURE 8. WINDOW OF CORRECT OPERATION

Test Circuit



CRYSTAL PARAMETER
f = 4.194304MHz
RS = 35Ω
CM = 17mpF
CO = 2.5pF
(PARALLEL RESONANT)

Detailed Description

Supply Voltage Considerations

The ICM7213 may be used to provide various precision outputs with frequencies from 2048Hz to $^1/_{60}$Hz using a 4.194304MHz quartz oscillator, and other output frequencies may be obtained using other quartz crystal frequencies. Since the ICM7213 uses dynamic high frequency dividers for the initial frequency division there are limitations on the V_{SUPPLY} range depending on the oscillator frequency. If, for example, a low frequency quartz crystal is selected, the V_{SUPPLY} should be selected in the center of the operating window, or approximately 1.7V.

The V_{SUPPLY} to the ICM7213 may be derived from a high voltage supply by using a simple resistor divider (if power is of no concern), by using a series resistor for minimum current consumption, or by means of a regulator.

Outputs

Pull up resistors will generally be required to interface with other logic families. These resistors must be connected between the various outputs and the positive power supply.

Oscillator Considerations

The oscillator consists of a CMOS inverter and a feedback resistor whose value is dependent on the voltage at the oscillator input and output terminals and the V_{SUPPLY}. Oscillator stabilities of approximately 0.1ppm per 0.1V variation are achievable with a nominal V_{SUPPLY} of 5V and a single voltage dropping resistor. The crystal specifications are shown in the Test Circuit.

It is recommended that the crystal load capacitance (CL) be no greater than 22pF for a crystal having a series resistance equal to or less than 75Ω, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

It a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10ppm, a low series resistance (less than 25Ω), a low motional capacitance of 5mpF and a load capacitance of 20pF. The fixed capacitor C_{IN} should be 30pF and the oscillator tuning capacitor should range between approximately 16pF and 60pF.

Use of a high quality crystal will result in typical stabilities of 0.05ppm per 0.1V change of V_{SUPPLY}.

Control Inputs

The TEST input inhibits the 2^{18} output and applies the 2^9 output to the 2^{21} divider, thereby permitting a speedup of the testing of the ÷ 60 section by a factor of 2048 times. This also results in alternative output frequencies (see table).

The WIDTH input may be used to change the pulse width of OUT 4 from 125ms to 1s, or to change the state of OUT 4 from ON to OFF during INHIBIT.

See Figures 1 and 2 for output waveforms and effect of control inputs.

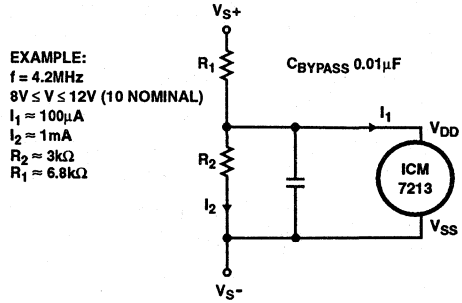


FIGURE 9A.

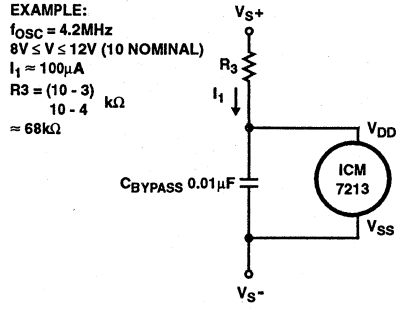


FIGURE 9B.

FIGURE 9. BIASING SCHEMES WITH HIGH VOLTAGE SUPPLIES

HARRIS SEMICONDUCTOR

ICM7216A, ICM7216B ICM7216D

8-Digit Multi-Function Frequency Counter/Timer

December 1993

Features All Versions

- Functions as a Frequency Counter (DC to 10MHz)
- Four Internal Gate Times: 0.01s, 0.1s, 1s, 10s in Frequency Counter Mode
- Directly Drives Digits and Segments of Large Multiplexed LED Displays (Common Anode and Common Cathode Versions)
- Single Nominal 5V Supply Required
- Highly Stable Oscillator, Uses 1MHz or 10MHz Crystal
- Internally Generated Decimal Points, Interdigit Blanking, Leading Zero Blanking and Overflow Indication
- Display Off Mode Turns Off Display and Puts Chip into Low Power Mode
- Hold and Reset Inputs for Additional Flexibility

Features ICM7216A and ICM7216B

- Functions Also as a Period Counter, Unit Counter, Frequency Ratio Counter or Time Interval Counter
- 1 Cycle, 10 Cycles, 100 Cycles, 1000 Cycles in Period, Frequency Ratio and Time Interval Modes
- Measures Period From 0.5μs to 10s

Features ICM7216D

- Decimal Point and Leading Zero Banking May Be Externally Selected

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7216AIJI	-25°C to +85°C	28 Lead Ceramic DIP
ICM7216BIPI	-25°C to +85°C	28 Lead Plastic DIP
ICM7216DIPI	-25°C to +85°C	28 Lead Plastic DIP

The ICM7216A and ICM7216B are fully integrated Timer Counters with LED display drivers. They combine a high frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexers and 8 segment and 8 digit drivers which directly drive large multiplexed LED displays. The counter inputs have a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7216A and ICM7216B can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10MHz or 1MHz quartz crystal timebase. For period and time interval, the 10MHz timebase gives a 0.1μs resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01s, 0.1s, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1Hz in the least significant digit. There is 0.2s between measurements in all ranges.

The ICM7216D functions as a frequency counter only, as described above.

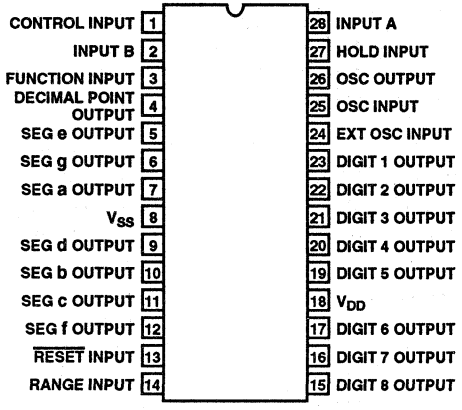
All versions of the ICM7216 incorporate leading zero blanking. Frequency is displayed in kHz. In the ICM7216A and ICM7216B, time is displayed in μs. The display is multiplexed at 500Hz with a 12.2% duty cycle for each digit. The ICM7216A is designed for common anode displays with typical peak segment currents of 25mA. The ICM7216B and ICM7216D are designed for common cathode displays with typical peak segment currents of 12mA. In the display off mode, both digit and segment drivers are turned off, enabling the display to be used for other functions.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

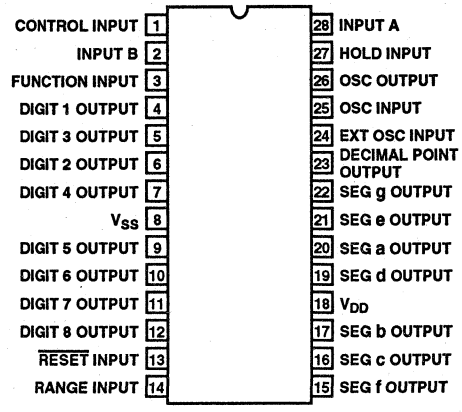
File Number 3166

Pinouts

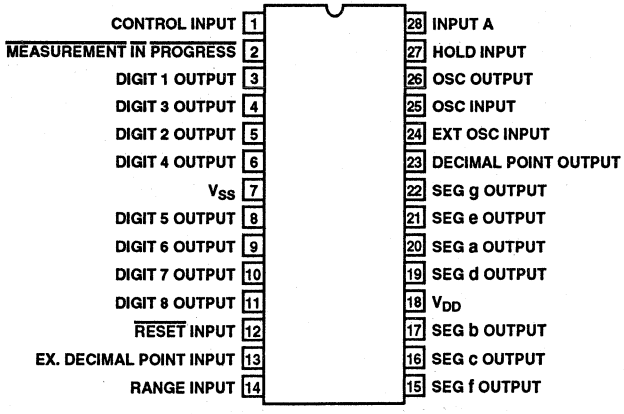
ICM7216A
COMMON ANODE
(CDIP)
TOP VIEW



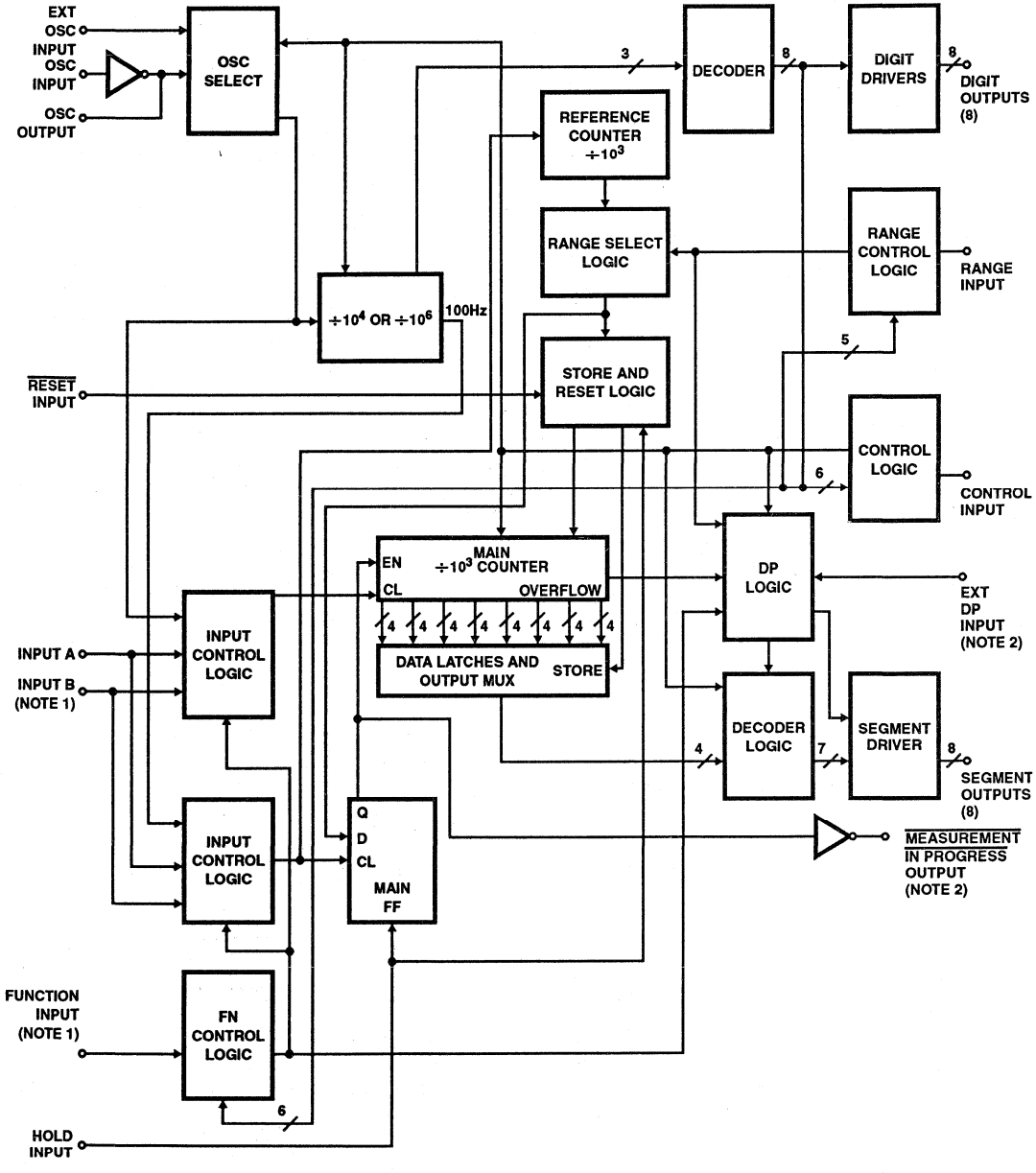
ICM7216B
COMMON CATHODE
(PDIP)
TOP VIEW



ICM7216D
COMMON CATHODE
(PDIP)
TOP VIEW



Functional Block Diagram



NOTES:

1. Function input and input B available on ICM7216A/B only.
2. Ext DP input and $\overline{\text{MEASUREMENT IN PROGRESS}}$ output available on ICM7216D only.

Absolute Maximum Ratings

Maximum Supply Voltage (V_{DD} - V_{SS}) 6.5V
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
Voltage On Any Input or
Output Terminal (Note 1) ..... (V_{DD} +0.3V) to (V_{SS} -0.3V)
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	55°C/W	20°C/W
Plastic DIP Package	55°C/W	-

Junction Temperature
Ceramic Packages ..... +175°C
Plastic Packages ..... +150°C
Operating Temperature Range ..... -25°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = 5.0V, V_{SS} = 0V, T_A = +25°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ICM7216A/B					
Operating Supply Current, I_{DD}	Display Off, Unused Inputs to V_{SS}	-	2	5	mA
Supply Voltage Range (V_{DD} -V_{SS}), V_{SUPPLY}	INPUT A, INPUT B Frequency at f_{MAX}	4.75	-	6.0	V
Maximum Frequency INPUT A, Pin 28, $f_{A(MAX)}$	Figure 9, Function = Frequency, Ratio, Unit Counter	10	-	-	MHz
	Function = Period, Time Interval	2.5	-	-	MHz
Maximum Frequency INPUT B, Pin 2, $f_{B(MAX)}$	Figure 10	2.5	-	-	MHz
Minimum Separation INPUT A to INPUT B Time Interval Function	Figure 1	250	-	-	ns
Maximum Oscillator Frequency and External Oscillator Frequency, f_{OSC}		10	-	-	MHz
Minimum External Oscillator Frequency, f_{OSC}		-	-	100	kHz
Oscillator Transconductance, g_M	V_{DD} = 4.75V, T_A = +85°C	2000	-	-	µS
Multiplex Frequency, f_{MUX}	f_{OSC} = 10MHz	-	500	-	Hz
Time Between Measurements	f_{OSC} = 10MHz	-	200	-	ms
Input Voltages: Pins 2, 13, 25, 27, 28					
Input Low Voltage, V_{INL}		-	-	1.0	V
Input High Voltage, V_{INH}		3.5	-	-	V
Input Resistance to V_{DD} Pins 13, 24, R_{IN}	V_{IN} = V_{DD} -1.0V	100	400	-	kΩ
Input Leakage Pin 27,28,2, I_{ILK}		-	-	20	µA
Input Range of Change, dV_{IN}/dt	Supplies Well Bypassed	-	15	-	mV/µs
ICM7216A					
Digit Driver: Pins 15, 16, 17, 19, 20, 21, 22, 23					
High Output Current, I_{OH}	V_{OUT} = V_{DD} -2.0V	-140	-180	-	mA
Low Output Current, I_{OL}	V_{OUT} = V_{SS} +1.0V	-	0.3	-	mA
Segment Driver: Pins 4, 5, 6, 7, 9,10, 11, 12					
Low Output Current, I_{OL}	V_{OUT} = V_{SS} +1.5V	20	35	-	mA
High Output Current, I_{OH}	V_{OUT} = V_{DD} -2.5V		-100	-	µA
Multiplex Inputs: Pins 1,3,14					
Input Low Voltage, V_{INL}		-	-	0.8	V
Input High Voltage, V_{INH}		2.0	-	-	V
Input Resistance to V_{SS}, R_{IN}	V_{IN} = V_{SS} +1.0V	50	100	-	kΩ

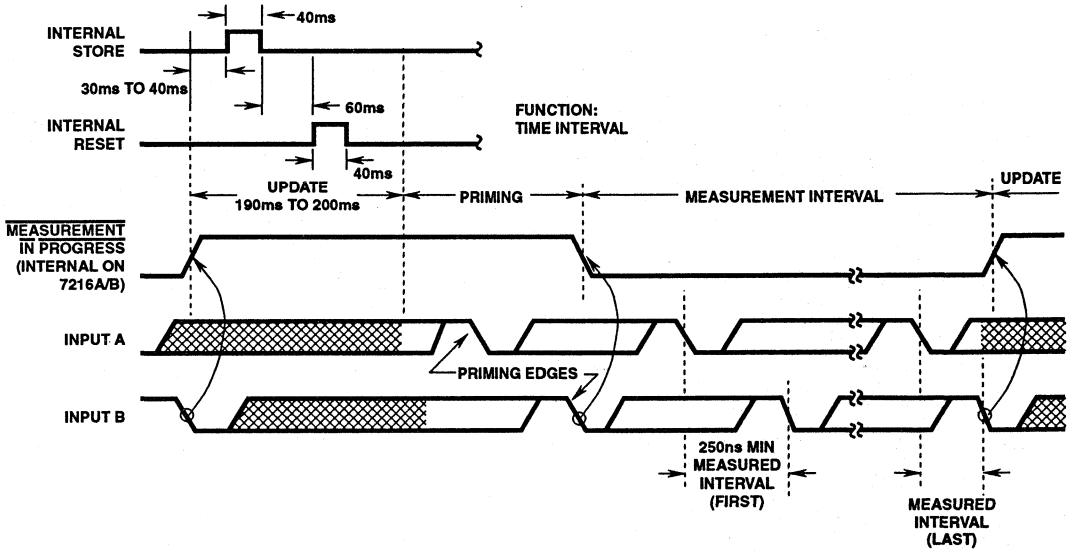
Electrical Specifications V_{DD} = 5.0V, V_{SS} = 0V, T_A = +25°C, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
ICM7216B					
Digit Driver: Pins 4, 5, 6, 7, 9, 10, 11, 12					
Low Output Current, I_{OL}	$V_{OUT} = V_{SS}$ +1.3V	50	75	-	mA
High Output Current, I_{OH}	$V_{OUT} = V_{DD}$ -2.5V	-	-100	-	µA
Segment Driver: Pins 15, 16, 17, 19, 20, 21, 22, 23					
High Output Current, I_{OH}	$V_{OUT} = V_{DD}$ -2.0V	-10	-	-	mA
Leakage Current, I_{SLK}	$V_{OUT} = V_{DD}$ -2.5V	-	-	10	µA
Multiplex Inputs: Pins 1, 3, 14					
Input Low Voltage, V_{INL}		-	-	V_{DD} -2.0	V
Input High Voltage, V_{INH}		V_{DD} -0.8	-	-	V
Input Resistance to V_{DD}, R_{IN}	$V_{IN} = V_{DD}$ -2.5V	100	360	-	kΩ
ICM7216D					
Operating Supply Current, I_{DD}	Display Off, Unused Inputs to V_{SS}	-	2	5	mA
Supply Voltage Range (V_{DD} -V_{SS}), V_{SUPPLY}	INPUT A Frequency at f_{MAX}	4.75	-	6.0	V
Maximum Frequency INPUT A, Pin 28, $f_{A(MAX)}$	Figure 9	10	-	-	MHz
Maximum Oscillator Frequency and External Oscillator Frequency, f_{OSC}		10	-	-	MHz
Minimum External Oscillator Frequency, f_{OSC}		-	-	100	kHz
Oscillator Transconductance, g_M	V_{DD} = 4.75V, T_A = +85°C	2000	-	-	µS
Multiplex Frequency, f_{MUX}	f_{OSC} = 10MHz	-	500	-	Hz
Time Between Measurements	f_{OSC} = 10MHz	-	200	-	ms
Input Voltages: Pins 12, 27, 28					
Input Low Voltage, V_{INL}		-	-	1.0	V
Input High Voltage, V_{INH}		3.5	-	-	V
Input Resistance to V_{DD} Pins 12, 24, R_{IN}	$V_{IN} = V_{DD}$ -1.0V	100	400	-	kΩ
Input Leakage, Pins 27, 28, I_{ILK}		-	-	20	µA
Output Current, Pin 2, I_{OL}	V_{OL} = +0.4V	0.36	-	-	mA
Output Current, Pin 2, I_{OH}	$V_{OH} = V_{DD}$ -0.8V	265	-	-	µA
Input Rate of Change, dV_{IN}/dt	Supplies Well Bypassed	-	15	-	mV/µs
Digit Driver: Pins 3, 4, 5, 6, 8, 9, 10, 11					
Low Output Current, I_{OL}	V_{OUT} = +1.3V	50	75	-	mA
High Output Current, I_{OH}	$V_{OUT} = V_{DD}$ -2.5V	-	100	-	µA
Segment Driver: Pins 15, 16, 17, 19, 20, 21, 22, 23					
High Output Current, I_{OH}	$V_{OUT} = V_{DD}$ -2.0V	10	15		mA
Leakage Current, I_{SLK}	$V_{OUT} = V_{DD}$ -2.5V	-	-	10	µA
Multiplex Inputs: Pins 1, 13, 14					
Input Low Voltage, V_{INL}		-	-	V_{DD} -2.0	V
Input High Voltage, V_{INH}		V_{DD} -0.8	-	-	V
Input Resistance to V_{DD}, R_{IN}	$V_{IN} = V_{DD}$ -1.0V	100	360	-	kΩ

NOTE:

1. The ICM7216 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V_{DD} to V_{SS} by more than 0.3V.

Timing Diagram



NOTE:

1. If range is set to 1 event, first and last measured interval will coincide.

FIGURE 1. WAVEFORMS FOR TIME INTERVAL MEASUREMENT (OTHERS ARE SIMILAR, BUT WITHOUT PRIMING PHASE)

Typical Performance Curves

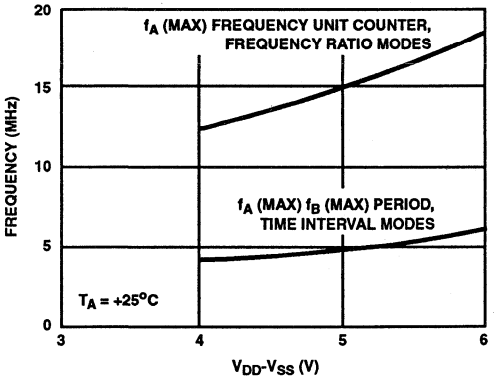


FIGURE 2. f_A(MAX), f_B(MAX) AS A FUNCTION OF SUPPLY

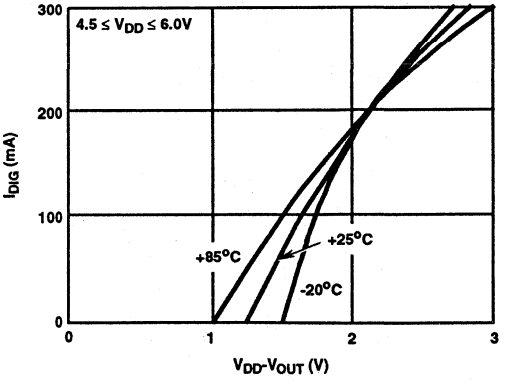


FIGURE 3. ICM7216A TYPICAL I_{DIG} vs V_{DD}-V_{OUT}

Typical Performance Curves (Continued)

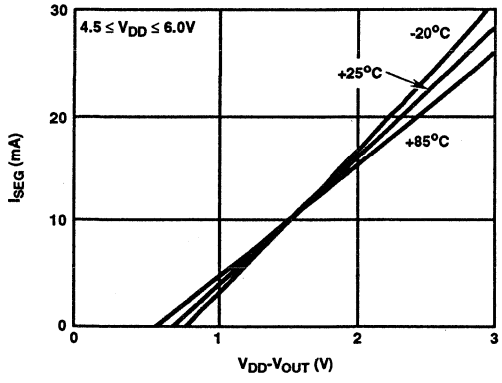


FIGURE 4. ICM7216B & ICM7216D TYPICAL I_{SEG} vs V_{DD}-V_{OUT}

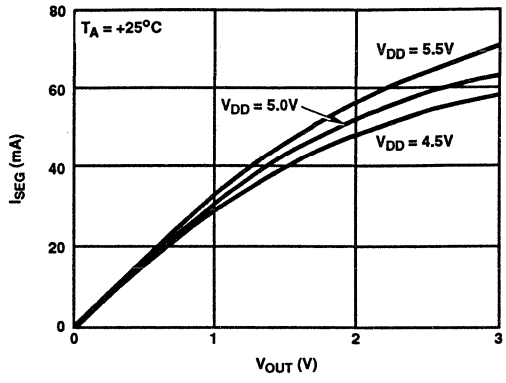


FIGURE 5. ICM7216A TYPICAL I_{SEG} vs V_{OUT}

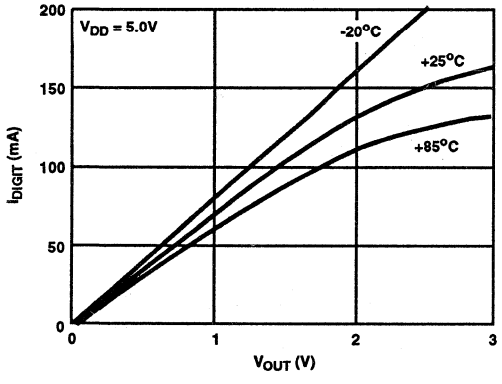


FIGURE 6. ICM7216B & ICM7216D TYPICAL I_{DIGIT} vs V_{OUT}

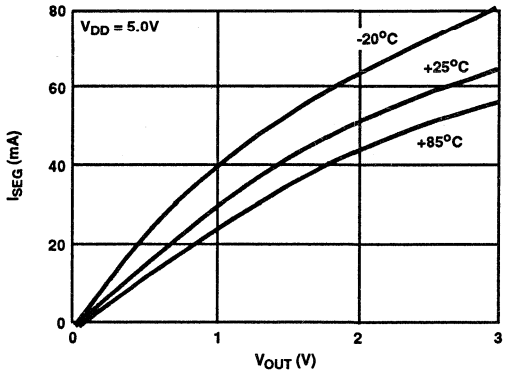


FIGURE 7. ICM7216A TYPICAL I_{SEG} vs V_{OUT}

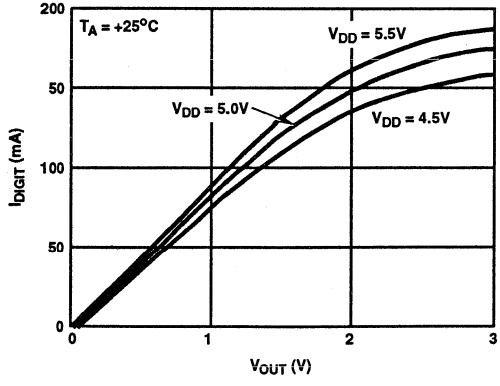


FIGURE 8. ICM7216B & ICM7216D TYPICAL I_{DIGIT} vs V_{OUT}

Description

INPUTS A and B

INPUTS A and B are digital inputs with a typical switching threshold of 2.0V at V_{DD} = 5.0V. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs. (INPUT B is available only on ICM7216A and ICM7216B).

Note that the amplitude of the input should not exceed the device supply (above the V_{DD} and below the V_{SS}) by more than 0.3V, otherwise the device may be damaged.

Multiplexed Inputs

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the function desired. This is achieved by connecting the appropriate Digit driver output to the inputs. The function, range and control inputs must be stable during the last half of each digit output, (typically 125µs). The multiplexed inputs are active high for the common anode ICM7216A and active low for the common cathode ICM7216B and ICM7216D.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplexed inputs as shown in the application circuits.

Table 1 shows the functions selected by each digit for these inputs.

TABLE 1. MULTIPLEXED INPUT FUNCTIONS

	FUNCTION	DIGIT
FUNCTION INPUT (Pin 3, ICM7216A and B Only)	Frequency	D1
	Period	D8
	Frequency Ratio	D2
	Time Interval	D5
	Unit Counter	D4
	Oscillator Frequency	D3
RANGE INPUT, Pin 14	0.01s/1 Cycle	D1
	0.1s/10 Cycles	D2
	1s/100 Cycles	D3
	10s/1K Cycles	D4
CONTROL INPUT, Pin 1	Display Off	D4 and Hold
	Display Test	D8
	1MHz Select	D2
	External Oscillator Enable	D1
	External Decimal Point Enable	D3
External DP INPUT (Pin 13, ICM7216D Only)	Decimal point is output for same digit that is connected to this input.	

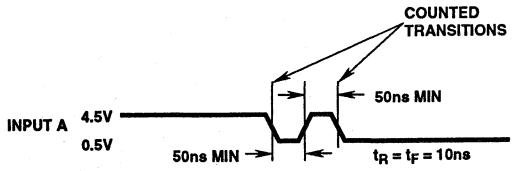


FIGURE 9. WAVEFORM FOR GUARANTEED MINIMUM f_A(MAX) FUNCTION = FREQUENCY, FREQUENCY RATIO, UNIT COUNTER

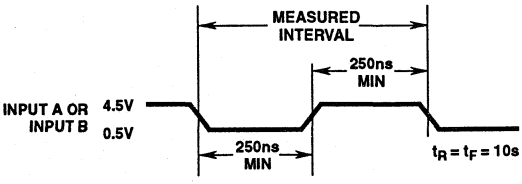


FIGURE 10. WAVEFORM FOR GUARANTEED MINIMUM f_B(MAX) AND f_A(MAX) FOR FUNCTION = PERIOD AND TIME INTERVAL

Function Input

The six functions that can be selected are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio** and **Oscillator Frequency.** This input is available on the ICM7216A and ICM7216B only.

The implementation of different functions is done by routing the different signals to two counters, called "Main Counter" and "Reference Counter". A simplified block diagram of the device for functions realization is shown in Figure 11. Table 2 shows which signals will be routed to each counter in different cases. The output of the Main Counter is the information which goes to the display. The Reference Counter divides its input by 1, 10, 100 and 1000. One of these outputs will be selected through the range selector and drive the enable input of the Main Counter. This means that the Reference Counter, along with its' associated blocks, directs the Main Counter to begin counting and determines the length of the counting period. Note that Figure 11 does not show the complete functional diagram (See the Functional Block Diagram). After the end of each counting period, the output of the Main Counter will be latched and displayed, then the counter will be reset and a new measurement cycle will begin. Any change in the FUNCTION INPUT will stop the present measurement without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION INPUT is changed. In all cases, the 1-0 transitions are counted or timed.

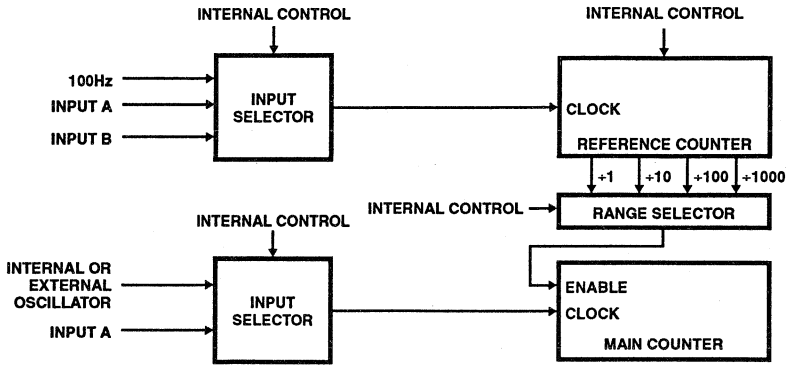


FIGURE 11. SIMPLIFIED BLOCK DIAGRAM OF FUNCTIONS IMPLEMENTATION

TABLE 2. 7216A/B INPUT ROUTING

FUNCTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (f_A)	Input A	100Hz (Oscillator $\div 10^5$ or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A→B)	Oscillator	Input A Input B
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{OSC})	Oscillator	100Hz (Oscillator $\div 10^5$ or 10^4)

Frequency - In this mode input A is counted by the Main Counter for a precise period of time. This time is determined by the time base oscillator and the selected range. For the 10MHz (or 1MHz) time base, the resolutions are 100Hz, 10Hz, 1Hz and 0.1Hz. The decimal point on the display is set for kHz reading.

Period - In this mode, the timebase oscillator is counted by the Main Counter for the duration of 1,10,100 or 1000 (range selected) periods of the signal at input A. A 10MHz timebase gives resolutions of 0.1µs to 0.0001µs for 1000 periods averaging. Note that the maximum input frequency for period measurement is 2.5MHz.

Frequency Ratio - In this mode, the input A is counted by the Main Counter for the duration of 1,10,100 or 1000 (range selected) periods of the signal at input B. The frequency at input A should be higher than input B for meaningful result. The result in this case is unitless and its resolution can go up to 3 digits after decimal point.

Time Interval - In this mode, the timebase oscillator is counted by the Main Counter for the duration of a 1-0 transition of input A until a 1-0 transition of input B. This means input A starts the counting and input B stops it. If other ranges, except 0.01s/1 cycle are selected the sequence of input A and B transitions must happen 10,100 or 1000 times until the display becomes updated; note this when measuring long time intervals to give enough time for measurement completion. The resolution in this mode is the same as for period measurement. See the Time Interval Measurement section also.

Unit Counter - In this mode, the Main Counter is always enabled. The input A is counted by the Main Counter and displayed continuously.

Oscillator Frequency - In this mode, the device makes a frequency measurement on its timebase. This is a self test mode for device functionality check. For 10MHz timebase the display will show 10000.0, 10000.00, 10000.000 and Overflow in different ranges.

Range Input

The RANGE INPUT selects whether the measurement period is made for 1,10,100 or 1000 counts of the Reference Counter. As it is shown in Table 1, this gives different counting windows for frequency measurement and various cycles for other modes of measurement.

In all functional modes except Unit Counter, any change in the RANGE INPUT will stop the present measurement without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the RANGE INPUT is changed.

Control Input

Unlike the other multiplexed inputs, to which only one of the digit outputs can be connected at a time, this input can be tied to different digit lines to select combination of controls. In this case, isolation diodes must be used in digit lines to avoid crosstalk between them (see Figure 17). The direction of diodes depends on the device version, common anode or common cathode. For maximum noise immunity at this input, in addition to the 10K resistor which was mentioned before, a 39pF to 100pF capacitor should also be placed between this input and the V_{DD} or V_{SS} (See Figure 17).

Display Off - To disable the display drivers, it is necessary to tie the D4 line to the CONTROL INPUT and have the HOLD input at V_{DD}. While in Display Off mode, the segments and

digit drivers are all off, leaving the display lines floating, so the display can be shared with other devices. In this mode, the oscillator continues to run with a typical supply current of 1.5mA with a 10MHz crystal, but no measurements are made and multiplexed inputs are inactive. A new measurement cycle will be initiated when the HOLD input is switched to V_{SS}.

Display Test - Display will turn on with all the digits showing 8s and all decimal points on. The display will be blanked if Display Off is selected at the same time.

1MHz Select - The 1MHz select mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurement as with a 10MHz crystal. This is done by dividing the oscillator frequency by 10^4 rather than 10^5. The decimal point is also shifted one digit to the right in period and time interval, since the least significant digit will be in µs increment rather than 0.1µs increment.

External Oscillator Enable - In this mode, the signal at EXT OSC INPUT is used as a timebase instead of the on-board crystal oscillator (built around the OSC INPUT, OSC OUTPUT inputs). This input can be used for an external stable temperature compensated crystal oscillator or for special measurements with any external source. The on-board crystal oscillator continues to work when the external oscillator is selected. This is necessary to avoid hang-up problems, and has no effect on the chip's functional operation. If the on-board oscillator frequency is less than 1MHz or only the external oscillator is used, THE OSC INPUT MUST BE CONNECTED TO THE EXT OSC INPUT providing the timebase has enough voltage swing for OSC INPUT (See Electrical Specifications). If the external timebase is TTL level a pullup resistor must be used for OSC INPUT. The other way is to put a 22MΩ resistor between OSC INPUT and OSC OUTPUT and capacitively couple the EXT OSC INPUT to OSC INPUT. This will bias the OSC INPUT at its threshold and the drive voltage will need to be only $2V_{P-P}$. The external timebase frequency must be greater than 100kHz or the chip will reset itself to enable the on-board oscillator.

External Decimal Point Enable - In this mode, the EX DP INPUT is enabled (ICM7216D only). A decimal point will be displayed for the digit that its output line is connected to this input (EX DP INPUT). Digit 8 should not be used since it will override the overflow output. Leading zero blanking is effective for the digits to the left of selected decimal point.

Hold Input

Except in the **unit counter mode**, when the HOLD input is at V_{DD}, any measurement in progress (before $\overline{\text{STORE}}$ goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD input is at V_{DD}, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the new counter.

$\overline{\text{RESET}}$ Input

The $\overline{\text{RESET}}$ input resets the main counter, stops any measurement in progress, and enables the main counter latches, resulting in an all zero output. A capacitor to ground will prevent any hang-ups on power-up.

$\overline{\text{MEASUREMENT IN PROGRESS}}$

This output is provided in ICM7216D. It stays low during measurements and goes high for intervals between measurements. It is provided for system interfacing and can drive a low power Schottky TTL or one ECL load if the ECL device is powered from the same supply as ICM7216D.

Decimal Point Position

Table 3 shows the decimal point position for different modes of ICM7216 operation. Note that the digit 1 is the least significant digit. Table 3 is for 10MHz timebase frequency.

Overflow Indication

When overflow happens in any measurement it will be indicated on the decimal point of the digit 8. A separate LED indicator can be used. Figure 12 shows how to connect this indicator.

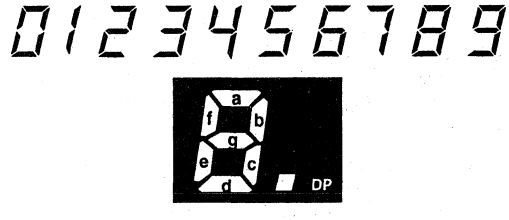


FIGURE 12. SEGMENT IDENTIFICATION AND DISPLAY FONT

Overflow will be indicated on the decimal point output of digit 8. A separate LED overflow indicator can be connected as follows:

DEVICE	CATHODE	ANODE
ICM7216A	Decimal Point	D8
ICM7216B/D	D8	Decimal Point

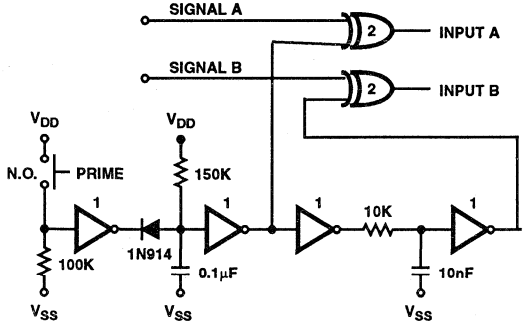
TABLE 3. DECIMAL POINT POSITIONS

RANGE	FREQUENCY	PERIOD	FREQUENCY RATIO	TIME INTERVAL	UNIT COUNTER	OSCILLATOR FREQUENCY
0.01s/1 Cycle	D2	D2	D1	D2	D1	D2
0.1s/10 Cycle	D3	D3	D2	D3	D1	D3
1s/100 Cycle	D4	D4	D3	D4	D1	D4
10s/1K Cycle	D5	D5	D4	D5	D1	D5

Time Interval Measurement

When in the **time interval** mode and measuring a single event, the ICM7216A and ICM7216B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval". The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

Priming can be easily accomplished using the circuit in Figure 13.



DEVICE	TYPE
1	CD4049B Inverting Buffer
2	CD4070B Exclusive - OR

FIGURE 13. PRIMING CIRCUIT, SIGNALS A & B BOTH HIGH OR LOW

Following the priming procedure (when in single event or 1 cycle range) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7216A and ICM7216B as the first alternating signal states automatically prime the device. See Figure 1.

During any time interval measurement cycle, the ICM7216A and ICM7216B require 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.

Oscillator Considerations

The oscillator is a high gain CMOS inverter. An external resistor of 10MΩ to 22MΩ should be connected between the OSCillator INPUT and OUTPUT to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35Ω.

For a specific crystal and load capacitance, the required g_M can be calculated as follows:

$$g_M = \omega^2 C_{IN} C_{OUT} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where $C_L = \left(\frac{C_{IN} C_{OUT}}{C_{IN} + C_{OUT}}\right)$

C_O = Crystal Static Capacitance

R_S = Crystal Series Resistance

C_{IN} = Input Capacitance

C_{OUT} = Output Capacitance

$\omega = 2\pi f$

The required g_M should not exceed 50% of the g_M specified for the ICM7216 to insure reliable startup. The OSCillator INPUT and OUTPUT pins each contribute about 5pF to C_{IN} and C_{OUT}. For maximum stability of frequency, C_{IN} and C_{OUT} should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10MHz or 1MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate is

$f_{MUX} = \frac{f_{OSC}}{2 \times 10^4}$ for 10MHz mode and $f_{MUX} = \frac{f_{OSC}}{2 \times 10^3}$ for the 1MHz mode. The time between measurements is $\frac{2 \times 10^6}{f_{OSC}}$ in the 10MHz mode and $\frac{2 \times 10^5}{f_{OSC}}$ in the 1MHz mode.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the EXTERNAL OSCILLATOR INPUT to the OSCILLATOR OUTPUT or INPUT can cause undesirable shifts in oscillator frequency.

Display Considerations

The display is multiplexed at a 500Hz rate with a digit time of 244µs. An interdigit blanking time of 6µs is used to prevent display ghosting (faint display of data from previous digit superimposed on the next digit). Leading zero blanking is provided, which blanks the left hand zeroes after decimal point or any non zero digits. Digits to the right of the decimal point are always displayed. The leading zero blanking will be disabled when the Main Counter overflows.

The ICM7216A is designed to drive common anode LED displays at peak current of 25mA/segment, using displays with V_F = 1.8V at 25mA. The average DC current will be over 3mA under these conditions. The ICM7216B and ICM7216D are designed to drive common cathode displays at peak current of 15mA/segment using displays with V_F = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. The Typical Performance Curves show the digit and segment currents as a function of output voltage.

To get additional brightness out of the displays, V_{DD} may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

The segment and digit outputs in ICM7216's are not directly compatible with either TTL or CMOS logic when driving LEDs. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

Accuracy

In a Universal Counter crystal drift and quantization effects cause errors. In **frequency, period** and **time interval** modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of $20_{PPM}/^{o}C$ will cause a measurement error of $20_{PPM}/^{o}C$.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode the maximum accuracy is obtained with high frequency inputs and in **period** mode maximum accuracy is obtained with low frequency inputs (as can be seen in Figure 14). In **time interval** measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 15. In **frequency ratio** measurement can be more accurately obtained by averaging over more cycles of INPUT B as shown in Figure 16.

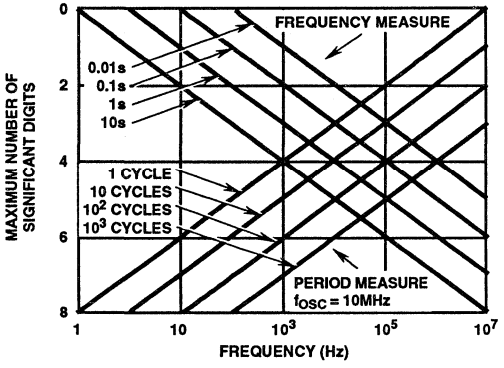


FIGURE 14. MAXIMUM ACCURACY OF FREQUENCY AND PERIOD MEASUREMENTS DUE TO LIMITATIONS OF QUANTIZATION ERRORS

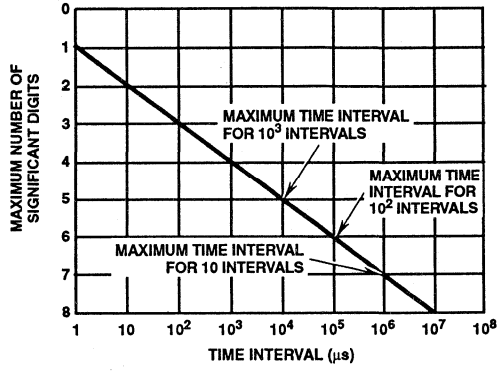


FIGURE 15. MAXIMUM ACCURACY OF TIME INTERVAL MEASUREMENT DUE TO LIMITATIONS OF QUANTIZATION ERRORS

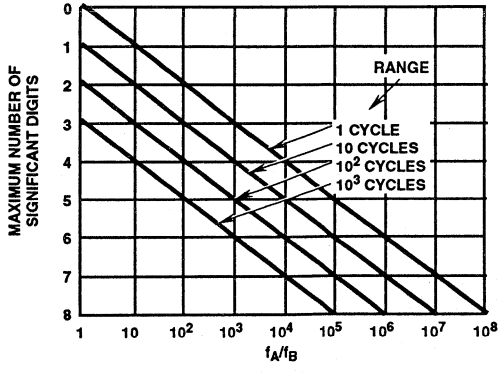


FIGURE 16. MAXIMUM ACCURACY FOR FREQUENCY RATIO MEASUREMENT DUE TO LIMITATION OF QUANTIZATION ERRORS

Test Circuit

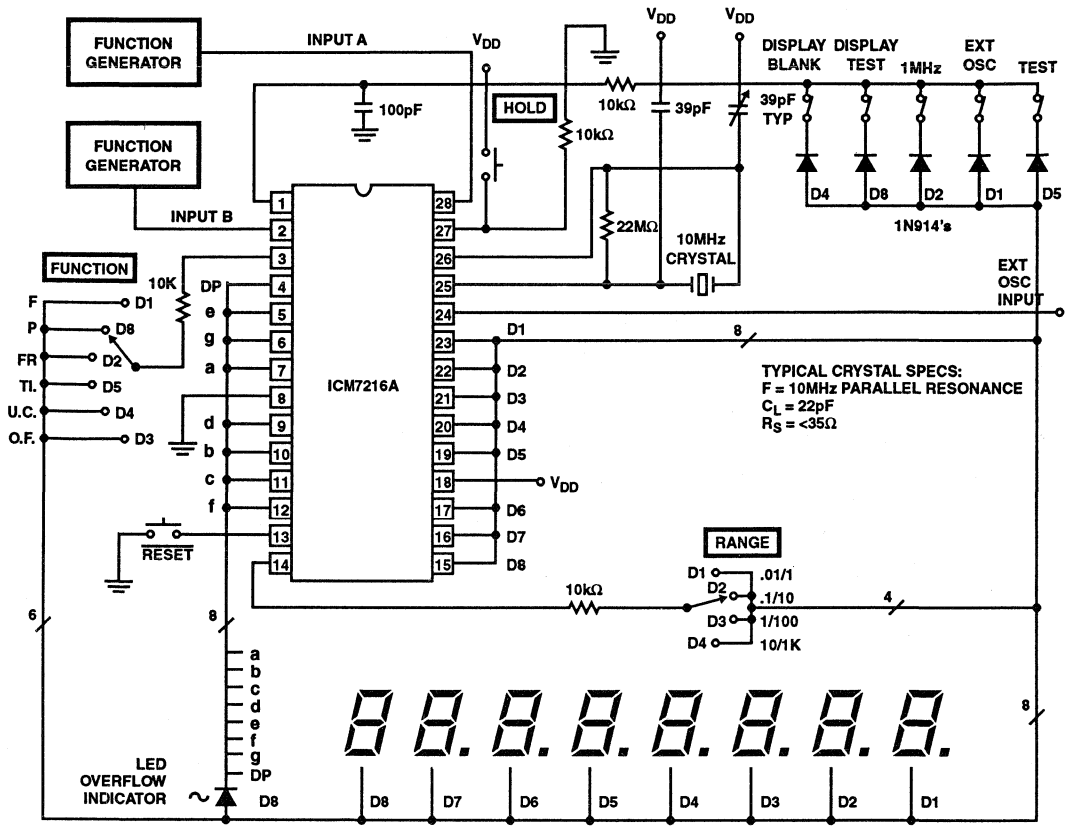


FIGURE 17. TEST CIRCUIT (ICM7216A SHOWN, OTHERS SIMILAR)

Typical Applications

The ICM7216 has been designed for use in a wide range of Universal and Frequency counters. In many cases, prescalers will be required to reduce the input frequencies to under 10MHz. Because INPUT A and INPUT B are digital inputs, additional circuitry is often required for input buffering, amplification, hysteresis, and level shifting to obtain a good digital signal.

The ICM7216A or ICM7216B can be used as a minimum component complete Universal Counter as shown in Figure 18. This circuit can use input frequencies up to 10MHz at INPUT A and 2MHz at INPUT B. If the signal at INPUT A has a very low duty cycle it may be necessary to use a 74LS121 monostable multivibrator or similar circuit to stretch the input pulse width to be able to guarantee that it is at least 50ns in duration.

To measure frequencies up to 40MHz the circuit of Figure 19 can be used. To obtain the correct measured value, it is necessary to divide the oscillator frequency by four as well as the input frequency. In doing this the time between measurements is also lengthened to 800ms and the display multiplex rate is decreased to 125Hz.

If the input frequency is prescaled by ten, then the oscillator can remain at 10MHz or 1MHz, but the decimal point must be moved one digit to the right. Figure 20 shows a frequency counter with a ÷10 prescaler and an ICM7216A. Since there is no external decimal point control with the ICM7216A and ICM7216B, the decimal point may be controlled externally with additional drivers as shown in Figure 20. Alternatively, if separate anodes are available for the decimal points, they can be wired up to the adjacent digit anodes. Note that there can be one zero to the left of the decimal point since the internal leading zero blanking cannot be changed. In Figure 21 additional logic has been added to count the input directly in **period** mode for maximum accuracy. In Figures 20 and 21, INPUT A comes from Q_C of the prescaler rather than Q_D to obtain an input duty cycle of 40%.

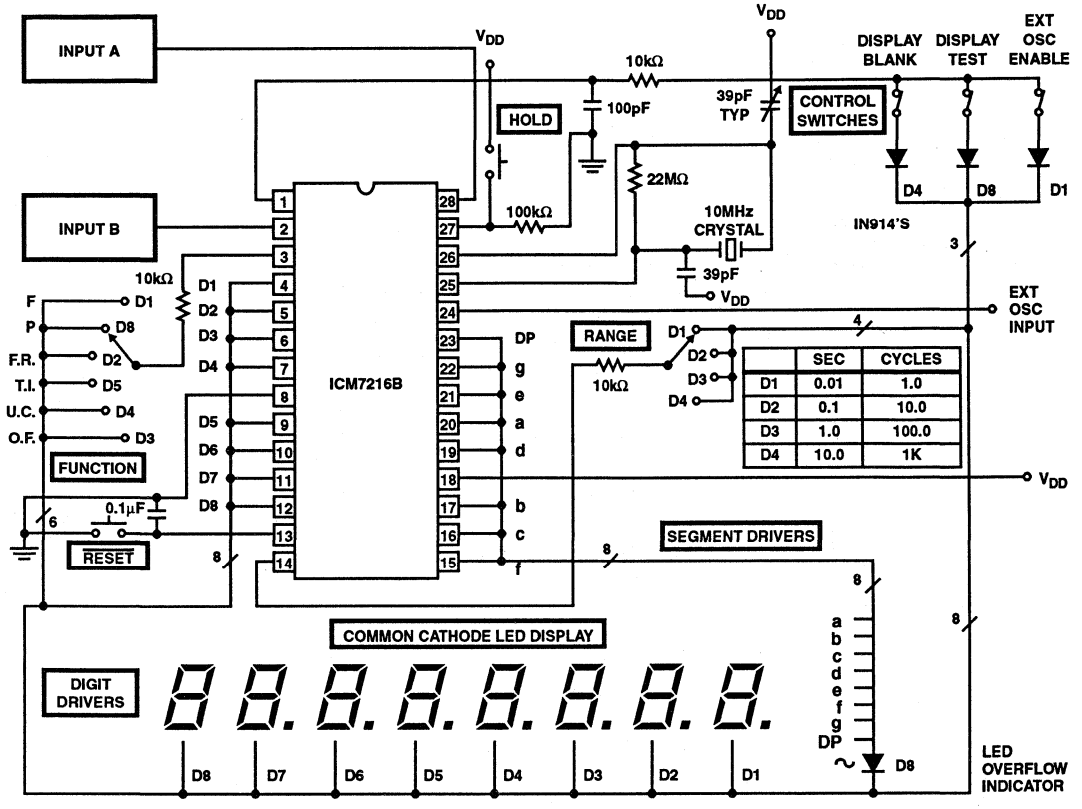


FIGURE 18. 10MHz UNIVERSAL COUNTER

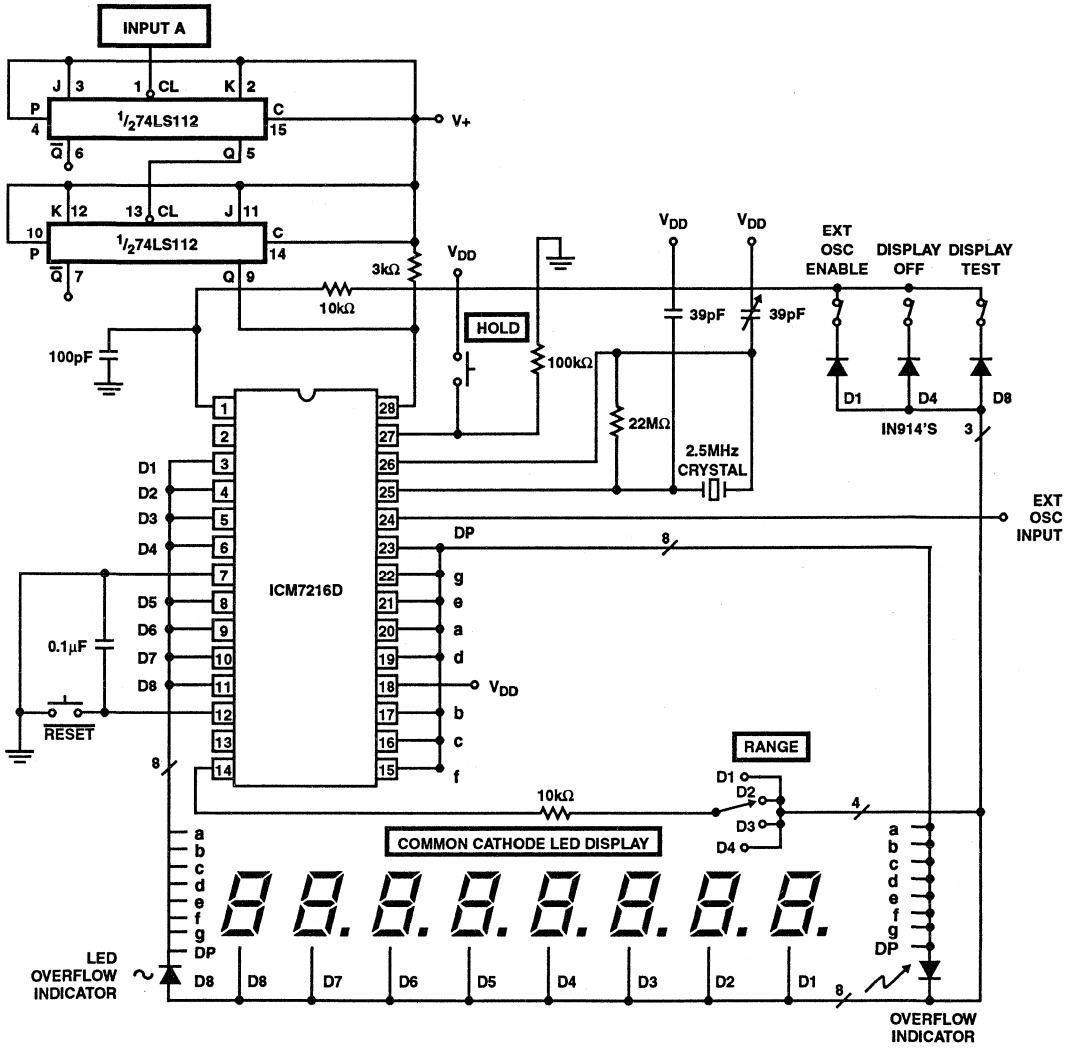


FIGURE 19. 40MHz FREQUENCY COUNTER

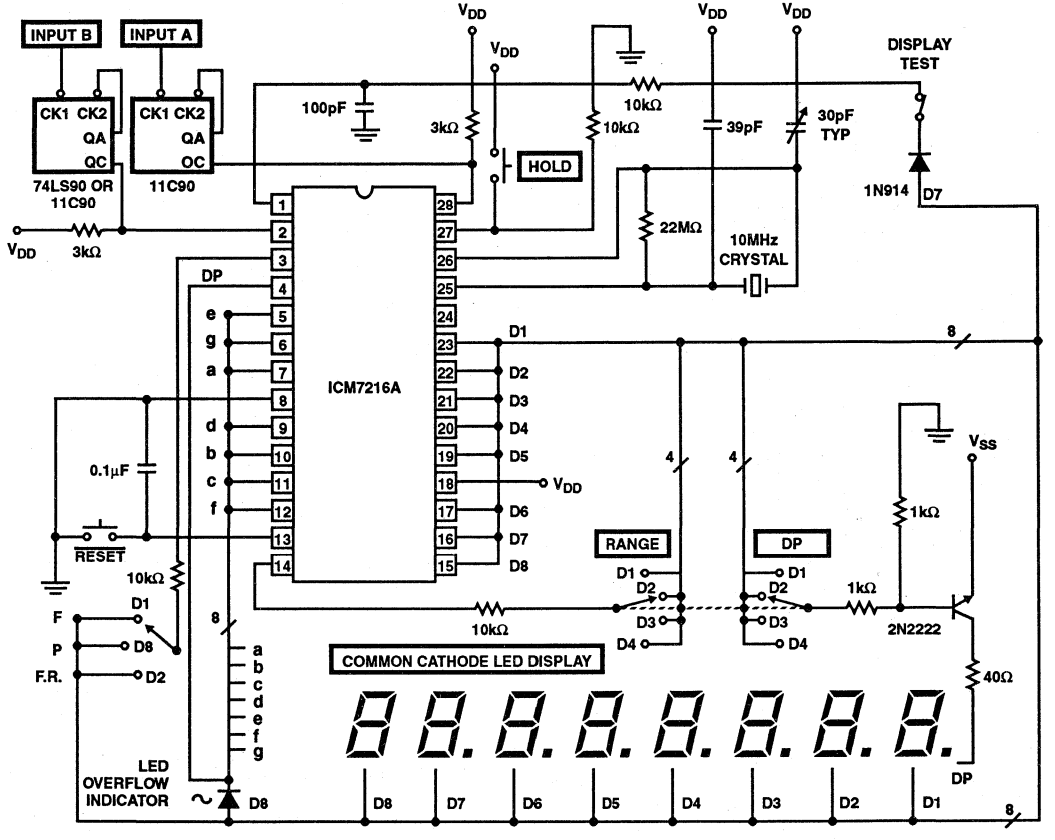


FIGURE 20. 100MHz MULTIFUNCTION COUNTER

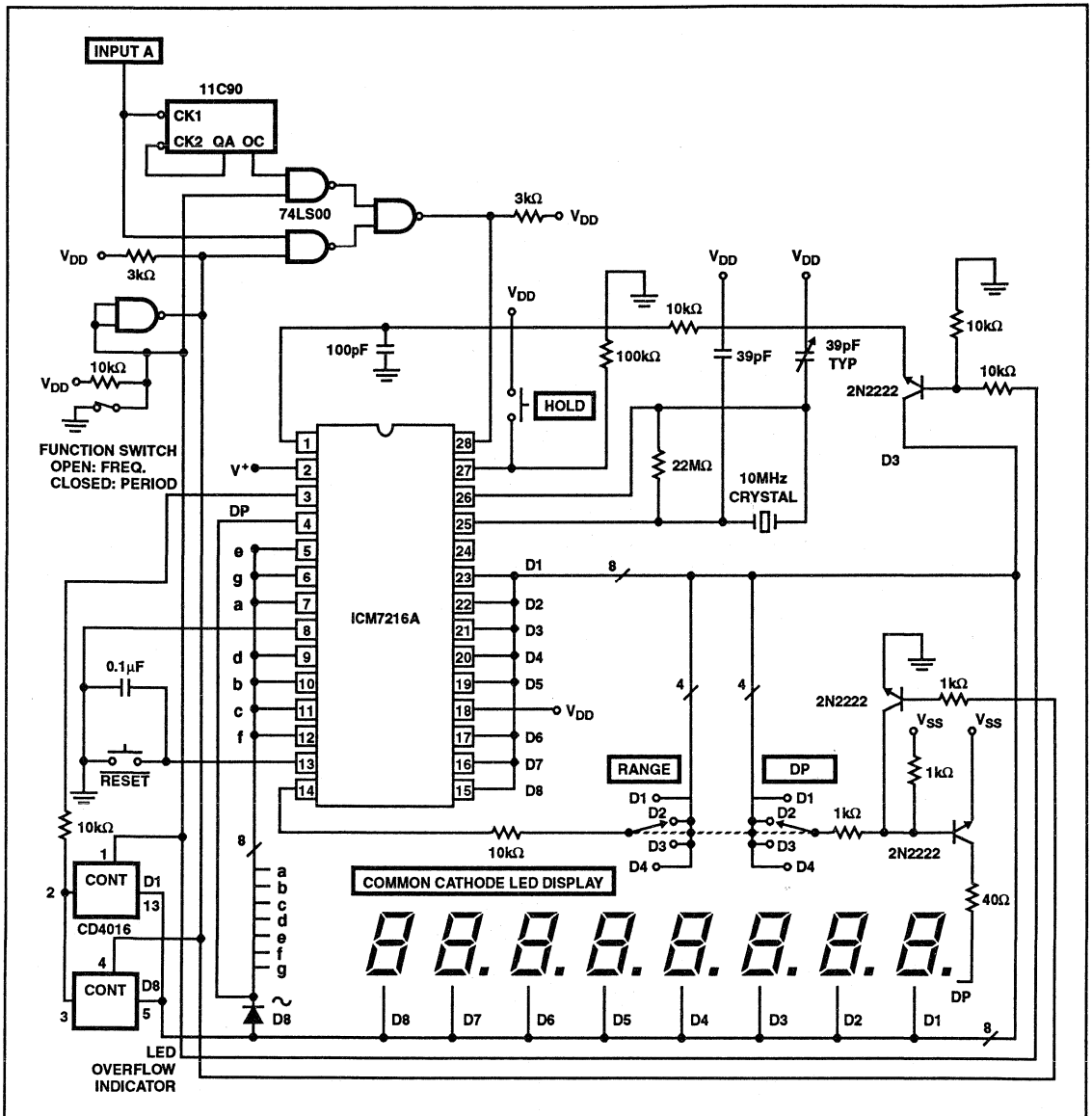


FIGURE 21. 100MHz FREQUENCY, 2MHz PERIOD COUNTER

HARRIS SEMICONDUCTOR

ICM7217

4-Digit LED Display Programmable Up/Down Counter

December 1993

Features

- **Four Decade, Presettable Up-Down Counter with Parallel Zero Detect**
- **Settable Register with Contents Continuously Compared to Counter**
- **Directly Drives Multiplexed 7 Segment Common Anode or Common Cathode LED Displays**
- **On-Board Multiplex Scan Oscillator**
- **Schmitt Trigger On Count Input**
- **TTL Compatible BCD I/O Port, Carry/Borrow, Equal, and Zero Outputs**
- **Display Blank Control for Lower Power Operation; Quiescent Power Dissipation <5mW**
- **All Terminals Fully Protected Against Static Discharge**
- **Single 5V Supply Operation**

Description

The ICM7217 is a four digit, presettable up/down counter with an onboard presettable register continuously compared to the counter. The ICM7217 is intended for use in hard-wired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control.

This circuit provides multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to 0.8 inch character height (common anode) at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeros can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

The ICM7217 (common anode) and ICM7217A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B (common anode) and ICM7217C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

This circuit provides 3 main outputs; a CARRY/BORROW output, which allows for direct cascading of counters, a $\overline{\text{ZERO}}$ output, which indicates when the count is zero, and an $\overline{\text{EQUAL}}$ output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a tri-state BCD I/O port. The CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$ outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2MHz, although the device will typically run with f_{IN} as high as 5MHz. Counting and comparing ($\overline{\text{EQUAL}}$ output) will typically run 750kHz maximum.

Ordering Information

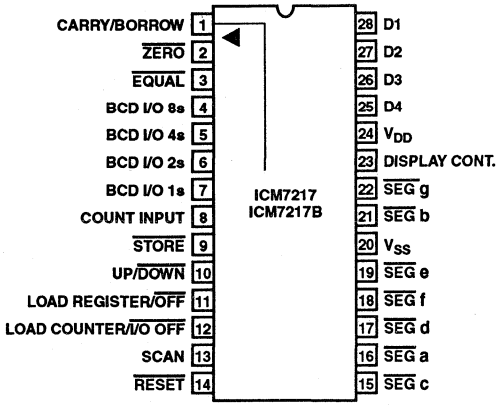
PART NUMBER	TEMPERATURE RANGE	PACKAGE	DISPLAY DRIVER TYPE	COUNT OPTION/ MAX COUNT
ICM7217AIPI	-25°C to +85°C	28 Lead Plastic DIP	Common Cathode	Decade/9999
ICM7217CIPI	-25°C to +85°C	28 Lead Plastic DIP	Common Cathode	Timing/5959
ICM7217IJI	-25°C to +85°C	28 Lead Ceramic DIP	Common Anode	Decade/9999
ICM7217BIJI	-25°C to +85°C	28 Lead Ceramic DIP	Common Anode	Timing/5959

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

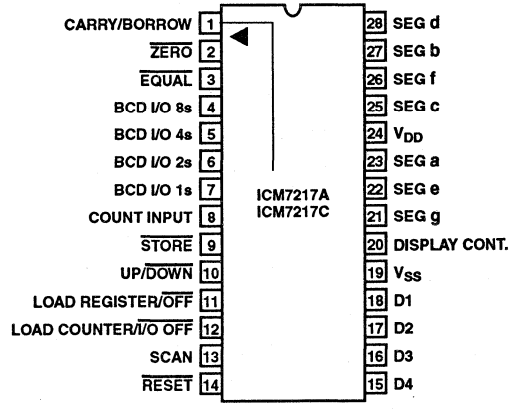
File Number 3167

Pinouts

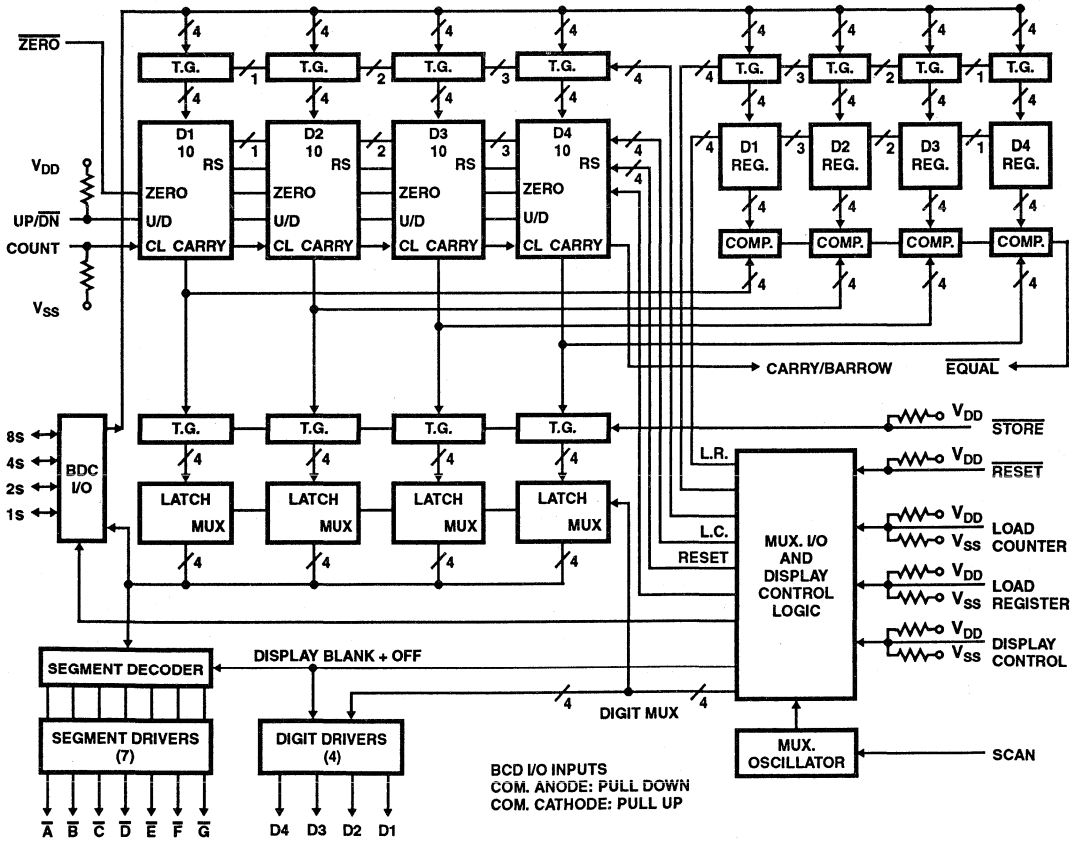
ICM7217 (PDIP)
COMMON ANODE
TOP VIEW



ICM7217 (CDIP)
COMMON CATHODE
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) 6V
Input Voltage (any terminal) ..... (V_{SS} - 0.3)V to (V_{DD} + 0.3)V
(Note 2)
Operating Temperature Range ..... -25°0 to +85°C
Storage Temperature Range ..... -65°0 to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	55°C/W	20°C/W
Plastic DIP Package	55°C/W	-

Junction Temperature
Plastic Package ..... +150°C
Ceramic Package ..... +175°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = 5V, V_{SS} = 0V, T_A = +25°C, Display Diode Drop 1 .7V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current (Lowest Power Mode), IDD (7217)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V_{DD} (Note 3)	-	350	500	µA
Supply Current, OPERATING, I_{OP}	Common Anode, Display On, all "8's"	140	200	-	mA
Supply Current, OPERATING, I_{OP}	Common Cathode, Display On, all "8's"	50	100	-	mA
V_{SUPPLY}, VDD		4.5	5	5.5	V
Digit Driver Output Current, I_{DIG}	Common Anode, V_{OUT} = V_{DD} - 2.0V	140	200	-	mA peak
SEGment Driver Output Current, ISEG	Common Anode, V_{OUT} = +1.5V	20	35	-	mA peak
Digit Driver, Output Current, I_{DIG}	Common Cathode, V_{OUT} = +1.0V	-50	-75	-	mA peak
SEGment Driver Output Current, ISEG	Common Cathode V_{OUT} = V_{DD} - 2V	-9	-12.5	-	mA peak
$\overline{ST}$, $\overline{RS}$, UP/$\overline{DN}$ Input Pullup Current, IP	V_{IN} = V_{DD} - 2V (Note 3)	5	25	-	µA
3 Level Input Impendance, ZIN		40	-	350	kΩ
BCD I/O Input, High Voltage VBIH	ICM7217 Common Anode (Note 4)	1.5	-	-	V
	ICM7217 Common Cathode (Note 4)	4.40	-	-	V
BCD I/O Input, Low Voltage VBIL	ICM7217 Common Anode (Note 4)	-	-	0.60	V
	ICM7217 Common Cathode (Note 4)	-	-	3.2V	V
BCD I/O Input, Pullup Current IBPU	ICM7217 Common Cathode V_{IN} = V_{DD} - 2V (Note 3)	5	25	-	µA
BCD I/O Input Pulldown Current, IBPD	ICM7217 Common Anode V_{IN} = +2V (Note 3)	5	25	-	µA
BCD I/O, $\overline{ZERO}$, $\overline{EQUAL}$ Outputs Output High Voltage, VOH	I_{OH} = -100µA	3.5	-	-	V
BCD I/O, CARRY/BORROW $\overline{ZERO}$, $\overline{EQUAL}$ Outputs Output Low Voltage, VOL	I_{OL} = 1.6mA	-	-	0.4	V
Count Input Frequency, f_{IN}	-20°C < T_A < +70°C	-	5	-	MHz
	Guaranteed	0	-	2	MHz
Count Input Threshold, VTH	(Note 5)	-	2	-	V
Count Input Hysteresis, VHYS	(Note 5)	-	0.5	-	V
Count Input LO, VCIL		-	-	0.40	V
Count Input HI, VCIH		3.5	-	-	V
Display Scan Oscillator Frequency, F_{DS}	Free-running (SCAN Terminal Open Circuit)	-	2.5	10	kHz

Switching Specifications V_{DD} = 5V, V_{SS} = 0V, T_A = +25°C

PARAMETER	MIN	TYP	MAX	UNIT
UP/$\overline{\text{DOWN}}$ Setup Time, t_{UCS}	300	-	-	ns
UP/$\overline{\text{DOWN}}$ Hold Time, t_{UCH}	1500	750	-	ns
COUNT Pulse Width High, t_{CWH}	250	100	-	ns
COUNT Pulse Width Low, t_{CWI}	250	100	-	ns
COUNT to CARRY/BORROW Delay, t_{CB}	-	750	-	ns
CARRY/BORROW Pulse Width t_{BW}	-	100	-	ns
COUNT to $\overline{\text{EQUAL}}$ Delay, t_{CE}	-	500	-	ns
COUNT to $\overline{\text{ZERO}}$ Delay, t_{CZ}	-	300	-	ns
RESET Pulse Width, t_{RST}	1000	500	-	ns

NOTES:

1. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217 be turned on first.
2. In the ICM7217 the UP/$\overline{\text{DOWN}}$, $\overline{\text{STORE}}$, $\overline{\text{RESET}}$ and the BCD I/O as inputs have pullup or pulldown devices which consume power when connected to the opposite supply. Under these conditions, with the display off, the device will consume typically 750µA.
3. These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217. Note that a high level is taken as an input logic zero for ICM7217 common-cathode versions.
4. Parameters not tested (Guaranteed by Design).

Timing Waveforms

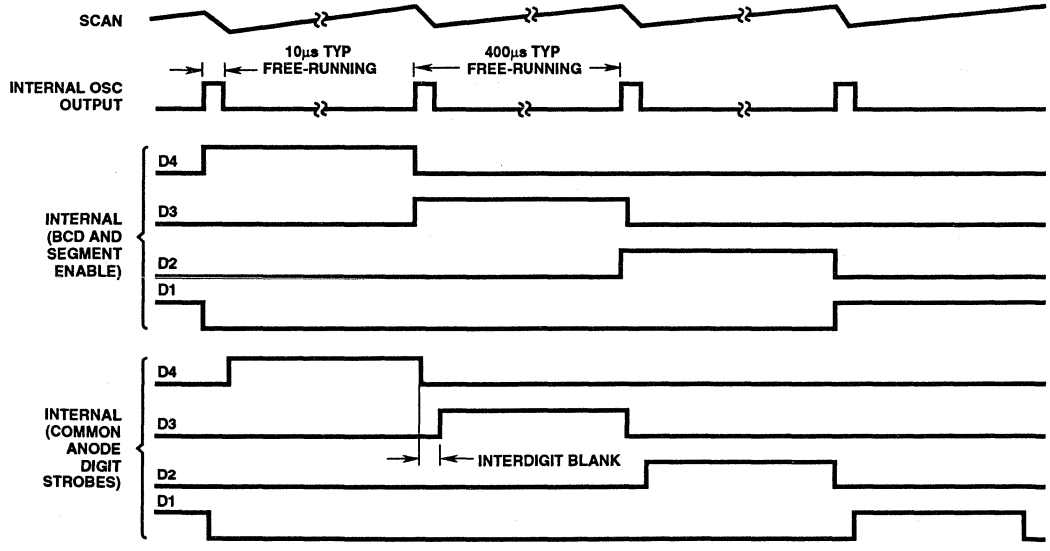


FIGURE 1. MULTIPLEX TIMING

Timing Waveforms

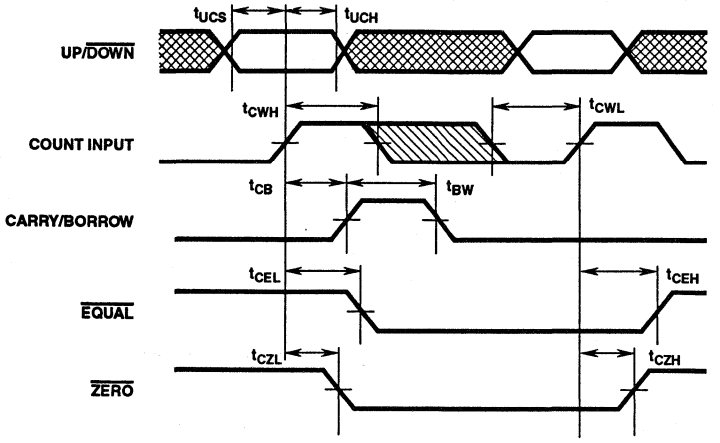


FIGURE 2. COUNT AND OUTPUTS TIMING

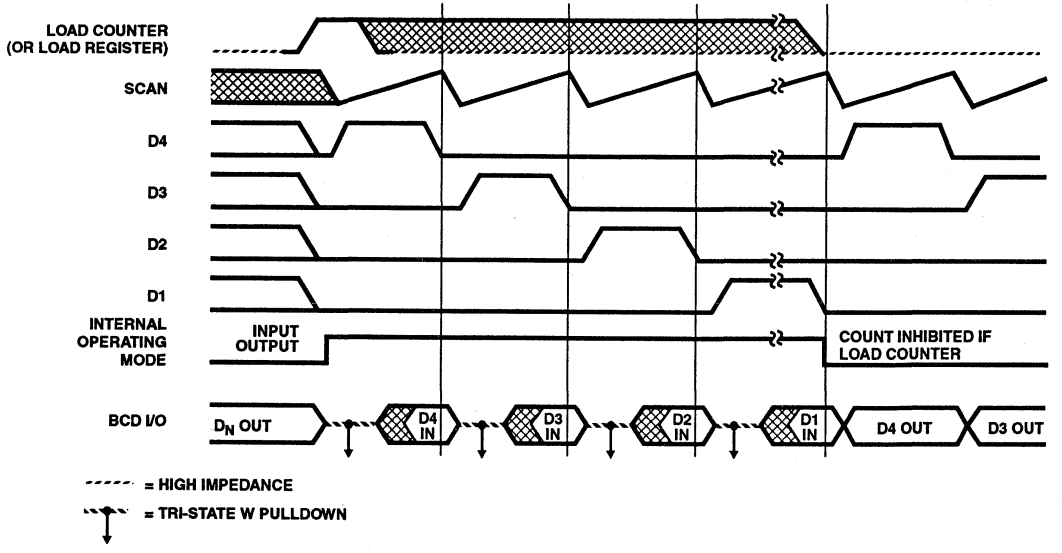


FIGURE 3. BCD I/O AND LOADING TIMING

Typical Performance Curves

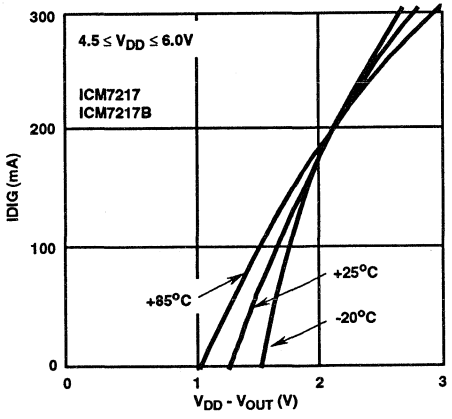


FIGURE 4. TYPICAL IDIG vs V+

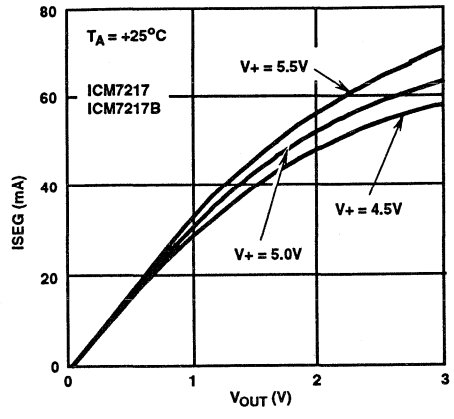


FIGURE 5. TYPICAL ISEG vs V_{OUT}

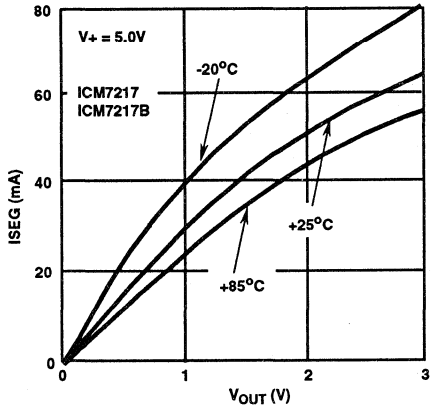


FIGURE 6. TYPICAL ISEG vs V_{OUT}

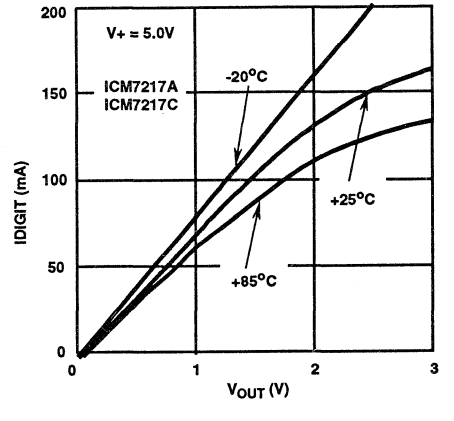


FIGURE 7. TYPICAL IDIGIT vs V_{OUT}

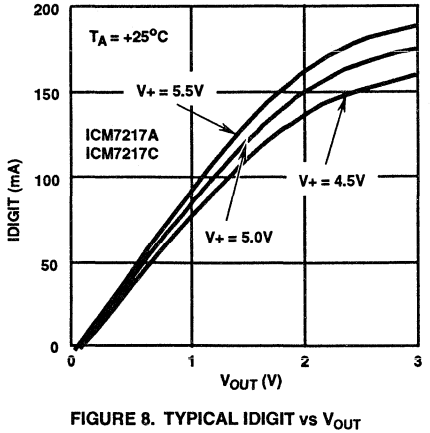


FIGURE 8. TYPICAL IDIGIT vs V_{OUT}

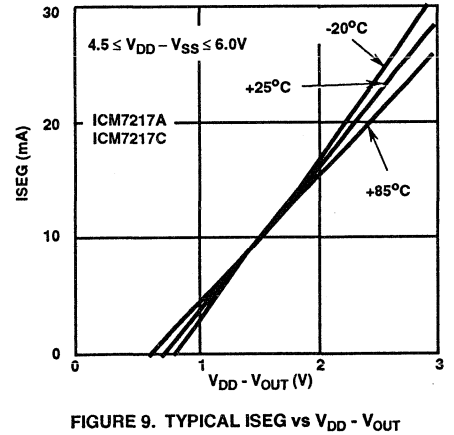


FIGURE 9. TYPICAL ISEG vs V_{DD} - V_{OUT}

Detailed Description

Control Outputs

The CARRY/BORROW output is a positive going pulse occurring typically 500ns after the positive going edge of the COUNT INPUT. It occurs when the counter is clocked from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters. The CARRY/BORROW output is not valid during load counter and reset operation. When the count is 6000 or higher, a reset generates a CARRY/BORROW pulse.

The $\overline{\text{EQUAL}}$ output assumes a negative level when the contents of the counter and register are equal.

The $\overline{\text{ZERO}}$ output assumes a negative level when the content of the counter is 0000.

The CARRY/BORROW, $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 1.6mA at 0.4V and for a logic one, the outputs will source >60µA. A 10kΩ pull-up resistor to V_{DD} on the $\overline{\text{EQUAL}}$ or $\overline{\text{ZERO}}$ outputs is recommended for highest speed operation, and on the CARRY/BORROW output when it is being used for cascading. Figure 2 shows control outputs timing diagram.

Display Outputs and Control

The Digit and SEGment drivers provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 35mA/seg. This corresponds to average currents of 8mA/seg at 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. Figure 1 shows the multiplex timing. The DISPLAY pin controls the display output using three level logic. The pin is self-biased to a voltage approximately $^1/_2$ (V_{DD}); this corresponds to normal operation. When this pin is connected to V_{DD}, the segments are disabled and when connected to V_{SS}, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin should be left open. The display may be controlled with a 3 position SPDT switch; see Test Circuit.

Multiplex SCAN Oscillator

The on-board multiplex scan oscillator has a nominal free-running frequency of 2.5kHz. This may be reduced by the addition of a single capacitor between the SCAN pin and the positive supply. Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times are shown in Table 1.

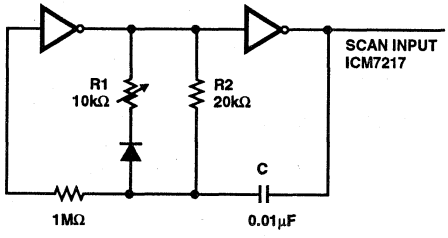


FIGURE 10A.

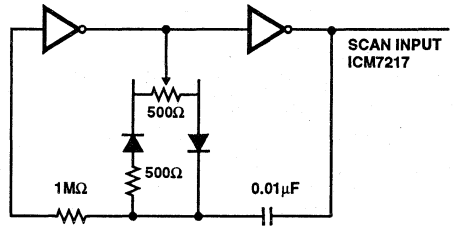


FIGURE 10B.

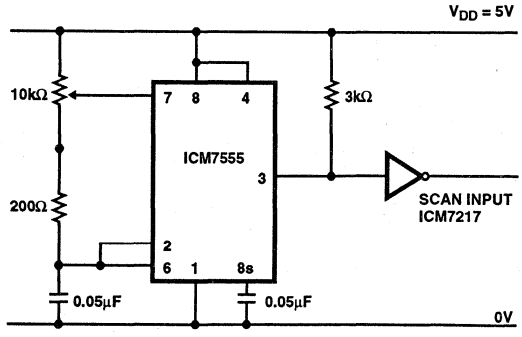


FIGURE 10C.

FIGURE 10. BRIGHTNESS CONTROL CIRCUITS

TABLE 1. ICM7217 MULTIPLEXED RATE CONTROL

SCAN CAPACITOR	NOMINAL OSCILLATOR FREQUENCY	DIGIT REPETITION RATE	SCAN CYCLE TIME (4 DIGITS)
None	2.5kHz	625Hz	1.6ms
20pF	1.25kHz	300Hz	3.2ms
90pF	600Hz	150Hz	8ms

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing interdigit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Figure 1 for the display digit multiplex timing.

During load counter and load register operations, the multiplex oscillator is disconnected from the SCAN input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven to about 20kHz, however the external oscillator signal should have the same duty cycle as the internal signal, since the digits are blanked during the time the external signal is at a positive level (see Figure 1). To insure proper leading zero blanking, the interdigit blanking time should not be less than about 2µs. Overdriving the oscillator at less than 200Hz may cause display flickering.

The display brightness may be altered by varying the duty cycle. Figure 10 shows several variable-duty-cycle oscillators suitable for brightness control at the ICM7217 SCAN input. The inverters should be CMOS CD4000 series and the diodes may be any inexpensive device such as IN914.

Counting Control, $\overline{\text{STORE}}$, $\overline{\text{RESET}}$

As shown in Figure 2, the counter is incremented by the rising edge of the COUNT INPUT signal when UP/$\overline{\text{DOWN}}$ is high. It is decremented when UP/$\overline{\text{DOWN}}$ is low. A Schmitt trigger on the COUNT INPUT provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments. The COUNT INPUT is inhibited during reset and load counter operations.

The $\overline{\text{STORE}}$ pin controls the internal latches and consequently the signals appearing at the 7-Segment and BCD outputs. Bringing the $\overline{\text{STORE}}$ pin low transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the $\overline{\text{RESET}}$ pin low. The circuit performs the reset operation by forcing the BCD input lines to zero, and "presetting" all four decades of counter in parallel. This affects register loading; if LOAD REGISTER is activated when the $\overline{\text{RESET}}$ input is low, the register will also be set to zero. The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$ and UP/$\overline{\text{DOWN}}$ pins are provided with pullup resistors of approximately 75kΩ.

BCD I/O Pins

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions can multiplex data into the counter or register via thumbwheel switches, depending on inputs to the LOAD COUNTER or LOAD REGISTER pins; (see below). When functioning as outputs, the BCD I/O pins will drive one standard TTL load. Common anode versions have internal pull down resistors and common cathode versions have internal pull up resistors on the four BCD I/O lines when used as inputs.

LOADing the COUNTER and REGISTER

The BCD I/O pins, the LOAD COUNTER (LC), and LOAD REGISTER (LR) pins combine to provide presetting and compare functions. LC and LR are 3-level inputs, being self-biased at approximately $^1/_2V_{DD}$ for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex.

When either the LOAD COUNTER (Pin 12) or LOAD REGISTER (Pin 11) is taken low, the drivers are turned off and the BCD pins become high-impedance inputs. When LC is connected to V_{DD}, the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V_{DD}, the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V_{DD}, the count is inhibited and both register and counter will be loaded.

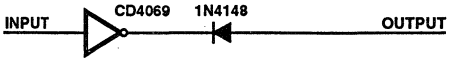
The LOAD COUNTER and LOAD REGISTER inputs are edge-triggered, and pulsing them high for 500ns at room temperature will initiate a full sequence of data entry cycle operations (see Figure 3). When the circuit recognizes that either or both of the LC or LR pins input is high, the multiplex oscillator and counter are reset (to D4). The internal oscillator is then disconnected from the SCAN pin and the preset circuitry is enabled. The oscillator starts and runs with a frequency determined by its internal capacitor, (which may vary from chip to chip). When the chip finishes a full 4 digit multiplex cycle (loading each digit from D4 to D3 to D2 to D1 in turn), it again samples the LOAD REGISTER and LOAD COUNTER inputs. If either or both is still high, it repeats the load cycle, if both are floating or low, the oscillator is reconnected to the SCAN pin and the chip returns to normal operation. Total load time is digit "on" time multiplied by 4. If the Digit outputs are used to strobe the BCD data into the BCD I/O inputs, the input must be synchronized to the appropriate digit (Figure 3). Input data must be valid at the trailing edge of the digit output.

When LR is connected to GROUND, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the CARRY/BORROW, $\overline{\text{EQUAL}}$, $\overline{\text{ZERO}}$, UP/$\overline{\text{DOWN}}$, $\overline{\text{RESET}}$ and $\overline{\text{STORE}}$ functions operate as normal. When LC is connected to ground, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input Definitions" (Table 2) for a list of the pins that function as tri-state self-biased inputs and their respective operations.

Note that the ICM7217 and ICM7217B have been designed to drive common anode displays. The BCD inputs are high true, as are the BCD outputs.

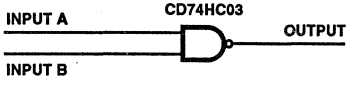
INPUT	OUTPUT
High	High
Low	Disconnected

FIGURE 11A. CMOS INVERTER



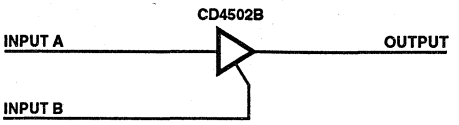
INPUT	OUTPUT
High	Disconnected
Low	High

FIGURE 11B. CMOS INVERTER



INPUT B	INPUT A	OUTPUT
High	High	Low
High	Low	Disconnected
Low	High	Disconnected
Low	Low	Disconnected

FIGURE 11C. CMOS OPEN DRAIN



INPUT B	INPUT A	OUTPUT
High	High	Disconnected
High	Low	Disconnected
Low	High	High
Low	Low	Low

FIGURE 11D. CMOS TRI-STATE BUFFER

FIGURE 11. DRIVING 3-LEVEL INPUTS OF ICM7217

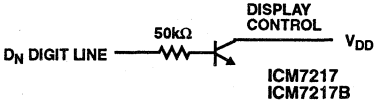


FIGURE 12A. COMMON ANODE

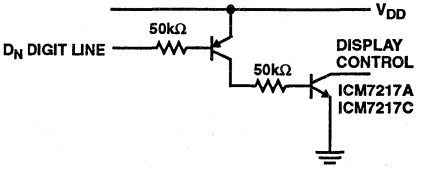


FIGURE 12B. COMMON CATHODE

FIGURE 12. FORCING LEADING ZERO DISPLAY

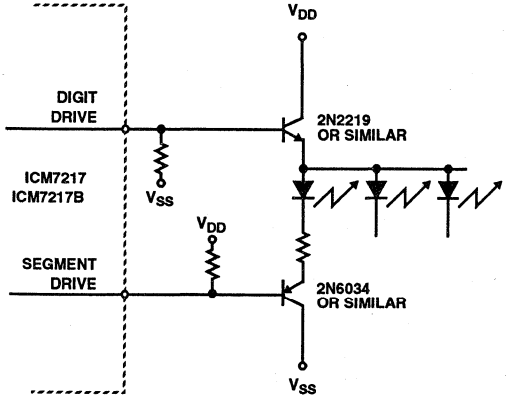


FIGURE 13A. COMMON ANODE DISPLAY

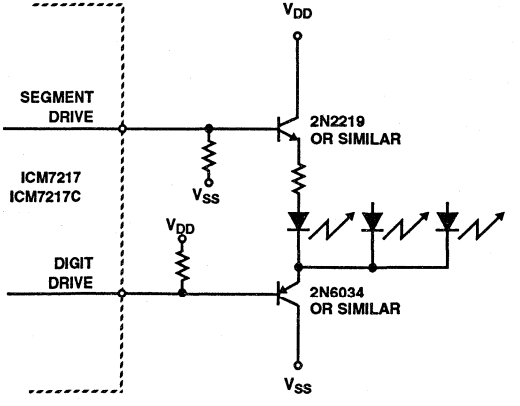


FIGURE 13B. COMMON CATHODE DISPLAY

FIGURE 13. DRIVING HIGH CURRENT DISPLAYS

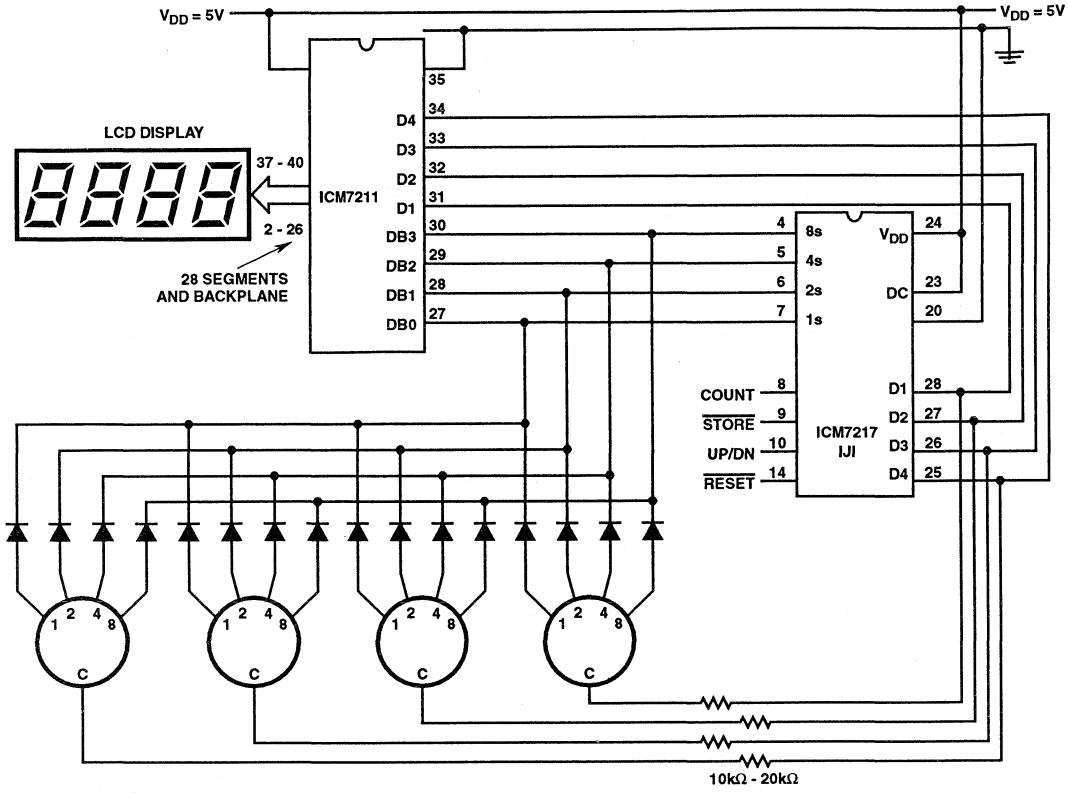


FIGURE 14. LCD DISPLAY INTERFACE (WITH THUMBWHEEL SWITCHES

The ICM7217A and the ICM7217C are used to drive common cathode displays, and the BCD inputs are low true. BCD outputs are high true.

Notes on Thumbwheel Switches and Multiplexing

As it was mentioned, the ICM7217 is basically designed to be used with thumbwheel switches for loading the data to the device. See Figure 14 and Figure 17.

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000. Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops (IN914). Similarly, if the BCD outputs are to be used, resistors should be inserted in the Digit lines to avoid loading problems.

Output and Input Restrictions

LOAD COUNTER and LOAD REGISTER operations take 1.6ms typical (5ms maximum) after LC or LR are released. During this load period the $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs are not valid (see Figure 3). Since the Counter and register are compared by XOR gates, loading the counter or register can cause erroneous glitches on the $\overline{\text{EQUAL}}$ and $\overline{\text{ZERO}}$ outputs when codes cross.

LOAD COUNTER or LOAD REGISTER, and $\overline{\text{RESET}}$ input can not be activated at the same time or within a short period of each other. Operation of each input must be delayed 1.6ms typical (5ms for guaranteed proper operation) relating to the preceding one.

Counter and register can be loaded together with the same value if LC and LR inputs become activated exactly at the same time.

Notice the setup and hold time of UP/DOWN input when it is changing during counting operation. Violation of UP/ $\overline{\text{DOWN}}$ hold time will result in incrementing or decrementing the counter by 1000, 100 or 10 where the preceding digit is transitioning from 5 to 6 or 6 to 5.

The $\overline{\text{RESET}}$ input may be susceptible to noise if its input rise time is greater than about 500µs This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any

capacitance to the $\overline{\text{RESET}}$ input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the $\overline{\text{RESET}}$ input is shown on Figure 11.

When using the circuit as a programmable divider (÷ by n with equal outputs) a short time delay (about 1μs) is needed from the $\overline{\text{EQUAL}}$ output to the $\overline{\text{RESET}}$ input to establish a pulse of adequate duration. (See Figure 16).

When the circuit is configured to reload the counter or register with a new value from the BCD lines (upon reaching $\overline{\text{EQUAL}}$), loading time will be digit "on" time multiplied by four. If this load time is longer than one period of the input count, a count can be lost. Since the circuit will retain data in the register, the register need only be updated when a new value is to be entered. $\overline{\text{RESET}}$ will not clear the register.

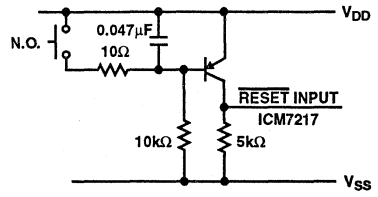


FIGURE 15. POWER ON RESET

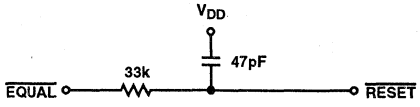
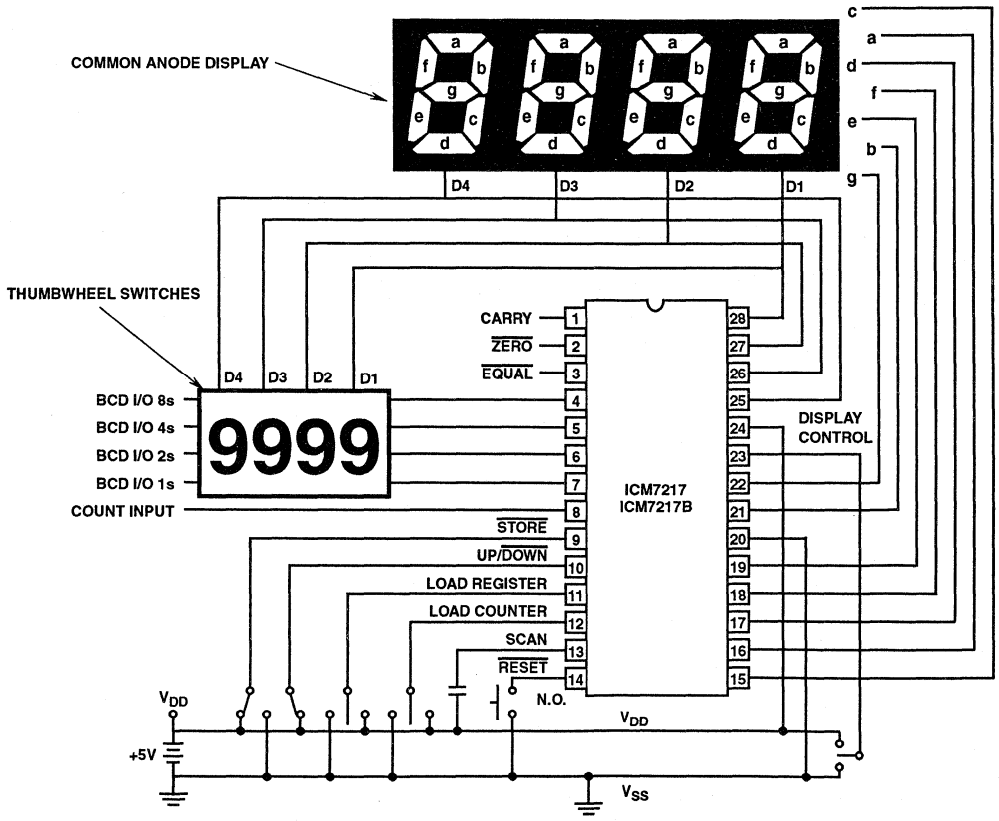


FIGURE 16. $\overline{\text{EQUAL}}$ TO $\overline{\text{RESET}}$ DELAY

Test Circuit



Applications

3-level Inputs

ICM7217 has three inputs with 3-level logic states; High, Low and Disconnected. These inputs are: LOAD REGISTER/$\overline{OFF}$, LOAD COUNTER/I/O $\overline{OFF}$ and DISPLAY CONT.

The circuits illustrated on Figure 11 can be used to drive these inputs in different applications.

Fixed Decimal Point

In the common anode versions, a fixed decimal point may be activated by connecting the DP segment lead from the appropriate digit (with separate digit displays) through a 39Ω series resistor to Ground. With common cathode devices, the DP segment lead should be connected through a 75Ω series resistor to V_{DD}.

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that shown in Figure 12 with the resistor connected to the digit output driving the DP for left hand DP displays, and to the next least significant digit output for right hand DP display.

Driving Larger Displays

For displays requiring more current than the ICM7217 can provide, the circuits of Figure 13 can be used.

LCD Display Interface

The low-power operation of the ICM7217 makes an LCD interface desirable. The Harris ICM7211 4 digit BCD to LCD display driver easily interfaces to the ICM7217 as shown in Figure 14. Total system power consumption is less than 5mW. System timing margins can be improved by using capacitance to ground to slow down the BCD lines.

The 10kΩ - 20kΩ resistors on the switch BCD lines serve to isolate the switches during BCD output.

Unit Counter with BCD Output

The simplest application of the ICM7217 is a 4 digit unit counter (Figure 18). All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using an ICM7217A with a common-cathode calculator-type display results in the least expensive digital counter/display system available.

Inexpensive Frequency Counter/ Tachometer

This circuit uses the low power ICM7555 (CMOS 555) to generate the gating, $\overline{STORE}$ and $\overline{RESET}$ signals as shown in Figure 19. To provide the gating signal, the timer is configured as an a stable multivibrator, using R_A, R_B and C to provide an output that is positive for approximately one second and negative for approximately 300µs - 500µs. The positive waveform time is given by $t_{WP} = 0.693 (R_A + R_B)C$ while the negative waveform is given by two = $0.693 R_BC$. The system is calibrated by using a 5MΩ potentiometer for R_A as a "coarse" control and a 1kΩ potentiometer for R_B as a "fine" control. CD40106Bs are used as a monostable multivibrator and reset time delay.

Tape Recorder Position Indicator/controller

The circuit in Figure 20 shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position.

In the tape recorder application, the LOAD REGISTER, $\overline{EQUAL}$ and $\overline{ZERO}$ outputs are used to control the recorder. To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the $\overline{EQUAL}$ output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the $\overline{ZERO}$ output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1MΩ resistor and 0.0047µF capacitor on the COUNT INPUT provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the COUNT INPUT of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

Precision Elapsed Time/Countdown Timer

The circuit in Figure 21 uses an ICM7213 precision one minute/one second timebase generator using a 4.1943MHz crystal for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the $\overline{EQUAL}$ output used to reset the counter. Note the 10k resistor connected between the LOAD COUNTER terminal and Ground. This resistor pulls the LOAD COUNTER input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used.

This technique may be used on any 3-level input. The 100kΩ pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, an ICM7555 timer may be used in a configuration like that shown in Figure 19 to generate a 1Hz reference.

8-Digit Up/down Counter

This circuit (Figure 22) shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments $\overline{a}$ or $\overline{b}$ is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but since the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize.

Precision Frequency Counter/Tachometer

The circuit shown in Figure 23 is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the STORE and RESET signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to V_{DD}, the gating time will be 0.1s; this will display tens of hertz at the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536MHz crystal), giving a 0.01s gating with Pin 11 connected to V_{DD}, and a 0.1s gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-dector. For faster updating, use 0.1s gating, and multiply the rotational frequency by 600.

Auto-tare System

This circuit uses the count-up and count-down functions of the ICM7217, controlled via the EQUAL and ZERO outputs, to count in SYNC with an ICL7109A and ICL7109D Converter as shown in Figure 24. By RESETing the ICM7217 on a "tare" value conversion, and STORE-ing the result of a true value conversion, an automatic fare subtraction occurs in the result.

The ICM7217 stays in step with the ICL7109 by counting up and down between 0 and 4095, for 8192 total counts, the same number as the ICL7109 cycle. See applications note No. A047 for more details.

TABLE 2. CONTROL INPUT DEFINITIONS ICM7217

INPUT	TERMINAL	VOLTAGE	FUNCTION
STORE	9	V_{DD} (or floating) V_{SS}	Output Latches Not Updated Output Latches Updated
UP/DOWN	10	V_{DD} (or floating) V_{SS}	Counter Counts Up Counter Counts Down
RESET	14	V_{DD} (or floating) V_{SS}	Normal Operation Counter Reset
LOAD COUNTER/ I/O OFF	12	Unconnected V_{DD} V_{SS}	Normal Operation Counter Loaded with BCD data BCD Port Forced to Hi Z Condition
LOAD REGISTER/ OFF	11	Unconnected V_{DD} V_{SS}	Normal Operation Register Loaded with BCD Data Display Drivers Disabled; BCD Port Forced to Hi Z Condition, mpx Counter Reset to D4; mpx Oscillator Inhibited
DISPLAY CONTrol	23 Common Anode 20 Common Cathode	Unconnected V_{DD} V_{SS}	Normal Operation Segment Drivers Disabled Leading Zero Blanking Inhibited

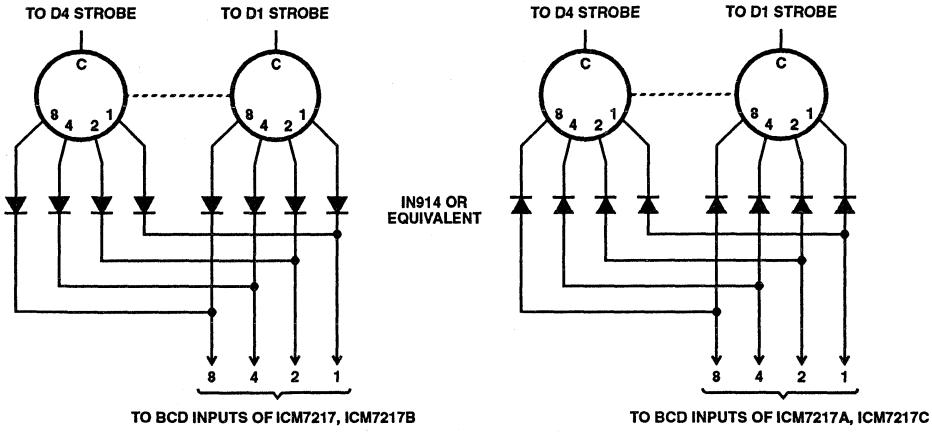


FIGURE 17. THUMBWHEEL SWITCH/DIODE CONNECTIONS

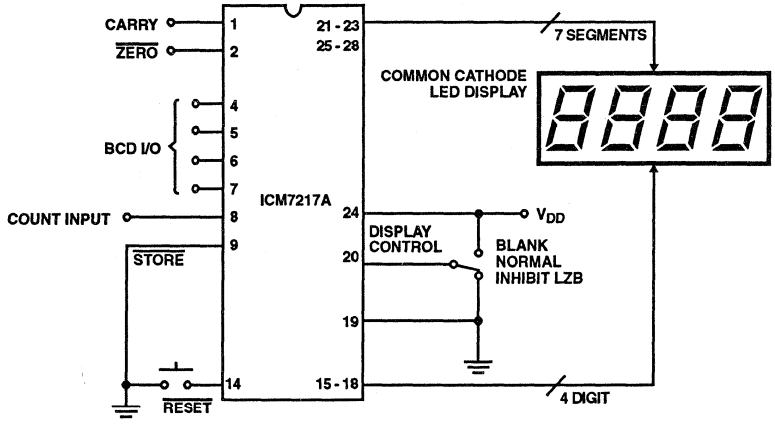


FIGURE 18. UNIT COUNTER

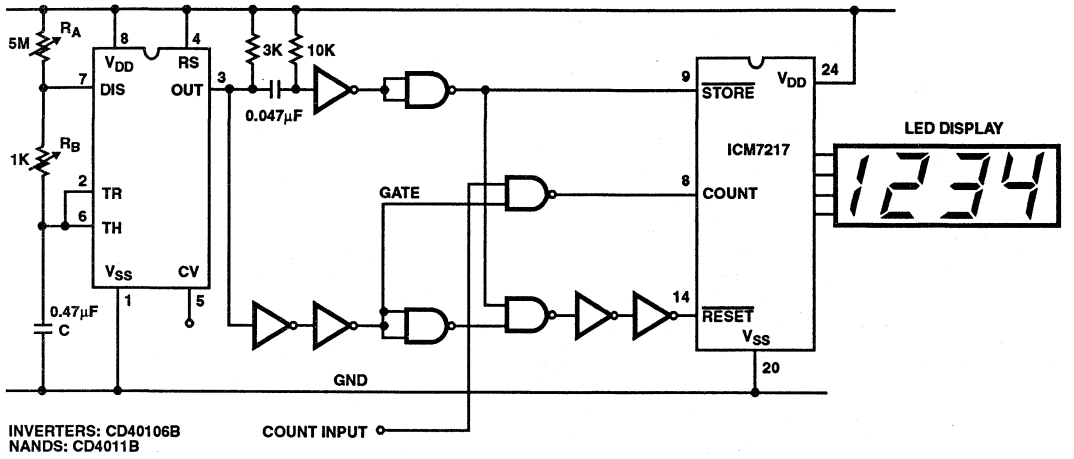


FIGURE 19A.

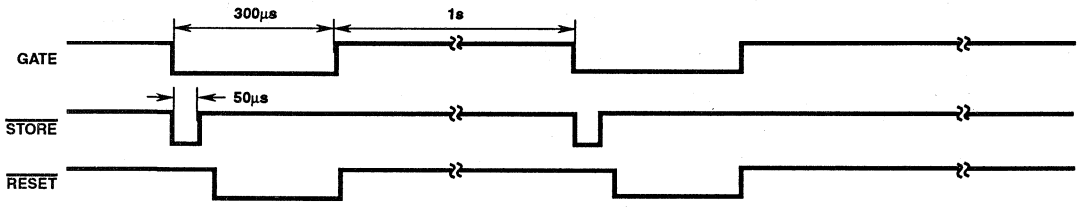


FIGURE 19B.

FIGURE 19. INEXPENSIVE FREQUENCY COUNTER

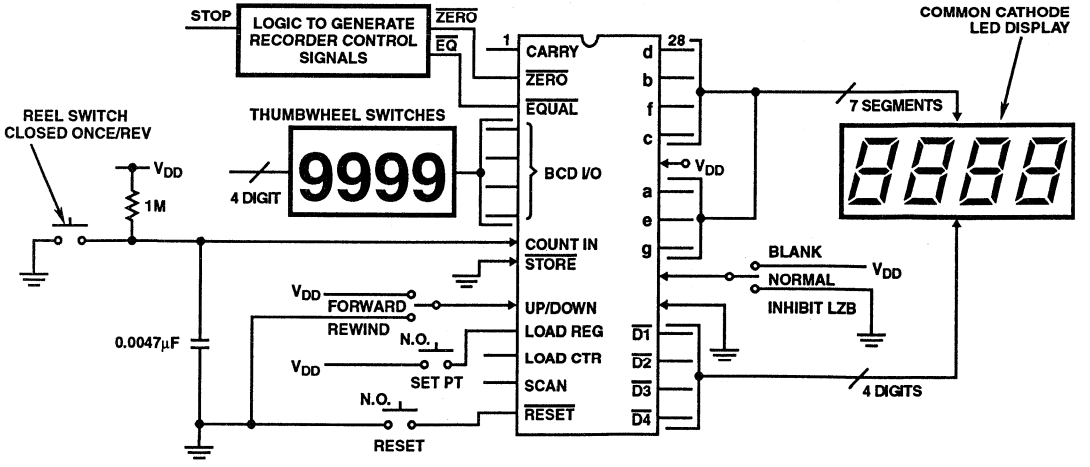


FIGURE 20. TAPE RECORDER POSITION INDICATOR

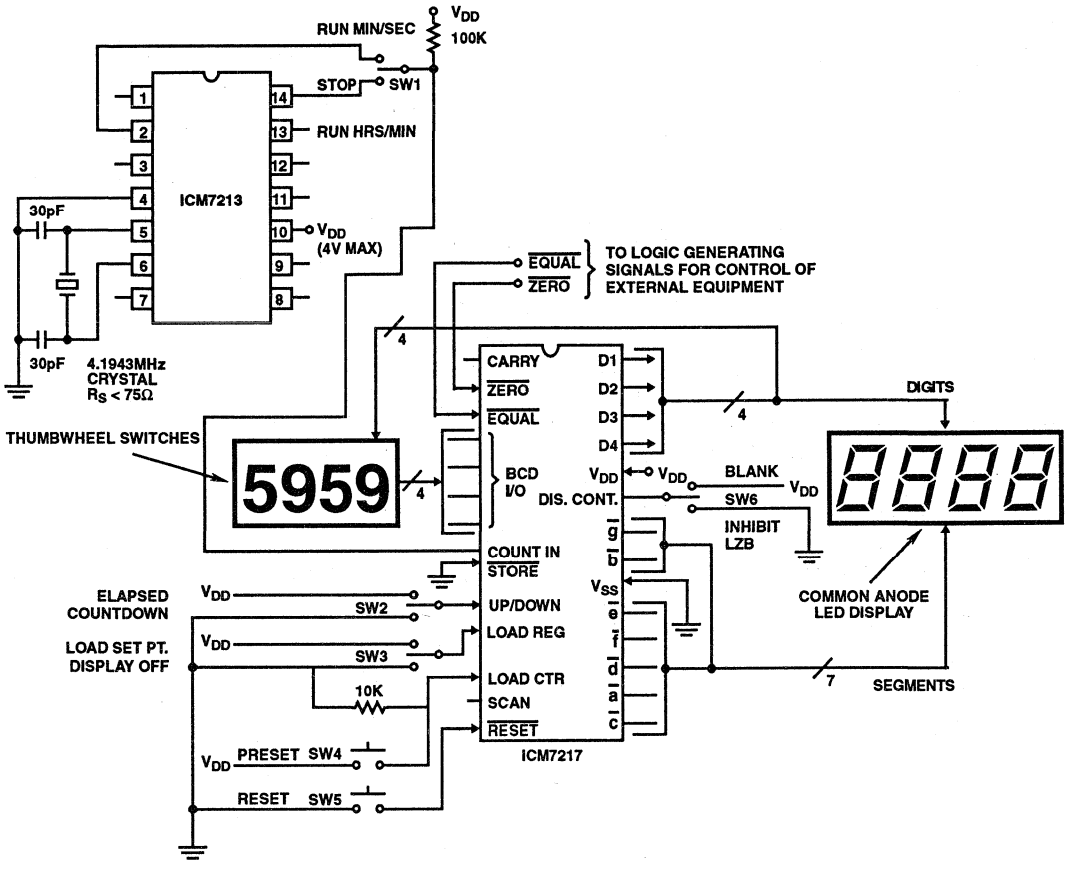


FIGURE 21. PRECISIONS TIMER

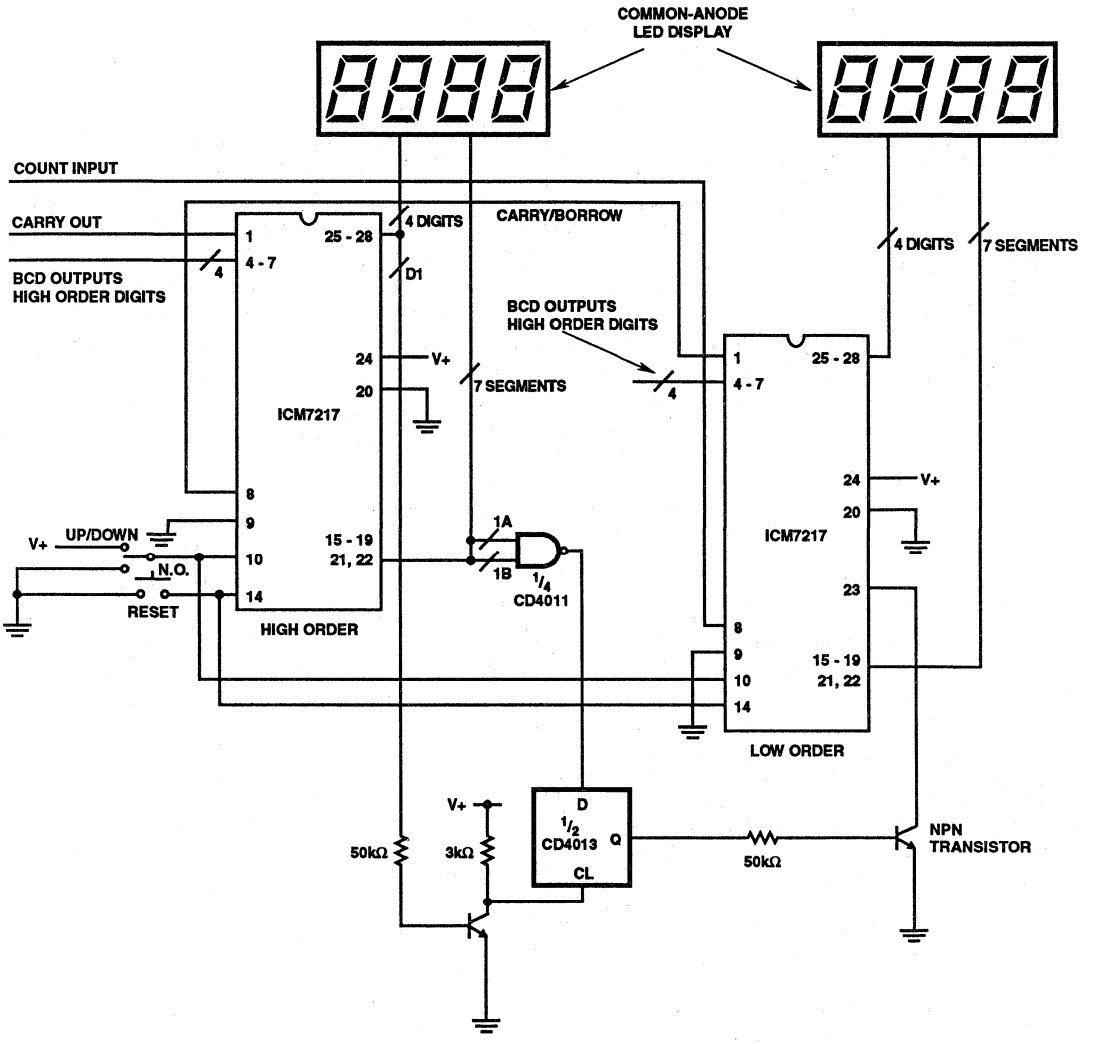


FIGURE 22. 8 DIGIT UP/DOWN COUNTER

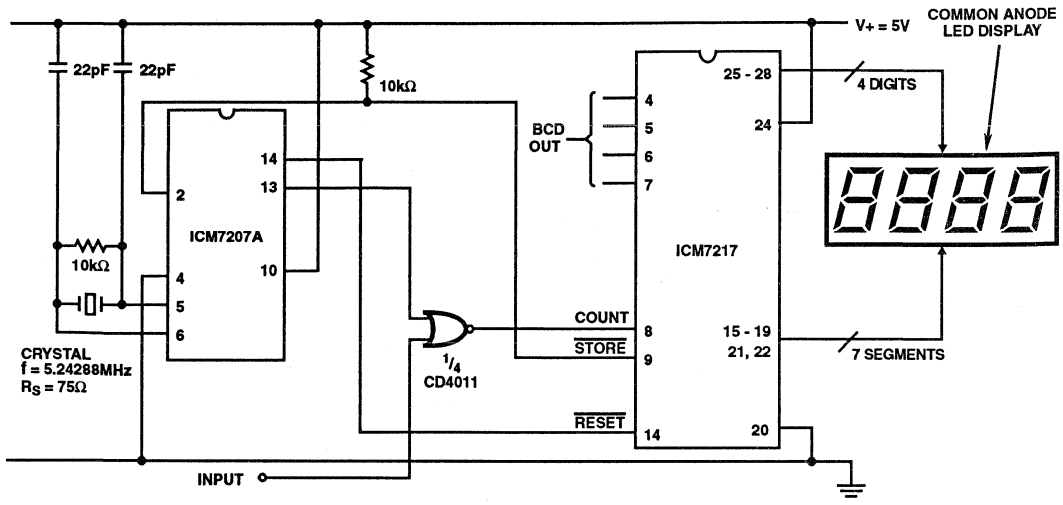


FIGURE 23. PRECISION FREQUENCY COUNTER (MHZ MAXIMUM)

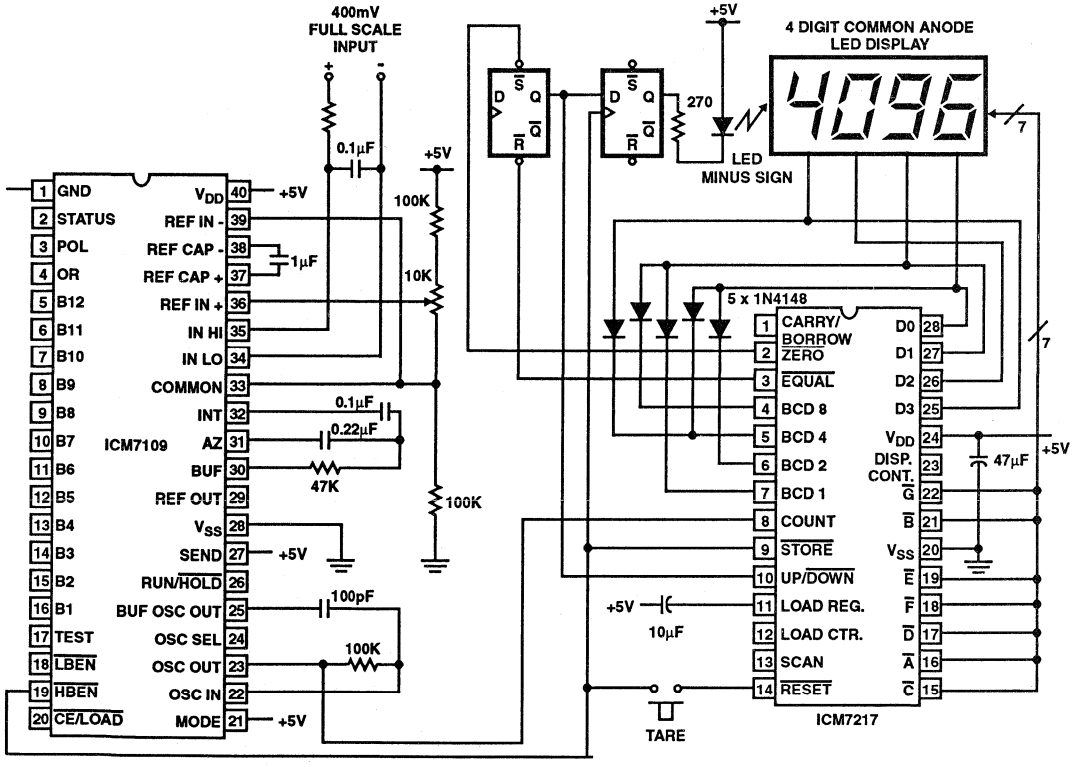


FIGURE 24. AUTO-TARE SYSTEM FOR A/D CONVERTER

HARRIS SEMICONDUCTOR

ICM7224

December 1993

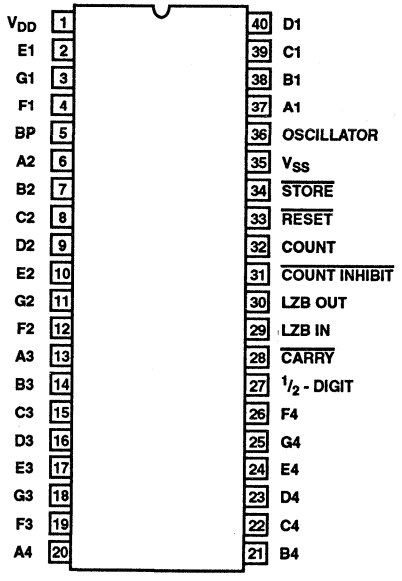
$4^1/_2$ Digit LCD Display Counter

Features

- **High Frequency Counting - Guaranteed 15MHz, Typically 25MHz at 5V**
- **Low Power Operation - Typically Less Than 100µW Quiescent**
- **$\overline{\text{STORE}}$ and $\overline{\text{RESET}}$ Inputs Permit Operation as Frequency or Period Counter**
- **True $\overline{\text{COUNT INHIBIT}}$ Disables First Counter Stage**
- **$\overline{\text{CARRY}}$ Output for Cascading Four-Digit Blocks**
- **Schmitt-Trigger on the COUNT Input Allows Operation in Noisy Environments or with Slowly Changing Inputs**
- **Leading Zero Blanking INput and OUTput for Correct Leading Zero Blanking with Cascaded Devices**
- **Provides Complete Onboard Oscillator and Divider Chain to Generate Backplane Frequency, or Backplane Driver May be Disabled Allowing Segments to be Slaved to a Master Backplane Signal**

Pinout

(PDIP, CDIP)
TOP VIEW



Description

The ICM7224 device is a high-performance CMOS $4^1/_2$ digit counter, including decoder, output latch, display driver, count inhibit, leading zero blanking, and reset circuitry.

The counter section provides direct static counting, guaranteed from DC to 15MHz, using a 5V ± 10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25MHz. The COUNT input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. The COUNT INHIBIT, STORE and RESET inputs allow a direct interface with the ICM7207 and ICM7207A to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The $\overline{\text{CARRY}}$ output allows the counter to be cascaded, while the Leading Zero Blanking INput and OUTput allows correct Leading Zero Blanking between four-decade blocks. The BackPlane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, necessary when using an eight or twelve digit, single backplane display.

These devices provide maximum count of 19999. The display drivers are not of the multiplexed type and each display segment has its own individual drive pin, providing high quality display outputs.

Ordering Information

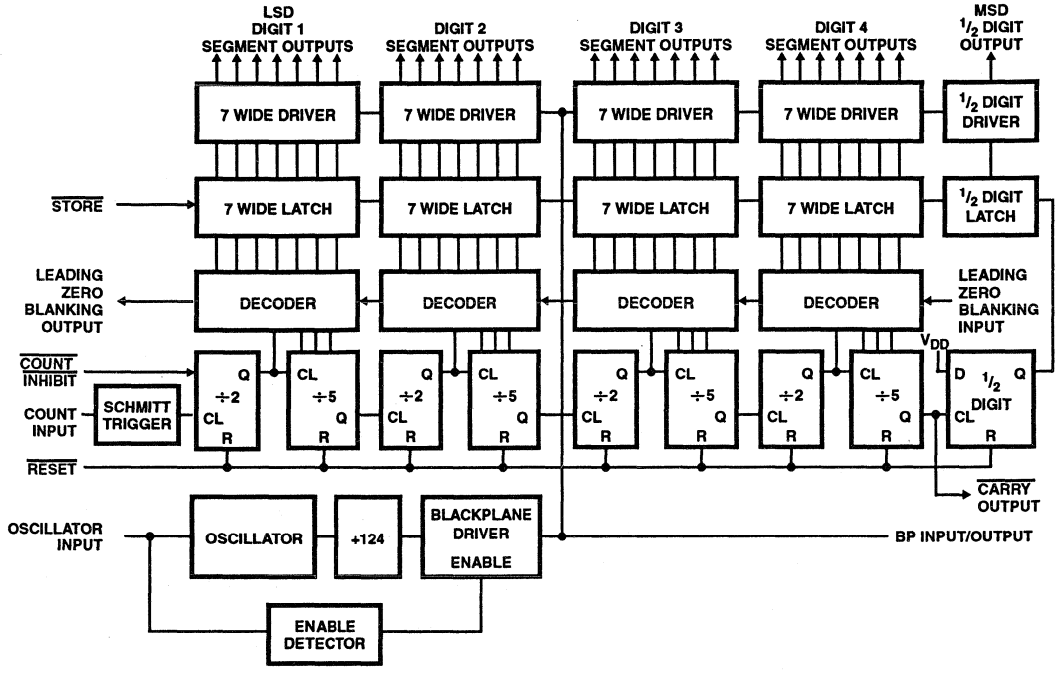
PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7224IPL	-25°C to +85°C	40 Lead Plastic DIP
ICM7224RIPL †	-25°C to +85°C	40 Lead Plastic DIP

† "R" Indicates Device With Reversed Leads Configuration.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3168**

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) 6.5V
Input Voltage (Any Terminal) (Note 1) .... (V_{DD} + 0.3V) to (V_{SS} - 0.3V)
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic Package ..... 50°C/W
Operating Temperature Range ..... -25°C to +85°C
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = 5V, V_{SS} = 0V, T_A = +25°C, Unless Otherwise Indicated

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Current, I_{DD}	Test Circuit, Display Blank	-	10	50	µA
Operating Supply Voltage Range (V_{DD} - V_{SS}), V_{SUPPLY}		3	-	6	V
OSCILLATOR Input Current, I_{OSCI}	Pin 36	-	±2	±10	µA
Segment Rise/Fall Time, t_R, t_F	C_{LOAD} = 200pF	-	0.5	-	µs
BackPlane Rise/Fall Time, t_R, t_F	C_{LOAD} = 5000pF	-	1.5	-	µs
Oscillator Frequency, f_{OSC}	Pin 36 Floating	-	19	-	kHz
Backplane Frequency, f_{BP}	Pin 36 Floating	-	150	-	Hz
Input Pullup Currents, I_P	Pins 29, 31,33, 34, V_{IN} = V_{DD} - 3V	-	10	-	µA
Input High Voltage, V_{IH}	Pins 29,31,33,34	3	-	-	V
Input Low Voltage, V_{IL}	Pins 29,31,33,34	-	-	1	V
$\overline{\text{COUNT}}$ Input Threshold, V_{CT}		-	2	-	V
$\overline{\text{COUNT}}$ Input Hysteresis, V_{CH}		-	0.5	-	V
Output High Current, I_{OH}	$\overline{\text{CARRY}}$ Pin 28 Leading Zero Blanking OUT Pin 30 V_{OUT} = V_{DD} - 3V	-350	-500	-	µA
Output Low Current, I_{OL}	$\overline{\text{CARRY}}$ Pin 28 Leading Zero Blanking OUT Pin 30 V_{OUT} = +3V	350	500	-	µA
Count Frequency, f_{COUNT}	4.5V < V_{DD} < 6V	0	-	15	MHz
$\overline{\text{STORE}}$, $\overline{\text{RESET}}$ Minimum Pulse Width, t_S, t_R		3	-	-	µs

NOTE:

1. Due to the SCR structure inherent in the CMOS process, connecting any terminal to voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from sources operating on a different power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224 be turned on first.

Timing Waveforms

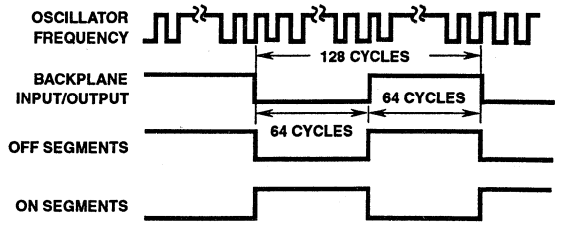


FIGURE 1. ICM7224 DISPLAY WAVEFORMS

Typical Performance Curves

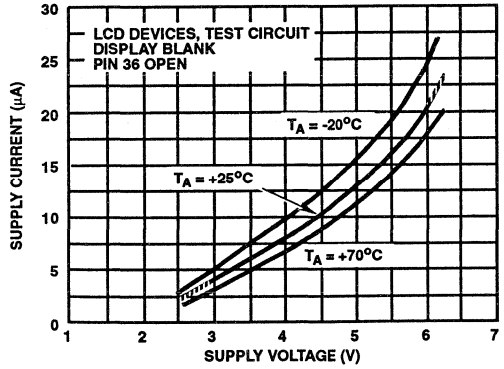


FIGURE 2. OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

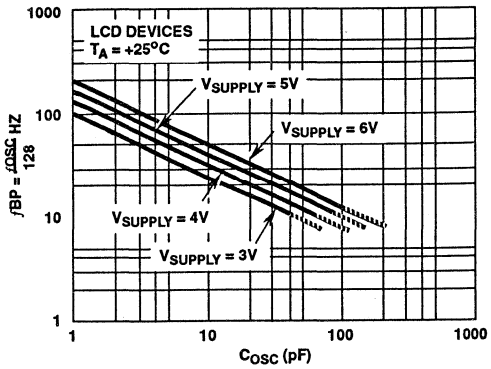


FIGURE 3. BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR C_{OSC}

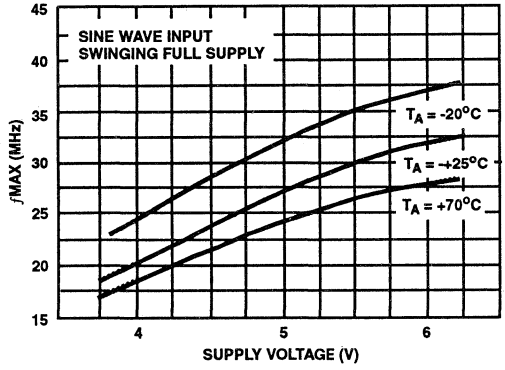


FIGURE 4. MAXIMUM COUNT FREQUENCY (TYPICAL) AS A FUNCTION OF SUPPLY VOLTAGE

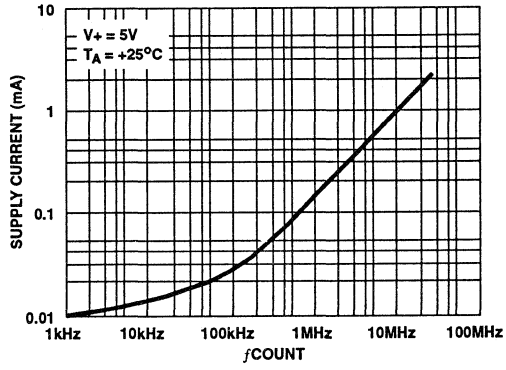


FIGURE 5. SUPPLY CURRENT AS A FUNCTION OF COUNT FREQUENCY

TABLE 1. CONTROL INPUT DEFINITIONS

TERMINAL	INPUT	VOLTAGE	FUNCTION
29	Leading Zero Blanking INput	V_{DD} or Floating	Leading Zero Blanking Enabled
		V_{SS}	Leading Zeroes Displayed
31	$\overline{\text{COUNT INHIBIT}}$	V_{DD} or Floating	Counter Enabled
		V_{SS}	Counter Disabled
33	$\overline{\text{RESET}}$	V_{DD} or Floating	Inactive
		V_{SS}	Counter Reset to 0000
34	$\overline{\text{STORE}}$	V_{DD} or Floating	Output Latches not Updated
		V_{SS}	Output Latches Updated

Control Input Definitions

In Table 1, V_{DD} and V_{SS} are considered to be normal operating input logic levels. Actual input low and high levels are specified in the Operating Characteristics. For lowest power consumption, input signals should swing over the full supply.

Detailed Description

The ICM7224 provides outputs suitable for driving conventional $4^1/_2$ digit by seven segment LCD displays. It includes 29 individual segment drivers, a backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency (See Functional Block Diagram).

The segment and backplane drivers each consist of a CMOS inverter, with the n-channel and p-channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any D.C. component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output can be disabled by connecting the OSCILLATOR input (pin 36) to V_{SS}. This synchronizes the 29 segment outputs directly with a signal input at the BP terminal (pin 5) and allows cascading of several slave devices to the backplane output of one master device. The backplane may also be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200pF (comparable to one additional segment). The limitation on the number of devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption, is to keep the rise and fall times less than about 5 microseconds. The backplane driver of one device should handle the back-plane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5µs (i.e., 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7224 devices be slaved to it.

This external backplane signal should be capable of driving very large capacitive loads with short (1-2µs) rise and fall times. The maximum frequency for a backplane signal should be about 150Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 19kHz, at microampere power levels. The oscillator frequency is divided by 126 to provide the backplane frequency, which will be approximately 150Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor between the OSCillator terminal (pin 36) and V_{DD}; see the plot of oscillator/back-plane frequency in "Typical Performance Curves" for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a D.C. component to the display). This can be done by driving the OSCILLATOR input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

Counter Section

The ICM7224 implements a four-digit ripple carry resettable counter, including a Schmitt trigger on the COUNT input and a $\overline{\text{CARRY}}$ output. Also included is an extra D-type flip-flop, clocked by the $\overline{\text{CARRY}}$ signal which controls the half-digit segment driver. This output driver can be used as either a true half-digit or as an overflow indicator. The counter will increment on the negative-going edge of the signal at the COUNT input, while the $\overline{\text{CARRY}}$ output provides a negative-going edge following the count which increments the counter from 9999 to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the $\overline{\text{RESET}}$ terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half-digit is set, and subsequent $\overline{\text{CARRY}}$ outputs will not be affected.

A negative level at the $\overline{\text{COUNT INHIBIT}}$ input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true inhibit, not sensitive to the state of the COUNT input, which prevents false counts that can result from using a normal logic gate to prevent counting.

Each decade of the counter directly drives a four-to-seven segment decoder which develops the required output data. The output data is latched at the driver. When the $\overline{\text{STORE}}$ pin is low, these latches are updated, and when it is high or floating, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the Leading Zero Blanking INput is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When it is low, or the half-digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The Leading Zero Blanking OUTput is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked; this can only occur when the Leading Zero Blanking INput is at a positive level and the half-digit is not set.

For example, in an eight-decade counter with overflow using two ICM7224 devices, the Leading Zero Blanking OUTput of the high order digit would be connected to the Leading Zero Blanking INput of the low order digit device. This will assure correct leading zero blanking for all eight digits.

The $\overline{\text{STORE}}$, $\overline{\text{RESET}}$, $\overline{\text{COUNT INHIBIT}}$, and Leading Zero Blanking INputs are provided with pullup devices, so that they may be left open when a positive level is desired. The $\overline{\text{CARRY}}$ and Leading Zero Blanking OUTputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of the devices in four-digit blocks.

Applications

Figure 8 shows an 8 digit precision frequency counter. The circuit uses two ICM7224s cascaded to provide an 8 digit display. Backplane output of the second device is disabled and is driven by the first device. The $^1/_2$ digit output of the second device is used for overflow indication. The input signal is fed to the first device and the COUNT input of the second is driven by the $\overline{\text{CARRY}}$ output of the first. Notice that leading zero blanking is controlled on the second device and the LZB OUT of the second one is tied to LZB IN of the first one. An ICM7207A device is used as a timebase generator and frequency counter controller. It generates count window, store and reset signals which are directly compatible with ICM7224 inputs (notice the need for an inverter at $\overline{\text{COUNT INHIBIT}}$ input). The ICM7207A provides two count window signals (1s and 0.1s gating) for displaying frequencies in Hz or tens of Hz (x10Hz).

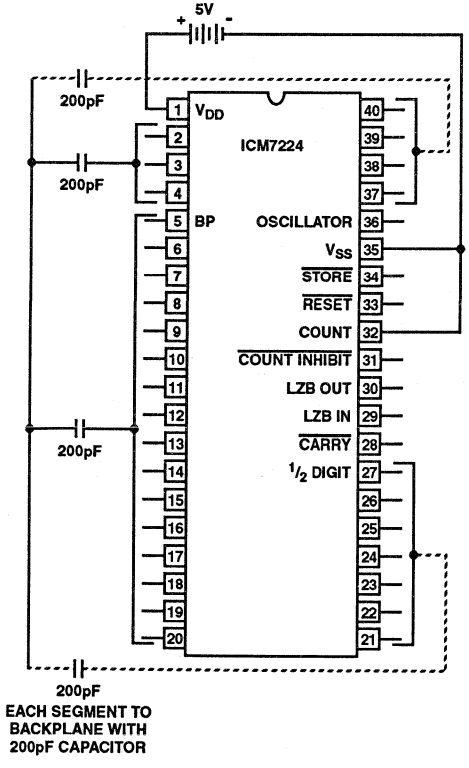
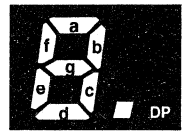


FIGURE 6. TEST CIRCUIT



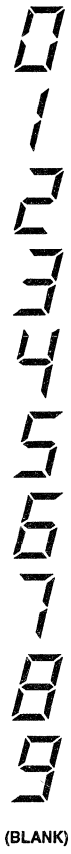


FIGURE 7. SEGMENT ASSIGNMENT AND DISPLAY FONT

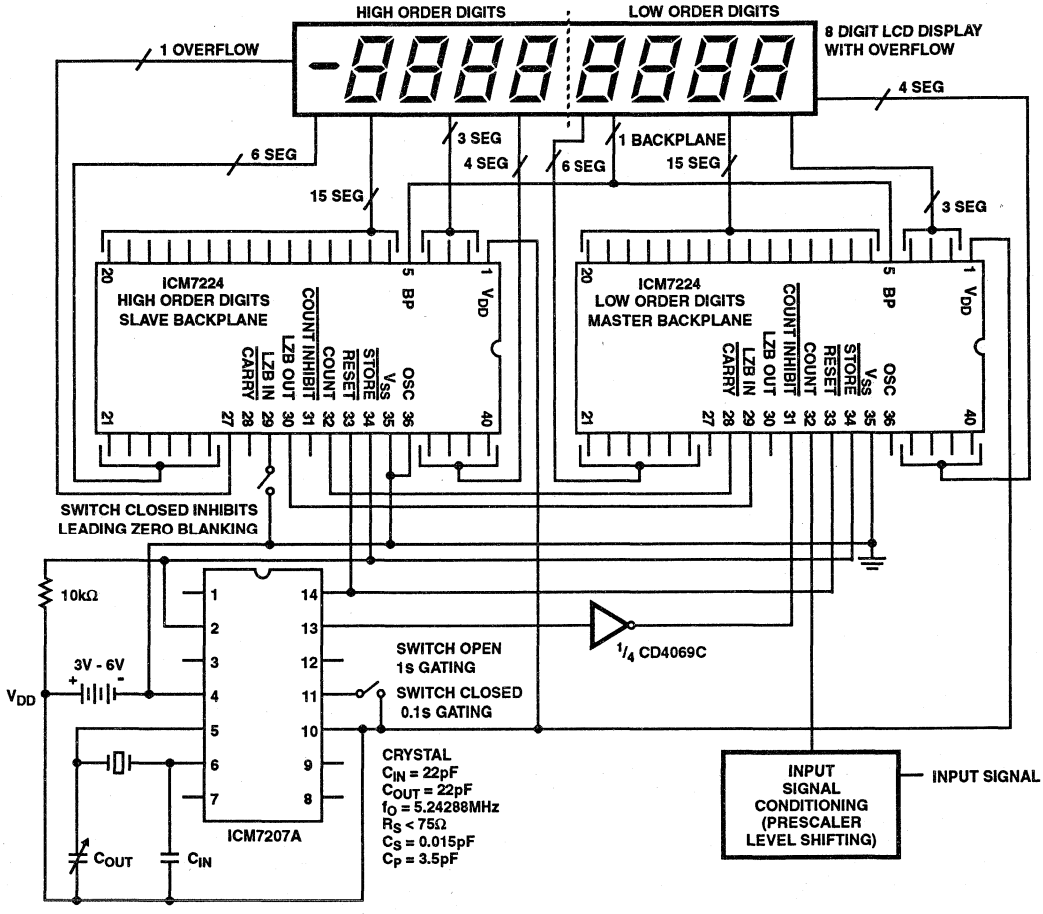


FIGURE 8. EIGHT-DIGIT PRECISION FREQUENCY COUNTER

HARRIS SEMICONDUCTOR

ICM7226A
ICM7226B

8-Digit Multi-Function Frequency Counter/Timers

December 1993

Features

- CMOS Design for Very Low Power
- Output Drivers Directly Drive Both Digits and Segments of Large 8 Digit LED Displays
- Measures Frequencies from DC to 10MHz; Periods from 0.5µs to 10s
- Stable High Frequency Oscillator uses either 1MHz or 10MHz Crystal
- Both Common Anode and Common Cathode Available
- Control Signals Available for External Systems Interfacing
- Multiplexed BCD Outputs

Applications

- Frequency Counter
- Period Counter
- Unit Counter
- Frequency Ratio Counter
- Time Interval Counter

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7226AIJL	-25°C to +85°C	40 Lead Ceramic DIP
ICM7226BIPL	-25°C to +85°C	40 Lead Plastic DIP

Description

The ICM7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8-decade data counter and latches, a 7-segment decoder, digit multiplexer and segment and digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7226 can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The devices require either a 10MHz or 1MHz quartz crystal timebase, or if desired an external timebase can also be used. For period and time interval, the 10MHz timebase gives a 0.1µs resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01s, 0.1s, 1s and 10s. With a 10s accumulation time, the frequency can be displayed to a resolution of 0.1Hz. There is 0.2s between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

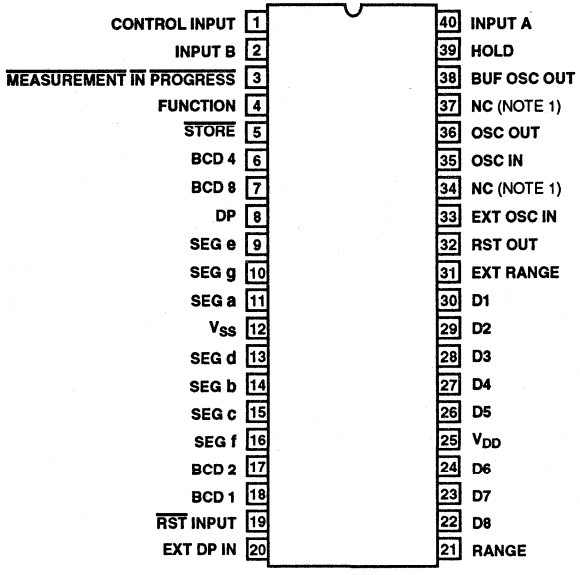
Leading zero blanking has been incorporated with frequency display in kHz and time in µs. The display is multiplexed at a 500Hz rate with a 12.2% duty cycle for each digit. The ICM7226A is designed for common anode displays with typical peak segment currents of 25mA, and the ICM7226B is designed for common cathode displays with typical segment currents of 12mA. In the display off mode, both digit drivers and segment drivers are turned off, allowing the display to be used for other functions.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

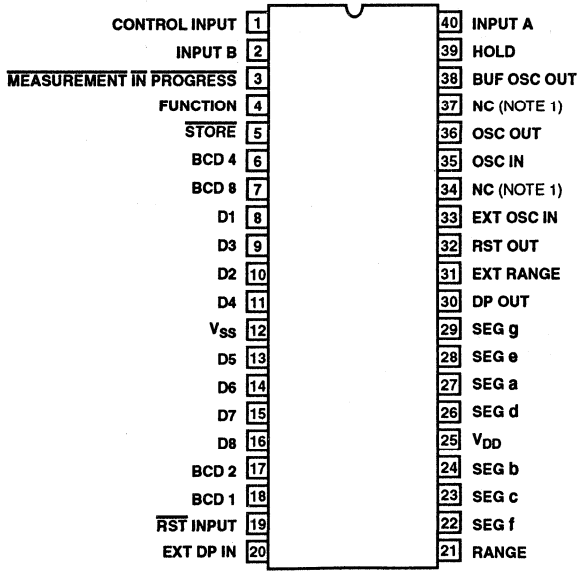
File Number 3169

Pinouts

ICM7226A
COMMON ANODE (CDIP)
TOP VIEW



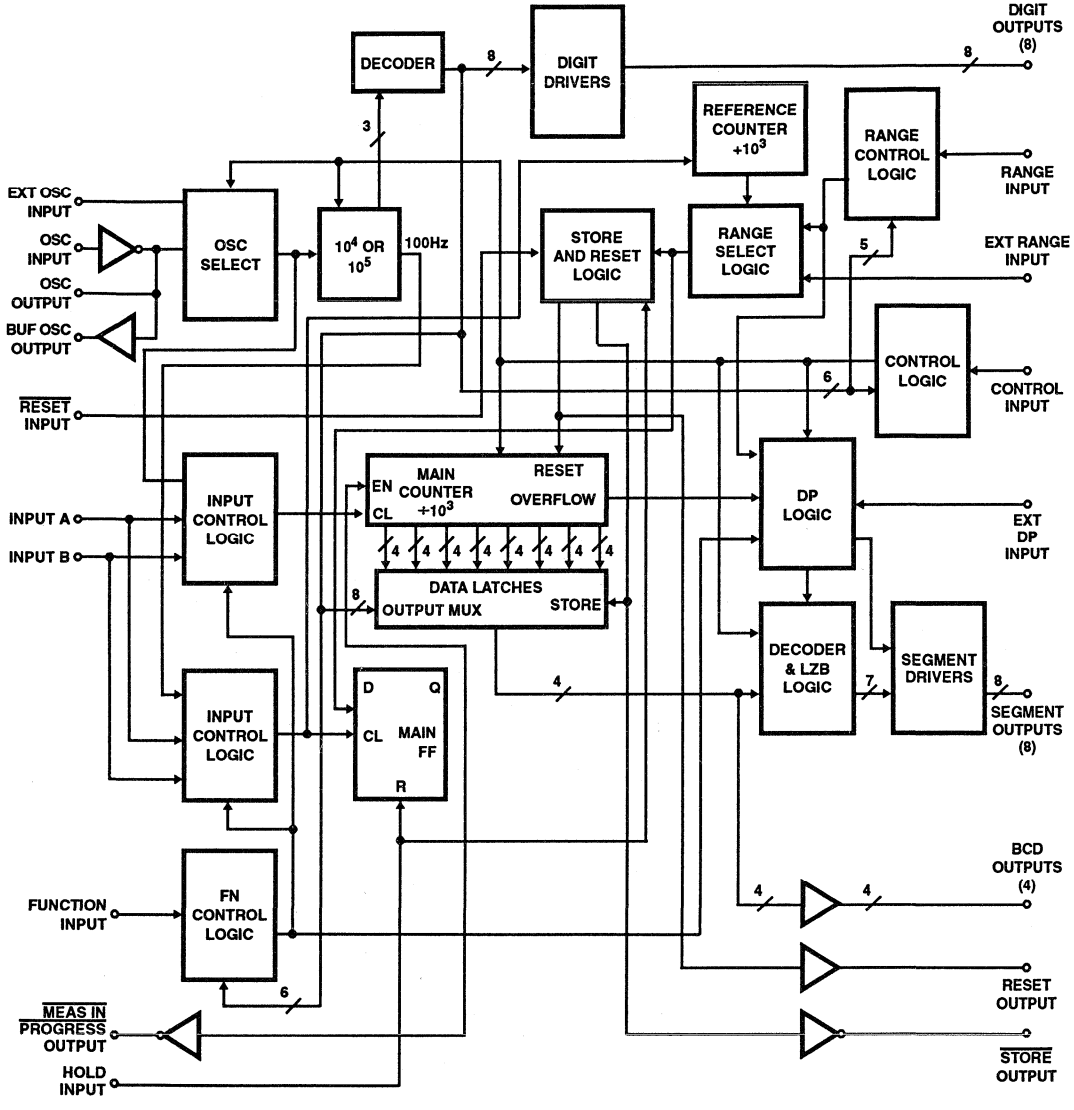
ICM7226B
COMMON CATHODE (PDIP)
TOP VIEW



NOTE:

1. For maximum frequency stability, connect to V_{DD} or V_{SS}

Functional Block Diagram



Absolute Maximum Ratings

Maximum Supply Voltage (V_{DD} - V_{SS}) 6.5V
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
Voltage On Any Input or
Output Terminal (Note 1) ..... (V_{DD} +0.3V) to (V_{SS} -0.3V)
Storage Temperature Range ..... -55°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Ceramic DIP Package	45°C/W	15°C/W
Plastic DIP Package	50°C/W	-

Junction Temperature
Ceramic DIP Package ..... +175°C
Plastic DIP Package ..... +150°C
Operating Temperature Range ..... -25°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

V_{DD} = 5.0V, T_A = +25°C, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Current, I_{DD}	Display Off, Unused Inputs to V_{SS}	-	2	5	mA
Supply Voltage Range (V_{DD} -V_{SS}), V_{SUPPLY}	-25°C < T_A < +85°C, INPUT A, INPUT B Frequency at f_{MAX}	4.75	-	6.0	V
Maximum Frequency INPUT A, Pin 40, $f_{A(MAX)}$	-25°C < T_A < +85°C 4.75V < V_{DD} < 6.0V, Figure 9 Function = Frequency, Ratio, Unit Counter	10	14	-	MHz
	Function = Period, Time Interval	2.5	-	-	MHz
Maximum Frequency INPUT B, Pin 2, $f_{B(MAX)}$	-25°C < T_A < +85°C 4.75V < V_{DD} < 6.0V, Figure 10	2.5	-	-	MHz
Minimum Separation INPUT A to INPUT B, Time Interval Function	-25°C < T_A < +85°C 4.75V < V_{DD} < 6.0V, Figure 1	250	-	-	ns
Oscillator Frequency and External Oscillator Frequency, f_{OSC}	-25°C < T_A < +85°C 4.75V < V_{DD} < 6.0V	0.1	-	10	MHz
Oscillator Transconductance, g_M	V_{DD} -4.75V, T_A = +85°C	2000	-	-	µS
Multiplex Frequency, f_{MUX}	f_{OSC} = 10MHz	-	500	-	Hz
Time Between Measurements	f_{OSC} = 10MHz	-	200	-	ms
Input Rate of Charge, dV_{IN}/dt	Inputs A, B	-	15	-	mV/µs
Input Voltages: Pins 2, 19, 33, 39, 40, 35					
Input Low Voltage, V_{IL}	-25°C < T_A < +85°C	-	-	1.0	V
Input High Voltage, V_{IH}		3.5	-	-	V
Pins 2, 39, 40, Input Leakage, A, B, I_{ILK}		-	-	20	µA
Input Resistance to V_{DD} Pins 19, 33, R_{IN}	V_{IN} = V_{DD} -1.0V	100	400	-	kΩ
Input Resistance to V_{SS} Pin 31, R_{IN}	V_{IN} = +1.0V	50	100	-	kΩ
Output Current					
Low Output Current, Pins 3, 5-7, 17, 18, 32, 38, I_{OL}	V_{OL} = +0.4V	400	-	-	µA
High Output Current, Pins 5-7, 17, 18, 32, H_{OL}	V_{OH} = +2.4V	100	-	-	µA
High Output Current, Pins 3, 38, H_{OL}	V_{OH} = V_{DD} -0.8V	265	-	-	µA
ICM7226A					
Segment Driver: Pins 8-11, 13-16					
Low Output Current, I_{OL}	V_O = +1.5V	25	35	-	mA
High Output Current, I_{OH}	V_O = V_{DD} -1.0V	-	100	-	µA
Multiplex Inputs: Pins 1, 4, 20, 21					
Input Low Voltage, V_{IL}		-	-	0.8	V
Input High Voltage, V_{IH}		2.0	-	-	V
Input Resistance to V_{SS}, R_{IN}	V_{IN} = +1.0V	50	100	-	kΩ

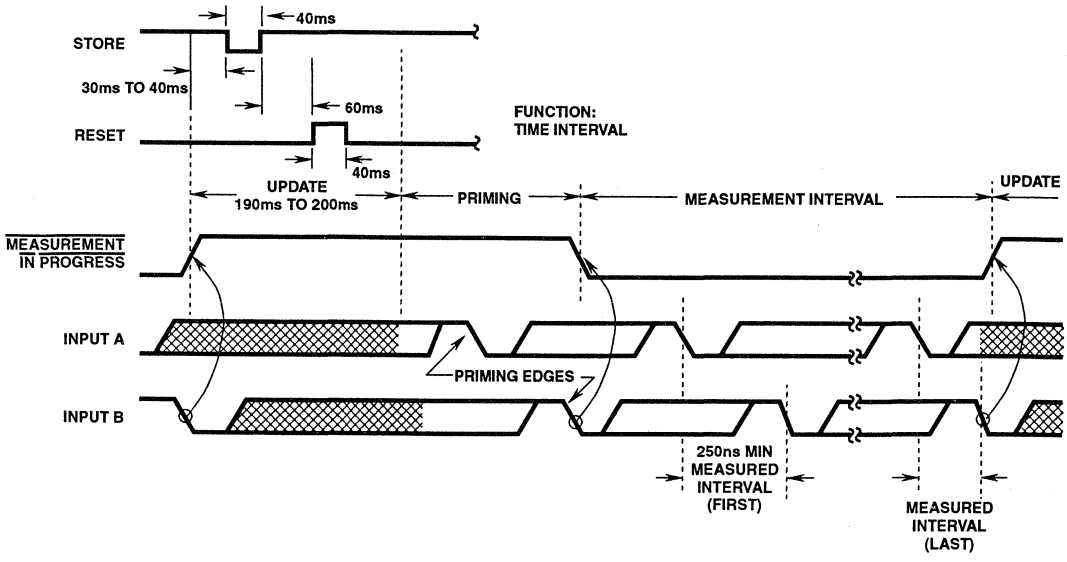
Electrical Specifications V_{DD} = 5.0V, T_A = +25°C, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Digit Driver: Pins 22-24, 26-30					
Low Output Current, I_{OL}	V_O = +1.0V	-	-0.3	-	mA
High Output Current, I_{OH}	$V_O = V_{DD}$ -2.0V	150	180	-	mA
ICM7226B					
Segment Driver: Pins 22-24, 26-30					
Leakage Current, I_L	$V_O = V_{SS}$	-	-	10	µA
High Output Current, I_{OH}	$V_O = V_{DD}$ -2.0V	10	15	-	mA
Multiplex Inputs: Pins 1, 4, 20, 21					
Input Low Voltage, V_{IL}		-	-	V_{DD}-2.0	V
Input High Voltage, V_{IH}		V_{DD}-0.8	-	-	V
Input Resistance to V_{SS}, R_{IN}	$V_{IN} = V_{DD}$ -1.0V	100	360	-	kΩ
Digit Driver: Pins 8-11, 13-16					
Low Output Current, I_{OL}	V_O = +1.0V	50	75	-	mA
High Output Current, I_{OH}	$V_O = V_{DD}$ -2.5V	-	100	-	µA

NOTES:

1. Destructive latchup may occur if input signals are applied before the power supply is established or if inputs or outputs are forced to voltages exceeding V_{DD} or V_{SS} by 0.3V.
2. Assumes all leads soldered or welded to PC board and free air flow.
3. Typical values are not tested.

Timing Waveform



NOTE:

1. If range is set to 1 event, first and last measured interval will coincide.

FIGURE 1. WAVEFORMS FOR TIME INTERVAL MEASUREMENT (OTHERS ARE SIMILAR, BUT WITHOUT PRIMING PHASE)

Typical Performance Curves

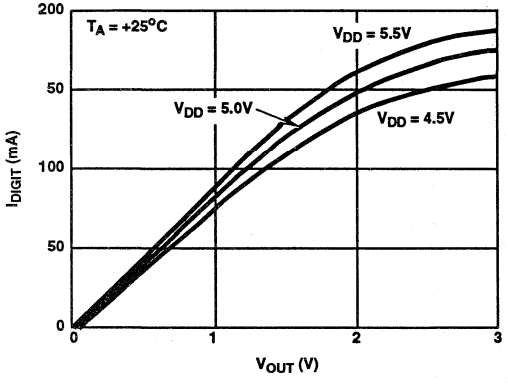


FIGURE 2. ICM7226B TYPICAL I_{DIGIT} vs V_{OUT}

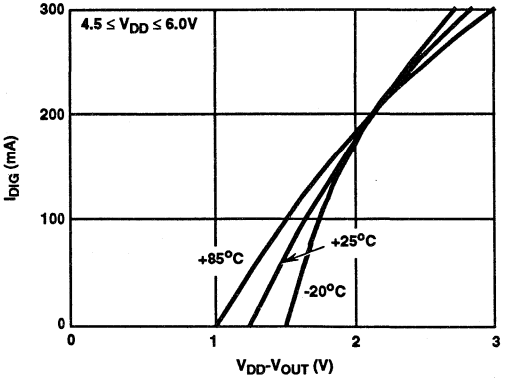


FIGURE 3. ICM7226A TYPICAL I_{DIG} vs V_{DD}-V_{OUT}

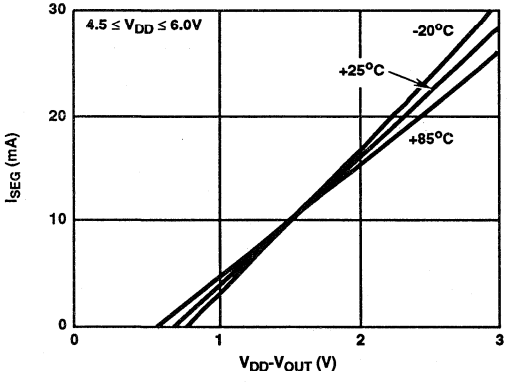


FIGURE 4. ICM7226B TYPICAL I_{SEG} vs V_{DD}-V_{OUT}

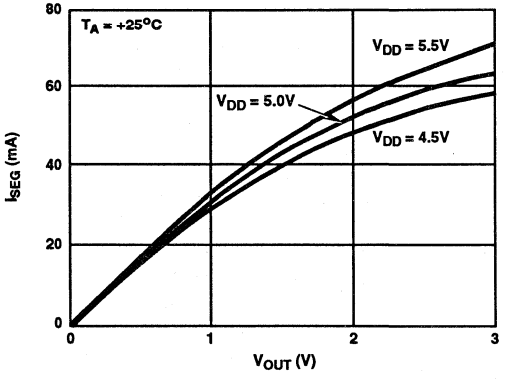


FIGURE 5. ICM7226A TYPICAL I_{SEG} vs V_{OUT}

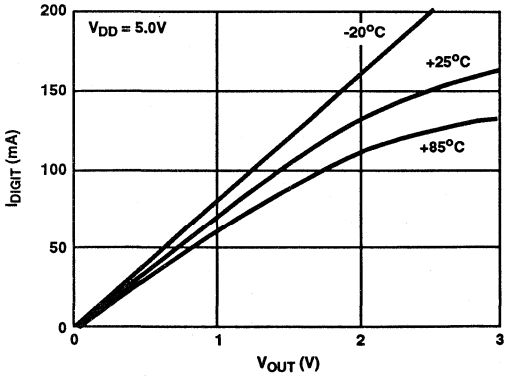


FIGURE 6. ICM7226B TYPICAL I_{DIGIT} vs V_{OUT}

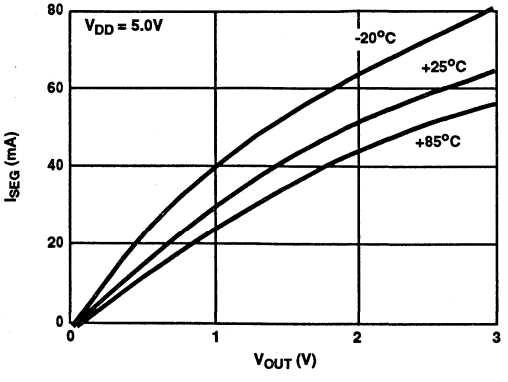


FIGURE 7. ICM7226A TYPICAL I_{SEG} vs V_{OUT}

Typical Performance Curves (Continued)

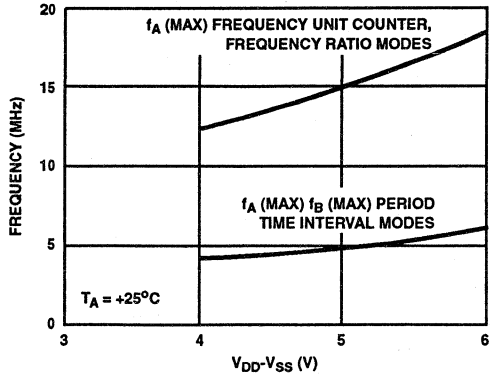


FIGURE 8. f_A(MAX), f_B(MAX) AS A FUNCTION OF SUPPLY

Description

INPUTS A and B

The signal to be measured is applied to INPUT A in frequency period, unit counter, frequency ratio and time interval modes. The other input signal to be measured is applied to INPUT B in frequency ratio and time interval. f_A should be higher than f_B during frequency ratio.

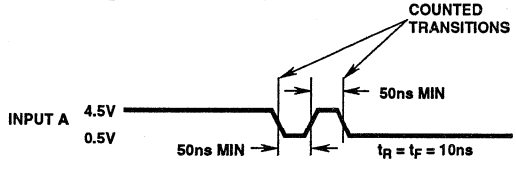


FIGURE 9. WAVEFORM FOR GUARANTEED MINIMUM f_A(MAX) FUNCTION = FREQUENCY, FREQUENCY RATIO, UNIT COUNTER

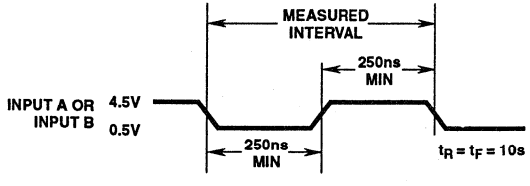


FIGURE 10. WAVEFORM FOR GUARANTEED MINIMUM f_B(MAX) AND f_A(MAX) FOR FUNCTION = PERIOD AND TIME INTERVAL

Both inputs are digital inputs with a typical switching threshold of 2.0V at V_{DD} = 5.0V and input impedance of 250kΩ. For optimum performance, the peak to peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs

Note that the amplitude of the input should not exceed the device supply (above the V_{DD} and below the V_{SS}) by more than 0.3V, otherwise the device may be damaged.

Multiplexed Inputs

The FUNCTION, RANGE, CONTROL and EXTERNAL DECIMAL POINT inputs are time multiplexed to select the function desired. This is achieved by connecting the appropriate Digit driver output to the inputs. The function, range and control inputs must be stable during the last half of each digit output, (typically 125μs). The multiplexed inputs are active high for the common anode ICM7226A and active low for the common cathode ICM7226B.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the **unit counter** mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10kΩ resistor should be placed in series with the multiplexed inputs as shown in the application circuits.

Table 1 shows the functions selected by each digit for these inputs.

TABLE 1. MULTIPLEXED INPUT FUNCTIONS

	FUNCTION	DIGIT
FUNCTION INPUT Pin 4	Frequency	D1
	Period	D8
	Frequency Ratio	D2
	Time Interval	D5
	Unit Counter	D4
	Oscillator Frequency	D3
RANGE INPUT Pin 21	0.01s/1 Cycle	D1
	0.1s/10 Cycles	D2
	1s/100 Cycles	D3
	10s/1K Cycles	D4
	Enable External Range Input	D5
CONTROL INPUT Pin 1	Display Off	D4 and Hold
	Display Test	D8
	1MHz Select	D2
	External Oscillator Enable	D1
	External Decimal Point Enable	D3
External DP INPUT Pin 20	Decimal point is output for same digit that is connected to this input.	

Function Input

The six functions that can be selected are: **Frequency, Period, Time Interval, Unit Counter, Frequency Ratio** and **Oscillator Frequency.**

The implementation of different functions is done by routing the different signals to two counters, called "Main Counter" and "Reference Counter". A simplified block diagram of the device for functions realization is shown in Figure 11. Table 2 shows which signals will be routed to each counter in different cases. The output of the Main Counter is the information which goes to the display. The Reference Counter divides its input to 1, 10, 100 and 1000. One of these outputs will be selected through the range selector and drive the enable input of the Main Counter. This means that the Reference Counter, along with its' associated blocks, directs the Main Counter to begin counting and determines the length of the counting period. Note that Figure 11 does not show the complete functional diagram (See the Functional Block Diagram). After the end of each counting period, the output of the Main Counter will be latched and displayed, then the counter will be reset and a new measurement cycle will begin. Any change in the FUNCTION INPUT will stop the present measurement without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the FUNCTION INPUT is changed. In all cases, the 1-0 transitions are counted or timed.

TABLE 2. INPUT ROUTING

FUNCTION	MAIN COUNTER	COUNTER
Frequency (f_A)	Input A	100Hz (Oscillator $\div 10^5$ or 10^4)
Period (t_A)	Oscillator	Input A
Ratio (f_A/f_B)	Input A	Input B
Time Interval (A→B)	Oscillator	Input A Input B
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (f_{OSC})	Oscillator	100Hz (Oscillator $\div 10^5$ or 10^4)

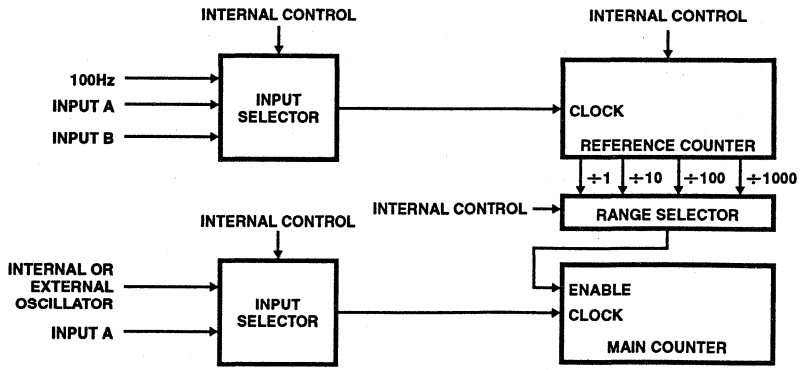


FIGURE 11. SIMPLIFIED BLOCK DIAGRAM OF FUNCTIONS IMPLEMENTATION

Frequency - In this mode input A is counted by the Main Counter for a precise period of time. This time is determined by the time base oscillator and the selected range. For the 10MHz (or 1MHz) time base, the resolutions are 100Hz, 10Hz, 1Hz and 0.1Hz. The decimal point on the display is set for kHz reading.

Period - In this mode, the timebase oscillator is counted by the Main Counter for the duration of 1,10,100 or 1000 (range selected) periods of the signal at input A. A 10MHz timebase gives resolutions of 0.1µs to 0.0001µs for 1000 periods averaging. Note that the maximum input frequency for period measurement is 2.5MHz.

Frequency Ratio - In this mode, the input A is counted by the Main Counter for the duration of 1,10,100 or 1000 (range selected) periods of the signal at input B. The frequency at input A should be higher than input B for meaningful result. The result in this case is unitless and its resolution can go up to 3 digits after decimal point.

Time Interval - In this mode, the timebase oscillator is counted by the Main Counter for the duration of a 1-0 transition of input A until a 1-0 transition of input B. This means input A starts the counting and input B stops it. If other ranges, except 0.01s/1 cycle are selected the sequence of input A and B transitions must happen 10,100 or 1000 times until the display becomes updated; note this when measuring long time intervals to give enough time for measurement completion. The resolution in this mode is the same as for period measurement. See the Time Interval Measurement section also.

Unit Counter - In this mode, the Main Counter is always enabled. The input A is counted by the Main Counter and displayed continuously.

Oscillator Frequency - In this mode, the device makes a frequency measurement on its timebase. This is a self test mode for device functionality check. For 10MHz timebase the display will show 10000.0, 10000.00, 10000.000 and Overflow in different ranges.

Range Input

The RANGE INPUT selects whether the measurement period is made for 1,10,100 or 1000 counts of the Reference Counter or it is controlled by EXT RANGE input. As it is shown in Table 1, this gives different counting windows for frequency measurement and various cycles for other modes of measurement.

In all functional modes except Unit Counter, any change in the RANGE INPUT will stop the present measurement without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the RANGE INPUT is changed.

Control Input

Unlike the other multiplexed inputs, to which only one of the digit outputs can be connected at a time, this input can be tied to different digit lines to select combination of controls. In this case, isolation diodes must be used in digit lines to avoid crosstalk between them (see Figure 19). The direction of diodes depends on the device version, common anode or common cathode. For maximum noise immunity at this input, in addition to the 10K resistor which was mentioned before, a 39pF to 100pF capacitor should also be placed between this input and the V_{DD} or V_{SS} (See Figure 19).

Display Off - To disable the display drivers, it is necessary to tie the D4 line to the CONTROL INPUT and have the HOLD input at V_{DD}. While in Display Off mode, the segments and digit drivers are all off, leaving the display lines floating, so the display can be shared with other devices. In this mode, the oscillator continues to run with a typical supply current of 1.5mA with a 10MHz crystal, but no measurements are made and multiplexed inputs are inactive. A new measurement cycle will be initiated when the HOLD input is switched to V_{SS}.

Display Test - Display will turn on with all the digits showing 8s and all decimal points also on. The display will be blanked if Display Off is selected at the same time.

1MHz Select - The 1MHz select mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurement as with a 10MHz crystal. This is done by dividing the oscillator frequency by 10^4 rather than 10^5. The decimal point is also shifted one digit to the right in period and time interval, since the least significant digit will be in µs increment rather than 0.1µs increment.

External Oscillator Enable - In this mode, the signal at EXT OSC INPUT is used as a timebase instead of the on-board crystal oscillator (built around the OSC INPUT, OSC OUTPUT inputs). This input can be used for an external stable temperature compensated crystal oscillator or for special measurements with any external source. The on-board crystal oscillator continues to work when the external oscillator is selected. This is necessary to avoid hang-up problems, and has no effect on the chip's functional operation. If the on-board oscillator frequency is less than 1MHz or only the external oscillator is used, THE OSC INPUT MUST BE CONNECTED TO THE EXT OSC INPUT providing the timebase has enough voltage swing for OSC INPUT (See Electrical Specifications). If the external timebase is TTL level a pullup resistor must be used for OSC INPUT. The other way is to put a 22MΩ resistor between OSC INPUT and OSC OUTPUT and capacitively couple the EXT OSC INPUT to OSC INPUT. This will bias the OSC INPUT at its threshold and the drive voltage will need to be only $2V_{P-P}$. The external timebase frequency must be greater than 100kHz or the chip will reset itself to enable the on-board oscillator.

External Decimal Point Enable - In this mode, the EX DP INPUT is enabled. A decimal point will be displayed for the digit that its output line is connected to this input (EX DP INPUT). Digit 8 should not be used since it will override the overflow output. Leading zero blanking is effective for the digits to the left of selected decimal point.

Hold Input

Except in the **unit counter mode**, when the HOLD input is at V_{DD}, any measurement in progress (before $\overline{\text{STORE}}$ goes low) is stopped, the main counter is reset and the chip is held ready to initiate a new measurement as soon as HOLD goes low. The latches which hold the main counter data are not updated, so the last complete measurement is displayed. In **unit counter** mode when HOLD input is at V_{DD}, the counter is not stopped or reset, but the display is frozen at that instantaneous value. When HOLD goes low the count continues from the new value in the new counter.

$\overline{\text{RST}}$ IN Input

The $\overline{\text{RST}}$ IN is provided to reset the Main Counter, stop any measurement in progress, and enable the display latches, resulting in the all zero display. It is suggested to have a capacitor at this input to V_{SS} to prevent any hangup problem on power up. See application circuits.

EXT RANGE Input

This input is provided to select ranges other than those provided in the chip. In any mode of measurement the duration of measurement is determined by the EXT RANGE if this input is enabled. This input is sampled at 10ms intervals by the 100Hz reference derived from the timebase. Figure 12 shows the relationship between this input, 100Hz reference signal and $\overline{\text{MEAS IN PROGRESS}}$. EXT RANGE can change state anywhere during the period of 100Hz reference by will be sampled at the trailing edge of the period to start or stop measurement.

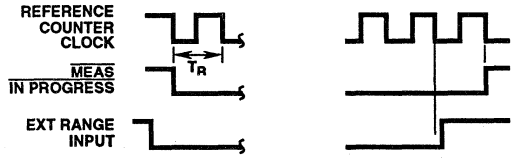


FIGURE 12. EXTERNAL RANGE INPUT TO END OF $\overline{\text{MEASUREMENT IN PROGRESS}}$

This input should not be used for short arbitrary ranges (because of its sampling period), it is provided for very long gating purposes. A way of using the ICM7226 for a short arbitrary range is to feed the gating signal into the INPUT B and run the device in the Frequency Ratio mode. Note that the gating period will be from one positive edge until the next positive edge of INPUT B (0.01 s/1 cycle range).

$\overline{\text{MEAS IN PROGRESS}}$, $\overline{\text{STORE}}$, RST OUT Outputs

These outputs are provided for external system interfacing. $\overline{\text{MEAS IN PROGRESS}}$ stays low during measurements and goes high for intervals between measurements. Figure 13 shows the relationship between these outputs for intervals between measurements. All these outputs can drive a low power Schottky TTL. The $\overline{\text{MEAS IN PROGRESS}}$ can drive one ECL load if the ECL device is powered from the same power supply as the ICM7226.

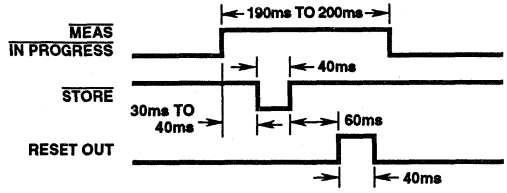


FIGURE 13. RESET OUT, $\overline{\text{STORE}}$ AND $\overline{\text{MEASUREMENT IN PROGRESS}}$ OUTPUTS BETWEEN MEASUREMENTS

BCD Outputs

The BCD representation of each display digit is available at the BCD outputs in a multiplexed fashion. See Table 3 for digits truth table. The BCD output of each digit is available when its corresponding digit output is activated. Note that the digit outputs are multiplexed from D8 (MSD) to D1 (LSD). The positive going (ICM7226A, common anode) or the negative going (ICM7226B, common cathode) digit drive signals lag the BCD data by 2µs to 6µs. This starting edge of each digit drive signal should be used to externally latch the BCD data. Each BCD output drives one low power Schottky TTL load. Leading zero blanking has no effect on the BCD outputs.

TABLE 3. TRUTH TABLE BCD OUTPUTS

NUMBER	BCD 8 PIN 7	BCD 4 PIN 6	BCD 2 PIN 17	BCD 1 PIN 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

BUF OSC OUT Output

The BUFFered OSCillator OUTput is provided for use of the on-board oscillator signal, without loading the oscillator itself. This output can drive one low power Schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

Decimal Point Position

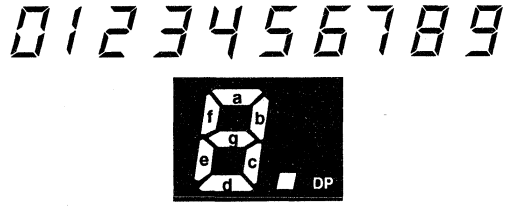
Table 4 shows the decimal point position for different modes of ICM7226 operation. Note that the digit 1 is the least significant digit. Table is given for 10MHz timebase frequency.

TABLE 4. DECIMAL POINT POSITIONS

RANGE	FREQUENCY	PERIOD	FREQUENCY RATIO	TIME INTERVAL	UNIT COUNTER	OSCILLATOR FREQUENCY
0.01s/1 Cycle	D2	D2	D1	D2	D1	D2
0.1s/10 Cycle	D3	D3	D2	D3	D1	D3
1s/100 Cycle	D4	D4	D3	D4	D1	D4
10s/1K Cycle	D5	D5	D4	D5	D1	D5
External	N/A	N/A	N/A	N/A	N/A	N/A

Overflow Indication

When overflow happens in any measurement it will be indicated on the decimal point of the digit 8. A separate LED indicator can be used. Figure 14 shows how to connect this indicator.



LED overflow indicator connections: Overflow ill be indicated on the decimal point output of digit 8.

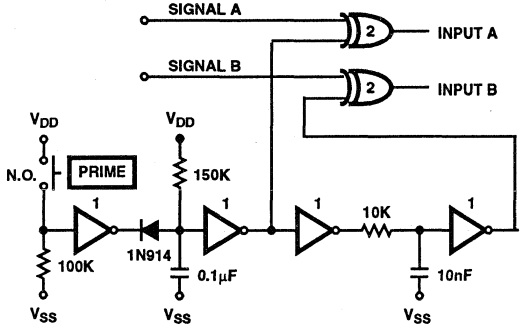
DEVICE	CATHODE	ANODE
ICM7226A	Decimal Point	D8
ICM7226B	D8	Decimal Point

FIGURE 14. SEGMENT IDENTIFICATION AND DISPLAY FONT

Time Interval Measurement

When in the **time interval** mode and measuring a single event, the ICM7226A and ICM7226B must first be "primed" prior to measuring the event of interest. This is done by first generating a negative going edge on Channel A followed by a negative going edge on Channel B to start the "measurement interval". The inputs are then primed ready for the measurement. Positive going edges on A and B, before or after the priming, will be needed to restore the original condition.

Priming can be easily accomplished using the circuit in Figure 15.



DEVICE	TYPE
1	CD4049B Inverting Buffer
2	CD4070B Exclusive - OR

FIGURE 15. PRIMING CIRCUIT, SIGNALS A & B BOTH HIGH OR LOW

Following the priming procedure (when in single event or 1 cycle range) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7226A and ICM7226B as the first alternating signal states automatically prime the device. See Figure 1.

During any time interval measurement cycle, the ICM7226A and ICM7226B requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.

Oscillator Considerations

The oscillator is a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonant 10MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35Ω. Among suitable crystals is the 10MHz CTS KNIGHTS ISI-002

For a specific crystal and load capacitance, the required g_M can be calculated as follows:

$$g_M = \omega^2 C_{IN} C_{OUT} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

where $C_L = \left(\frac{C_{IN} C_{OUT}}{C_{IN} + C_{OUT}}\right)$

C_O = Crystal Static Capacitance

R_S = Crystal Series Resistance

C_{IN} = Input Capacitance

C_{OUT} = Output Capacitance

$\omega = 2\pi f$

The required g_M should not exceed 50% of the g_M specified for the ICM7226 to insure reliable startup. The OSCillator INPUT and OUTPUT pins each contribute about 4pF to C_{IN} and C_{OUT}. For maximum stability of frequency, C_{IN} and C_{OUT} should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used, it may be desirable to use a crystal which is neither 10MHz or 1MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate is

$f_{MUX} = \frac{f_{OSC}}{2 \times 10^4}$ for 10MHz mode and $f_{MUX} = \frac{f_{OSC}}{2 \times 10^3}$ for the 1MHz mode. The time between measurements is $\frac{2 \times 10^6}{f_{OSC}}$ in the 10MHz mode and $\frac{2 \times 10^5}{f_{OSC}}$ in the 1MHz mode.

The buffered oscillator output should be used as an oscillator test point or to drive additional logic; this output will drive one low power Schottky TTL load. When the buffered oscillator output is used to drive CMOS or the external oscillator input, a 10kΩ resistor should be added from the buffered oscillator output to V_{DD}.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the EXTERNAL OSCILLATOR INPUT to the OSCILLATOR OUTPUT or INPUT can cause undesirable shifts in oscillator frequency.

Display Considerations

The display is multiplexed at a 500Hz rate with a digit time of 244µs. An interdigit blanking time of 6µs is used to prevent display ghosting (faint display of data from previous digit superimposed on the next digit). Leading zero blanking is provided, which blanks the left hand zeroes after decimal point or any non zero digits. Digits to the right of the decimal point are always displayed. The leading zero blanking will be disabled when the Main Counter overflows.

The ICM7226A is designed to drive common anode LED displays at peak current of 25mA/segment, using displays with V_F = 1.8V at 25mA. The average DC current will be greater than 3mA under these conditions. The ICM7226B is designed to drive common cathode displays at peak current of 15mA/segment using displays with V_F = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current, if required. The Typical Performance Curves show the digit and segment currents as a function of output voltage for common anode and common cathode drivers.

To increase the light output from the displays, V_{DD} may be increased to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

The SEGment and Digit outputs in both the ICM7226A and ICM7226B are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals. External latching should be down on the leading edge of the digit signal.

Accuracy

In a Universal Counter, crystal drift and quantization errors cause errors. In **frequency, period** and **time interval** modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter, and in these modes, an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the **frequency** mode maximum accuracy is obtained with high frequency inputs and in **period** mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 16. In **time interval** measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 17. In **frequency ratio** measurement can be more accurately obtained by averaging over more cycles of INPUT B as shown in Figure 18.

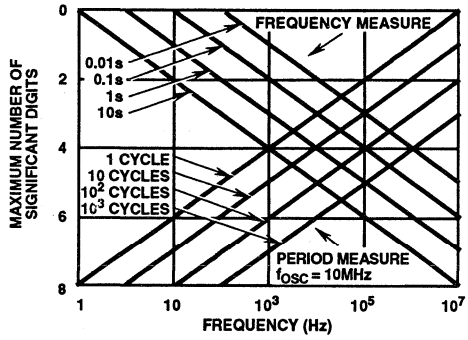


FIGURE 16. MAXIMUM ACCURACY OF FREQUENCY AND PERIOD MEASUREMENTS DUE TO LIMITATIONS OF QUANTIZATION ERRORS

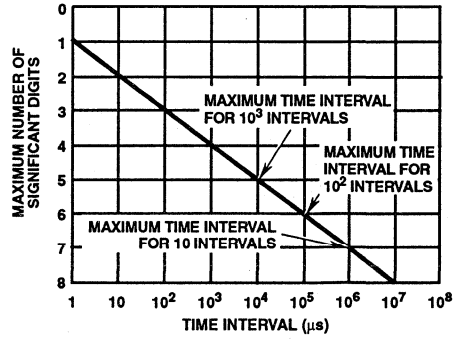


FIGURE 17. MAXIMUM ACCURACY OF TIME INTERVAL MEASUREMENT DUE TO LIMITATIONS OF QUANTIZATION ERRORS

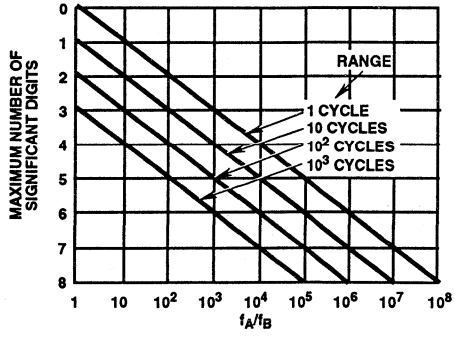
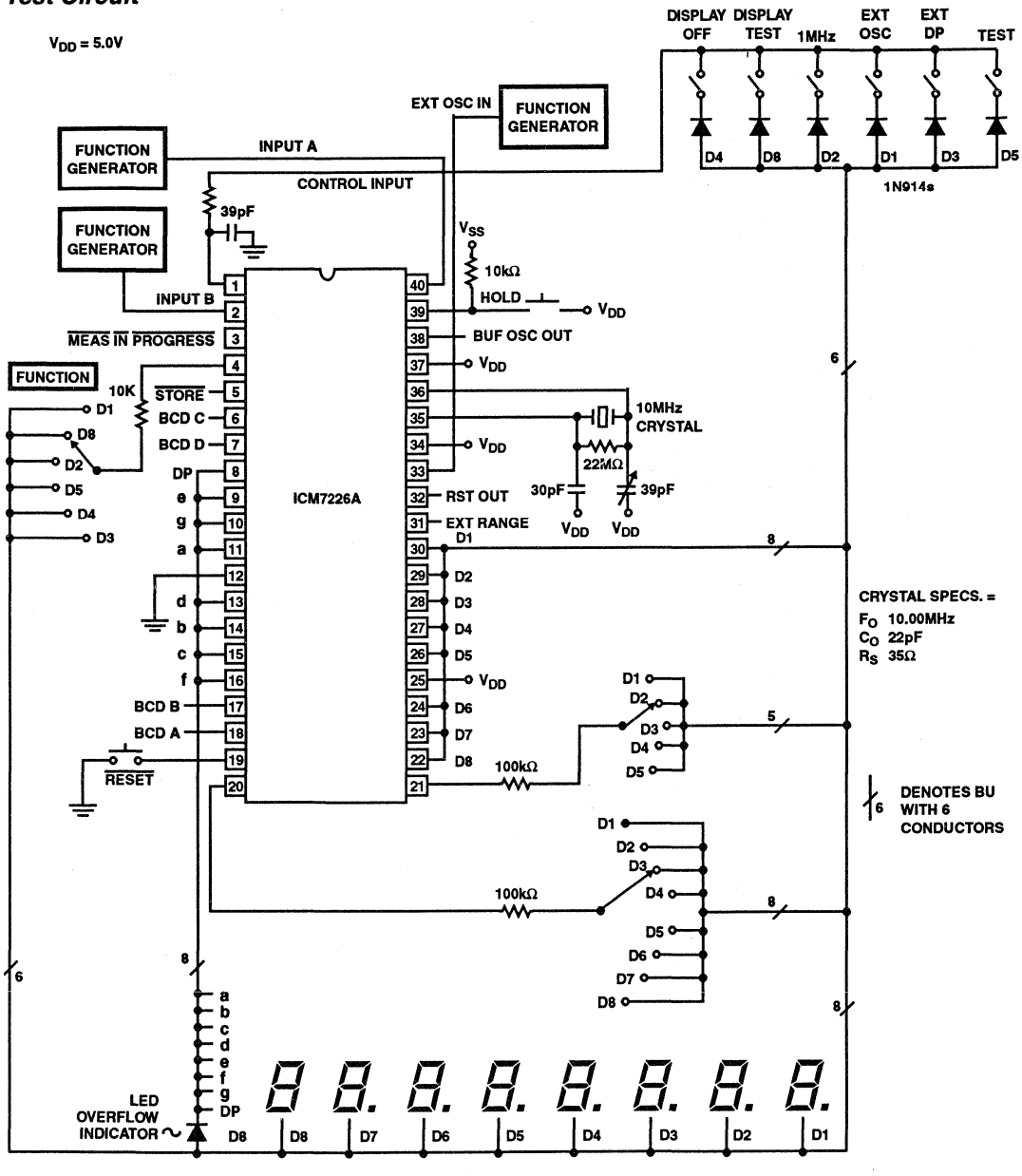


FIGURE 18. MAXIMUM ACCURACY FOR FREQUENCY RATIO MEASUREMENT DUE TO LIMITATION OF QUANTIZATION ERRORS

Test Circuit



LED OVERFLOW INDICATOR CONNECTIONS

DEVICE	CATHODE	ANODE
ICM7226A	DP	D8
ICM7226B	D8	DP

NOTE: Overflow will be indicated on the decimal point output of digit 7.

FIGURE 19.

Typical Applications

The ICM7226 has been designed as a complete stand alone Universal Counter, or used with prescalers and other circuitry in a variety of applications. Since INPUT A and INPUT B are digital inputs, additional circuitry will be required in many applications, for input buffering, amplification, hysteresis, and level shifting to obtain the required digital voltages. For many applications a FET source follower can be used for input buffering, and an ECL 10116 line receiver can be used for amplification and hysteresis to obtain high impedance input, sensitivity and bandwidth. However, cost and complexity of this circuitry can vary widely, depending upon the sensitivity and bandwidth required. When TTL prescalers or input buffers are used, a pull up resistors to V_{DD} should be used to obtain optimal voltage swing at INPUTS A and B.

If prescalers aren't required, the ICM7226 can be used to implement a minimum component Universal Counter as shown in Figure 20.

For input frequencies up to 40MHz, the circuit shown in Figure 21 can be used to implement a **frequency and period counter**. To obtain the correct value when measuring frequency and period, it is necessary to divide the 10MHz oscillator frequency down to 2.5MHz. In doing this the time between measurements is lengthened to 800ms and the display multiplex rate is decreased to 125Hz.

If the input frequency is prescaled by ten, the oscillator frequency can remain at either 10MHz or 1MHz, but the decimal point must be moved. Figure 22 shows use of a ÷10 prescaler in **frequency counter** mode. Additional logic has been added to enable the ICM7226 to count the input directly in **period** mode for maximum accuracy.

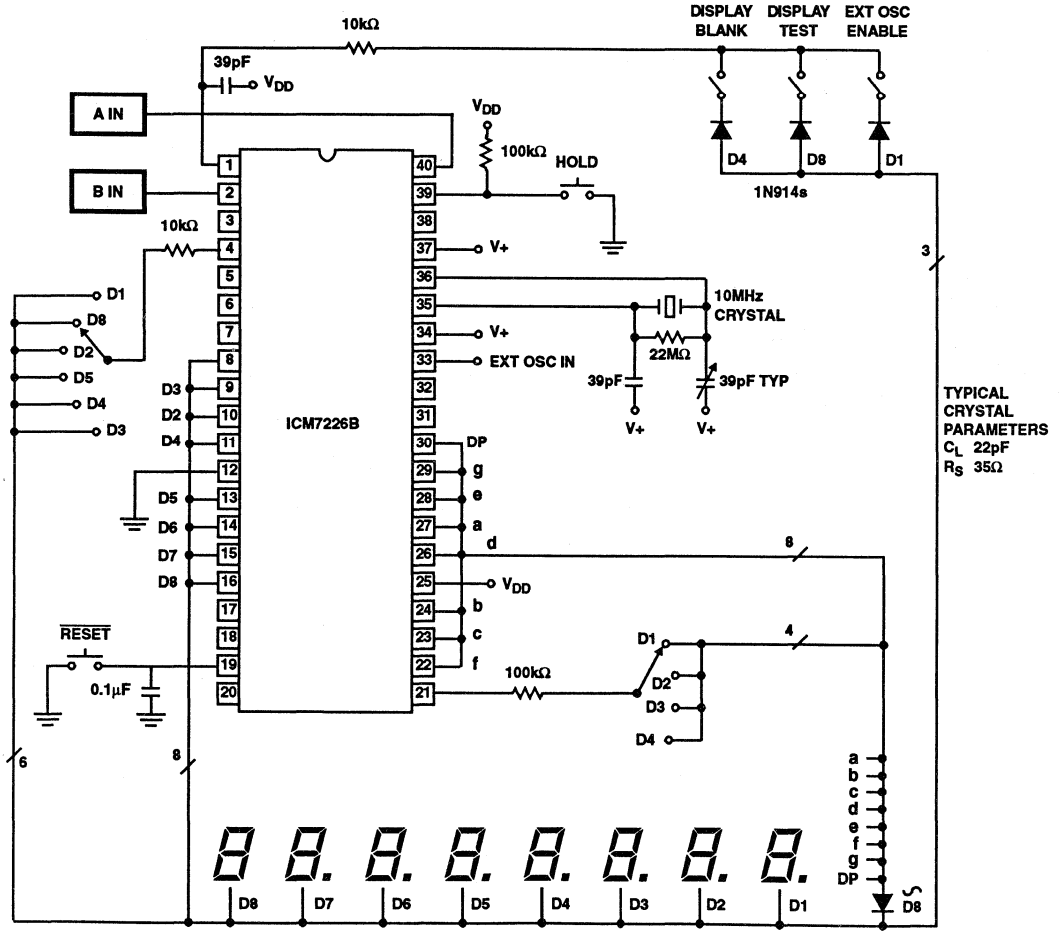


FIGURE 20. 10MHz UNIVERSAL COUNTER

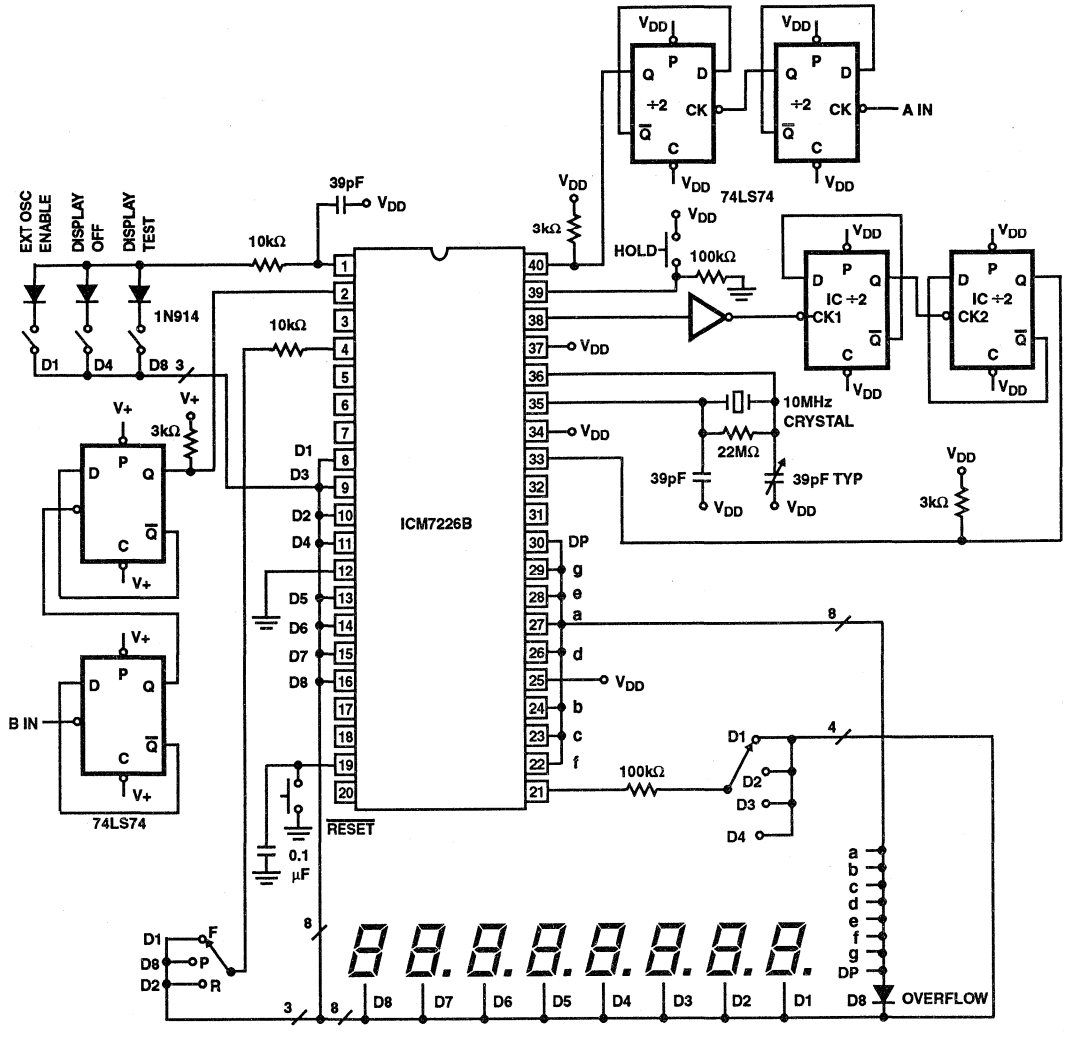


FIGURE 21. 40MHz FREQUENCY, PERIOD COUNTER

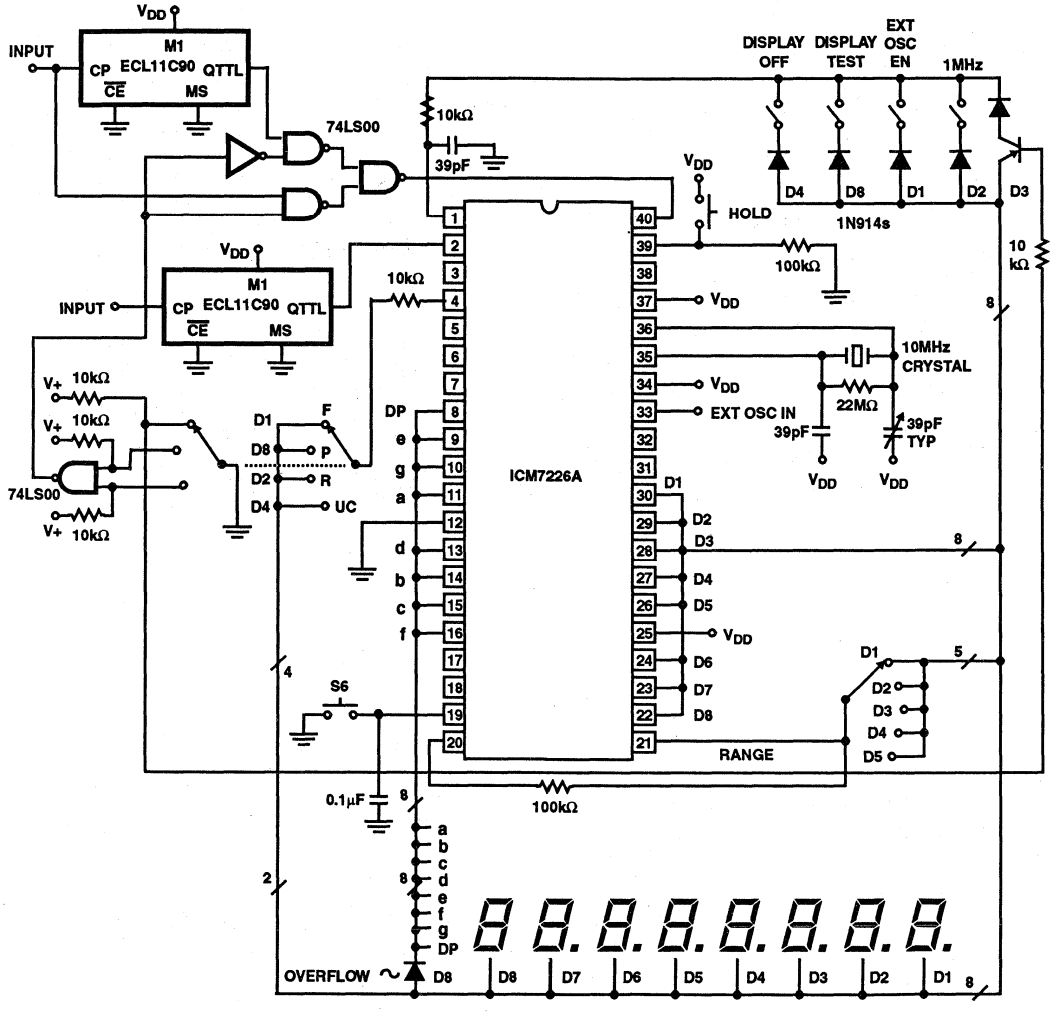


FIGURE 22. 100MHz MULTI-FUNCTION COUNTER

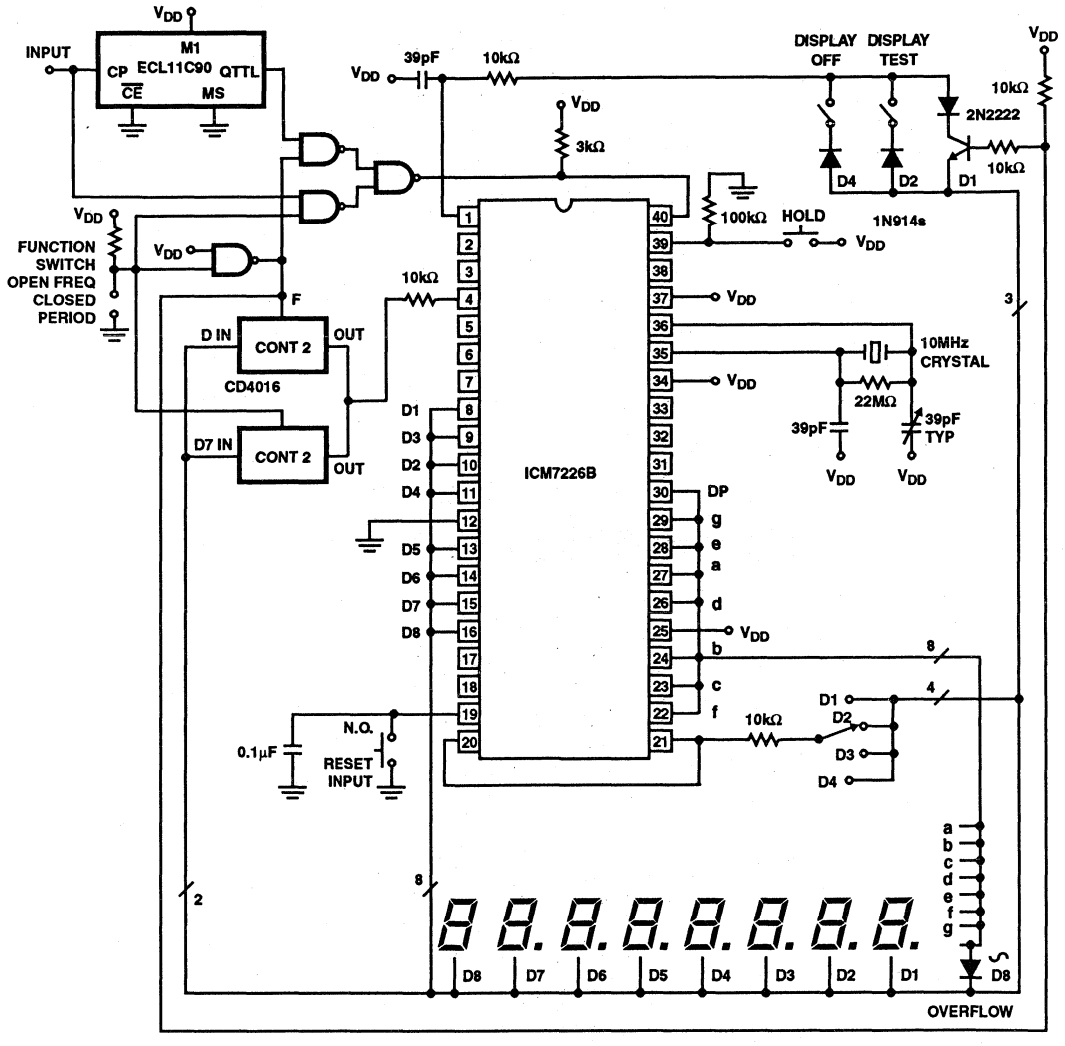


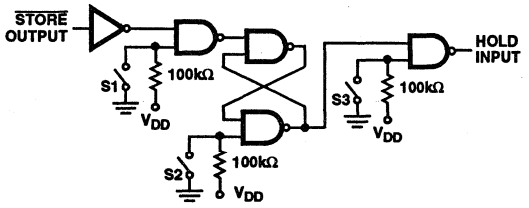
FIGURE 23. 100MHz FREQUENCY, PERIOD COUNTER

Figure 23 shows the use of a CD4016 analog multiplexer to multiplex the digital outputs back to the FUNCTION Input. Since the CD4016 is a digitally controlled analog transmission gate, no level shifting of the digit output is required. CD4051's or CD4052's could also be used to select the proper inputs for the multiplexed input on the ICM7226 from 2 or 3 bit digital inputs. These analog multiplexers may also be used in systems in which the mode of operation is controlled by a microprocessor rather than directly from front panel switches. TTL multiplexers such as the 74LS153 or 74LS251 may also be used, but some additional circuitry will be required to convert the digit output to TTL compatible logic levels.

The circuit shown in Figure 24 can be used in any of the circuit applications shown to implement a single measurement mode of operation. This circuit uses the $\overline{\text{STORE}}$ output to put the ICM7226 into a hold mode. The HOLD input can also be used to reduce the time between measurements. The circuit shown in Figure 25 puts a short pulse into the HOLD input a short time after STORE goes low. A new measurement will be initiated at the end of the pulse on the HOLD input. This circuit reduces the time between measurements to about 40ms from 200ms; use of the circuit shown in Figure 25 on the circuit shown in Figure 21 will reduce the time between measurements from 800ms to about 160ms.

Using LCD Display

Figure 26 shows the ICM7226 being interfaced to LCD displays, by using its BCD outputs and 8 digit lines to drive two ICM7211 display drivers.



SWITCH	FUNCTION
S1	Open-Single Meas Mode Enabled
S2	Closed-Initiate New Measurement
S3	Closed-Hold Input

FIGURE 24. SINGLE MEASUREMENT CIRCUIT FOR USE WITH ICM7226

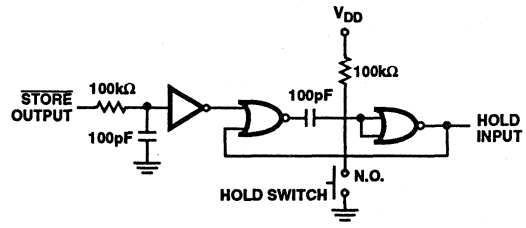


FIGURE 25. CIRCUIT FOR REDUCING TIME BETWEEN MEASUREMENTS

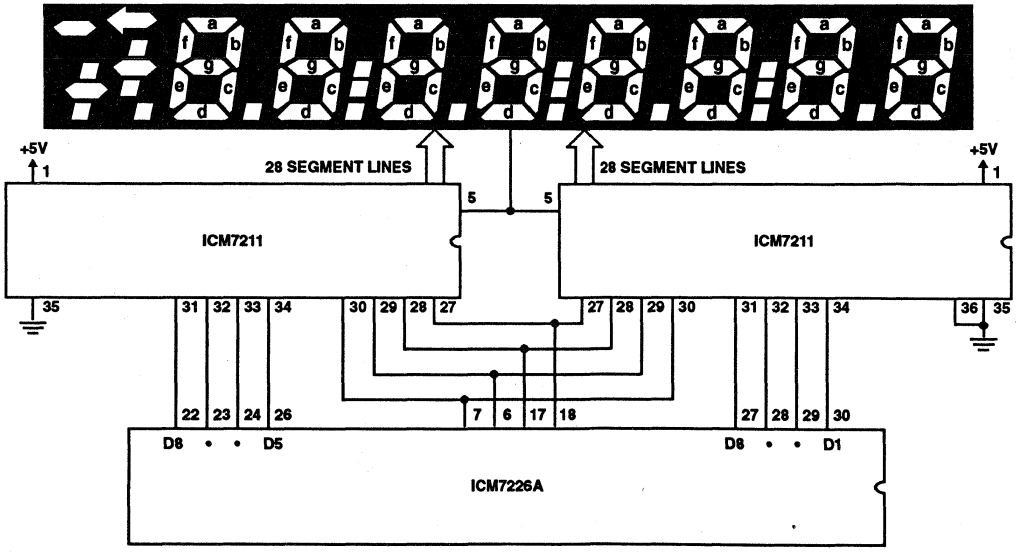


FIGURE 26. 10MHz UNIVERSAL COUNTER SYSTEM WITH LCD DISPLAY

HARRIS SEMICONDUCTOR

ICM7249

December 1993

$5^1/_2$ Digit LCD μ-Power Event/Hour Meter

Features

- Hour Meter Requires Only 4 Parts Total
- Micropower Operation: < 1μA at 2.8V Typical
- 10 Year Operation On One Lithium Cell. $2^1/_2$ Year Battery Life with Display Connected
- Directly Drives $5^1/_2$ Digit LCD
- 14 Programmable Modes of Operation
- Times Hrs., 0.1 Hrs., 0.01 Hrs., 0.1 Mins.
- Counts 1's, 10's, 100's, 1000's
- Dual Funtion Input Circuit
  - Selectable Debounce for Counter
  - High-Pass Filter for Timer
- Direct AC Line Triggering with Input Resistor
- Winking "Timer Active" Display Output
- Display Test Feature

Applications

- AC or DC Hour Meters
- AC or DC Totalizers
- Portable Battery Powered Equipment
- Long Range Service Meters

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7249IPM	-20°C to +85°C	48 Lead Plastic DIP

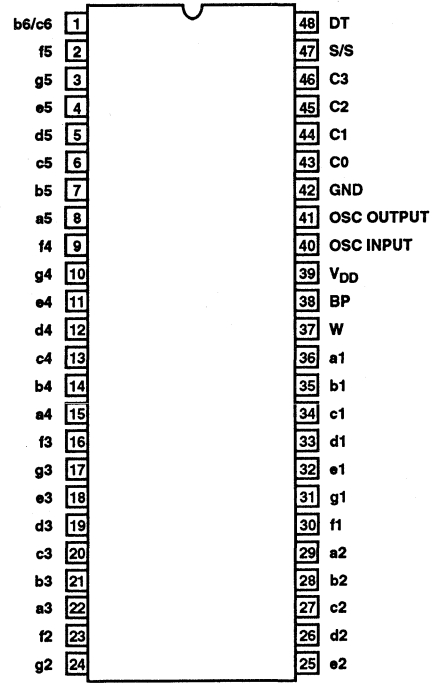
Description

The ICM7249 Timer/Counter is intended for long-term battery-supported industrial applications. The ICM7249 typically draws 1μA during active timing or counting, due to Harris' special low-power design techniques. This allows more than 10 years of continuous operation without battery replacement. The chip offers four timing modes, eight counting modes and four test modes.

The ICM7249 is a 48 lead device, powered by a single DC voltage source and controlled by a 32.768kHz quartz crystal. No other external components are required. Inputs to the chip are TTL-compatible and outputs drive standard direct drive LCD segments.

Pinout

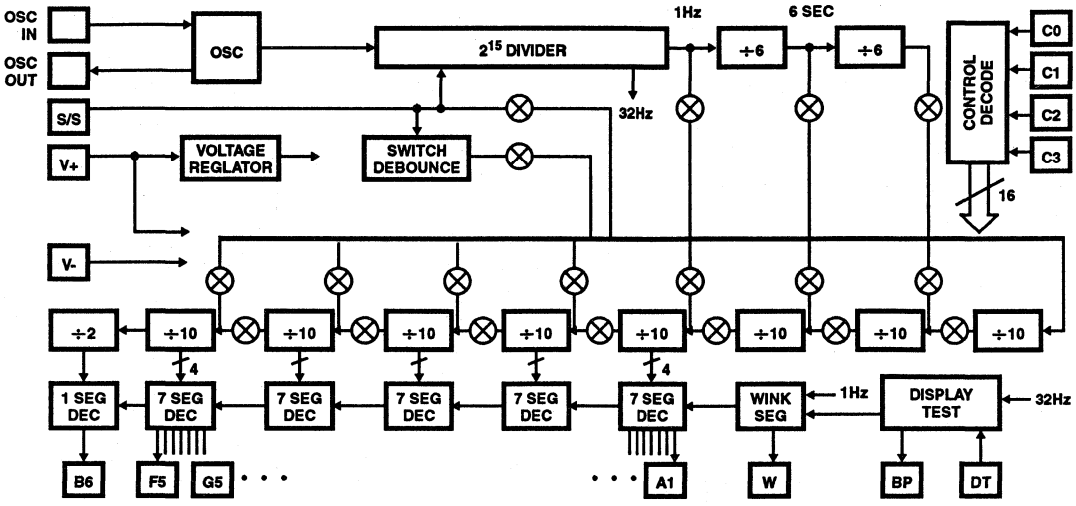
ICM7249
(PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number 3170

Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage (V_{DD} - V_{SS}) 6V
Input Voltage, Pins 43 - 48 (Note 1) ... (V_{SS} - 0.3V) to (V_{DD} + 0.3V)
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C

Thermal Information

Thermal Resistance θ_{JA}
Plastic Package ..... 50°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications

Temperature = -40°C to +85°C, V_{DD} = 2.5V to 5.5V, V_{SS} = 0V, Unless Otherwise Specified. Typical Specifications Measured at Temperature = +25°C and V_{DD} = 2.8V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Operating Voltage, V_{DD}	Note 2	2.5	-	5.5	V
Operating Current, I_{DD}	All Inputs = V_{DD} or GND, Note 3				
	V_{DD} = 2.8V	-	1.0	10.0	µA
	V_{DD} = 5.5V	-	4.0	20.0	µA
INPUT CURRENT					
C0 - C3, I_{IN}	All Inputs V_{DD} or GND	0.0	-	1	µA
S/S, I_{SS}	V_{DD} = 2.8V Note 4	0.5	1.5	3.0	µA
DT, I_{DT}		40.0	-	110	µA
INPUT VOLTAGE					
C0 - C3, DT, S/S					
V_{IL}		-	-	$0.3V_{DD}$	V
V_{IH}		$0.7V_{DD}$	-	-	V
Segment Output Voltage					
V_{OL}	I_{OL} = 1µA	-	-	0.8	V
V_{OH}	I_{OH} = 1µA	V_{DD} - 0.8	-	-	V
Backplane Output Voltage					
V_{OL}	I_{OL} = 10µA	-	-	0.8	V
V_{OH}	I_{OH} = 10µA	V_{DD} - 0.8	-	-	V
OSCILLATOR STABILITY					
Temperature = +25°C, V_{DD} = 2.5V to 5.5V		-	0.1	-	ppm
Temperature = -40°C to +85°C, V_{DD} = 2.5V to 5.5V		-	5	-	ppm
S/S PULSE WIDTH					
High-Pass Filter (Modes 0 - 3), T_{HP}		5	-	10,000	µs
Debounce (Modes 4, 6, 8, 10), T_{DE}		10,000	-	-	µs
Without Debounce (Modes 5, 7, 9, 11), T_{DE}		5	-	-	µs

NOTES:

1. Due to the SCR structure inherent in junction-isolated CMOS devices. the circuit can be put in a latchup mode it large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs or outputs before power is applied. If only inputs are affected, latchup also can be prevented by limiting the current into the input terminal to less than 1mA.
2. Internal reset to 00000 requires a maximum V_{DD} rise time of 1µs. Longer rise times at power-up may cause improper reset.
3. Operating current is measured with the LCD disconnected, and input current I_{SS} and I_{DT} supplied externally.
4. Inputs C0 - C3 are latched internally and draw no DC current after switching. During switching. a 90µA peak current may be drawn for 10ns.

Timing Waveforms

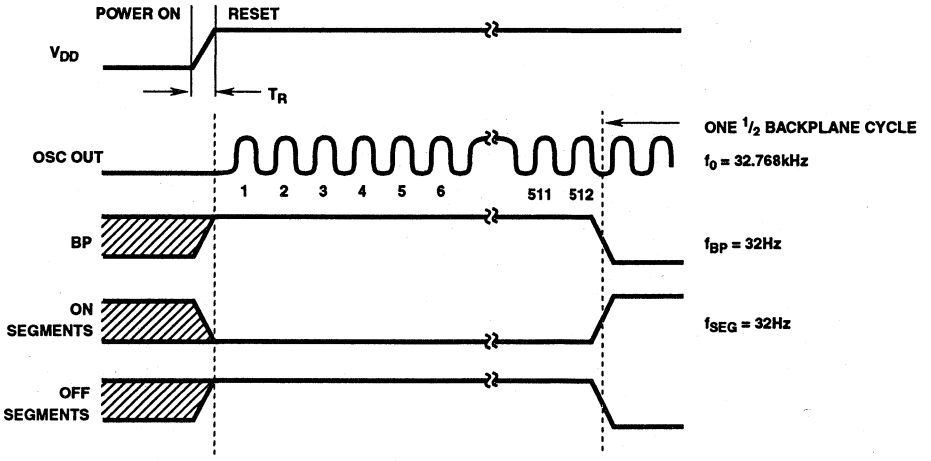


FIGURE 1. POWER ON/RESET WAVEFORMS

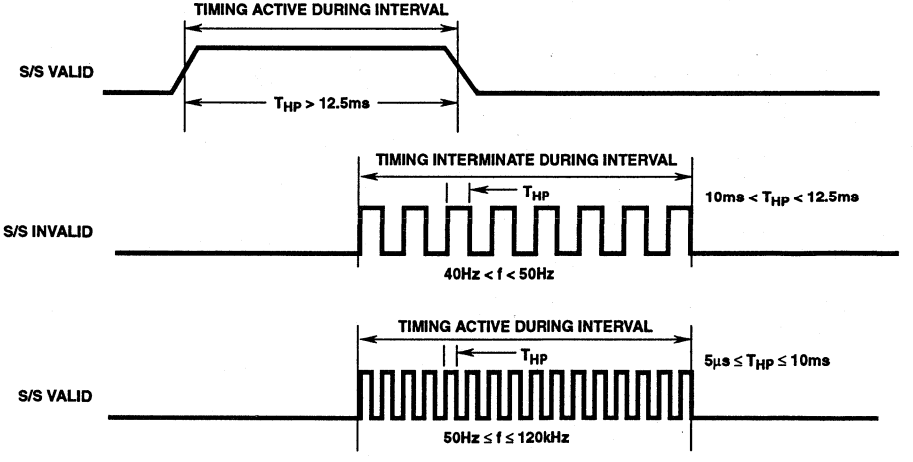


FIGURE 2. START/STOP INPUT HIGH-PASS FILTERING IN TIMING MODES

Timing Waveforms (Continued)

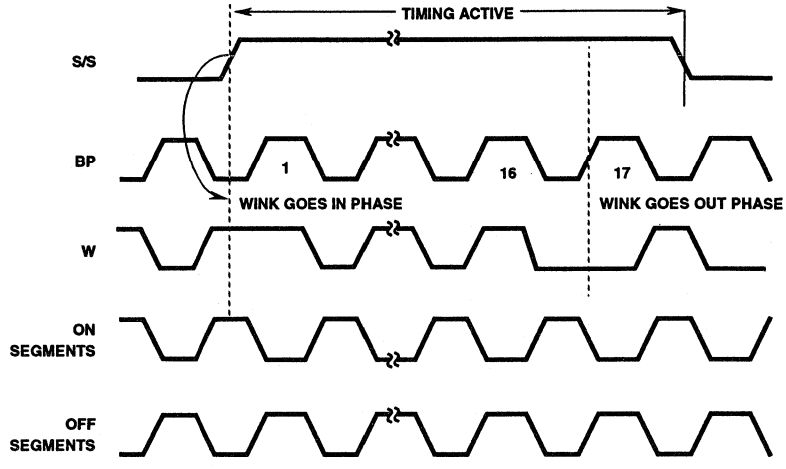


FIGURE 3. WINK WAVEFORMS IN TIMING MODES

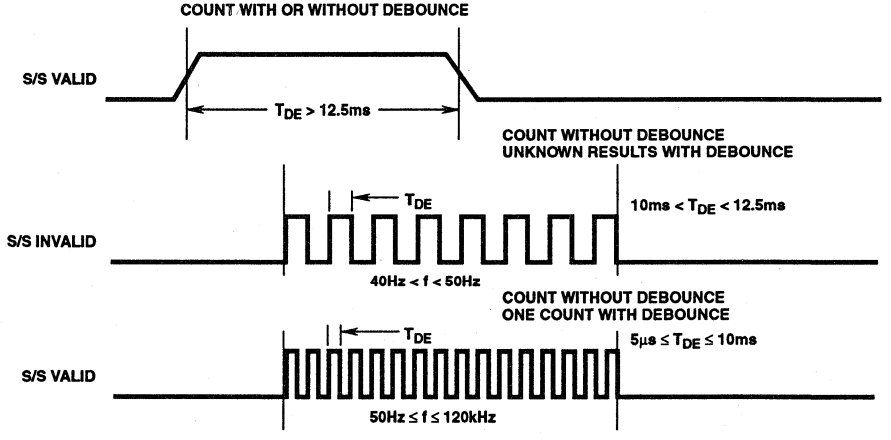


FIGURE 4. START/STOP INPUT DEBOUNCE FILTERING IN COUNTING MODES

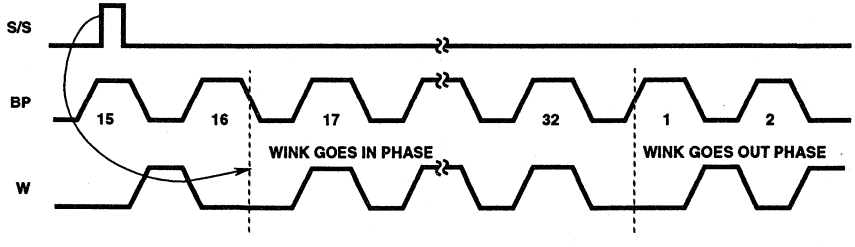


FIGURE 5. WINK WAVEFORMS IN COUNTING MODES

Timing Waveforms (Continued)

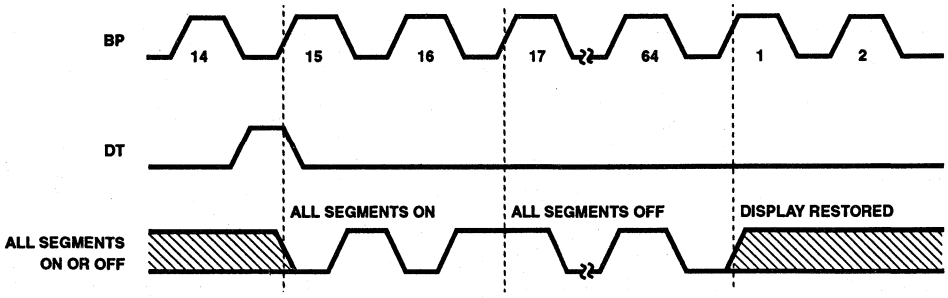


FIGURE 6. DISPLAY TESTING

Pin Descriptions

PIN	NAME	DESCRIPTION
1	b6/c6	Half-Digit LCD Segment Output.
2	f5	Seven-Segment LCD Output.
3	g5	Seven-Segment LCD Output.
4	e5	Seven-Segment LCD Output.
5	d5	Seven-Segment LCD Output.
6	c5	Seven-Segment LCD Output.
7	b5	Seven-Segment LCD Output.
8	a5	Seven-Segment LCD Output.
9	f4	Seven-Segment LCD Output.
10	g4	Seven-Segment LCD Output.
11	e4	Seven-Segment LCD Output.
12	d4	Seven-Segment LCD Output.
13	c4	Seven-Segment LCD Output.
14	b4	Seven-Segment LCD Output.
15	a4	Seven-Segment LCD Output.
16	f3	Seven-Segment LCD Output.
17	g3	Seven-Segment LCD Output.
18	e3	Seven-Segment LCD Output.
19	d3	Seven-Segment LCD Output.
20	c3	Seven-Segment LCD Output.
21	b3	Seven-Segment LCD Output.
22	a3	Seven-Segment LCD Output.
23	f2	Seven-Segment LCD Output.
24	g2	Seven-Segment LCD Output.

PIN	NAME	DESCRIPTION
25	e2	Seven-Segment LCD Output.
26	d2	Seven-Segment LCD Output.
27	c2	Seven-Segment LCD Output.
28	b2	Seven-Segment LCD Output.
29	a2	Seven-Segment LCD Output.
30	f1	Seven-Segment LCD Output.
31	91	Seven-Segment LCD Output.
32	e1	Seven-Segment LCD Output.
33	d1	Seven-Segment LCD Output.
34	c1	Seven-Segment LCD Output.
35	b1	Seven-Segment LCD Output.
36	a1	Seven-Segment LCD Output.
37	W	Wink-Segment Output.
38	BP	Backplane for LCD Reference.
39	V_{DD}	Positive Supply Voltage.
40	OSC IN	Quartz Crystal Connection
41	OSC OUT	Quartz Crystal Connection
42	GND	Supply GRouND.
43	C0	Mode-select Control Input.
44	C1	Mode-select Control Input.
45	C2	Mode-select Control Input.
46	C3	Mode-select Control Input.
47	S/S	Start/Stop Input.
48	DT	Display Test Input.

TABLE 2. MODE SELECT TABLE

MODE	CONTROL PIN INPUTS C3	C2	C1	C0	FUNCTION
0	0	0	0	0	1 Hour Interval Timer
1	0	0	0	1	0.1 Hour Interval Timer
2	0	0	1	0	0.01 Hour Interval Timer
3	0	0	1	1	0.1 Minute Interval Timer
4	0	1	0	0	1's Counter with Debounce
5	0	1	0	1	1's Counter
6	0	1	1	0	10's Counter with Debounce
7	0	1	1	1	10's Counter
8	1	0	0	0	100's Counter with Debounce
9	1	0	0	1	100's Counter
10	1	0	1	0	1000's Counter with Debounce
11	1	0	1	1	1000's counter
12	1	1	0	0	Test Display Digits
13	1	1	0	1	Internal Test
14	1	1	1	0	Internal Test
15	1	1	1	1	Reset

Detailed Description

As the Functional Diagram shows the device consists of the following building blocks:

- A 32.768kHz crystal oscillator with the associated dividers to generate timebase signals for periods of 1s (frequency of 1Hz), 6s (1/10 min) and 36s (1/100 hour), and 32Hz signal for LCD drivers.
- A debounce/high-pass detect circuit for the S/S (Start/Stop) input.
- A chain of cascaded decade counters, 3 decade counters for prescaling and $5^1/_2$ BCD decade counters for display driving.
- Display control circuitry and BCD to 7-segment decoder/drivers.
- A control decoder to select different modes of operation. This is done by routing different signals to the different points in the chain of decade counters.

The control decoder has 4 inputs for selecting 16 possible modes of operation, numbered 0 to 15. The 16 modes are selected by placing the binary equivalent of the mode number on inputs C0 to C3. Table 2 shows the control inputs and the modes of operation.

After applying power, the ICM7249 requires a rise time of T_R to become active and for oscillation to begin, as shown in Figure 1. The BP (backplane) output changes state once every 512 cycles of the crystal oscillator, resulting in a square wave of 32Hz. The display segments drive signal has the same level and frequency as BP. Segments are off when in phase with BP and are on when out of phase with BP.

A non-multiplexed LCD display is used because it is more stable over temperature and allows many standard LCD displays to be used.

Timer Mode of Operation

In modes 0 to 3 the device functions as an interval timer. In this mode, one of the timebase signals will be routed to the decade counters at a proper point in the chain. Depending on the selected mode the display will be incremented at 0.1 min, 0.01 hour, 0.1 hour or 1 hour rates.

Control of timing function is handled by the S/S input. There is a high-pass filtering effect on the S/S input in timer modes. Referring to Figure 2, timing is active when either S/S is held high for more than 12.5ms, or if input frequency is 50Hz to 120kHz. Driving S/S with a frequency between 40Hz to 50Hz has an indeterminate effect on timing and should be avoided. Note that the T_{HP} intervals shown on Figure 1 are also applied to the intervals when the S/S input is low.

Counter Mode of Operation

In modes 4 to 11 the device functions as an event counter or totalizer. In this mode the S/S input will be routed to the decade counters at a proper point in the chain. Each positive transition of the S/S will be registered as one count. Depending on the selected mode, the display will be incremented by each pulse, every 10 pulses, every 100 pulses or every 1000 pulses.

In counter modes 4, 6, 8 and 10 the S/S input is subjected to debounce filtering. Referring to Figure 4, only the pulses with a frequency of less than 40Hz are valid and will be counted. Input pulses with a frequency of 50Hz to 120kHz are not counted individually, but each burst of input pulses will be counted as one pulse if it lasts at least 12.5ms. Driving S/S with a frequency between 40Hz to 50Hz has an indeterminate result and should be avoided.

In counter modes 5, 7, 9 and 11 the S/S input is not subjected to any debouncing action and input pulses will be counted up to a frequency of 120kHz.

Wink Segment

The wink segment is provided as a annunciator to indicate the ICM7249 is working. It can be connected to any kind of annunciator on an LCD, like the flashing colons in a clock type LCD.

In the timer modes, the wink segment flashes while timing is taking place. The wink segment waveform is shown on Figure 3 for timer modes. On the positive transition of S/S, the wink output turns off. It remains off for 16 BP cycles and turns back on for another 16 cycles. If timing is still active, this will be repeated, giving a wink flash rate of 1Hz; otherwise, the wink segment remains on while timing is not active.

In the counter modes, the wink segment stays on until a pulse occurs on S/S input, then it winks off indicating a pulse is counted. This will happen regardless of whether the display is incremented. Figure 5 shows the wink waveform for counter modes. When a count occurs, the wink segment

turns off at the end of the 16th BP cycle and turns back on at the end of the 32nd BP cycle, giving a half-second wink. If the counting occurs more frequently than once a second, the wink output will continue to flash at the constant rate of 1Hz.

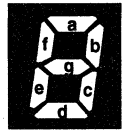


FIGURE 7. DIGITS SEGMENT ASSIGNMENT

Display Test and Reset

The display may be tested at any time without disturbing operation by pulsing DT high, as seen in Figure 6. On the next positive transition of BP, all the segments turn on and remain on until the end of the 16th BP cycle. This takes a half-second or less. All the segments then turn off for an additional 48 BP cycles (the end of the 64th cycle), after which valid data returns to the display. As long as DT is held high, the segments will remain on.

Additional display testing is provided by using mode 12. In this mode each displayed decade is incremented on each positive transition of S/S. Modes 13 and 14 are manufacturer testing only.

Mode 15 resets all the decades and internal counters to zero, essentially bringing everything back to power-up status.

Applications

A typical use of the ICM7249 is seen in Figure 8, the Motor Hour Meter. In this application the ICM7249 is configured as an hours-in-use meter and shows how many whole hours of line voltage have been applied. The resistor network and high-pass filtering allow AC line activation of the S/S input. This configuration, which is powered by a 3V lithium cell, will operate continuously for $2^1/_2$ years. Without the display, which only needs to be connected when a reading is required, the span of operation is extended to 10 years.

When the ICM7249 is configured as an attendance counter, as shown in Figure 9, the display shows each increment. By using mode 2, external debouncing of the gate switch is unnecessary, provided the switch bounce is less than 10ms.

The 3V lithium battery can be replaced without disturbing operation if a suitable capacitor is connected in parallel with it. The display should be disconnected, if possible, during the procedure to minimize current drain. The capacitor should be large enough to store charge for the amount of time needed to physically replace the battery ($\Delta t = \Delta VC/I$). A 100µF capacitor initially charged to 3V will supply a current of 1.0µA for 50 seconds before its voltage drops to 2.5V, which is the minimum operating voltage for the ICM7249.

Before the battery is removed, the capacitor should be placed in parallel, across the V_{DD} and GND terminals. After the battery is replaced, the capacitor can be removed and the display reconnected.

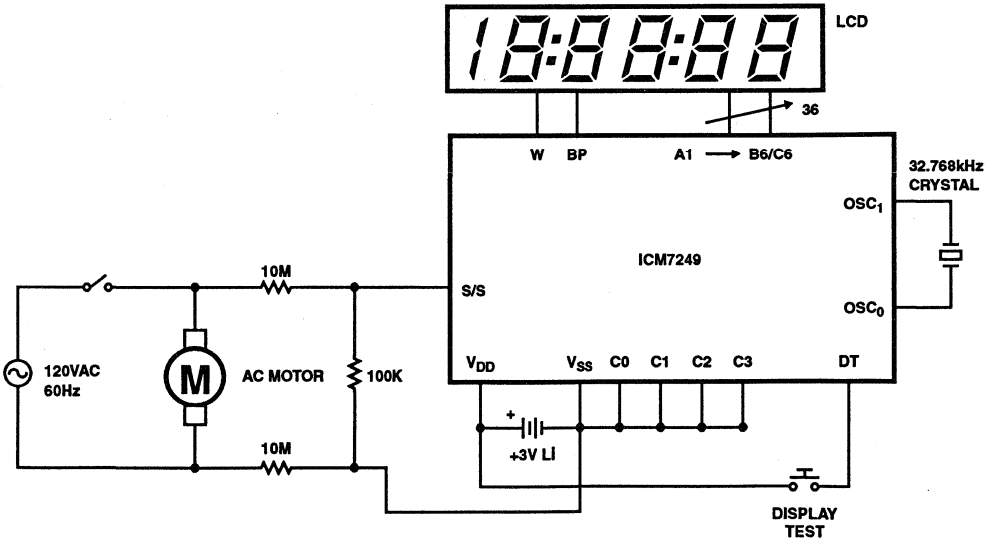


FIGURE 8. MOTOR HOUR METER

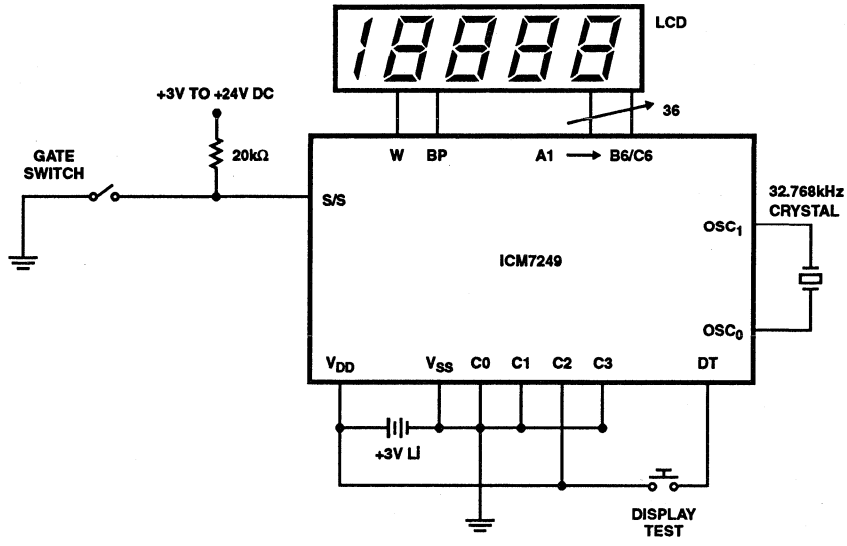


FIGURE 9. ATTENDANCE COUNTER

DATA ACQUISITION 14

SPECIAL PURPOSE

HARRIS SEMICONDUCTOR

AD590

2 Wire Current Output Temperature Transducer

December 1993

Features

- **Linear Current Output 1μA/°K**
- **Wide Temperature Range -55°C to + 150°C**
- **Two-Terminal Device Voltage In/Current Out**
- **Wide Power Supply Range +4V to +30V**
- **Sensor Isolation From Case**
- **Low Cost**

Ordering Information

PART NUMBER	NON-LINEARITY (°C)	TEMPERATURE RANGE	PACKAGE
AD590IH	±3.0	-55°C to + 150°C	TO-52
AD590JH	±1.5	-55°C to + 150°C	TO-52

Description

The AD590 is an integrated-circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance constant current regulator, passing 1μA/°K for supply voltages between +4V and +30V. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2°K (+25°C).

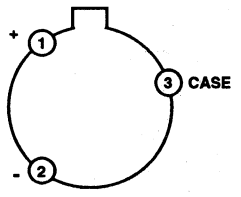
The AD590 should be used in any temperature-sensing application between -55°C to +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance measuring circuitry and cold junction compensation are not needed in applying the AD590. In the simplest application, a resistor, a power source and any voltmeter can be used to measure temperature.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, and biasing proportional to absolute temperature.

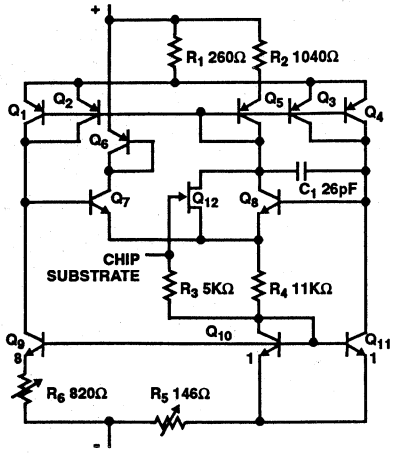
The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high-impedance current output. Any well insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

Pinout

AD590
(TO-52 CAN)



Functional Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

File Number **3171**

Absolute Maximum Ratings (T_A + 25°C)

Supply Forward Voltage (V+ to V-) . . . . . +44V
Supply Reverse Voltage (V+ to V-) . . . . . -20V
Breakdown Voltage (Case to V+ to V-) . . . . . ±200V
Rated Performance Temperature Range TO-52. . . -55°C to + 150°C
Lead Temperature (Soldering, 10s) . . . . . +300°C
Storage Temperature Range . . . . . -65°C to +150°C

Thermal Information

Maximum Package Power Dissipation
TO-52 Package 15mW
Operating Temperature Range . . . . . -55°C to +150°C
Junction Temperature . . . . . +175°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications Typical Values at T_A = +25°C, V+ = 5V, Unless Otherwise Specified

PARAMETERS	TEST CONDITIONS	AD590I	AD590J	UNITS
Nominal Output Current at +25°C (+298.2°K)		298.2	298.2	µA
Nominal Temperature Coefficient		1.0	1.0	µA/°K
Calibration Error at +25°C	Notes 1, 5	±10.0 Max	±5.0 Max	°C
Absolute Error	-55°C to + 150°C, Note 7			
Without External Calibration Adjustment		±20.0 Max	±10.0 Max	°C
With External Calibration Adjustment		±5.8 Max	±3.0 Max	°C
Non-Linearity	Note 6	±3.0 Max	±1.5 Max	°C
Repeatability	Notes 2, 6	±0.1 Max	±0.1 Max	°C
Long Term Drift	Notes 3, 6	±0.1 Max	±0.1 Max	°C/Month
Current Noise		40	40	pA/$\sqrt{Hz}$
Power Supply Rejection				
+4V < V+ < +5V		0.5	0.5	µA/V
+5V < V+ < +15V		0.2	0.2	µA/V
+15V < V+ < +30V		0.1	0.1	µA/V
Case Isolation to Either Lead		10^{10}	10^{10}	Ω
Effective Shunt Capacitance		100	100	pF
Electrical Turn-On Time	Note1	20	20	µs
Reverse Bias Leakage Current	Note 4	10	10	pA
Power Supply Range		+4 to +30	+4 to +30	V

NOTE:

1. Does not include self heating effects.
2. Maximum deviation between +25°C reading after temperature cycling between -55°C and +150°C.
3. Conditions constant +5V, constant +125°C.
4. Leakage current doubles every +10°C.
5. Mechanical strain on package may disturb calibration of device.
6. Guaranteed but not tested.
7. -55°C Guaranteed by testing at +25°C and +150°C.

Trimming Out Errors

The ideal graph of current versus temperature for the AD590 is a straight line, but as Figure 1 shows, the actual shape is slightly different. Since the sensor is limited to the range of -55°C to +150°C, it is possible to optimize the accuracy by trimming. Trimming also permits extracting maximum performance from the lower-cost sensors.

The circuit of Figure 2 trims the slope of the AD590 output. The effect of this is shown in Figure 3.

The circuit of Figure 4 trims both the slope and the offset. This is shown in Figure 5. The diagrams are exaggerated to show effects, but it should be clear that these trims can be used to minimize errors over the whole range, or over any selected part of the range. In fact, it is possible to adjust the I-grade device to give less than 0.1°C error over the range 0°C to +90°C and less than 0.05°C error from +25°C to +60°C.

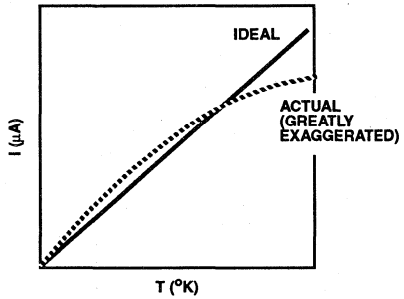


FIGURE 1. TRIMMING OUT ERRORS

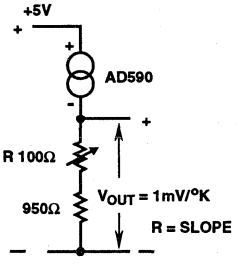


FIGURE 2. SLOPE TRIMMING

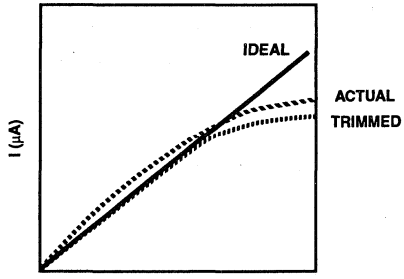


FIGURE 3. EFFECT OF SLOPE TRIM

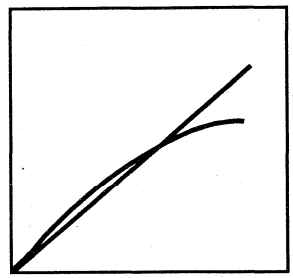


FIGURE 5A. UNTRIMMED

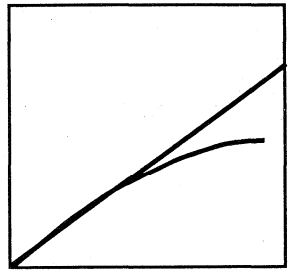


FIGURE 5B. TRIM ONE: OFFSET

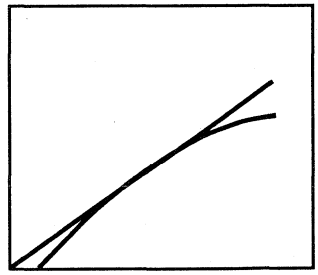


FIGURE 5C. TRIM TWO: SLOPE

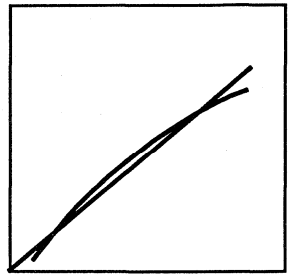


FIGURE 5D. TRIM THREE: OFFSET AGAIN

FIGURE 5. EFFECT OF SLOPE AND OFFSET TRIMMING

Accuracy

Maximum errors over limited temperature spans, with V_S = +5V, are listed by device grade in the following tables. The tables reflect the worst-case linearities, which invariably occur at the extremities of the specified temperature range. The trimming conditions for the data in the tables are shown in Figure 2 and Figure 4.

All errors listed in the tables are ±°C. For example, if ±1°C maximum error is required over the +25°C to +75°C range (i.e., lowest temperature of +25°C and span of 50°C), then the trimming of a J-grade device, using the single-trim circuit (Figure 2), will result in output having the required accuracy over the stated range. An I-grade device with two trims (Figure 4) will have less than ±0.2°C error. If the requirement is for less than ±1.4°C maximum error, from -25°C to +75°C (100° span from -25°C), it can be satisfied by an I-grade device with two trims.

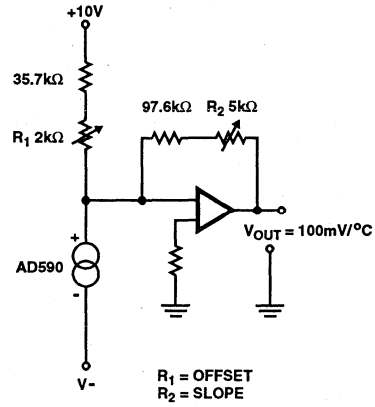


FIGURE 4. SLOPE AND OFFSET TRIMMING

I Grade Maximum Errors, °C

NUMBER OF TRIMS	TEMPERATURE SPAN (°C)	LOWEST TEMPERATURE IN SPAN (°C)							
		-55	-25	0	+25	+50	+75	+100	+125
None	10	8.4	9.2	10.0	10.8	11.6	12.4	13.2	14.4
None	25	10.0	10.4	11.0	11.8	12.0	13.8	15.0	16.0
None	50	13.0	13.0	12.8	13.8	14.6	16.4	18.0	-
None	100	15.2	16.0	16.6	17.4	18.8	-	-	-
None	150	18.4	19.0	19.2	-	-	-	-	-
None	205	20.0	-	-	-	-	-	-	-
One	10	0.6	0.4	0.4	0.4	0.4	0.4	0.4	0.6
One	25	1.8	1.2	1.0	1.0	1.0	1.2	1.6	1.8
One	50	3.8	3.0	2.0	2.0	2.0	3.0	3.8	-
One	100	4.8	4.5	4.2	4.2	5.0	-	-	-
One	150	5.5	4.8	5.5	-	-	-	-	-
One	205	5.8	-	-	-	-	-	-	-
Two	10	0.3	0.2	0.1	(Note 1)	(Note 1)	0.1	0.2	0.3
Two	25	0.5	0.3	0.2	(Note 1)	0.1	0.2	0.3	0.5
Two	50	1.2	0.6	0.4	0.2	0.2	0.3	0.7	-
Two	100	1.8	1.4	1.0	2.0	2.5	-	-	-
Two	150	2.6	2.0	2.8	-	-	-	-	-
Two	205	3.0	-	-	-	-	-	-	-

NOTE:

1. 1. Less than ±0.05°C.

J Grade Maximum Errors, °C

NUMBER OF TRIMS	TEMPERATURE SPAN (°C)	LOWEST TEMPERATURE IN SPAN (°C)							
		-55	-25	0	+25	+50	+75	+100	+125
None	10	4.2	4.6	5.0	5.4	5.8	6.2	6.6	7.2
None	25	5.0	5.2	5.5	5.9	6.0	6.9	7.5	8.0
None	50	6.5	6.5	6.4	6.9	7.3	8.2	9.0	-
None	100	7.7	8.0	8.3	8.7	9.4	-	-	-
None	150	9.2	9.5	9.6	-	-	-	-	-
None	205	10.0	-	-	-	-	-	-	-
One	10	0.3	0.2	0.2	0.2	0.2	0.2	0.2	0.3
One	25	0.9	0.6	0.5	0.5	0.5	0.6	0.8	0.9
One	50	1.9	1.5	1.0	1.0	1.0	1.5	1.9	-
One	100	2.3	2.2	2.0	2.0	2.3	-	-	-
One	150	2.5	2.4	2.5	-	-	-	-	-
One	205	3.0	-	-	-	-	-	-	-
Two	10	0.1	(Note 1)	(Note 1)	(Note 1)	(Note 1)	(Note 1)	(Note 1)	0.1
Two	25	0.2	0.1	(Note 1)	(Note 1)	(Note 1)	(Note 1)	0.1	0.2
Two	50	0.4	0.2	0.1	(Note 1)	(Note 1)	0.1	0.2	(Note 1)
Two	100	0.7	0.5	0.3	0.7	1.0	-	-	-
Two	150	1.0	0.7	1.2	-	-	-	-	-
Two	205	1.6	-	-	-	-	-	-	-

NOTE:

1. Less than ±0.05°C.

Notes

1. Maximum errors over all ranges are guaranteed based on the known behavior characteristic of the AD590.
2. For one-trim accuracy specifications, the 205°C span is assumed to be trimmed at +25°C; for all other spans, it is assumed that the device is trimmed at the midpoint.
3. For the 205°C span, it is assumed that the two-trim temperatures are in the vicinity of +0°C and +140°C; for all other spans, the specified trims are at the endpoints.
4. In precision applications, the actual errors encountered are usually dependent upon sources of error which are often overlooked in error budgets. These typically include:
   a. Trim error in the calibration technique used
   b. Repeatability error
   c. Long term drift errors

Trim Error is usually the largest error source. This error arises from such causes as poor thermal coupling between the device to be calibrated and the reference sensor; reference sensor errors; lack of adequate time for the device being calibrated to settle to the final temperature; radically different thermal resistances between the case and the surroundings ($R_{\theta CA}$) when trimming and when applying the device.

Repeatability Errors arise from a strain hysteresis of the package. The magnitude of this error is solely a function of the magnitude of the temperature span over which the device is used. For example, thermal shocks between +0°C and +100°C involve extremely low hysteresis and result in repeatability errors of less than ±0.05°C. When the thermal-shock excursion is widened to -55°C to +150°C, the device will typlcally exhibit a repeatability error of ± 0.05 °C (± 0.10 guaranteed maximum).

Long Term Drift Errors are related to the average operating temperature and the magnitude of the thermal-shocks experienced by the device. Extended use of the AD590 at temperatures above +100°C typically results in long-term drift of ±0.03°C per month; the guaranteed maximum is ± 0.10 °C per month. Continuous operation at temperatures below +100°C induces no measurable drifts in the device. Besides the effects of operating temperature, the severity of thermal shocks incurred will also affect absolute stability. For thermal-shock excursions less than +100°C, the drift is difficult to measure (<0.03°C). However, for +200°C excursions, the device may drift by as much as ±0.10°C after twenty such shocks. If severe, quick shocks are necessary in the application of the device, realistic simulated life tests are recommended for a thorough evaluation of the error introduced by such shocks.

Typical Applications

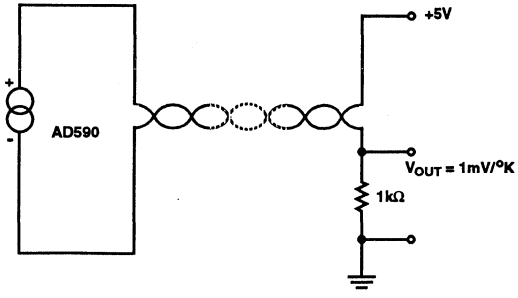


FIGURE 6A.

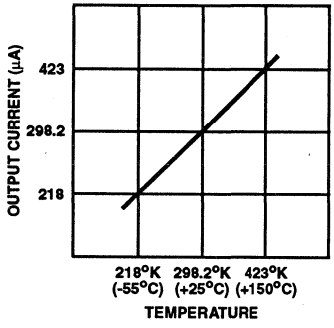


FIGURE 6B.

FIGURE 6. SIMPLE CONNECTION. OUTPUT IS PROPORTIONAL TO ABSOLUTE TEMPERATURE

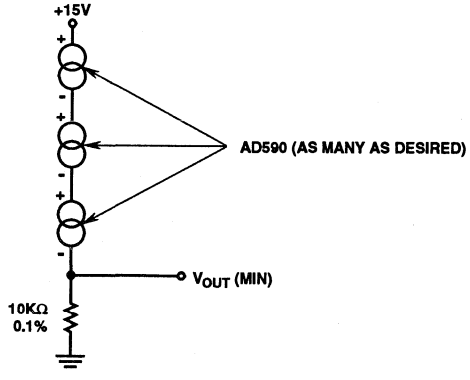


FIGURE 7. LOWEST TEMPERATURE SENSING SCHEME. AVAILABLE CURRENT IS THAT OF THE "COLDEST" SENSOR

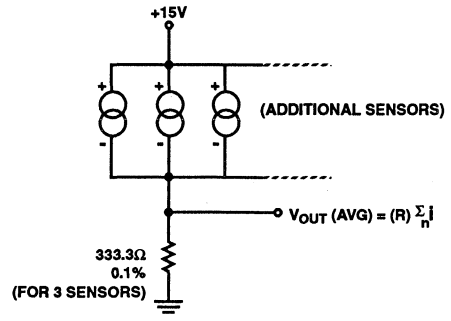


FIGURE 8. AVERAGE TEMPERATURE SENSING SCHEME

The sum of the AD590 currents appears across R, which is chosen by the formula: $R = \frac{10k\Omega}{n}$

n being the number of sensors. See Figure 8.

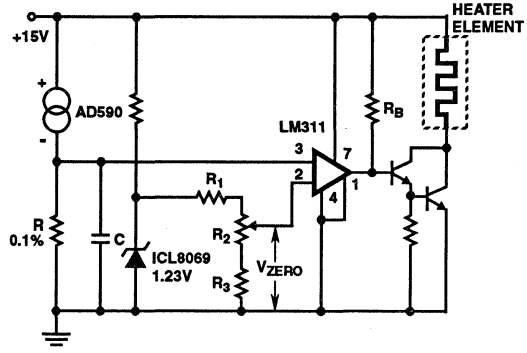


FIGURE 9. SINGLE SETPOINT TEMPERATURE CONTROLLER

The AD590 produces a temperature-dependent voltage across R (C is for filtering noise). Setting R_2 produces a scale-zero voltage. For the celsius scale, make R = 1kΩ and V_{ZERO} = 0.273V. For Fahrenheit, R = 1.8kΩ and V_{ZERO} = 0.460V. See Figure 9.

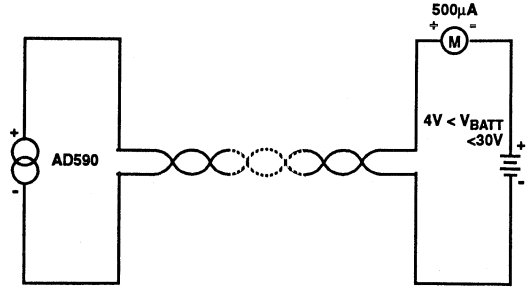


FIGURE 10. SIMPLEST THERMOMETER.

Meter displays current output directly in degrees Kelvin. using the AD590J, sensor output is within ±10 degrees over the entire range. See Figure 10.

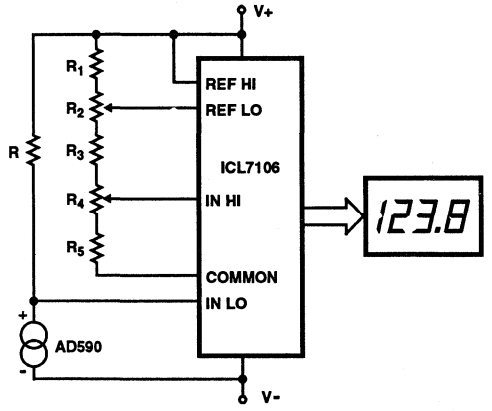


FIGURE 11. BASIC DIGITAL THERMOMETER, CELSIUS AND FAHRENHEIT SCALES

	R	R_1	R_2	R_3	R_4	R_5
°F	9.00	4.02	2.0	12.4	10.0	0
°C	5.00	4.02	2.0	5.11	5.0	11.8

$$\sum_{n=1}^{5} R_n = 28k\Omega \text{ nominal}$$

ALL values in kΩ

The ICL7106 has a V_{IN} span of ±2.0V and a V_{CM} range of (V+ -0.5) volts to (V- +1) volts. R is scaled to bring each range within V_{CM} while not exceeding V_{IN}. V_{REF} for both scales is 500mV maximum rending on the celsius range +199.9°C limited by the (short-term) maximum allowable sensor temperature. Maximum reading on the fahrenheit range is +199.9°F (+93.3°C) limited by the number of display digits. See Figure 11 and notes below.

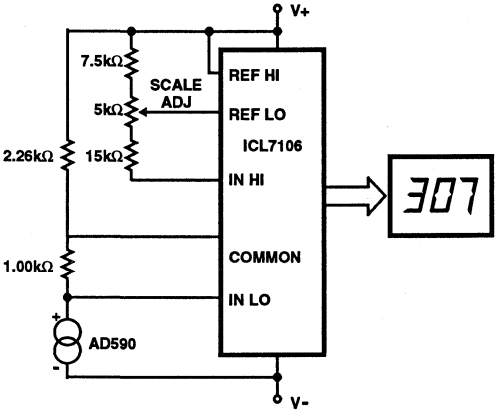


FIGURE 12. BASIC DIGITAL THERMOMETER, KELVIN SCALE

The Kelvin scale version reads from 0 to +1999°K theoretically, and from +223°K to +473°K actually. The 2.26kΩ resistor brings the input within the ICL7106 V_{CM} range: 2 qeneral-purpose silicon diodes or an LED may be substituted. See Figure 12 and notes below.

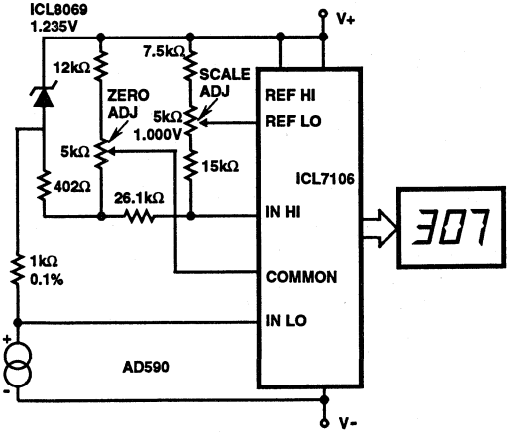


FIGURE 13. BASIC DIGITAL THERMOMETER, KELVIN SCALE WITH ZERO ADJUST

This circuit allows "zero adjustment" as well as slope adjustment. the ICL8069 brings the input within the common-mode range, while the 5kΩ pots trim any offset at +218°K (-55°C), and set the scale factor. See Figure 13 and notes below.

Notes for Figure 11, Figure 12 and Figure 13

Since all 3 scales have narrow V_{IN} spans, some optimization of ICL7106 components can be made to lower noise and preserve CMR. The table below shows the suggested values. Similar scaling can be used with the ICL7126 and ICL7136.

SCALE	V_{IN} RANGE (V)	R_{INT} (kΩ)	C_{AZ} (µF)
K	0.223 to 0.473	220	0.47
C	-0.25 to +1.0	220	0.1
F	-0.29 to +0.996	220	0.1

For all:
$C_{REF} = 0.1\mu F$
$C_{INT} = 0.22\mu F$
$C_{OSC} = 100pF$
$R_{OSC} = 100k\Omega$

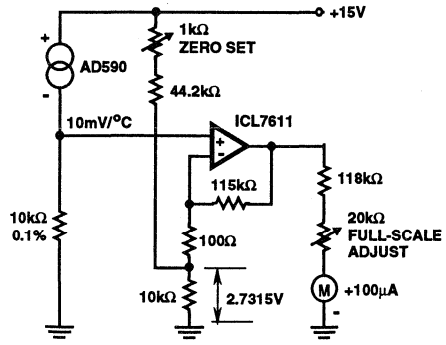


FIGURE 14. CENTIGRADE THERMOMETER (0°C - +100°C)

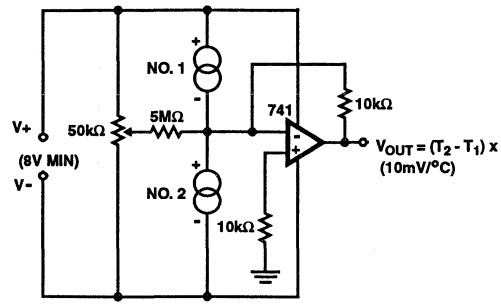


FIGURE 15. DIFFERENTIAL THERMOMETER

The ultra-low bias current of the ICL7611 allows the use of large value gain resistors, keeping meter current error under $^1/_2$%, and therefore saving the expense of an extra meter driving amplifier. See Figure 14.

The 50kΩ pot trims offsets in the devices whether internal or external, so it can be used to set the size of the difference interval. this also makes it useful for liquid level detection (where there will be a measurable temperature difference). See Figure 15.

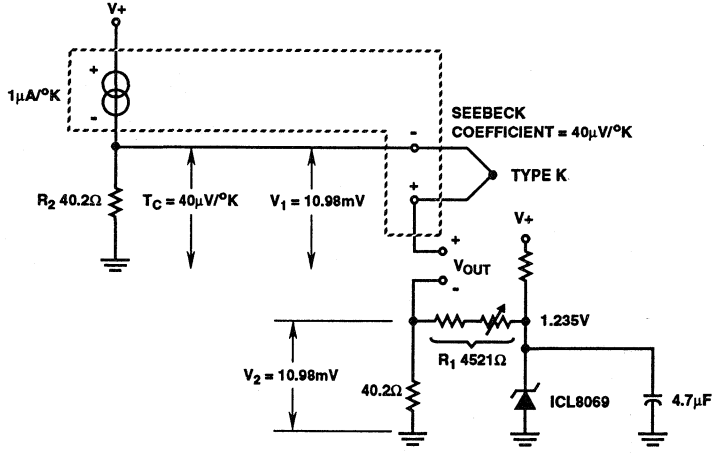


FIGURE 16. COLD JUNCTION COMPENSATION FOR TYPE K THERMOCOUPLE

The reference junction(s) should be in close thermal contact with the AD590 case. V+ must be at least 4V, while ICL8069 current should be set at 1mA - 2mA. Calibration does not require shorting or removal of the thermocouple: set R_1 for V_2 = 10.98mV. If very precise measurements are needed, adjust R_2 to the exact Seebeck coefficient for the thermocouple used (measured or from table) note V_1, and set R_1 to buck out this voltage (i.e., set $V_2 = V_1$). For other thermocouple types, adjust values to the appropriate Seebeck coefficient. See Figure 16.

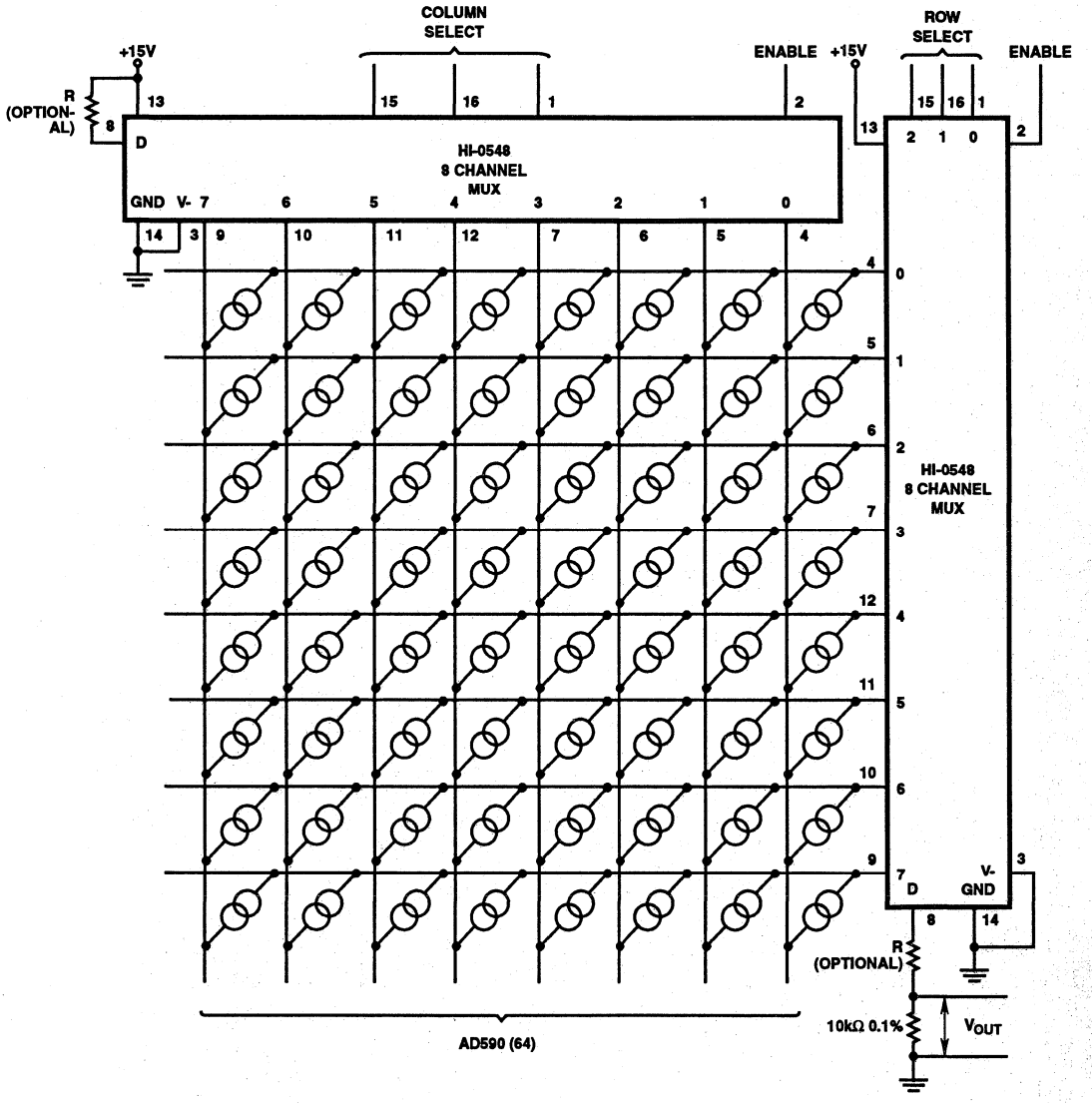


FIGURE 17. MULTIPLEXING SENSORS

If shorted sensors are possible, a series resistor in series with the D line will limit the current (shown as R, above: only one is needed). A six-bit digital word will select one of 64 sensors.

Die Characteristics

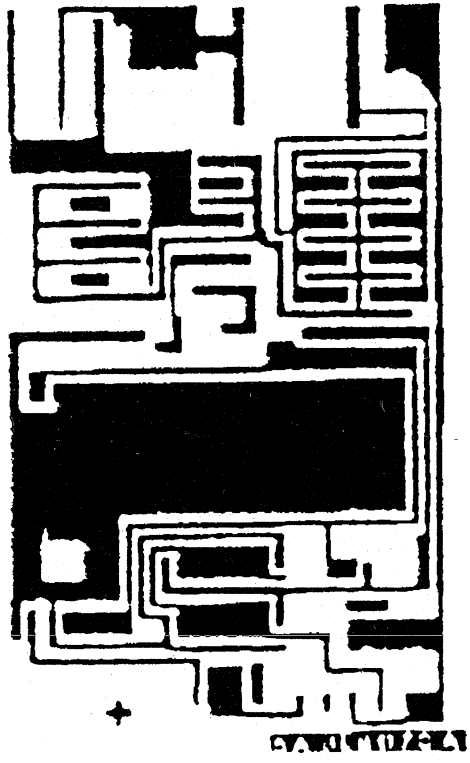
DIE DIMENSIONS:
37 x 58 x 14 ± 1mils

METALLIZATION:
Type: Aluminum 100%
Thickness: 15kÅ ± 1kÅ

GLASSIVATION:
Type: PSG/Nitride
PSG Thickness: 7kÅ ± 1.4kÅ
Nitride Thickness: 8kÅ ± 1.2kÅ

Metallization Mask Layout

AD590



HARRIS SEMICONDUCTOR

ICL8069

December 1993

Low Voltage Reference

Features

- **Low Bias Current - 50μA Min**
- **Low Dynamic Impedance**
- **Low Reverse Voltage**
- **Low Cost**

Description

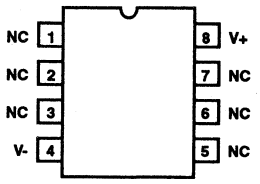
The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principle to achieve excellent stability and low noise at reverse currents down to 50μA. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

Ordering Information

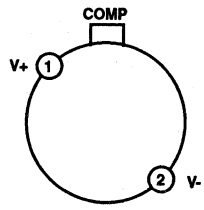
PART NUMBER	MAXIMUM TEMPCO	TEMPERATURE RANGE	PACKAGE
ICL8069CCZR	0.005%/°C	0°C to +70°C	TO-92
ICL8069CCSQ	0.005%/°C	0°C to +70°C	TO-52
ICL8069DCZR	0.01%/°C	0°C to +70°C	TO-92
ICL8069DCSQ	0.01%/°C	0°C to +70°C	TO-52
ICL8069CCBA	0.005%/°C	0°C to +70°C	8 Lead SOIC
ICL8069DCBA	0.01%/°C	0°C to +70°C	8 Lead SOIC
ICL8069CMSQ	0.005%/°C	-55°C to +125°C	TO-52
ICL8069DMSQ	0.01%/°C	-55°C to +125°C	TO-52

Pinouts

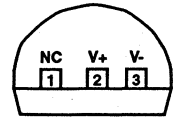
ICL8069 (SOIC) TOP VIEW



ICL8069 (TO-52) TOP VIEW



ICL8069 (TO-92) TOP VIEW



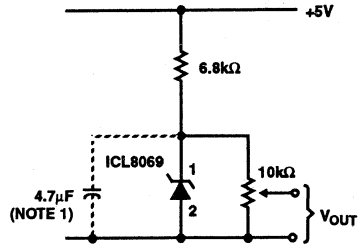
14 SPECIAL PURPOSE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

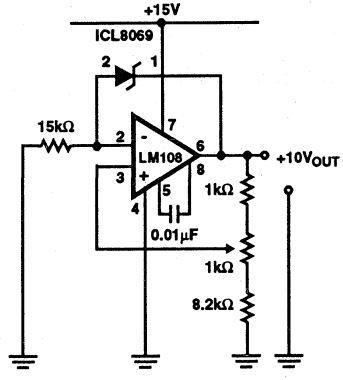
File Number **3172**

Functional Block Diagrams

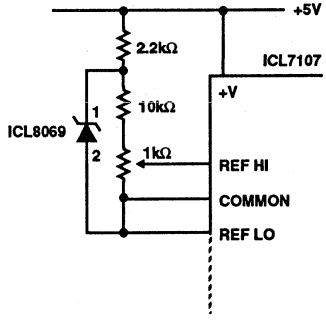
SIMPLE REFERENCE (1.2V OR LESS)



BUFFERED 10V REFERENCE USING A SINGLE SUPPLY



DOUBLE REGULATED 100mV REFERENCE FOR ICL7107 ONE-CHIP DPM CIRCUIT



Absolute Maximum Ratings

Reverse Voltage ..... See Note 2
Forward Current 10mA
Reverse Current 10mA
Storage Temperature ..... -65°C to +150°C
Lead Temperature (Soldering, 10s) ..... +300°C
Junction Temperature
SOP ..... +150°C

Thermal Information

Thermal Resistance θ_{JA}
SOIC Package ..... 160°C/W
Operating Temperature
ICL8069C ..... 0°C to +70°C
ICL8069M ..... -55°C to +125°C
Power Dissipation ..... Limited by MAX Forward/Reverse Current

Electrical Specifications T_A = +25°C Unless Otherwise Specified

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Breakdown Voltage	I_R = 500µA	1.20	1.23	1.25	V
Reverse Breakdown Voltage Change	50µA ≤ I_R ≤ 5mA	-	15	20	mV
Reverse Dynamic Impedance	I_R = 50µA	-	1	2	Ω
	I_R = 500µA	-	1	2	Ω
Forward Voltage Drop	I_F = 500µA	-	0.7	1	V
RMS Noise Voltage	10Hz ≤ F ≤ 10kHz I_R = 500µA	-	5	-	µV
Long Term Stability	I_R = 4.75mA T_A = +25°C	-	1	-	ppm/kHR
Breakdown Voltage Temperature Coefficient ICL8069C	I_R = 500µA, T_A = Operating Temperature Range (Note 3)	-	-	0.005	%/°C
ICL8069D		-	-	0.01	%/°C
Reverse Current Range	1.18V to 1.27V	0.050	-	5	mA

NOTES:

1. If circuit strays in excess of 200pF are anticipated, a 4.7µF shunt capacitor will ensure stability under all operating conditions.
2. In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.
3. For the military part, measurements are made at +25°C, -55°C, and +125°C. The unit is then classified as a function of the worst case TC from +25°C to -55°C, or +25°C to +125°C.

Typical Performance Curves

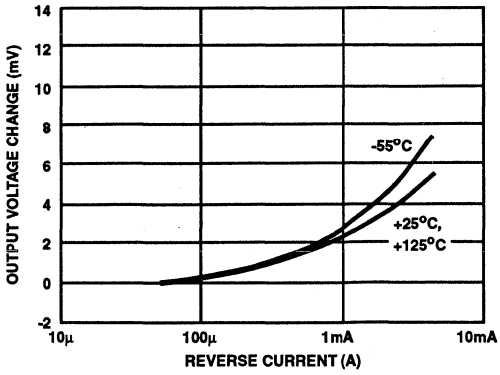


FIGURE 1. VOLTAGE CHANGE AS A FUNCTION OF REVERSE CURRENT

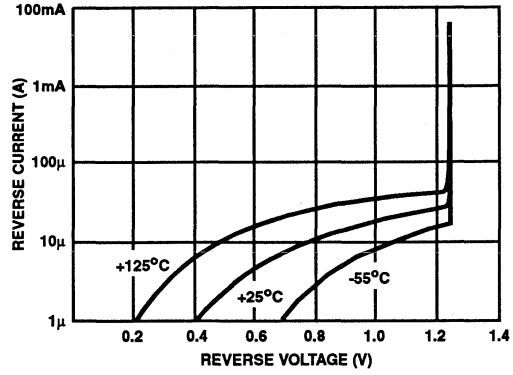


FIGURE 2. REVERSE VOLTAGE AS A FUNCTION OF CURRENT

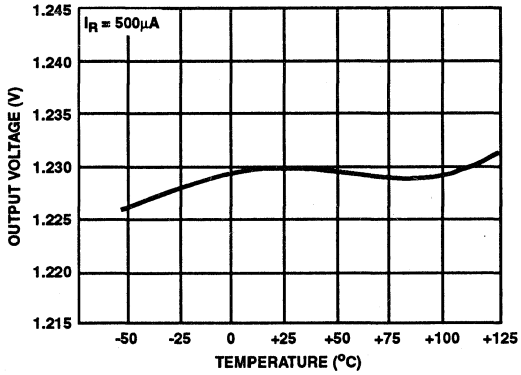


FIGURE 3. REVERSE VOLTAGE AS A FUNCTION OF TEMPERATURE

HARRIS SEMICONDUCTOR

ICM7170

December 1993

µP-Compatible Real-Time Clock

Features

- 8-bit µP Bus Compatible
  - Multiplexed or Direct Addressing
- Regulated Oscillator Supply Ensures Frequency Stability and Low Power
- Time From 1/100 Seconds to 99 Years
- Software Selectable 12/24 Hour Format
- Latched Time Data Ensures No Roll Over During Read
- Full Calendar with Automatic Leap Year Correction
- On-Chip Battery Backup Switchover Circuit
- Access Time Less than 300ns
- 4 Programmable Crystal Oscillator Frequencies Over Industrial Temperature Range
- 3 Programmable Crystal Oscillator Frequencies Over Military Temperature Range
- On-Chip Alarm Comparator and RAM
- Interrupts from Alarm and 6 Selectable Periodic Intervals
- Standby Micro-Power Operation: 1.2µA Typical at 3.0V and 32kHz Crystal

Applications

- Portable and Personal Computers
- Data Logging
- Industrial Control Systems
- Point Of Sale

Ordering Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7170IPG	-40°C to +85°C	24 Lead Plastic DIP
ICM7170IDG	-40°C to +85°C	24 Lead Ceramic
ICM7170IBG	-40°C to +85°C	24 Lead SOIC
ICM7170MDG	-55°C to +125°C	24 Lead Ceramic
ICM7170AIPG	-40°C to +85°C	24 Lead Plastic DIP
ICM7170AIDG	-40°C to +85°C	24 Lead Ceramic
ICM7170AIBG	-40°C to +85°C	24 Lead SOIC
ICM7170AMDG	-55°C to +125°C	24 Lead Ceramic

NOTE: "A" Parts Screened to <5µA I_{STBY} at 32kHz

Description

The ICM7170 real time clock is a microprocessor bus compatible peripheral, fabricated using Harris' silicon gate CMOS LSI process. An 8-bit bidirectional bus is used for the data I/O circuitry. The clock is set or read by accessing the 8 internal separately addressable and programmable counters from $^1/_{100}$ seconds to years. The counters are controlled by a pulse train divided down from a crystal oscillator circuit, and the frequency of the crystal is selectable with the on-chip command register. An extremely stable oscillator frequency is achieved through the use of an on-chip regulated power supply.

The device access time (t_{ACC}) of 300ns eliminates the need for wait states or software overhead with most microprocessors. Furthermore, an ALE (Address Latch Enable) input is provided for interfacing to microprocessors with a multiplexed address/data bus. With these two special features, the ICM7170 can be easily interfaced to any available microprocessor.

The ICM7170 generates two types of interrupts, periodic and alarm. The periodic interrupt (100Hz, 10Hz, etc.) can be programmed by the internal interrupt control register to provide 6 different output signals. The alarm interrupt is set by loading an on-chip 51-bit RAM that activates an interrupt output through a comparator. The alarm interrupt occurs when the real time counter and alarm RAM time are equal. A status register is available to indicate the interrupt source.

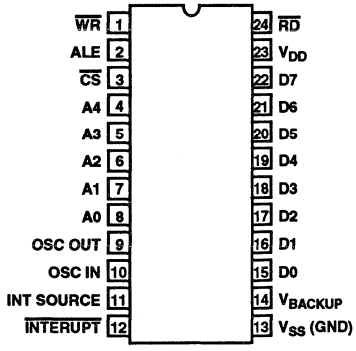
An on-chip Power Down Detector eliminates the need for external components to support the battery back-up function. When a power down or power failure occurs, internal logic switches the on-chip counters to battery back-up operation. Read/write functions become disabled and operation is limited to time-keeping and interrupt generation, resulting in low power consumption.

Internal latches prevent clock roll-over during a read cycle. Counter data is latched on the chip by reading the 100th-seconds counter and is held indefinitely until the counter is read again, assuring a stable and reliable time value.

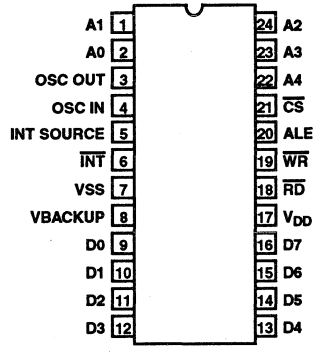
File Number 3019

Pinouts

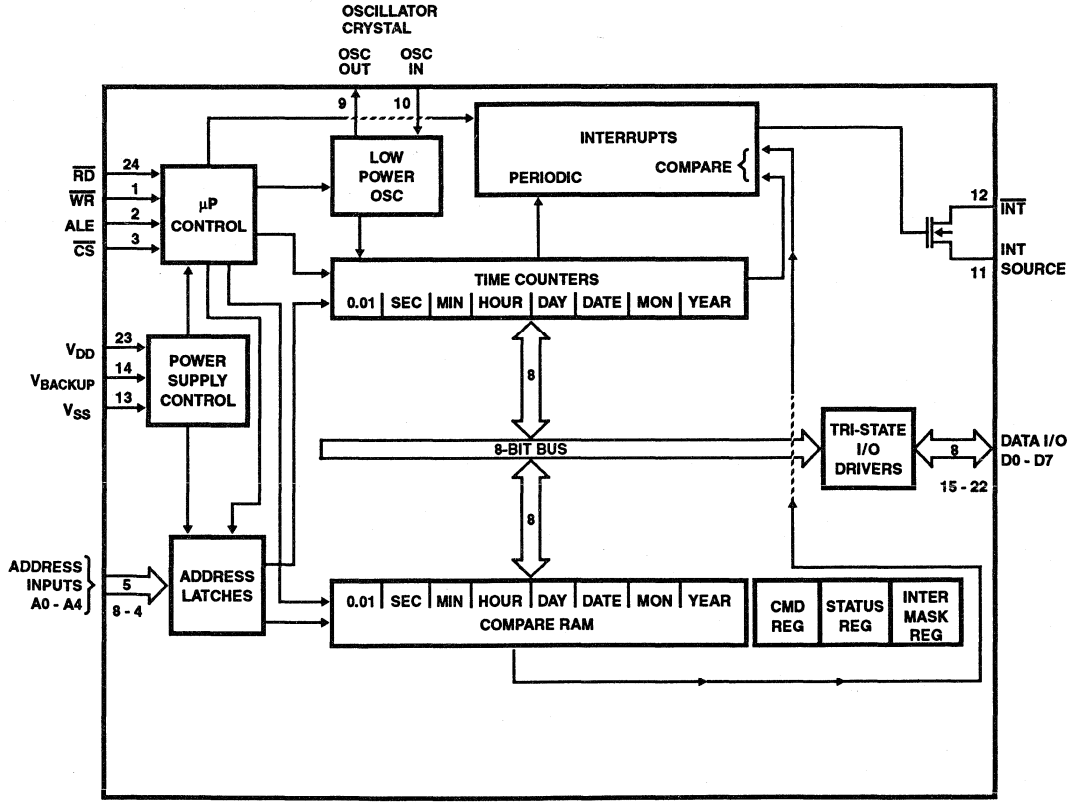
ICM7170 (PDIP, CDIP)
TOP VIEW



ICM7170 (SOIC)
TOP VIEW



Functional Block Diagram



Absolute Maximum Ratings

Supply Voltage ..... +8.0V
Power Dissipation (Note 1) 500mW
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
Input Voltage (Any Terminal) (Note 2) ..... V_{DD} +0.3V to V_{SS} -0.3V

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
Plastic Package	75°C/W	-
Ceramic DIP Package	63°C/W	12°C/W
SOIC Package	75°C/W	-

Junction Temperature
Plastic Package ..... +150°C
Ceramic Package ..... +175°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Electrical Specifications

T_A = -40°C to +85°C, V_{DD} +5V ±10%, V_{BACKUP} V_{DD}, V_{SS} = 0V Unless Otherwise Specified
All I_{DD} specifications include all input and output leakages (ICM7170 and ICM7170A)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Supply Range, V_{DD}	F_{OSC} = 32kHz		1.9	-	5.5	V
	F_{OSC} = 1, 2, 4MHz		2.6	-	5.5	V
Standby Current, $I_{STBY(1)}$	F_{OSC} = 32kHz Pins 1 - 8,15 - 22 and 24 = V_{DD}	ICM7170	-	1.2	20.0	µA
	V_{DD} = V_{SS}; V_{BACKUP} = V_{DD} - 3.0V For ICM7170A See General Notes 5	ICM7170A	-	1.2	5.0	µA
Standby Current, I_{STBY}(2)	F_{OSC} =4MHz Pins 1 - 8,15 - 22 and 24 = V_{DD} V_{DD} = V_{SS}; V_{BACKUP} = V_{DD} - 3.0V		-	20	150	µA
Operating Supply Current, $I_{DD(1)}$	F_{OSC} = 32kHz Read/Write Operation at 100Hz		-	0.3	1.2	mA
Operating Supply Current, $I_{DD(2)}$	F_{OSC} = 32kHz Read/Write Operation at 1MHz		-	1.0	2.0	mA
Input Low Voltage (Except Osc.), V_{IL}	V_{DD} = 5.0V		-	-	0.8	V
Input High Voltage (Except Osc.), V_{IH}	V_{DD} = 5.0V		2.4	-	-	V
Output Low Voltage (Except Osc.), V_{OL}	I_{OL} = 1.6mA		-	-	0.4	V
Output High Voltage Except $\overline{INTERRUPT}$ (Except Osc.), V_{OH}	I_{OH} = -400µA		2.4	-	-	V
Input Leakage Current, I_{IL}	V_{IN} =V_{DD} or V_{SS}		-10	0.5	+10	µA
Tri-state Leakage Current (D0 - D7), I_{OL}(1)	V_O =V_{DD} or V_{SS}		-10	0.5	+10	µA
Backup Battery Voltage, $V_{BATTERY}$	F_{OSC} = 1, 2, 4MHz		2.6	-	V_{DD} - 1.3	V
Backup Battery Voltage, $V_{BATTERY}$	F_{OSC} = 32kHz		1.9	-	V_{DD} - 1.3	V
Leakage Current $\overline{INTERRUPT}$, I_{OL}(2)	V_O = V_{DD}	INT SOURCE Connected to V_{SS}	-	0.5	10	µA
CAPACITANCE D0 - D7, $C_{I/O}$			-	8	-	pF
CAPACITANCE A0 - A4, $C_{ADDRESS}$			-	6	-	pF
CAP. $\overline{RD}$, $\overline{WR}$, $\overline{CS}$ ALE, $C_{CONTROL}$			-	6	-	pF
Total Osc. Input Cap., C_{IN} Osc.			-	3	-	pF

AC Electrical Specifications T_A = -40°C to +85°C, V_{DD} = +5V ± 10%, V_{BACKUP} = V_{DD}, D0 - D7 Load Capacitance = 150pF, V_{IL} = 0.4V, V_{IH} = 2.8V, Unless Otherwise Specified

PARAMETER	MIN	MAX	UNITS
READ CYCLE TIMING			
READ to DATA Valid, t_{RD}	-	250	ns
ADDRESS Valid to DATA Valid, t_{ACC}	-	300	ns
READ Cycle Time, t_{CYC}	400	-	ns
Read High Time, t_{RH}	150	-	ns
$\overline{RD}$ High to Bus Tri-state, t_{RH}	-	25	ns
ADDRESS to READ Set Up Time, t_{AS}	50	-	ns
ADDRESS HOLD Time After READ, t_{AR}	0	-	ns
WRITE CYCLE TIMING			
ADDRESS Valid to WRITE Strobe, t_{AD}	50	-	ns
ADDRESS Hold Time for WRITE, t_{WA}	0	-	ns
WRITE Pulse Width, Low, t_{WL}	100	-	ns
WRITE High Time, t_{WH}	300	-	ns
DATA IN to WRITE Set Up Time, t_{DW}	100	-	ns
DATA IN Hold Time After WRITE, t_{WD}	30	-	ns
WRITE Cycle Time, t_{CYC}	400	-	ns
MULTIPLEXED MODE TIMING			
ALE Pulse Width, High, t_{LL}	50	-	ns
ADDRESS to ALE Set Up Time, t_{AL}	30	-	ns
ADDRESS Hold Time After ALE, t_{LA}	30	-	ns

NOTE:

1. T_A = 25°C
2. Due to the SCR structure inherent in the CMOS process, connecting any terminal at voltages greater than V_{DD} or less than V_{SS} may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7170 be turned on first.

Timing Diagrams

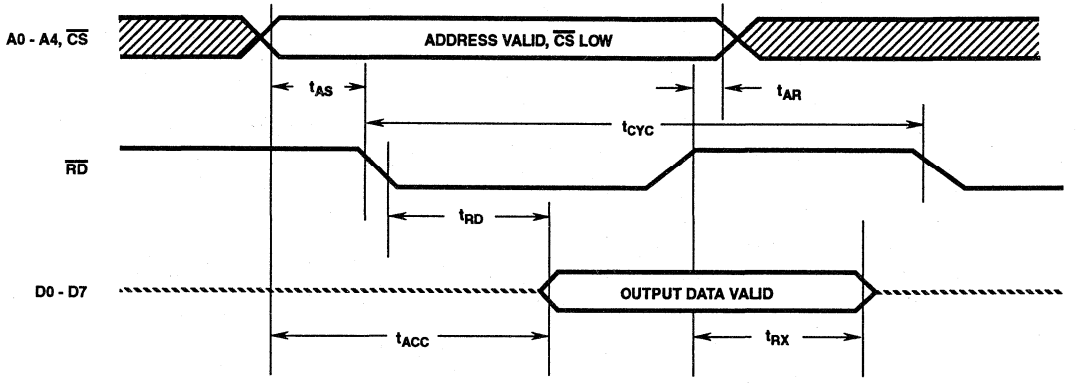


FIGURE 1. READ CYCLE TIMING FOR NON-MULTIPLEXED BUS (ALE = V_{IH}, $\overline{WR}$ = V_{IH})

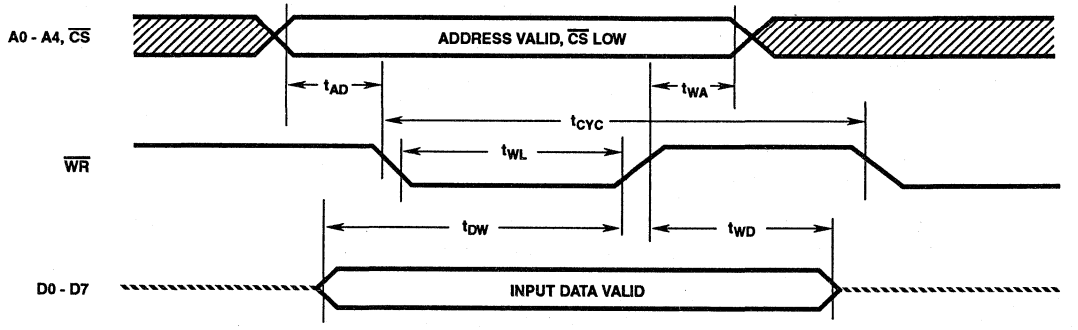


FIGURE 2. WRITE CYCLE TIMING FOR NON-MULTIPLEXED BUS (ALE = V_{IH}, $\overline{RD}$ = V_{IH})

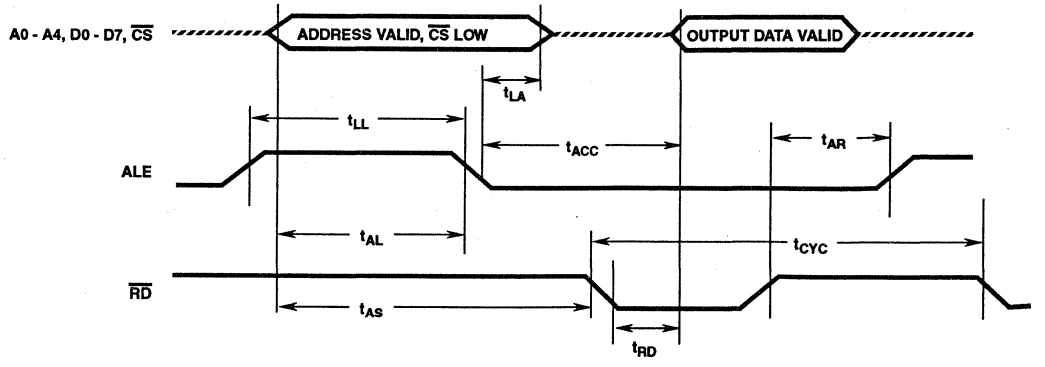


FIGURE 3. READ CYCLE TIMING FOR MULTIPLEXED BUS ($\overline{WR}$ = V_{IH})

Timing Diagrams (Continued)

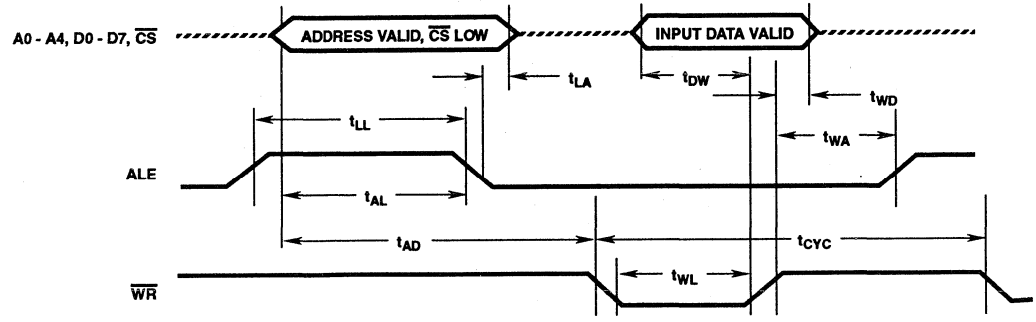


FIGURE 4. WRITE CYCLE TIMING FOR MULTIPLEXED BUS ($\overline{RD}$ = V_{IH})

Pin Description

SIGNAL	PIN NUMBER	SOIC PIN NUMBER	DESCRIPTION
$\overline{WR}$	1	19	$\overline{Write}$ Input
ALE	2	20	Address Latch Enable Input
$\overline{CS}$	3	21	$\overline{Chip\ Select}$ Input
A4-A0	4 - 8	22 - 2	Address Inputs
OSC OUT	9	3	Oscillator Output
OSC IN	10	4	Oscillator Input
INT SOURCE	11	5	Interrupt Source
$\overline{INTERRUPT}$	12	6	$\overline{Interrupt}$ Output
V_{SS} (GND)	13	7	Digital Common
V_{BACKUP}	14	8	Battery Negative Side
D0 - D7	15 - 22	9 - 16	Data I/O
V_{DD}	23	17	Positive Digital Supply
$\overline{RD}$	24	18	$\overline{Read}$ Input

TABLE 1. COMMAND REGISTER FORMAT

COMMAND REGISTER ADDRESS (10001b, 11h) WRITE-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
n/a	n/a	Normal/Test Mode	Interrupt Enable	Run/Stop	12/24 Hour Format	Crystal Frequency	Crystal Frequency

TABLE 2. COMMAND REGISTER BIT ASSIGNMENTS

D5	TEST BIT	D4	INTERRUPT ENABLE	D3	RUN/STOP	D2	24/12 HOUR FORMAT	D1	D0	CRYSTAL FREQUENCY
0	Normal Mode	0	Interrupt disabled	0	Stop	0	12 Hour Mode	0	0	32.768kHz
1	Test Mode	1	Interrupt enable	1	Run	1	24 Hour Mode	0	1	1.048576MHZ
								1	0	2.097152MHz
								1	1	4.194304MHz

TABLE 3. ADDRESS CODES AND FUNCTIONS

ADDRESS							DATA								
A4	A3	A2	AI	A0	HEX	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0	VALUE
0	0	0	0	0	00	Counter-1/100 seconds	-								0 - 99
0	0	0	0	1	01	Counter-hours	-	-	-						0 - 23
						12 Hour Mode	†	-	-	-					1 - 12
0	0	0	1	0	02	Counter-minutes	-	-							0 - 59
0	0	0	1	1	03	Counter-seconds	-	-							0 - 59
0	0	1	0	0	04	Counter-month	-	-	-	-					1 - 12
0	0	1	0	1	05	Counter-date	-	-	-						1 - 31
0	0	1	1	0	06	Counter-year	-								0 - 99
0	0	1	1	1	07	Counter-day of week	-	-	-	-	-				0 - 6
0	1	0	0	0	08	RAM-1/100 seconds	M								0 - 99
0	1	0	0	1	09	RAM-hours	-	M	-						0 - 23
						12 Hour Mode	†	M	-	-					1 - 12
0	1	0	1	0	0A	RAM-minutes	M	-	.	.					0 - 59
0	1	0	1	1	0B	RAM-seconds	M	-	.	.					0 - 59
0	1	1	0	0	0C	RAM-month	M	-	-	-					1 - 12
0	1	1	0	1	0D	RAM-date	M	-	-						1 - 31
0	1	1	1	0	0E	RAM-year	M								0 - 99
0	1	1	1	1	0F	RAM-day of week	M	-	-	-	-				0 - 6
1	0	0	0	0	10	Interrupt Status and Mask Register	+								
1	0	0	0	1	11	Command register	-	-							

NOTES:

Addresses 10010 to 11111 (12h to 1Fh) are unused.
'+' Unused bit for interrupt Mask Register, MSB bit for interrupt Status Register.
'-' Indicates unused bits.
'†' AM/PM indicator bit in 12 hour format Logic "0" indicates AM, logic "1" indicates PM
'M' Alarm compare for particular counter will be enabled if bit is set to logic "0"

TABLE 4. INTERRUPT AND STATUS REGISTERS FORMAT

INTERRUPT MASK REGISTER ADDRESS (10000b, 10h) WRITE-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
NOT USED	DAY	HOUR	MIN	SEC	1/10 SEC	1/100 SEC	ALARM
	←	Periodic Interrupt Mask Bits				→	Alarm/Compare Mask Bit
INTERRUPT STATUS REGISTER ADDRESS (10000b, 10h) READ-ONLY							
D7	D6	D5	D4	D3	D2	D1	D0
GLOBAL INTERRUPT	DAY	HOUR	MIN	SEC	1/10 SEC	1/100 SEC	ALARM
Periodic and Alarm Flags	←	Periodic Interrupt Flags				→	Alarm Compare Flag

Detailed Description

Oscillator

The ICM7170 has an onboard CMOS Pierce oscillator with an internally regulated voltage supply for maximum accuracy, stability, and low power consumption. It operates at any of four popular crystal frequencies: 32.768kHz, 1.046576MHz, 2.097152MHz, and 4.194304MHz (Note 1). The crystal should be designed for the parallel resonant mode of oscillation. In addition to the crystal, 2 or 3 load capacitors are required, depending on the circuit topology used.

The oscillator output is divided down to 4000Hz by one of four divider ratios, determined by the two frequency selection bits in the Command Register (D0 and D1 at address 11H). This 4000Hz is then divided down to 100Hz, which is used as the clock for the counters.

Time and calendar information is provided by 8 consecutive, programmable counters: 100ths of seconds, seconds, minutes, hours, day of week, date, month, and year. The data is in binary format with 8 bits per digit. See Table 3 for address information. Any unused bits are held to a logic "0" during a read and ignored during a write operation.

NOTE:

1. 4.94304MHz is not available over military temperature range.

Alarm Compare RAM

On the chip are 51 bits of Alarm Compare RAM grouped into words of different lengths. These are used to store the time, ranging from 10ths of seconds to years, for comparison to the real-time counters. Each counter has a corresponding RAM word. In the Alarm Mode an interrupt is generated when the current time is equal to the alarm time. The RAM contents are compared to the counters on a word by word basis. If a comparison to a particular counter is unnecessary, then the appropriate 'M' bit in Compare RAM should be set to logic "1".

The 'M' bit, referring to Mask bit, causes a particular RAM word to be masked off or ignored during a compare. Table 3 shows addresses and Mask bit information.

Periodic Interrupts

The interrupt output can be programmed for 6 periodic signals: 100Hz, 10Hz, once per second, once per minute, once per hour, or once per day. The 100Hz and 10Hz interrupts have instantaneous errors of ±2.5% and ±0.15% respectively. This is because non-integer divider circuitry is used to generate these signals from the crystal frequency, which is a power of 2. The time average of these errors over a 1 second period, however, is zero. Consequently, the 100Hz or 10Hz interrupts are not suitable as an aid in tuning the oscillator; the 1 second interrupt must be used instead.

See General Notes 6.

The periodic interrupts can occur concurrently and in addition to alarm interrupts. The periodic interrupts are controlled by bits in the interrupt mask register, and are enabled by setting the appropriate bit to a "1" as shown in Table 4. Bits D1 through D6 in the mask register, in conjunction with bits D1 through D6 of the status register, control the generation of interrupts according to Figure 4.

The interrupt status register, when read, indicates the cause of the interrupt and resets itself on the rising edge of the RD signal. When any of the counters having a corresponding bit in the status register increments, that bit is set to a "1" regardless of whether the corresponding bit in the interrupt mask register is set or not.

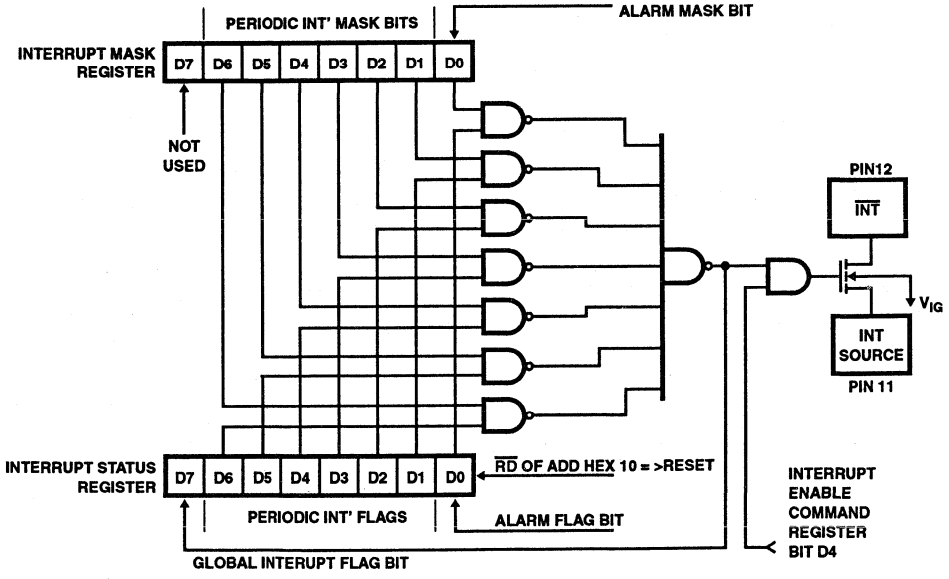


FIGURE 4. INTERRUPT OUTPUT CIRCUIT

Consequently, when the status register is read it will always indicate which counters have increments and if an alarm compare occurred, since the last time it was read. This requires some special software considerations. If a slow interrupt is enabled (i.e. hourly or daily), the program must always check the slowest interrupt that has been enabled first, because all the other lower order bits in the status register will be set to "1" as well.

Bit D7 is the global interrupt bit, and when set to a "1", indicates that the ICM7170 did indeed generate a hardware interrupt. This is useful when other interrupting devices in addition to the ICM7170 are attached to the system microprocessor, and all devices must be polled to determine which one generated the interrupt.

See General Notes 6.

Interrupt Operation

The Interrupt Output N-channel MOSFET (Figure 4) is enabled whenever both the Interrupt Enable bit (D4 of the Command Register) and a mask bit (D0 - D6 of the Interrupt Mask Register) are set. The transistor is turned ON when a flag bit is set that corresponds to one of the set mask bits. This also sets the Global Interrupt Flag Bit (D7 of the Interrupt Status Register). It is turned OFF when the Interrupt Status Register is read. An interrupt can occur in both the operational and standby modes of operation.

Since system power is usually applied between V_{DD} and V_{SS}, the user can connect the Interrupt Source (pin No. 11) to V_{SS}. This allows the Interrupt Output to turn on only while system powers applied and will not be pulled to V_{SS} during standby operation. If interrupts are required only during standby operation, then the interrupt source pin should be connected to the battery's negative side (V_{BACKUP}). In this configuration, for example, the interrupt could be used to turn on power for a cold boot.

Power Down Detector

The ICM7170 contains an on-chip power down detector that eliminates the need for external components to support the battery-backup switchover function, as shown in Figure 5. Whenever the voltage from the V_{SS} pin to the V_{BACKUP} pin is less than approximately 1.0V (the V_{TH} of the N-channel MOSFET), the data bus I/O buffers in the ICM7170 are automatically disabled and the chip cannot be read or written to. This prevents random data from the microprocessor being written to the clock registers as the power supply is going down.

Actual switchover to battery operation occurs when the voltage on the V_{BACKUP} pin is within ±50mV of V_{SS}. This switchover uncertainty is due to the offset voltage of the CMOS comparator that is used to sense the battery voltage. During battery backup, device operation is limited to timekeeping and interrupt generation only, thus achieving micropower current drain. If an external battery-backup switchover circuit is being used with the ICM7170, or if standby battery operation is not required, the V_{BACKUP} pin should be pulled up to V_{DD} through a 2K resistor.

Time Synchronization

Time synchronization is achieved through bit D3 of the Command Register, which is used to enable or disable the 100Hz clock from the counters. A logic "1" allows the counters to function and a logic "0" disables the counters. To accurately set the time, a logic "0" should be written into D3 and then the desired times entered into the appropriate counters. The clock is then started at the proper time by writing a logic "1" into D3 of the Command Register.

Latched Data

To prevent ambiguity while the processor is gathering data from the registers, the ICM7170 incorporates data latches and a transparent transition delay circuit.

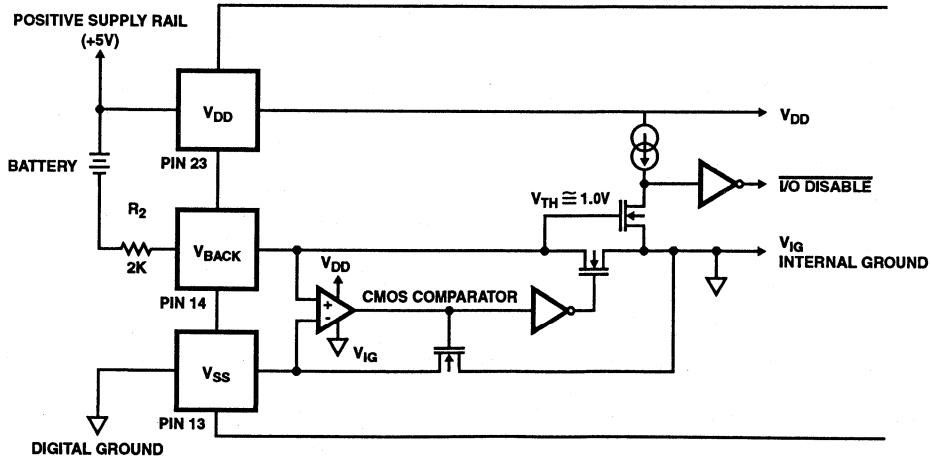


FIGURE 5. SIMPLIFIED ICM7170 BATTERY BACKUP CIRCUIT

By accessing the 100ths of seconds counter an internal store signal is generated and data from all the counters is transferred into a 36-bit latch. A transition delay circuit will delay a 100Hz transition during a READ cycle. The data stored by the latches is then available for further processing until the 100ths of seconds counter is read again. If a $\overline{RD}$ signal is wider than 0.01 sec., 100Hz counts will be ignored.

Control Lines

The $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ signals are active low inputs. Data is placed on the bus from counters or registers when $\overline{RD}$ is a logic "0". Data is transferred to counters or registers when $\overline{WR}$ is a logic "0". $\overline{RD}$ and $\overline{WR}$ must be accompanied by a logical "0" $\overline{CS}$ as shown in Figures 2 and 3. The ICM7170 will also work satisfactorily with $\overline{CS}$ grounded. In this mode, access to the ICM7170 is controlled by $\overline{RD}$ and $\overline{WR}$ only.

With the ALE (Address Latch Enable) input, the ICM7170 can be interfaced directly to microprocessors that use a multiplexed address/data bus by connecting the address lines A0 - A4 to the data lines D0 - D4. To address the chip, the address is placed on the bus and ALE is strobed. On the falling edge, the address and $\overline{CS}$ information is read into the address latch and buffer. $\overline{RD}$ and $\overline{WR}$ are used in the same way as on a non-multiplexed bus. If a non-multiplexed bus is used, ALE should be connected to V_{DD}.

Test Mode

The test mode is entered by setting D5 of the Command Register to a logic "1". This connects the 100Hz counter directly to the oscillator's output.

Oscillator Considerations

Load Design: A new oscillator load configuration, shown in Figure 6, has been found that eliminates start-up problems sometimes encountered with 32kHz tuning fork crystals.

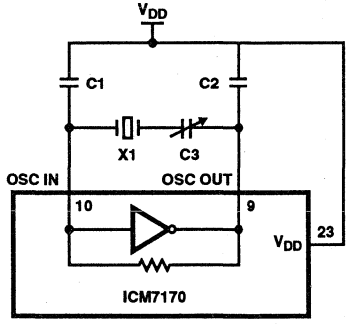


FIGURE 6. NEW OSCILLATOR CONFIGURATION

Two conditions must be met for best oscillator performance: the capacitive load must be matched to both the inverter and crystal to provide the ideal conditions for oscillation, and the resonant frequency of the oscillator must be adjustable to the desired frequency. In the original design (Figure 7), these two goals were often at odds with each other; either the oscillator was trimmed to frequency by detuning the load circuit, or stability was increased at the expense of absolute frequency accuracy.

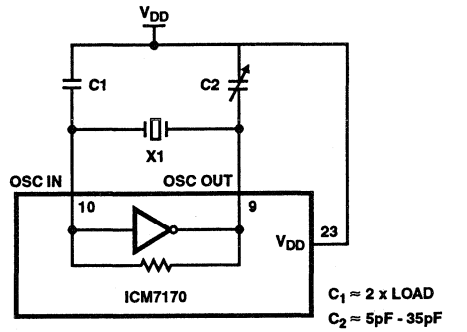


FIGURE 7. ORIGINAL OSCILLATOR CONFIGURATION

The new load configuration (Figure 6) allows these two conditions to be met independently. The two load capacitors, C1 and C2, provide a fixed load to the oscillator and crystal. C3 adjusts the frequency that the circuit resonates at by reducing the effective value of the crystal's motional capacitance, C0. This minute adjustment does not appreciably change the load of the overall system, therefore stability is no longer affected by tuning. Typical values for these capacitors are shown in Table 5. C1 and C2 must always be greater than twice the crystal's recommended load capacitance in order for C3 to be able to trim the frequency. Some experimentation may be necessary to determine the ideal values of C1 and C2 for a particular crystal.

TABLE 5. TYPICAL LOAD CAPACITOR VALUES

CRYSTAL FREQUENCY	LOAD CAPS (C1, C2)	TRIMMER CAP (C3)
32kHz	33pF	5 - 50pF
1MHz	33pF	5 - 50pF
2MHz	25pF	5 - 50pF
4MHz	22pF	5 - 100pF

This three capacitor tuning method will be more stable than the original design and is mandatory for 32kHz tuning fork crystals: without it they may leap into an overtone mode when power is initially applied.

The original two-capacitor circuit (Figure 7) will continue to work as well as it always has, and may continue to be used in applications where cost or space is a critical consideration. It is also easier to tune to frequency since one end of the trimmer capacitor is fixed at the AC ground of the circuit (V_{DD}), minimizing the disturbance cause by contact between the adjustment tool and the trimmer capacitor. Note that in both configurations the load capacitors are connected between the oscillator pins and V_{DD} - do not use V_{SS} as an AC ground.

Layout: Due to the extremely low current (and therefore high impedance) design of the ICM7170s oscillator, special attention must be given to the layout of this section. Stray capacitance should be minimized. Keep the oscillator traces on a

single layer of the PCB. Avoid putting a ground plane above or below this layer. The traces between the crystal, the capacitors, and the ICM7170 OSC pins should be as short as possible. Completely surround the oscillator components with a thick trace of V_{DD} to minimize coupling with any digital signals. The final assembly must be free from contaminants such as solder flux, moisture, or any other potential sources of leakage. A good solder mask will help keep the traces free of moisture and contamination over time.

Oscillator Tuning

Trimming the oscillator should be done indirectly. Direct monitoring of the oscillator frequency by probing OSC IN or OSC OUT is not accurate due to the capacitive loading of most probes. One way to accurately trim the ICM7170 is by turning on the 1 second periodic interrupt and trimming the oscillator until the interrupt period is exactly one second. This can be done as follows:

1. Turn on the system. Write a 00H to the Interrupt Mask Register (location 10H) to clear all interrupts.
2. Set the Command Register (location 11H) for the appropriate crystal frequency, set the Interrupt Enable and Run/Stop bits to 1, and set the Test bit to 0.
3. Write a 08H to the Interrupt Mask Register to turn on the 1 second interrupt.
4. Write an interrupt handler to read the Interrupt Status Register after every interrupt. This resets the interrupt and allows it to be set again. A software loop that reads the Interrupt Status Register several times each second will accomplish this also.
5. Connect a precision period counter capable of measuring 1 second within the accuracy desired to the interrupt output. If the interrupt is configured as active low, trigger on the falling edge. If the interrupt is active high, trigger on the rising edge. Be sure to measure the period between when the transistor turns ON, and when the transistor turns ON a second later.
6. Adjust C3 (C2 for the two-capacitor load configuration) for an interrupt period of exactly 1.000000 seconds.

Application Notes

Digital Input Termination During Backup

To ensure low current drain during battery backup operation, none of the digital inputs to the ICM7170 should be allowed to float. This keeps the input logic gates out of their transition region, and prevents crossover current from flowing which will shorten battery life. The address, data, $\overline{CS}$, and ALE pins should be pulled to either V_{DD} or V_{SS}, and the $\overline{RD}$ and $\overline{WR}$ inputs should be pulled to V_{DD}. This is necessary whether the internal battery switchover circuit is used or not.

IBM/PC Evaluation Circuit

Figure 8 shows the schematic of a board that has been designed to plug into an IBM PC/XT (Note 1.) or compatible computer. In this example $\overline{CS}$ is permanently tied low and access to the chip is controlled by the $\overline{RD}$ and $\overline{WR}$ pins. These signals are generated by U1, which gates the IBMs $\overline{IOR}$ and $\overline{IOW}$ with a device select signal from U3, which is functioning as an I/O block address decoder. DS1 selects the interrupt priority.

U5 is used to isolate the ICM7170 from the PC databus for test purposes. It is only required on heavily-loaded TTL databusses - the ICM7170 can drive most TTL and CMOS databusses directly.

Since the IBM PC/XT (Note 1) requires a positive interrupt transition, the ICM7170s interrupt output transistor has been configured as a source follower. As a source follower, the interrupt output signal will swing between 0V and 2.5V. When trimming the oscillator, the frequency counter must be triggered on the rising edge of the interrupt signal.

TABLE 6.

BATTERIES	CRYSTALS		
Panasonic	Saronix	32kHz	NTF3238
Rayovac	Statek	32kHz	CX - 1V
	Seiko	2MHz	GT - 38

NOTE:

1. IBM, IBM PC, and IBM XT are trademarks of IBM Corp.

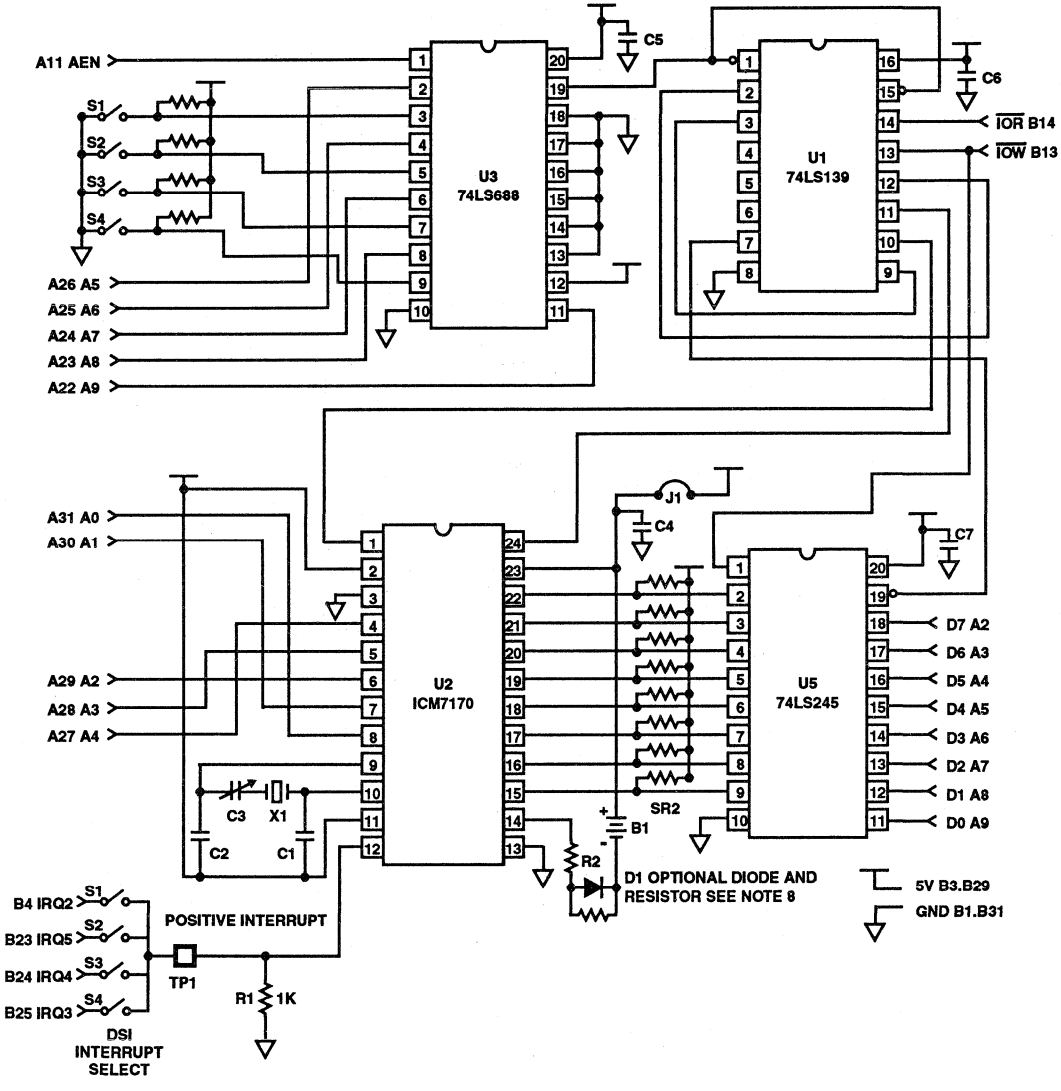


FIGURE 8. IBM PC INTERFACE FOR ICM7170

General Notes

1. TIME ACCESS - To update the present time registers (Hex 00 - 07) the $^1/_{100}$ register must be read first. The 7 real time counter registers (Hours, Minutes, Seconds, Month, Date, Day, and Year) data are latched only if the 1/100 second counter register is read. The 1/100 seconds data itself is not latched. The real time data will be held in the latches until the $^1/_{100}$ seconds is read again. See the data sheet section on LATCHED DATA. None of the RAM data is latched since it is static by nature.
2. REGULATED OSCILLATOR - The oscillator's power supply is voltage regulated with respect to V_{DD}. In the 32kHz mode the regulator's amplitude is ΣVtn + Vtp ($\cong$1.8V). In the 1, 2, and 4MHz mode the regulator's amplitude is ΣVtn + Vtn + Vtp ($\cong$2.6V). As a result, signal conditioning is necessary to drive the oscillator with an external signal. In addition, it is also necessary to buffer the oscillator's signal to drive other external clocks because of its reduced amplitude and offset voltage.
3. INTERNAL BATTERY BACKUP - When the ICM7170 is using its own internal battery backup circuitry, no other circuitry interfaced to the ICM7170 should be active during standby operation. When V_{DD} (+5V) is turned off (Standby operation), V_{DD} should equal V_{SS} = 0V. All ICM7170 I/O should also equal V_{SS}. At this time, the V_{BACKUP} pin should be 2.8V to 3.5V below V_{SS} when using a Lithium battery.
4. EXTERNAL BATTERY BACKUP - The ICM7170 may be placed on the same power supply as battery-backed up RAM by keeping the ICM7170 in its operational state and having an external circuit switch between system and backup power for the ICM7170 and the RAM. In this case V_{BACKUP} should be pulled up to V_{DD} through a 2K resistor. Although the ICM7170 is always "on" in this configuration, its current consumption will typically be less than a microamp greater than that of standby operation at the same supply voltage (See Note 9).

   Proper consideration must be given to disabling the ICM7170s and the RAMs I/O before system power is removed. This is important because many microprocessors can generate spurious write signals when their supply falls below their specified operating voltage limits. NANDing $\overline{CS}$ (or WR) with a POWERGOOD signal will create a $\overline{CS}$ (or $\overline{WR}$) that is only valid when system power is within specifications. The POWERGOOD signal should be generated by an accurate supply monitor such as the ICL7665 under/over voltage detector.

   An alternate method of disabling the ICM7170's I/O is to pull V_{BACKUP} down to under a volt above V_{SS} (V_{SS} < V_{BACKUP} <1.0V). This will cause the ICM7170 to internally disable all I/O. Do not allow V_{BACKUP} to equal V_{SS}, since this could cause oscillation of the battery backup comparator (See Figure 5). V_{BACKUP} = V_{SS} + 0.5V will disable the I/O and provide enough overdrive for the comparator.
5. ICM7170A PART - The ICM7170A part is binned at final test for a 32.768kHz maximum current of 5µA. All other specifications remain the same.
6. INTERRUPTS - The Interrupt Status Register (address 10H) always indicates which of the real time counters have been incremented since the last time the register was read. NOTE: This is independent of whether or not any mask bits are set.
   The status register is always reset immediately after it is read. If an interrupt from the ICM7170 has occurred since the last time the status register was read, bit D7 of the register will be set. If the source was an alarm interrupt, bit D0 will also be set. If the interrupt transistor has been turned on, reading the Interrupt Status Register will reset it.

   To enable the periodic interrupt, both the Command Register's Interrupt Enable bit (D4) and at least one bit in the Interrupt Mask Register (D1 - D6) must be set to a 1. The periodic interrupt is triggered when the counter corresponding to a mask bit that has been set is incremented. For example, if you enable the 1 second interrupt when the current value in the 100ths counter is 57, the first interrupt will occur 0.43 seconds later. All subsequent interrupts will be exactly one second apart. The interrupt service routine should then read the Interrupt Status Register to reset the interrupt transistor and, if necessary, determine the cause of the interrupt (periodic, alarm, or non-ICM7170 generated) from the contents of the status register.

   To enable the alarm interrupts, both the Command Register's Interrupt Enable bit (D4) and the Interrupt Mask Register's Alarm bit (D0) must be set to a 1. Each time there is an exact match between the values in the alarm register and the values in the real time counters, bits D0 and D7 of the Interrupt Status Register will be set to a 1 and the N-channel interrupt transistor will be turned on. As with a periodic interrupt, the service routine should then read the Interrupt Status Register to reset the interrupt transistor and, since periodic and alarm interrupts may be simultaneously enabled, determine the cause of the interrupt if necessary.

   Mask bits: The ICM7170 alarm interrupt compares the data in the alarm registers with the data in the real time registers, ignoring any registers with the mask bit set. For example, if the alarm register is set to 11-23-95 (Month-Day-Year), 10:59:00:00 (Hour-Minutes-Seconds-Hundredths), and DAY = XX (XX = masked off), the alarm will generate a single interrupt at 10:59 on November 23,1995. If the alarm register is set to 11-XX-95, 10:XX:00:00, and DAY = 2 (2 = Tuesday); the alarm will generate one interrupt every minute from 10:00-10:59 on every Tuesday in November, 1995.

   NOTE: Masking off the 100ths of a second counter has the same effect as setting it to 00.
7. RESISTOR IN SERIES WITH BATTERY - A 2K resistor (R2) must be placed in series with the battery backup pin of the ICM7170. The UL laboratories have requested the resistor to limit the charging and discharging current to the battery. The resistor also serves the purpose of degenerating parasitic SCR action. This SCR action may occur if an input is applied to the ICM7170, outside of its supply voltage range, while it is in the standby mode.
8. V_{BACKUP} DIODE - Lithium batteries may explode if charged or if discharged at too high a rate. These conditions could occur if the battery was installed backwards or in the case of a gross component failure. A 1N914-type diode placed in series with the battery as shown in Figure 8 will prevent this from occurring. A resistor of 2MΩ or so should parallel the diode to keep the V_{BACKUP} terminal from drifting toward the V_{SS} terminal and shutting off ICM7170 I/O during normal operation.
9. SUPPLY CURRENT - ICM7170 supply current is predominantly a function of oscillator frequency and databus activity. The lower the oscillator frequency, the lower the supply current. When there is little or no activity on the data, address or control lines, the current consumption of the ICM7170 in its operational mode approaches that of the backup mode.

DATA ACQUISITION 15

HARRIS QUALITY AND RELIABILITY

Harris Quality

Introduction

Success in the integrated circuit industry means more than simply meeting or exceeding the demands of today's market. It also includes anticipating and accepting the challenges of the future. It results from a process of continuing improvement and evolution, with perfection as the constant goal.

Harris Semiconductor's commitment to supply only top value integrated circuits has made quality improvement a mandate for every person in our work force – from circuit designer to manufacturing operator, from hourly employee to corporate executive. Price is no longer the only determinant in marketplace competition. Quality, reliability, and performance enjoy significantly increased importance as measures of value in integrated circuits.

Quality in integrated circuits cannot be added on or considered after the fact. It begins with the development of capable process technology and product design. It continues in manufacturing, through effective controls at each process or step. It culminates in the delivery of products which meet or exceed the expectations of the customer.

The Role of the Quality Organization

The emphasis on building quality into the design and manufacturing processes of a product has resulted in a significant refocus of the role of the Quality organization. In addition to facilitating the development of SPC and DOX, Quality professionals support other continuous improvement tools such as control charts, measurement of equipment capability, standardization of inspection equipment and processes, procedures for chemical controls, analysis of inspection data and feedback to the manufacturing areas, coordination of efforts for process and product improvement, optimization of environmental or raw materials quality, and the development of quality improvement programs with vendors.

At critical manufacturing operations, process and product quality is analyzed through random statistical sampling and product monitors. The Quality organization's role is changing from policing quality to leadership and coordination of quality programs or procedures through auditing, sampling, consulting, and managing Quality Improvement projects.

To support specific market requirements, or to ensure conformance to military or customer specifications, the Quality organization still performs many of the conventional quality functions (e.g., group testing for military products or wafer lot acceptance). But, true to the philosophy that quality is everyone's job, much of the traditional on-line measurement and control of quality characteristics is where it belongs – with the people who make the product. The Quality organization is there to provide leadership and assistance in the deployment of quality techniques, and to monitor progress.

The Improvement Process

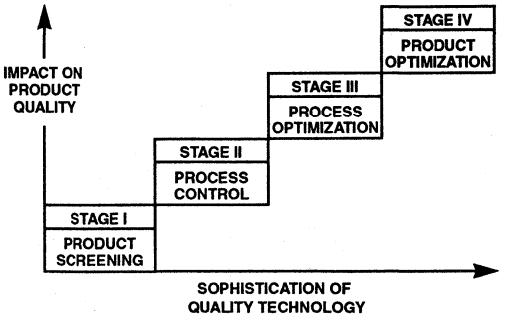


FIGURE 1. STAGES OF STATISTICAL QUALITY TECHNOLOGY

Harris Semiconductor's quality methodology is evolving through the stages shown in Figure 1. In 1981 we embarked on a program to move beyond Stage I, and we are currently in the transition from Stage III to Stage IV, as more and more of our people become involved in quality activities. The traditional "quality" tasks of screening, inspection, and testing are being replaced by more effective and efficient methods, putting new tools into the hands of all employees. Table 1 illustrates how our quality systems are changing to meet today's needs.

Designing for Manufacturability

Assuring quality and reliability in integrated circuits begins with good product and process design. This has always been a strength in Harris Semiconductor's quality approach. We have a very long lineage of high reliability, high performance products that have resulted from our commitment to design excellence. All Harris products are designed to meet the stringent quality and reliability requirements of the most demanding end equipment applications, from military and space to industrial and telecommunications. The application of new tools and methods has allowed us to continuously upgrade the design process.

Each new design is evaluated throughout the development cycle to validate the capability of the new product to meet the end market performance, quality, and reliability objectives.

The validation process has four major components:

1. Design simulation/optimization
2. Layout verification
3. Product demonstration
4. Reliability assessment.

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Wafer Fab	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Junction Depth	X	
	- Sheet Resistivities	X	
	- Defect Density	X	X
	- Critical Dimensions	X	X
	- Visual Inspection	X	X
	- Lot Acceptance	X	
	• Process		
	- Film Thickness	X	X
	- Implant Dosages	X	
	- Capacitance Voltage Changes	X	X
	- Conformance to Specification	X	X
	• Equipment		
	- Repeatability	X	X
	- Profiles	X	X
	- Calibration		X
	- Preventive Maintenance	X	X
Assembly	• JAN Self-Audit		X
	• Environmental		
	- Room/Hood Particulates	X	X
	- Temperature/Humidity	X	X
	- Water Quality		X
	• Product		
	- Documentation Check		X
	- Dice Inspection	X	X
	- Wire Bond Pull Strength/Controls	X	X
	- Ball Bond Shear/Controls		X
	- Die Shear Controls		X
	- Post-Bond/Pre-Seal Visual	X	X
	- Fine/Gross Leak	X	X
	- PIND Test	X	
	- Lead Finish Visuals, Thickness	X	X
	- Solderability		X
	• Process		
	- Operator Quality Performance	X	X
	- Saw Controls	X	
	- Die Attach Temperatures	X	X
	- Seal Parameters	X	
	- Seal Temperature Profile	X	X
	- Sta-Bake Profile	X	
	- Temp Cycle Chamber Temperature	X	X
	- ESD Protection	X	X
	- Plating Bath Controls	X	X
	- Mold Parameters	X	X

TABLE 1. TYPICAL ON-LINE MANUFACTURING/QUALITY FUNCTIONS (Continued)

AREA	FUNCTION	MANUFACTURING CONTROLS	QA/QC MONITOR AUDIT
Test	• JAN Self-Audit		X
	• Temperature/Humidity	X	
	• ESD Controls	X	
	• Temperature Test Calibration	X	
	• Test System Calibration	X	
	• Test Procedures		X
	• Control Unit Compliance	X	
	• Lot Acceptance Conformance	X	
	• Group A Lot Acceptance		X
Probe	• JAN Self-Audit		X
	• Wafer Repeat Correlation	X	
	• Visual Requirements	X	X
	• Documentation	X	X
	• Process Performance	X	X
Burn-In	• JAN Self-Audit		X
	• Functionality Board Check	X	
	• Oven Temperature Controls	X	
	• Procedural Conformance		X
Brand	• JAN Self-Audit		X
	• ESD Controls	X	X
	• Brand Permanency	X	X
	• Temperature/Humidity	X	
	• Procedural Conformance		X
QCI Inspection	• JAN Self-Audit		X
	• Group B Conformance		X
	• Group C and D Conformance		X

Harris designers have an extensive set of very powerful Computer-Aided Design (CAD) tools to create and optimize product designs (see Table 2).

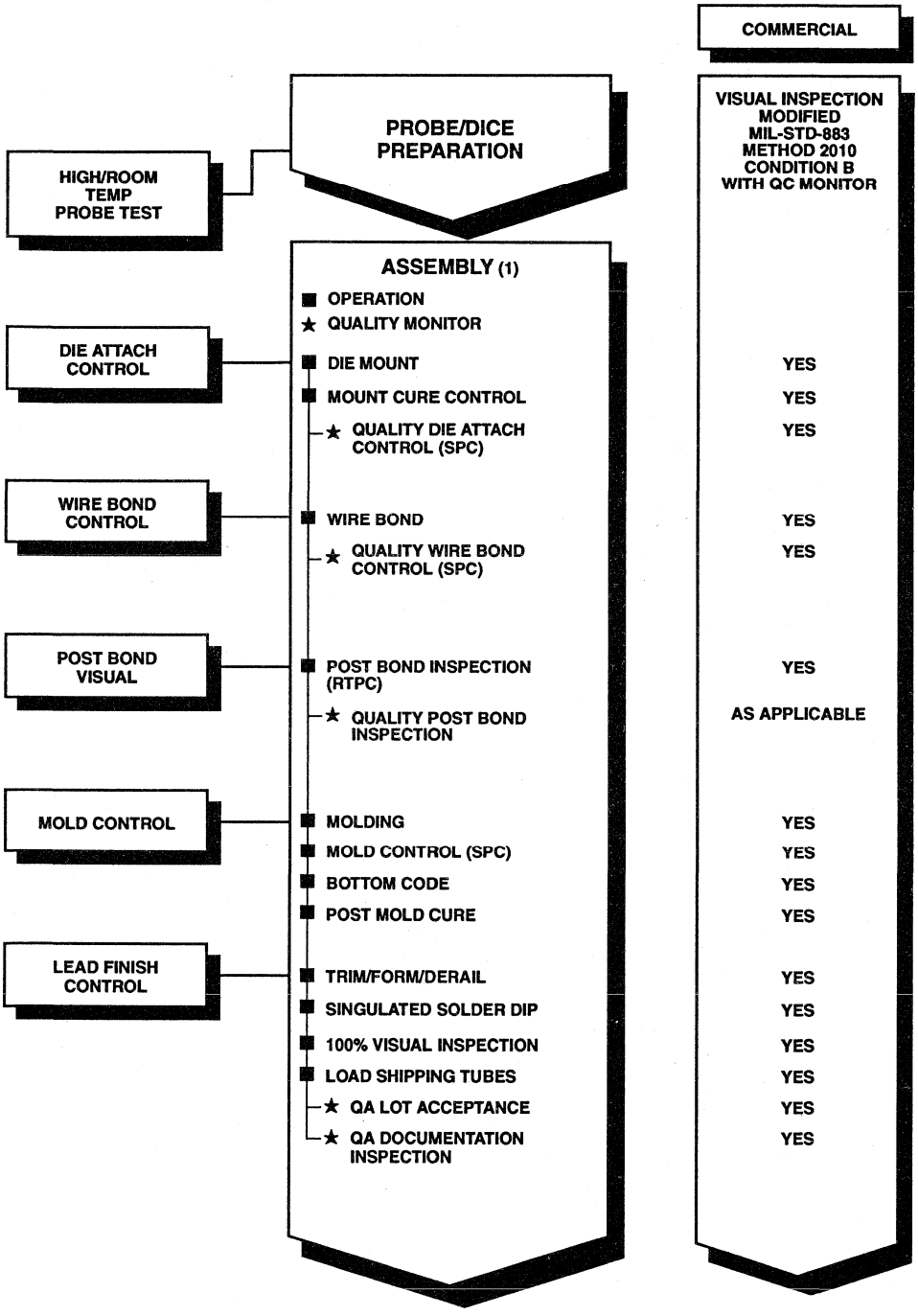
TABLE 2. HARRIS I.C. DESIGN TOOLS

DESIGN STEP	PRODUCTS	
	ANALOG	DIGITAL
Functional Simulation	Cds Spice	Cds Spice Verilog
Parametric Simulation	Cds Spice Monte Carlo	Cds Spice
Schematic Capture	Cadence	Cadence
Functional Checking	Cadence	Cadence
Rules Checking	Cadence	Cadence
Parasitic Extraction	Cadence	Cadence

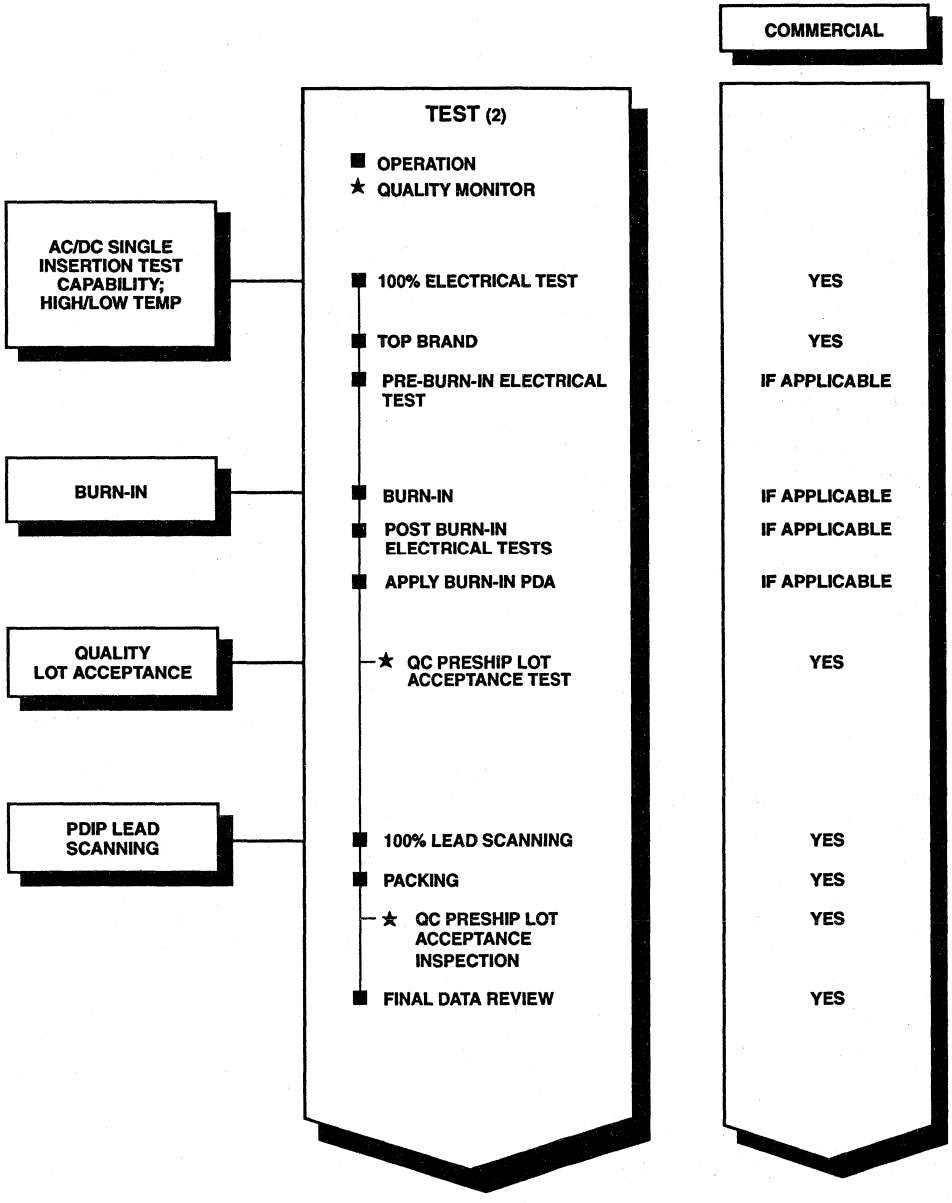
Special Testing

Harris Semiconductor offers several standard screen flows to support a customer's need for additional testing and reliability assurance. These flows include environmental stress testing, burn-in, and electrical testing at temperatures other than +25°C. The flows shown on pages 9-6 and 9-7 indicate the Harris standard processing flows for a Commercial Linear part in PDIP Package. In addition, Harris can supply products tested to customer specifications both for electrical requirements and for nonstandard environmental stress screening. Consult your field sales representative for details.

Harris Semiconductor Standard Processing Flows



(1) Example for a PDIP Package Part



(2) Example for a Linear Part in PDIP Package

TABLE 3. SUMMARIZING CONTROL APPLICATIONS

FAB			
• Diffusion - Junction Depth - Sheet Resistivities - Oxide Thickness - Implant Dose Calibration - Uniformity	• Thin Film - Film Thickness - Uniformity - Refractive Index - Film Composition	• Photo Resist - Critical Dimension - Resist Thickness - Etch Rates	• Measurement Equipment - Critical Dimension - Film Thickness - 4 Point Probe - Ellipsometer
ASSEMBLY			
• Pre-Seal - Die Prep Visuals - Yields - Die Attach Heater Block - Die Shear - Wire Pull - Ball Bond Shear - Saw Blade Wear - Pre-Cap Visuals	• Post-Seal - Internal Package Moisture - Tin Plate Thickness - PIND Defect Rate - Solder Thickness - Leak Tests - Module Rm. Solder Pot Temp. - Seal - Temperature Cycle	• Measurement - XRF - Radiation Counter - Thermocouples - GM-Force Measurement	
TEST			
	- Handlers/Test System - Defect Pareto Charts - Lot % Defective - ESD Failures per Month	- Monitor Failures - Lead Strengthening Quality - After Burn-In PDA	
OTHER			
• IQC - Vendor Performance - Material Criteria - Quality Levels	• Environment - Water Quality - Clean Room Control - Temperature - Humidity	• IQC Measurement/Analysis - XRF - ADE - 4 Point Probe - Chemical Analysis Equipment	

Controlling and Improving the Manufacturing Process - SPC/DOX

Statistical process control (SPC) is the basis for quality control and improvement at Harris Semiconductor. Harris manufacturing people use control charts to determine the normal variabilities in processes, materials, and products. Critical process variables and performance characteristics are measured and control limits are plotted on the control charts. Appropriate action is taken if the charts show that an operation is outside the process control limits or indicates a nonrandom pattern inside the limits. These same control charts are powerful tools for use in reducing variations in processing, materials, and products. Table 3 lists some typical manufacturing applications of control charts at Harris Semiconductor.

SPC is important, but still considered only part of the solution. Processes which operate in statistical control are not always capable of meeting engineering requirements. The conventional way of dealing with this in the semiconductor industry has been to implement 100% screening or inspection steps to remove defects, but these techniques are insufficient to meet today's demands for the highest reliability and perfect quality performance.

Harris still uses screening and inspection to "grade" products and to satisfy specific customer requirements for burn-in, multiple temperature test insertions, environmental screening, and visual inspection as value-added testing options. However, inspection and screening are limited in their ability to reduce product defects to the levels expected by today's buyers. In addition, screening and inspection have an associated expense, which raises product cost. (See Table 4).

TABLE 4. APPROACH AND IMPACT OF STATISTICAL QUALITY TECHNOLOGY

	STAGE	APPROACH	IMPACT
I	Product Screening	• Stress and Test • Defective Prediction	• Limited Quality • Costly • After-The-Fact
II	Process Control	• Statistical Process Control • Just-In-Time Manufacturing	• Identifies Variability • Reduces Costs • Real Time
III	Process Optimization	• Design of Experiments • Process Simulation	• Minimizes Variability • Before-The-Fact
IV	Product Optimization	• Design for Producibility • Product Simulation	• Insensitive to Variability • Designed-In Quality • Optimal Results

Harris engineers are, instead, using Design of Experiments (DOX), a scientifically disciplined mechanism for evaluating and implementing improvements in product processes, materials, equipment, and facilities. These improvements are aimed at reducing the number of defects by studying the key variables controlling the process, and optimizing the procedures or design to yield the best result. This approach is a more time-consuming method of achieving quality perfection, but a better product results from the efforts, and the basic causes of product nonconformance can be eliminated.

SPC, DOX, and design for manufacturability, coupled with our 100% test flows, combine in a product assurance program that delivers the quality and reliability performance demanded for today and for the future.

Average Outgoing Quality (AOQ)

Average Outgoing Quality is a yardstick for our success in quality manufacturing. The average outgoing electrical defective is determined by randomly sampling units from each lot and is measured in parts per million (PPM). The current procedures and sampling plans outlined in JEDEC STD 16, MIL-STD-883 and MIL-I-38535 are used by our quality inspectors.

The focus on this quality parameter has resulted in a continuous improvement to less than 100 PPM, and the goal is to continue improvement toward 0 PPM.

Training

The basis of a successful transition from conventional quality programs to more effective, total involvement is training. Extensive training of personnel involved in product manufacturing began in 1984 at Harris, with a comprehensive development program in statistical methods. Using the resources of Harris statisticians, private consultants, and internally developed programs, training of engineers, supervisors, and operators/technicians has been an ongoing activity in Harris Semiconductor.

Over the past years, Harris has also deployed a comprehensive training program for hourly operators and supervisors in job requirements and functional skills. All hourly manufacturing employees participate (see Table 5).

Incoming Materials

Improving the quality and reducing the variability of critical incoming materials is essential to product quality enhancement, yield improvement, and cost control. With the use of statistical techniques, the influence of silicon, chemicals, gases and other materials on manufacturing is highly measurable. Current measurements indicate that results are best achieved when materials feeding a statistically controlled manufacturing line have also been produced by statistically controlled vendor processes.

To assure optimum quality of all incoming materials, Harris has initiated an aggressive program, linking key suppliers with our manufacturing lines. This user-supplier network is the Harris Vendor Certification process by which strategic vendors, who have performance histories of the highest quality, participate with Harris in a lined network; the vendor's factory acts as if it were a beginning of the Harris production line.

SPC seminars, development of open working relationships, understanding of Harris' manufacturing needs and vendor capabilities, and continual improvement programs are all part of the certification process. The sole use of engineering limits no longer is the only quantitative requirement of incoming materials.

TABLE 5. SUMMARY OF TRAINING PROGRAMS

COURSE	AUDIENCE	TOPICS COVERED
SPC, Basic	Manufacturing Operators, Non-Manufacturing Personnel	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts
SPC, Intermediate	Manufacturing Supervisors, Technicians	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Introduction to Capability
SPC, Advanced	Manufacturing Engineers, Manufacturing Managers	Harris Philosophy of SPC, Statistical Definitions, Statistical Calculations, Problem Analysis Tools, Graphing Techniques, Control Charts, Distributions, Measurement Process Evaluation, Advanced Control Charts, Variance Component Analysis, Capability Analysis
Design of Experiments (DOX)	Engineers, Managers	Factorial and Fractional Designs, Blocking Designs, Nested Models, Analysis of Variance, Normal Probability Plots, Statistical Intervals, Variance Component Analysis, Multiple Comparison Procedures, Hypothesis Testing, Model Assumptions/Diagnostics
Regression	Engineers, Managers	Simple Linear Regression, Multiple Regression, Coefficient Interval Estimation, Diagnostic Tools, Variable Selection Techniques
Response Surface Methods (RSM)	Engineers, Managers	Steepest Ascent Methods, Second Order Models, Central Composite Designs, Contour Plots, Box-Behnken Designs

Specified requirements include centered means, statistical control limits, and the requirement that vendors deliver their products from their own statistically evaluated, in-control manufacturing processes.

In addition to the certification process, Harris has worked to promote improved quality in the performance of all our qualified vendors who must meet rigorous incoming inspection criteria (see Table 6).

TABLE 6. INCOMING QUALITY CONTROL MATERIAL QUALITY CONFORMANCE

MATERIAL	INCOMING INSPECTIONS	VENDOR DATA REQUIREMENTS
Silicon	• Resistivity • Crystal Orientation • Dimensions • Edge Conditions • Taper • Thickness • Total Thickness Variation • Backside Criteria • Oxygen • Carbon	• Equipment Capability Control Charts - Oxygen - Resistivity • Control Charts Related to - Enhanced Gettering - Total Thickness Variation - Total Indicated Reading - Particulates • Certificated of Analysis for all Critical Parameters • Control Charts from On-Line Processing • Certificate of Conformance
Chemicals/Photoresists/ Gases	• Chemicals - Assay - Major Contaminants • Molding Compounds - Spiral Flow - Thermal Characteristics • Gases - Impurities • Photoresists - Viscosity - Film Thickness - Solids - Pinholes	• Certificate of Analysis on all Critical Parameters • Certificate of Conformance • Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Water - Selected Parameters • Control Charts - Assay - Contaminants • Control Charts on - Photospeed - Thickness - UV Absorbance - Filterability - Water - Contaminants
Thin Film Materials	• Assay • Selected Contaminants	• Control Charts from On-Line Processing • Control Charts - Assay - Contaminants - Dimensional Characteristics • Certificate of Analysis for all Critical Parameters • Certificate of Conformance
Assembly Materials	• Visual Inspection • Physical Dimension Checks • Glass Composition • Bondability • Intermetallic Layer Adhesion • Ionic Contaminants • Thermal Characteristics • Lead Coplanarity • Plating Thickness • Hermeticity	• Certificate of Analysis • Certificate of Conformance • Process Control Charts on Outgoing Product Checks and In-Line Process Controls

Calibration Laboratory

Another important resource in the product assurance system is a calibration lab in each Harris Semiconductor operation site. These labs are responsible for calibrating the electronic, electrical, electro/mechanical, and optical equipment used in both production and engineering areas. The accuracy of instruments used at Harris is traceable to a national standards. Each lab maintains a system which conforms to the current revision of MIL-STD-45662, "Calibration System Requirements."

Each instrument requiring calibration is assigned a calibration interval based upon stability, purpose, and degree of use. The equipment is labeled with an identification tag on which is specified both the date of the last calibration and of the next required calibration. The Calibration Lab reports on a regular basis to each user department. Equipment out of calibration is taken out of service until calibration is performed. The Quality organization performs periodic audits to assure proper control in the using areas. Statistical procedures are used where applicable in the calibration process.

Manufacturing Science - CAM, JIT, TPM

In addition to SPC and DOX as key tools to control the product and processes, Harris is deploying other management mechanisms in the factory. On first examination, these tools appear to be directed more at schedules and capacity. However, they have a significant impact on quality results.

Computer Aided Manufacturing (CAM)

CAM is a computer based inventory and productivity management tool which allows personnel to quickly identify production line problems and take corrective action. In addition, CAM improves scheduling and allows Harris to more quickly respond to changing customer requirements and aids in managing work in process (WIP) and inventories.

The use of CAM has resulted in significant improvements in many areas. Better wafer lot tracking has facilitated a number of process improvements by correlating yields to process variables. In several places CAM has greatly improved capacity utilization through better planning and scheduling. Queues have been reduced and cycle times have been shortened - in some cases by as much as a factor of 2.

The most dramatic benefit has been the reduction of WIP inventory levels, in one area by 500%. This results in fewer lots in the area and a resulting quality improvement. In wafer fab, defect rates are lower because wafers spend less time in production areas awaiting processing. Lower inventory also improves morale and brings a more orderly flow to the area. CAM facilitates all of these advantages.

Just In Time (JIT)

The major focus of JIT is cycle time reduction and linear production. Significant improvements in these areas result in large benefits to the customer. JIT is a part of the Total Quality Management philosophy at Harris and includes Employee Involvement, Total Quality Control, and the total elimination of waste.

Some key JIT methods used for improvement are sequence of events analysis for the elimination of non-value added activities, demand/pull to improve production flow, TQC check points and Employee Involvement Teams using root cause analysis for problem solving.

JIT implementations at Harris Semiconductor have resulted in significant improvements in cycle time and linearity. The benefits from these improvements are better on time delivery, improved yield, and a more cost effective operation.

JIT, SPC, and TPM are complementary methodologies and used in conjunction with each other create a very powerful force for manufacturing improvement.

Total Productive Maintenance (TPM)

TPM or Total Productive Maintenance is a specific methodology which utilizes a definite set of principles and tools focusing on the improvement of equipment utilization. It focuses on the total elimination of the six major losses which are equipment failures, setup and adjustment, idling and minor stoppages, reduced speed, process defects, and reduced yield. A key measure of progress within TPM is the overall equipment effectiveness which indicates what percentage of the time is a particular equipment producing good parts. The basic TPM principles focus on maximum equipment utilization, autonomous maintenance, cross functional team involvement, and zero defects. There are some key tools within the TPM technical set which have proven to be very powerful to solve long standing problems. They are initial clean, P-M analysis, condition based maintenance, and quality maintenance.

Utilization of TPM has shown significant increases in utilization on many tools across the Sector and is rapidly becoming widespread and recognized as a very valuable tool to improve manufacturing competitiveness.

The major benefits of TPM are capital avoidance, reduced costs, increased capability, and increased quality. It is also very compatible with SPC techniques since SPC is a good stepping stone to TPM implementation and it is in turn a good stepping stone to JIT because a high overall equipment effectiveness guarantees the equipment to be available and operational at the right time as demanded by JIT.

Harris Reliability

The reliability operations for Harris Semiconductor are consolidated into three locations; in Palm Bay, Florida, and Research Triangle Park, North Carolina, for integrated circuits products, and Mountaintop, Pennsylvania for Power Discrete Products. This consolidation brought the reliability organizations together to form a team that possesses a broad cross section of expertise in:

- Custom Military
- Automotive ASICs
- Harsh Environment Plastic Packaging
- Advanced Methods for Design for Reliability (DFR)
- Strength in Power Semiconductor
- Chemical/Surface Analysis Capabilities

The reliability focus is customer satisfaction (external and internal) and is accomplished through the development of standards, performance metrics and service systems. These major systems are summarized below:

- A process and product development system which emphasizes getting new products to market over product design. Uses empowered cross functional development teams.
- Standard test vehicles (96 in all) for process characterization of wearout failure mechanisms using conventional stresses (for modeling FITs/MTTF) and wafer level reliability characterization during development.
- Common qualification standards and philosophy for all sites and developments.
- Matrix monitor standard - a reliability monitoring system for products in production to insure ongoing reliability and verification of continuous improvement.
- Field return failure analysis system deployed world wide to track and expedite root cause analysis and irreversible corrective actions in a timely manner for our customers. The system is called by the team name PFAST, Product Failure Analysis Solution Team. Failure analysis sites are located in Brussels, Mountaintop, Palm Bay, Singapore, Kuala Lumpur, and Toyko. In order to optimize our response time to the customer all locations are networked for optimum communication, trend analysis, and performance tracking.

Integrated circuits reliability home base is in Palm Bay, Florida. This new facility has consolidated the reliability organization of the standard products divisions reliability group from Palm Bay, Florida; Somerville, New Jersey; Santa Clara, California, and the Military and Aerospace Division in Palm Bay, Florida. This facility contains

- A 9,000 square foot reliability analysis laboratory,
- An 8,000 square foot reliability stress testing facility,
- A 5,000 square foot analytical (chemistry/surface analysis) laboratory,
- A 3,000 square foot of engineering office space.

The facilities are well equipped and manned with highly trained and disciplined analysts. The reliability facilities are JAN certified and certified by a host of customers including major automotive and telecommunications companies.

Process/Product/Package Qualifications

Qualification activities at Harris begin with the in-depth qualification of new wafer processes. These process qualifications focus on the use of test vehicles to characterize wearout mechanisms for each process. These data are used to establish design ground rules for each process to eliminate wearout failure during the useful life of the product. Products designed within the established ground rules are qualified individually prior to introduction. New package configurations are qualified individually prior to being available for new products. Harris qualification procedures are specified via controlled documentation.

Product/Package Reliability Monitors

Many of the accelerated stress-tests used during initial reliability qualification are also employed during the routine monitoring of standard production product. Harris' continuing reliability monitoring program consists of three groups of stress tests, labeled Matrix I, II and III. As an example, Table 7 outlines the Matrix tests used to monitor plastic packaged CMOS Logic ICs in Harris' Malaysia assembly plant, where each wafer fab technology is sampled weekly for both Matrix I and II. Matrix I consists of highly accelerated, short duration (48 hours or less) tests, which provide real-time feedback on product reliability. Matrix II consists of the more traditional, longer term stress-tests, which are similar to those used for product qualification. Finally, Matrix III, performed monthly on each package style, monitors the mechanical reliability aspects of the package. Any failures occurring on the Matrix monitors are fully analyzed and the failure mechanisms identified, with corrective actions obtained from Manufacturing and Engineering. This information along with all of the test results are routinely transmitted to a central data base in Reliability Engineering, where failure rate trends are analyzed and tracked on an ongoing basis. These data are used to drive product improvements, so as to ensure that failure rates are continuously being reduced over time.

TABLE 7. PLASTIC PACKAGED CMOS LOGIC ICS MALAYSIA RELIABILITY MONITORING TESTS.

MATRIX I

TEST	CONDITIONS	DURATION	SAMPLE
Bias Life	+175°C	48 Hours	40
HAST	+145°C, 85% RH	20 Hours	40

TABLE 7. PLASTIC PACKAGED CMOS LOGIC ICS MALAYSIA RELIABILITY MONITORING TESTS (Continued)

MATRIX II

TEST	CONDITIONS	DURATION	SAMPLE
Bias Life	+125°C	1000 Hours	50
Dynamic Life	+125°C	1000 Hours	50
Biased Humidity	+85°C, 85% RH	1000 Hours	50
Autoclave	15 PSIG, +121°C, 100% RH	192 Hours	50
Storage Life	+150°C	1000 Hours	50
Temp. Cycle	-65°C to +150°C	1000 Cycles	50
Thermal Shock	-65°C to +150°C	1000 Cycles	50

MATRIX III

TEST	CONDITIONS	SAMPLE
Solderability	Mil-Std 883/2003	15
Lead Fatigue	Mil-Std 883/2004	15
Brand Adhesion	Mil-Std 883/2015	20
Flammability	(UL-94 Vertical Burn)	5

Field Return Product Analysis System

The purpose of this system is to enable Harris' Field Sales and Quality operations to properly route, track and respond to our customers' needs as they relate to product analysis.

The Product Failure Analysis Solution Team (PFAST) consists of the group of people who must act together to provide timely, accurate and meaningful results to customers on units returned for analysis. This team includes the salesman or applications engineer who gets the parts from the customer, the PFAST controller who coordinates the response, the Product or Test Engineering people who obtain characterization and/or test data, the analysts who failure analyze the units, and the people who provide the ultimate corrective action. It is the coordinated effort of this team, through the system described in this document that will drive the Customer responsiveness and continuous improvement that will keep Harris on the forefront of the semiconductor business.

The system and procedures define the processing of product being returned by the customer for analysis performed by Product Engineering, Reliability Failure Analysis and/or Quality Engineering. This system is designed for processing "sample" returns, not entire lot returns or lot replacements.

The philosophy is that each site analyzes its own product. This applies the local expertise to the solutions and helps toward the goal of quick turn time.

Goals: quick, accurate response, uniform deliverable (consistent quality) from each site, traceability.

The PFAST system is summarized in the following steps:

1) Customer calls the sales rep about the unit(s) to return.
2) Fill out PFAST Action Request - see the PFAST form in this section. This form is all that is required to process a Field Return of samples for failure analysis. This form contains essential information necessary to perform root cause analysis. (See Figure 2).
3) The units must be packaged in a manner that prevents physical damage and prevents ESD. Send the units and PFAST form to the appropriate PFAST controller. This location can be determined at the field sales office or rep using "look-up"'tables in the PFAST document.
4) The PFAST controller will log the units and route them to ATE testing for data log.
5) Test results will be reviewed and compared to customer complaint and a decision will be made to route the failure to the appropriate analytical group.
6) The customer will be contacted with the ATE test results and interim findings on the analysis. This may relieve a line down situation or provide a rapid disposition of material. The customer contact is valuable in analytical process to insure root cause is found.
7) A report will be written and sent directly to the customer with copies to sales, rep, responsible individuals with corrective actions and to the PFAST controller so that the records will capture the closure of the cycle.
8) Each report will contain a feedback form (stamped and preaddressed) so that the PFAST team can assess their performance based on the customers assessment of quality and cycle time.
9) The PFAST team objectives are to have a report in the customers hands in 28 days, or 14 days based on agreements. Interim results are given real-time.

HARRIS SEMICONDUCTOR

Request # _____
Customer Analysis # _____

PFAST ACTION REQUEST

Date: _____

ORIGINATOR _____	CUSTOMER _____
LOCATION/PHONE NO. _____	LOCATION _____
DEVICE TYPE/PART NO. _____	PURCHASE ORDER NO. _____
NO. SAMPLES RETURNED _____	QUANTITY RECEIVED _____

THE COMPLETENESS AND TIMELY RESPONSE OF THE EVALUATION IS DIRECTLY RELATED TO THE COMPLETENESS OF THE DATA PROVIDED. PLEASE PROVIDE ALL PERTINENT DATA. ATTACH ADDITIONAL SHEETS IF NECESSARY.

TYPE OF PROBLEM

1. ☐ INCOMING INSPECTION
   - ☐ 100% SCREEN ☐ SAMPLE INSPECTION
   - NO. TESTED _____ NO. OF REJECTS _____
   - ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
     - ☐ YES ☐ NO
   - ☐ BRIEF DESCRIPTION OF EVALUATION AND RESULTS ATTACHED
2. ☐ IN PROCESS/MANUFACTURING FAILURE
   - ☐ BOARD CHECKOUT ☐ SYSTEM CHECKOUT
   - ☐ FAILED ON TURN-ON
   - ☐ FAILED AFTER _____ HOURS OPERATION
   - WAS UNIT RETESTED UNDER INCOMING INSPECTION CONDITIONS? ☐ YES ☐ NO
   - ☐ BRIEF DESCRIPTION OF HOW FAILURE WAS ISOLATED TO COMPONENT ATTACHED
3. ☐ FIELD FAILURE
   - FAILED AFTER _____ HOURS OPERATION
   - ESTIMATED FAILURE RATE _____% PER 1000 HOURS
   - END USER _____ LOCATION _____
   - AMBIENT TEMPERATURE _____C
   - MIN. _____ C MAX. _____ C
   - REL. HUMIDITY _____%
   - ☐ END USER FAILURE CORRESPONDENCE ATTACHED

ACTION REQUESTED BY CUSTOMER

SPECIFIC ACTION REQUESTED _____

IMPACT OF FAILED UNITS ON CUSTOMER'S SITUATION: _____

CUSTOMER CONTACTS WITH SPECIFIC KNOWLEDGE OF REJECTS
NAME _____
POSITION _____ PHONE _____

DETAILS OF REJECT

(Where appropriate serialize units and specify for each)

TEST CONDITIONS RELATING TO FAILURE
- ☐ TESTER USED (MFGR/MODEL) _____
- ☐ TEST TEMPERATURE _____
- ☐ TEST TIME: ☐ CONTINUOUS TEST ☐ ONE SHOT (T = _____ SEC)
- ☐ DESCRIPTION OF ANY OBSERVED CONDITION TO WHICH FAILURE APPEARS SENSITIVE: _____

1. ☐ DC FAILURES
   - ☐ OPENS ☐ SHORTS ☐ LEAKAGE ☐ STRESS
   - ☐ POWER DRAIN ☐ INPUT LEVEL ☐ OUTPUT LEVEL
   - ☐ LIST OF FORCING CONDITIONS AND MEASURED RESULTS FOR EACH PIN IS ATTACHED
   - ☐ POWER SUPPLY SEQUENCING ATTACHED
2. ☐ AC FAILURES
   - LIST FAILING CHARACTERISTICS _____
   - ADDRESS OF FAILING LOCATION (IF APPLICABLE) _____
   - ATTACHED:
     - ☐ LIST OF POWER SUPPLY AND DRIVER LEVELS (Include pictures of waveforms).
     - ☐ LIST OF OUTPUT LEVELS AND LOADING CONDITIONS
     - ☐ INPUT AND OUTPUT TIMING DIAGRAMS
     - ☐ DESCRIPTION OF PATTERNS USED (If not standard patterns, give very complete description including address sequence).
3. ☐ PROM PROGRAMMING FAILURES
   - ADDRESS OF FAILURES _____
   - PROGRAMMER USED (MFG/MODEL/REV. NO.) _____
4. ☐ PHYSICAL/ASSEMBLY RELATED FAILURES
   - ☐ SEE COMMENTS BELOW ☐ SEE ATTACHED

Additional Comments:

FIGURE 2. PFAST ACTION REQUEST

INSTRUCTIONS FOR COMPLETING PFAST ACTION REQUEST FORM

The purpose of this form is to help us provide you with a more accurate, complete, and timely response to failures which may occur. Accurate and complete information is essential to ensure that the appropriate corrective action can be implemented. Due to this need for accurate and complete information, requests without a completed PFAST Action Request form will be returned.

Source of Problem:
This section requests the product flow leading to the failure. Mark an "X" in the appropriate boxes up to and including the step which detected the failure. Also mark an "X" in the appropriate box under ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS? to indicate whether this is a rare failure or a repeated problem.

Example 1. No incoming electrical test was performed, the units were installed onto boards, the boards functioned correctly for two hours and then 1 unit failed. The customer rarely has a failure due to this Harris device.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE _____
2. INCOMING TEST ■ NOT PERFORMED
   ☐ 100% TESTED ☐ SAMPLE TESTED
   NO. TESTED _____ NO. OF REJECTS _____
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ■ BOARD TEST ☐ SYSTEM TEST
   HOW MANY UNITS FAILED? 1
   FAILED AFTER 2 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ■ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ☐ YES ■ NO
4. FIELD FAILURE
   FAILED AFTER _____ HOURS OPERATION
   ESTIMATED FAILURE RATE _____% PER _____
   END USER _____ LOCATION _____
   MIN. _____ °C AVE. _____ °C MAX. _____ °C
5. OTHER _____

Example 2. 100 out of the 500 units shipped were tested at incoming and all passed. The units were installed into boards and the boards passed. The boards were installed into the system and the system failed immediately when turned on. There were 3 system failures due to this part. The customer frequently has failures of this Harris device. The 3 units were not retested at incoming.

SOURCE OF PROBLEM
(Enter the sequence of events in the boxes provided)

1. VISUAL/MECHANICAL
   ☐ DESCRIBE _____
2. INCOMING TEST ☐ NOT PERFORMED
   ☐ 100% TESTED ■ SAMPLE TESTED
   NO. TESTED 100 NO. OF REJECTS 0
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ■ YES ☐ NO
3. IN PROCESS/MANUFACTURING FAILURE
   ■ BOARD TEST ■ SYSTEM TEST
   HOW MANY UNITS FAILED? 3
   FAILED AFTER 0 HOURS OF TESTING
   WAS UNIT RETESTED AT INCOMING INSPECTION?
   ☐ YES ■ NO
   ARE RESULTS REPRESENTATIVE OF PREVIOUS LOTS?
   ■ YES ☐ NO
4. FIELD FAILURE
   FAILED AFTER _____ HOURS OPERATION
   ESTIMATED FAILURE RATE _____% PER _____
   END USER _____ LOCATION _____
   MIN. _____ °C AVE. _____ °C MAX. _____ °C
5. OTHER _____

Action Requested by Customer:
This section should be completed with the customer's expectations. This information is essential for an appropriate response.

Reason for Electrical Reject:
This section should be completed if the type of failure could be identified. If this information is contained in attached customer correspondence there is no need to transpose onto the PFAST Action Request form.

PFAST REQUIREMENTS

The value of returning failing products is in the corrective actions that are generated. Failure to meet the following requirements can cause an erroneous conclusion and corrective action; therefore, failure to meet these requirements will result in the request being returned. Contact the local PFAST Coordinator if you have any questions.

Units with conformal coating should include the coating manufacturer and model. This is requested since the coating must be removed in order to perform electrical or hermeticity testing.

1) Units must be returned with proper ESD protection (ESD-safe shipping tubes within shielding box/bag or inserted into conductive foam within shielding box/bag). No tape, paper bags, or plastic bags should be used. This requirement ensures that the devices are not damaged during shipment back to Harris.

2) Units must be intact (lid not removed and at least part of each package lead present). This requirement is in place since the parts must be intact in order to perform electrical test. Also, opening the package can remove evidence of the cause for failure and lead to an incorrect conclusion.

3) Programmable parts (ROMs, PROMS, UVEPROMs, and EEPROMs) must include a master unit with the same pattern. This requirement is to provide the pattern so all failing locations can be identified. A master unit is required if a failure analysis is requested.

FIGURE 2. PFAST ACTION REQUEST (Continued)

Failure Analysis Laboratory

The Failure Analysis Laboratory's capabilities encompass the isolation and identification of all failure modes/failure mechanisms, preparing comprehensive technical reports, and assigning appropriate corrective actions. Research vital to understanding the basic physics of the failure is also undertaken.

Failure analysis is a method of enhancing product reliability and determining corrective action. It is the final and crucial step used to isolate potential reliability problems that may have occurred during reliability stressing. Accurate analysis results are imperative to assess effective corrective actions. To ensure the integrity of the analysis, correlation of the failure mechanism to the initial electrical failure is essential.

A general failure analysis procedure has been established in accordance with the current revision of MIL-STD-883, Section 5003. The analysis procedure was designed on the premise that each step should provide information on the failure without destroying information to be obtained from subsequent steps. The exact steps for an analysis are determined as the situation dictates. (See Figures 3 and 4). Records are maintained by laboratory personnel and contain data, the failure analyst's notes, and the formal Product Analysis Report.

Analytical Services Laboratory

Harris facilities, engineering, manufacturing, and product assurance are supported by the Analytical Services Laboratory. Organized into chemical or microbeam analysis methodology, staff and instrumentation from both labs cooperate in fully integrated approaches necessary to complete analytical studies. The capabilities of each area are shown below.

SPECTROSCOPIC METHODS: Colorimetry, Optical Emission, Ultraviolet Visible, Fourier Transform-Infrared, Flame Atomic Absorption, Furnace Organic Carbon Analyzer, Mass Spectrometer.

CHROMATOGRAPHIC METHODS: Gas Chromatography, Ion Chromatography.

THERMAL METHODS: Differential Scanning Colorimetry, Thermogravimetric Analysis, Thermomechanical Analysis.

PHYSICAL METHODS: Profilometry, Microhardness, Rheometry.

CHEMICAL METHODS: Volumetric, Gravimetric, Specific Ion Electrodes.

ELECTRON MICROSCOPE: Transmission Electron Microscopy, Scanning Electron Microscope.

X-RAY METHODS: Energy Dispersive X-ray Analysis (SEM), Wavelength Dispersive X-ray Analysis (SEM), X-ray Fluorescence Spectrometry, X-ray Diffraction Spectrometry.

SURFACE ANALYSIS METHODS: Scanning Auger Microprobe, Electron Spectroscopy/Chemical Analysis, Secondary Ion Mass Spectrometry, Ion Scattering Spectrometry, Ion Microprobe.

The department also maintains ongoing working arrangements with commercial, university, and equipment manufacturers' technical service laboratories, and can obtain any materials analysis in cases where instrumental capabilities are not available in our own facility.

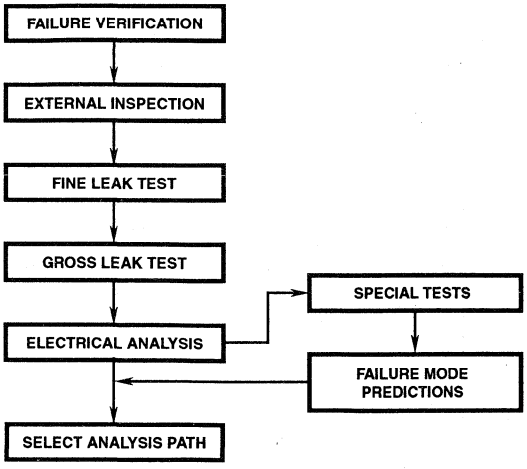


FIGURE 3. NON-DESTRUCTIVE

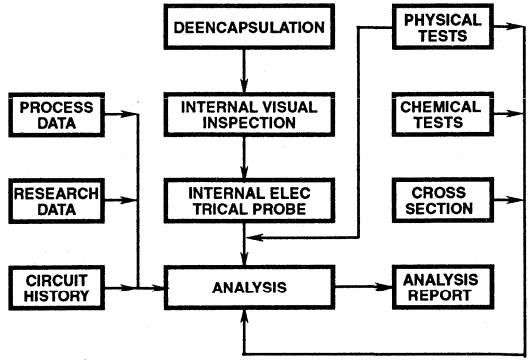


FIGURE 4. DESTRUCTIVE

Reliability Fundamentals and Calculation of Failure Rate

Table 8 below defines some of the more important terminology used in describing the lifetime of integrated circuits.

Of prime importance is the concept of "failure rate" and the calculation thereof.

Failure Rate Calculations

Reliability data may be composed of several different failure mechanisms and the combining of potentially diverse failure rates into one comprehensive failure rate is desired. The failure rate calculation is complicated because the failure mechanisms are thermally activated at differing rates. Additionally, this data is usually obtained on a number of life tests performed at unique stress temperatures. The equation below accounts for these considerations along with a statistical factor to obtain the upper confidence level (UCL) for the resulting failure rate.

$$\lambda = \left[\sum_{i=1}^{\beta} \frac{x_i}{\sum_{j=1}^{k} TDH_j \, AF_{ij}} \right] \bullet \frac{M \times 10^9}{\sum_{i=1}^{\beta} x_i}$$

where,

λ = failure rate in FITs (Number fails in 10^9 device hours)

β = # of distinct possible failure mechanisms

k = # of life tests being combined

x_i = # of failures for a given failure mechanism $i = 1, 2, \ldots \beta$

TDH_j = Total device hours of test time (unaccelerated) for Life Test j, $j = 1, 2, 3, \ldots k$

AF_{ij} = Acceleration factor for appropriate failure mechanism $i = 1, 2, \ldots k$

$$M = \frac{X^2(\alpha, 2r+2)}{2}$$

where,

X^2 = chi square factor for $2r + 2$ degrees of freedom

r = total number of failures (Σx_i)

α = risk associated with UCL;
i.e. α = (100-UCL(%))/100

In the failure rate calculation, Acceleration Factors (AFij) are used to derate the failure rate from the thermally accelerated life test conditions to a failure rate indicative of actual use temperature. Although no standard exists, a temperature of +55°C has been popular. Harris Semiconductor Reliability Reports will derate to +55°C and will express failure rates at 60% UCL. Other derating temperatures and UCLs are available upon request.

TABLE 8. FAILURE RATE PRIMER

TERMS	DEFINITIONS/DESCRIPTION
Failure Rate λ	Measure of failure per unit of time. The failure rate typically decreases slightly over early life, and then becomes relatively constant over time. The on set of wearout will show an increasing failure rate, which should occur well beyond useful life. The useful life failure rate is based on the exponential life distribution
FIT (Failure In Time)	Measure of failure rate in 10^9 device hours; e.g., 1 FIT = 1 failure in 10^9 device hours, 100 FITS = 100 failure in 10^9 device hours, etc.
Device Hours	The summation of the number of units in operation multiplied by the time of operation.
MTTF (Mean Time To Failure)	Mean of the life distribution for the population of devices under operation or expected lifetime of an individual, MTTF = $1/\lambda$, which is the time where 63.2% of the population has failed. Exampled: For λ = 10 FITS (or 10 E-9/Hr.), MTTF = $1/\lambda$ = 100 million hours.
Confidence Level (or Limit)	Probability level at which population failure rate estimates are derived from sample life test: 10 FITs at 95% UCL means that the population failure rate is estimated to be no more than 10 FITs with 95% certainty. The upper limit of the confidence interval is used.
Acceleration Factor (AF)	A constant derived from experimental data which relates the times to failure at two different stresses. The AF allows extrapolation of failure rates from accelerated test conditions to use conditions.

Acceleration Factors

Acceleration factor is determined from the Arrhenius Equation. This equation is used to describe physiochemical reaction rates and has been found to be an appropriate model for expressing the thermal acceleration of semiconductor failure mechanisms.

$$AF = EXP\left[\frac{E_a}{k}\left(\frac{1}{T_{use}} - \frac{1}{T_{stress}}\right)\right]$$

where,

AF = Acceleration Factor

E_a = Thermal Activation Energy (See Table 9)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

Both T_{use} and T_{stress} (in degrees Kelvin) include the internal temperature rise of the device and therefore represent the junction temperature.

Activation Energy

The Activation Energy (E_a) of a failure mechanism is determined by performing at least two tests at different levels of stress (temperature and/or voltage). The stresses will provide the time to failure (t_f) for the two (or more) populations thus allowing the simultaneous solution for the activation energy as follows:

$$\ln (t_{f1}) = C + \frac{E_a}{kT_1} \qquad \ln (t_{f2}) = C + \frac{E_a}{kT_2}$$

By subtracting the two equations, and solving for the activation energy, the following equation is obtained:

$$E_a = \frac{k\,[\ln(t_{f1}) - \ln(t_{f2})]}{(1/T1 - 1/T2)}$$

where,

E_a = Thermal Activation Energy (See Table 9)

k = Boltzmann's Constant (8.63×10^{-5} eV/°K)

T_1, T_2 = Life test temperatures in degrees Kelvin

TABLE 9. FAILURE MECHANISM

FAILURE MECHANISM	ACTIVATION ENERGY	SCREENING AND TESTING METHODOLOGY	CONTROL METHODOLOGY
Oxide Defects	0.3 - 0.5eV	High temperature operating life (HTOL) and voltage stress. Defect density test vehicles.	Statistical Process Control of oxide parameters, defect density control, and voltage stress testing.
Silicon Defects (Bulk)	0.3 - 0.5eV	HTOL & voltage stress screens.	Vendor statistical Quality Control programs, and Statistical Process Control on thermal processes.
Corrosion	0.45eV	Highly accelerated stress testing (HAST)	Passivation dopant control, hermetic seal control, improved mold compounds, and product handling.
Assembly Defects	0.5 - 0.7eV	Temperature cycling, temperature and mechanical shock, and environmental stressing.	Vendor Statistical Quality Control programs, Statistical Process Control of assembly processes, proper handling methods.
Electromigration - Al Line - Contact	 0.6eV 0.9eV	Test vehicle characterizations at highly elevated temperatures.	Design ground rules, wafer process statistical process steps, photoresist, metals and passivation
Mask Defects/ Photoresist Defects	0.7eV	Mask FAB comparator, print checks, defect density monitor in FAB, voltage stress test and HTOL.	Clean room control, clean mask, pellicles, Statistical Process Control of photoresist/etch processes.
Contamination	1.0eV	C-V stress at oxide/interconnect, wafer FAB device stress test and HTOL.	Statistical Process Control of C-V data, oxide/interconnect cleans, high integrity glassivation and clean assembly processes.
Charge Injection	1.3eV	HTOL & oxide characterization.	Design ground rules, wafer level Statistical Process Control and critical dimensions for oxides.

DATA ACQUISITION 16

APPLICATION NOTE ABSTRACTS

AN #	TITLE	ABSTRACTS
001	Glossary of Data Acquisition Terms	Specification definitions, terminology and most often used terms used in the field of data acquisition.
002	Principles of Data and Conversion	Basic Data Acquisition system design, quantizing theory, sampling theory, data coding, amplifiers and filters, settling time, DAC types, ADC types, reference circuits, analog multiplexers, sample and holds, specifications, and selection criteria.
004	The IH5009 Analog Switch Series	Circuit operation, logic compatibility, switching speed and crosstalk, and application circuits.
009	Pick Sample-Holds by Accuracy and Speed and Keep Hold Capacitors in Mind	Monolithic considerations, error analysis, droop discussion, capacitor characteristics, deglitching sample and holds, and cascaded sample and hold designs.
012	Switching Signals with Semiconductors	Analog switches are fast, low cost, and work well with the high impednace of most signal circuits. Often they can replace reed relays.
016	Selecting A/D Converters	Important selection parameters, the integrating converter, the SAR type converter, multiplexed data systems, and a definition of terms.
017	The Integrating A/D Converter	The dual slope conversion technique, analyzing errors, capacitor induced errors and a noise discussion.
018	Do's and Don'ts of Applying A/D Converters	System power routing errors, PCB layout rules, component selection, thermal effects, and maximizing the FSR range of the converter.
020	A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing	High speed system block diagram, layout considerations, multiplexer considerations differential amplifiers, sample and hold amplifier, SAR type ADCs, DAC design, and microprocessor interfacing
023	Low Cost Panel Meter Designs	Cost advantages of display converters, Evaluation kit usage, display types, capacitors recommended, and proper power supply range.
028	Building an Auto-Ranging DMM with the ICL7103A/ ICL8052A A/D Converter Pair	Basic circuit configuration and operation, decimal point drive, interface to parallel data systems, auto-ranging designs, issues and solutions for proper operation.

See page i for information on Ordering Literature

Application Note Abstracts (Continued)

AN #	TITLE	ABSTRACTS
030	ICL7104 A Binary Output A/D Converter for Microprocessors	Interfacing to a digital system in non-handshaking mode, a handshaking mode interface to various processors, performance enhancement techniques, and an auto-zero loop discussion.
032	Understanding the Auto-Zero and Common Mode Performance of the ICL7106/ 7107/7109 Family	Theory of operation for the four integration phases, CMRR and the common mode voltage effects, the auto-zero loop residual, and in depth error analysis.
042	Interpretation of Data Converter Accuracy Specifications	A Discussion of data converter transfer functions, quantization noise and dynamic range, non-ideal data converter operation, nonlinearity, temperature induced errors, error budgets, layout and grounding rules.
043	Video Analog to Digital Conversion	Comparator based flash converters, quantization noise, the decoder, a 2 stage flash converter, and hybrid considerations.
046	Building a Battery Operated Auto Ranging DVM with the ICL7106	Auto-ranging circuitry design, the input range/resistor divider, an auto-range clock circuit design, power supply requirements, measuring resistance and transconductance, and using the ICL7126 and ICL7107.
047	Games People Play with Harris A/D Converters	Various real world applications for A/D converters, LCD annunciator drivers, decimal point drivers, a low battery detect application, blanking the display on low battery detect, controlling LED brightness, instant continuity detector, high voltage display driver, a gas discharge plasma display, DVM circuit, a tachometer design, measuring the gain of a transistor, running off a 1.5V supply, a simple capacitor meter, and a weighing system
048	Know Your Converter Codes	Analyzing digital codes, ADC and DAC operating basics, Bipolar coding techniques, and coding limitations.
049	Applying the 7109 A/D Converter	A description of the ICL7109s, differential input section, differential reference, digital section and how to measure bridges, and offsets. Interface examples to parallel processors, serial interfaces and how to replace Voltage to frequency converters.
052	Tips for Using Single Chip $3^1/_2$ Digit A/D Converters	Some of the more commonly asked questions concerning the $3^1/_2$ digital display converters ranging from power supply inputs, display types and drive, to timing, ratiometric operation, and component selection. A troubleshooting guide is provided.
054	Display Driver Family Combines Convenience of Use with Microprocessor Interfaceability	Advantages of IC display drivers, non-multiplexed display operation, functional block diagrams, multiplexed display operation, and binary to bar graph display applications circuits.
059	Digital Panel Meter Experiments for the Hobbyist	Discusses the fundamentals of designing a panel meter for measuring, DC Voltages, AC Voltages, resistance measurements, current measurements, temperature measurement, and designing multi-range DVMs.
517	Applications of Monolithic Sample and Hold Amplifiers	General Sample and Hold information and fourteen specific applications, including filtered Sample and Hold DAC de-glitcher Integrate-Hold-Reset, gated op amp, etc.

See page i for information on Ordering Literature

Application Note Abstracts (Continued)

AN #	TITLE	ABSTRACTS
520	CMOS Analog Multiplexers and Switches; Application Considerations	Switch selection criteria, datasheet definitions, care and feeding of multiplexers and switches, digital interface, practical multiplexer applications alternative to CMOS switches and multiplexers.
521	Getting the Most Out of CMOS Devices for Analog Switching Jobs	CMOS vs bipolar device performances, over voltage and channel interaction conditions, JI technology and latch-up, floating body JI technology, fool proof CMOS analog multiplexer, other DI benefits.
522	Digital to Analog Converter Terminology	Explains DAC terminology, Resolution Gain Error, Offset Error, Linearity Error, Differential Linearity Error, Drift, Settling Time, etc.
524	Digital to Analog Converter High Speed ADC Applications	Use of High Speed DAC's in tracking, servo, and successive approximation Analog to Digital Converters. Design ideas for Data Acquisition Systems.
531	Analog Switch Applications in A/D Data Conversion Systems	System configurations, analog switch types, CMOS switch selection guidelines, alternative uses of CMOS switches.
532	Common Questions Concerning CMOS Analog Switches	Power supply considerations, input overvoltage protection, single supply operation, various questions about Harris DI switches.
534	Additional Information on the HI-300 Series Switch	"ON" resistance, leakage currents, switching speeds, power supply requirements, internal switch operation and schematics, single supply operation, charge injection, power supplies conditions and protective circuitry.
535	Design Considerations for a Data Acquisition System (DAS)	A collection of guidelines for the design of a Data Acquisition System. Includes signal conditioning, transducers, single-ended vs differential signal paths, low level signals, filters Programmable Gain Amplifiers, sampling rate, and computer interfacing.
538	Monolithic Sample/Hold Combines Speed and Precision	Description and electrical specifications for the HA-5320 Sample/Hold Amplifiers, explanation of error sources, and HA-5320 applications.
539	A Monolithic 16-Bit D/A Converter	Detailed description of a 16 bit DAC design and layout. Second order errors sources that contribute to linearity errors are discussed as well as architectural design, ground cancelation effects, settling time measurement techniques, suggested amplifier configurations for voltage output, and data-bus interfacing.
543	New High Speed Switch Offers Sub 50ns Switching Times	Application enhancement using the HI201HS, high speed multiplexers, high speed sample and hold, analog switch and op amp circuitry, integrator with start/reset, low pass filter with select break frequency, amplifier with programmable gain, future applications.
557	Recommended Test Procedures for Analog Switches	Description of analog switch test methods employed at Harris Semiconductor.
559	HI-222 Video/HF Switch Optimizes Key Parameters	Description of the key specifications of the HI222 such as, power supply range vs R_{ON}, T_{ON}, differential gain and phase errors, switching transients and charge injection, continuous and peak current capability, off isolation, crosstalk and PC board layout.

See page i for information on Ordering Literature

Application Note Abstracts (Continued)

AN #	TITLE	ABSTRACTS
8759	Low Cost Data Acquisition System Features SPI A/D Converter	Discussions of a typical serial interface system, detailed description of the 68HC68 architecture, multiple zone heating system design, digital storage scope design, and microcode for a low cost DAS.
9213	Advantages and Application of Display Integrating A/D Converters	Theory of operation of a dual slope integrating type A/D converter used for bridge measurement, low level sensors and several application circuits including, a capacitance meter, and digital thermometer.
9214	Using Harris High Speed A/D Converters	PCB layout, grounding and power considerations for high speed converter board design, suggested voltage reference circuits, analog input buffers, bandwidth considerations, accuracy adjustments, logic family compatibility and interface examples, antialiasing filter theory, multiplexed inputs and input clamping for video signals.
9215	Using the HI5700 Evaluation Board	Theory of operations discussion for the HI5700, a description and use of the evaluation board, typical performance curve data on the HI5700, board layout and schematics.
9216	Using the HI5701 Evaluation Board	Theory of operations discussion for the HI5701, a description and use of the evaluation board, typical performance curve data on the HI5701, board layout and schematics.
9309	Using the HI5800/HI5801 Evaluation Board	HI5800 and HI5801operation and architecture, an evaluation kit description, operating modes, layout and schematics.
9313	Circuit Considerations in Imaging Applications	Discussions of Video formats such as RS170, circuit design considerations, system design, test results and time division multiplexed systems.
9316	Power Supply Considerations for the HI-222 High Frequency Video Switch	A guide to proper power supply sequencing for the HI-222 Video Switch.
9328	Using the HI1166 Evaluation Board	A description of how to use the HI1166, 250MHz, 8-bit A/D evaluation board.
9329	Using the HI1176/1171 Evaluation Board	A description of how to use the HI1176/1171 Video A/D and D/A evaluation board.
9330	Using the HI1396 Evaluation Board	A description of how to use the HI1396, 125MHz, 8-bit A/D evaluation board.
9331	Using the HI1175 Evaluation Board	A description of how to use the HI1175 Video A/D evaluation board.
9332	Using the HI1276 Evaluation Board	A description of how to use the HI1276, 500MHz, 8-bit A/D evaluation board.
9333	Using the HI1386 Adapter Board	A description of how to use the HI1386 75MHz 8-bit A/D adaptor board. To be used with HI1396 evaluation board.
9337	Reduce CMOS Multiplexer Troubles through Proper Device Selection	How to deal with output leakage, Overvoltage fault protection techniques, and new architectural designs to provide better fault protection.

See page i for information on Ordering Literature

DATA ACQUISITION 17

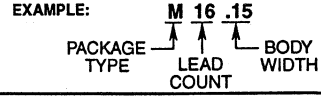
PACKAGING INFORMATION

Data Acquisition Package Selection Guide

Using the Selection Guide:

The first character of each entry indicates the package type, while the number preceding the decimal point details the package lead count. Except for MQFP, LCC, SIP, and Can packages, the decimal point and succeeding numbers specify the reference package width in inches (e.g. .15 = 150 mil width). The entire entry indicates the package table containing the appropriate package dimensions (e.g. 8 lead PDIP dimension are detailed in Table E8.3). The index on page 17-1 lists page numbers for PDIP, SOIC, PLCC, MQFP, CDIP, Sidebraze, LCC, SIP and Can tables.

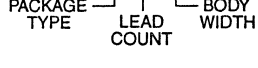
PART NUMBER	PDIP	SOIC/ SSOP	PLCC	MQFP	CERDIP	SIDE-BRAZE	LCC	SIP	CAN
AD590									T3.A
AD7520	E16.3				F16.3				
AD7521	E18.3								
AD7523	E16.3								
AD7530	E16.3								
AD7531	E18.3								
AD7533	E16.3								
AD7541	E18.3								
AD7545	E20.3				F20.3				
ADC0802	E20.3				F20.3				
ADC0803	E20.3	M20.3			F20.3				
ADC0804	E20.3				F20.3				
CA3161	E16.3								
CA3162	E16.3								
CA3162A	E16.3								
CA3304	E16.3	M16.3			F16.3				
CA3306	E18.3	M20.3			F18.3		J20.B		
CA3310	E24.3	M24.3			F24.3				
CA3310A	E24.3	M24.3			F24.3				
CA3318C	E24.6	M24.3			F24.6				
CA3338	E16.3	M16.3			F16.3				
CA3338A	E16.3	M16.3			F16.3				
DG200	E14.3				F14.3				T10.B
DG201	E16.3				F16.3				
DG201A	E16.3	M16.3			F16.3				
DG202	E16.3				F16.3				
DG211	E16.3	M16.15							
DG212	E16.3	M16.15							
DG300A	E14.3				F14.3				T10.B
DG301A	E14.3				F14.3				T10.B
DG302A	E14.3				F14.3				
DG303A	E14.3	M16.3			F14.3				
DG308A	E16.3	M16.15			F16.3				



Data Acquisition Package Selection Guide (Continued)

PART NUMBER	PDIP	SOIC/ SSOP	PLCC	MQFP	CERDIP	SIDE-BRAZE	LCC	SIP	CAN
DG309	E16.3	M16.15			F16.3				
DG401	E16.3	M16.15			F16.3				
DG403	E16.3	M16.15			F16.3				
DG405	E16.3	M16.15			F16.3				
DG406	E16.3	M16.15							
DG407	E16.3	M16.15							
DG408	E16.3	M16.15			F16.3				
DG409	E16.3	M16.15			F16.3				
DG411	E16.3	M16.15			F16.3				
DG412	E16.3	M16.15			F16.3				
DG413	E16.3	M16.15			F16.3				
DG441	E16.3	M16.15			F16.3				
DG442	E16.3	M16.15			F16.3				
DG444	E16.3	M16.15							
DG445	E16.3	M16.15							
DG458	E16.3	M16.3			F16.3				
DG459	E16.3	M16.3			F16.3				
DG506A	E28.6	M28.3			F28.6				
DG507A	E28.6	M28.3			F28.6				
DG508A	E16.3	M16.3			F16.3				
DG509A	E16.3	M16.3			F16.3				
DG526	E28.6	M28.3			F28.6				
DG527	E28.6	M28.3			F28.6				
DG528	E18.3	M18.3			F18.3				
DG529	E18.3	M18.3			F18.3				
HA7210	E8.3	M8.15							
HI-200	E14.3				F14.3				T10.B
HI-201	E16.3	M16.3	N20.35		F16.3				
HI-201-HS	E16.3	M16.3	N20.35		F16.3		J20.A		
HI-300	E14.3	M14.15			F14.3				T10.B
HI-301	E14.3	M14.15			F14.3				T10.B
HI-302	E14.3	M14.15			F14.3				
HI-303	E14.3	M14.15			F14.3				
HI-304	E14.3	M14.15			F14.3				T10.B
HI-305	E14.3	M14.15			F14.3				T10.B
HI-306	E14.3	M14.15			F14.3				
HI-307	E14.3	M14.15			F14.3				
HI-381	E14.3	M14.15			F14.3				T10.B

EXAMPLE: M 16 .15



Data Acquisition Package Selection Guide (Continued)

PART NUMBER	PDIP	SOIC/ SSOP	PLCC	MQFP	CERDIP	SIDE-BRAZE	LCC	SIP	CAN
HI-384	E16.3	M16.3			F16.3				
HI-387	E14.3	M14.15			F14.3				T10.B
HI-390	E16.3	M16.3			F16.3				
HI-506	E28.6	M28.3	N28.45		F28.6		J28.A		
HI-506A	E28.6				F28.6				
HI-507	E28.6	M28.3	N28.45		F28.6		J28.A		
HI-507A	E28.6				F28.6				
HI-508	E16.3	M16.15	N20.35		F16.3		J20.A		
HI-508A	E16.3				F16.3				
HI-509	E16.3	M16.15	N20.35		F16.3		J20.A		
HI-509A	E16.3				F16.3				
HI-516	E28.6	M28.3	N28.45		F28.6		J28.A		
HI-518	E18.3	M18.3	N20.35		F18.3		J20.A		
HI-524	E18.3		N20.35		F18.3		J20.A		
HI-539	E16.3		N20.35		F16.3				
HI-546	E28.6	M28.3	N28.45		F28.6		J28.A		
HI-547	E28.6	M28.3	N28.45		F28.6		J28.A		
HI-548	E16.3	M16.3	N20.35		F16.3		J20.A		
HI-549	E16.3	M16.3	N20.35		F16.3		J20.A		
HI-565A					F24.6				
HI-574A	E28.6					D28.6	J44.A		
HI-674A	E28.6					D28.6	J44.A		
HI-774	E28.6					D28.6	J44.A		
HI1166							J68.A		
HI1171		M24.2							
HI1175	E24.4	M24.2							
HI1176				Q32.A					
HI1276							J68.B		
HI1386	E28.6A						J44.B		
HI1396	E42.6A					D42.6	J68.A		
HI-1818A	E16.3		N20.35		F16.3				
HI-1828A	E16.3		N20.35		F16.3		J20.A		
HI-5040	E16.3				F16.3				
HI-5041	E16.3				F16.3				
HI-5042	E16.3				F16.3				
HI-5043	E16.3	M16.15			F16.3		J20.A		
HI-5044	E16.3				F16.3				
HI-5045	E16.3	M16.15			F16.3				

EXAMPLE: M 16 .15

PACKAGE TYPE — LEAD COUNT — BODY WIDTH

Data Acquisition Package Selection Guide (Continued)

PART NUMBER	PDIP	SOIC/ SSOP	PLCC	MQFP	CERDIP	SIDE-BRAZE	LCC	SIP	CAN
HI-5046	E16.3				F16.3				
HI-5046A	E16.3				F16.3				
HI-5047	E16.3				F16.3				
HI-5047A	E16.3				F16.3				
HI-5048	E16.3				F16.3				
HI-5049	E16.3	M16.15			F16.3				
HI-5050	E16.3				F16.3				
HI-5051	E16.3	M16.15	N20.35		F16.3		J20.A		
HI-5700	E28.6	M28.3							
HI-5701	E18.3	M18.3							
HI5800			N44.65			D40.6			
HI5810	E24.3	M24.3			F24.3				
HI5812	E24.3	M24.3			F24.3				
HI5813	E24.3	M24.3			F24.3				
HI7131	E40.6			Q44.A					
HI7133	E40.6			Q44.A					
HI7153	E40.6					D40.6			
HI7159A	E28.6								
HI7190	E20.3	M20.3			F20.3				
HI20201	E28.6A	M28.3A							
HI20203	E28.6A	M28.3A							
HI-DAC80V	E24.6								
HI-DAC85V	E24.6								
HIN230		M20.3							
HIN231		M16.3							
HIN232	E16.3	M16.3			F16.3				
HIN234		M16.3							
HIN236	E24.3	M24.3							
HIN237	E24.3	M24.3							
HIN238	E24.3	M24.3							
HIN239	E24.3	M24.3							
HIN240				Q44.B					
HIN241		M28.3/ M28.209							
ICL232	E16.3	M16.3			F16.3				
ICL7106	E40.6			Q44.B					
ICL7107	E40.6			Q44.B					
ICL7109	E40.6				F40.6	D40.6			

EXAMPLE: M 16 .15

PACKAGE TYPE — LEAD COUNT — BODY WIDTH

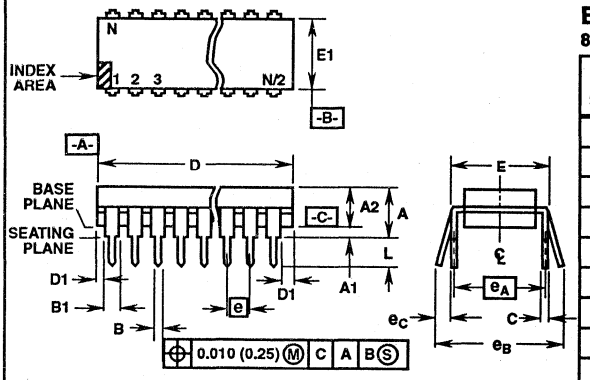
PART NUMBER	PDIP	SOIC/ SSOP	PLCC	MQFP	CERDIP	SIDE-BRAZE	LCC	SIP	CAN
ICL7116	E40.6			Q44.B					
ICL7117	E40.6								
ICL7129	E40.6			Q44.B					
ICL7135	E28.6								
ICL7136	E40.6			Q44.B					
ICL7137	E40.6			Q44.B					
ICL7139	E40.6								
ICL7149	E40.6			Q44.B					
ICL8069		M8.15		Q44.B				Z3.05A	T2.A
ICM7170	E24.6	M24.3			F24.6				
ICM7211	E40.6			Q44.B					
ICM7212	E40.6								
ICM7213	E14.3								
ICM7216A	E28.6				F28.6				
ICM7216B	E28.6				F28.6				
ICM7216D	E28.6				F28.6				
ICM7217	E28.6				F28.6				
ICM7224	E40.6								
ICM7226A	E40.6								
ICM7226B					F40.6				
ICM7228	E28.6	M28.3			F28.6				
ICM7231	E40.6				F40.6				
ICM7232	E40.6				F40.6				
ICM7243	E40.6				F40.6				
ICM7249	E48.6								
IH5043	E16.3	M16.3			F16.3				
IH5052					F16.3				
IH5053					F16.3				
IH5140	E16.3				F16.3				
IH5141	E16.3				F16.3				
IH5142	E16.3				F16.3				
IH5143	E16.3				F16.3				
IH5144	E16.3				F16.3				
IH5145	E16.3				F16.3				
IH5151	E16.3				F16.3				
IH5341	E14.3								T10.B
IH5352	E16.3	M20.3			F16.3				T10.B

EXAMPLE: **M 16 .15**

PACKAGE TYPE — LEAD COUNT — BODY WIDTH

Package Outlines

Dual-In-Line Plastic Packages



E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

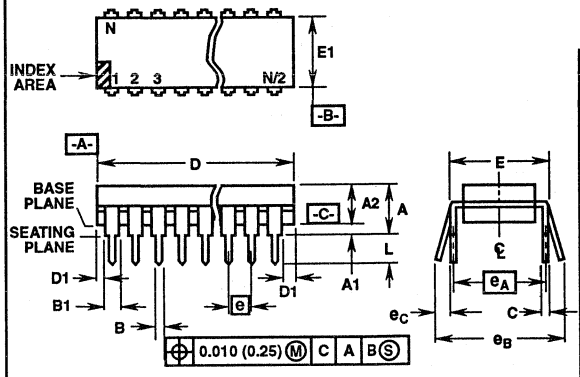
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

Dual-In-Line Plastic Packages (Continued)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

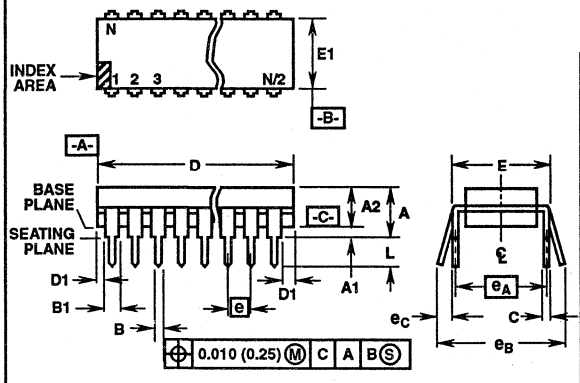
Rev. 0 12/93

E18.3 (JEDEC MS-001-BC ISSUE D)
18 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.845	0.880	21.47	22.35	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	18		18		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (Continued)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E20.3 (JEDEC MS-001-AD ISSUE D)
20 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.55	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.980	1.060	24.89	26.9	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	20		20		9

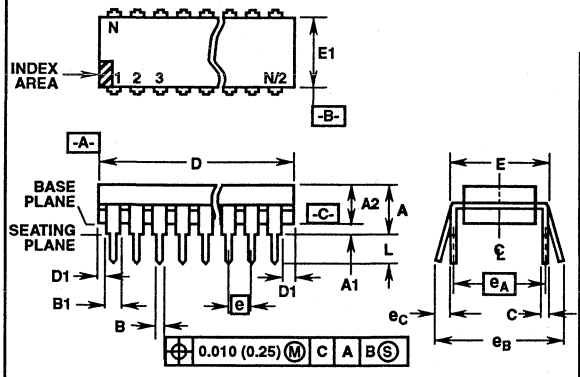
Rev. 0 12/93

E24.3 (JEDEC MS-001-AF ISSUE D)
24 LEAD NARROW BODY DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	1.230	1.280	31.24	32.51	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	24		24		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (Continued)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E24.6 (JEDEC MS-011-AA ISSUE B)
24 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.150	1.290	29.3	32.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	24		24		9

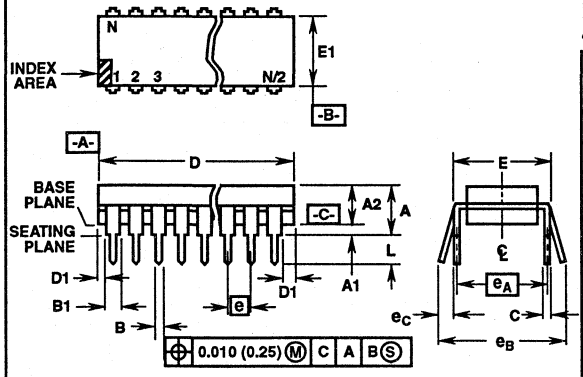
Rev. 0 12/93

E28.6 (JEDEC MS-011-AB ISSUE B)
28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.380	1.565	35.1	39.7	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	28		28		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (Continued)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E40.6 (JEDEC MS-011-AC ISSUE B)
40 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	1.980	2.095	50.3	53.2	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	40		40		9

Rev. 0 12/93

E48.6 (JEDEC MS-011-AD ISSUE B)
48 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.250	-	6.35	4
A1	0.015	-	0.39	-	4
A2	0.125	0.195	3.18	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.030	0.070	0.77	1.77	8
C	0.008	0.015	0.204	0.381	-
D	2.385	2.480	60.70	63.1	5
D1	0.005	-	0.13	-	5
E	0.600	0.625	15.24	15.87	6
E1	0.485	0.580	12.32	14.73	5
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		6
e_B	-	0.700	-	17.78	7
L	0.115	0.200	2.93	5.08	4
N	48		48		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (Continued)

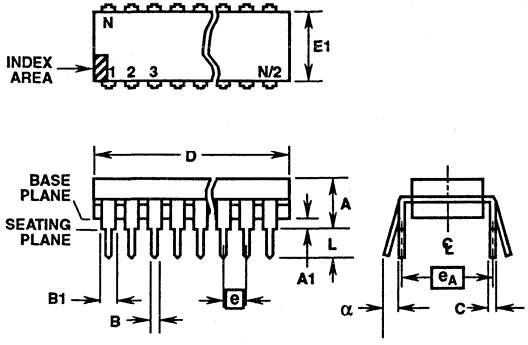


FIGURE 1

E24.4

24 LEAD DUAL-IN-LINE PLASTIC PACKAGE (400 MIL)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.142	0.161	3.60	4.10	2
A1	0.020	-	0.50	-	2
B	0.016	0.023	0.40	0.60	
B1	0.042	0.053	1.05	1.35	
C	0.008	0.013	0.20	0.35	
D	1.185	1.204	30.10	30.60	3
E1	0.331	0.346	8.40	8.80	3
e	0.100 BSC		2.54 BSC		
e_A	0.400 BSC		10.16 BSC		4
L	0.119	-	3.0	-	2
N	24		24		5
α	0°	15°	0°	15°	

Rev. 0 12/93

E28.6A

28 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.178	0.196	4.5	5.0	2
A1	0.020	-	0.50	-	2
B	0.016	0.023	0.40	0.60	-
B1	0.042	0.053	1.05	1.35	-
C	0.008	0.13	0.20	0.35	-
D	1.485	1.503	37.7	38.2	3
E1	0.508	0.523	12.9	13.3	3
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		4
L	0.119	-	3.0	-	2
N	28		28		5
α	0°	15°	0°	15°	

Rev. 0 12/93

E42.6A

42 LEAD DUAL-IN-LINE PLASTIC PACKAGE

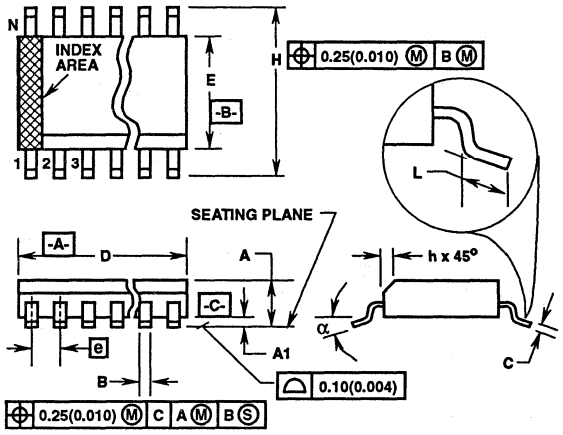
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.193	0.212	4.9	5.4	2
A1	0.040	-	1.0	-	2
B	0.018	0.025	0.45	0.65	-
B1	0.046	0.057	1.15	1.45	-
C	0.008	0.013	0.20	0.35	-
D	2.162	2.181	54.9	55.4	3
E1	0.516	0.531	13.1	13.50	3
e	0.100 BSC		2.54 BSC		-
e_A	0.600 BSC		15.24 BSC		4
L	0.119	-	3.0	-	2
N	42		42		5
α	0°	15°	0°	15°	

Rev. 0 12/93

NOTES:

1. Controlling Dimensions: MILLIMETER. In case of conflict between English and Metric dimensions, the metric dimensions control.
2. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
3. D and E1 dimensions do not include mold flash or protrusions.
4. e_A is measured with the leads constrained to be perpendicular to base plane.
5. N is the maximum number of terminal positions.

Small Outline (SOIC) Plastic Packages



M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

M16.15 (JEDEC MS-012-AC ISSUE C)
16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

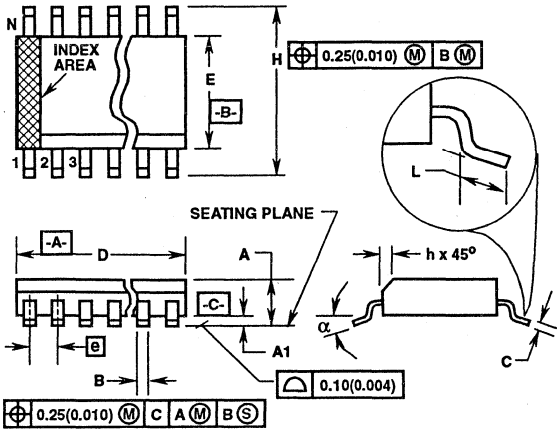
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.3859	0.3937	9.80	10.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline (SOIC) Plastic Packages (Continued)



M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

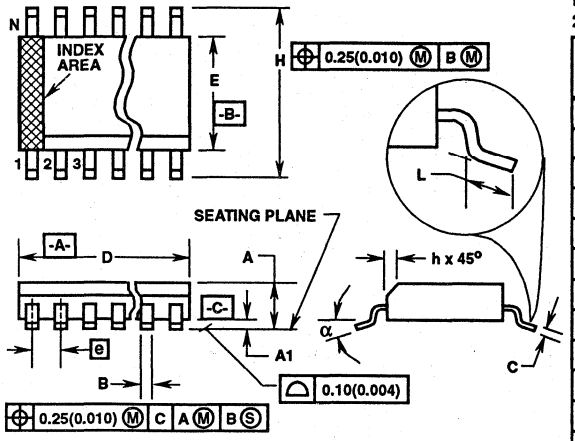
1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M18.3 (JEDEC MS-013-AB ISSUE C)
18 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4469	0.4625	11.35	11.75	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	18		18		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

Small Outline (SOIC) Plastic Packages (Continued)



M20.3 (JEDEC MS-013-AC ISSUE C)
20 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.4961	0.5118	12.60	13.00	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	20		20		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

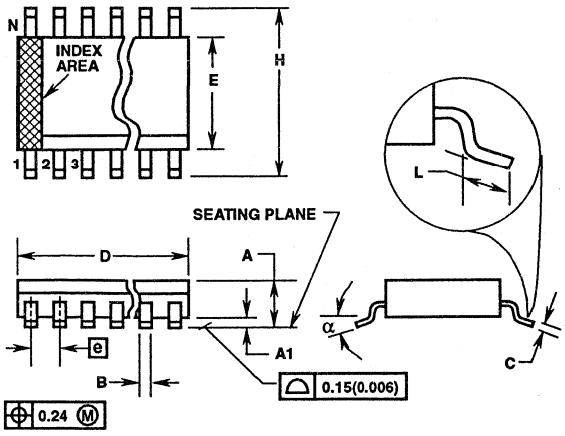
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Small Outline (SOIC) Plastic Packages (Continued)



M24.2

24 LEAD SMALL OUTLINE PLASTIC PACKAGE (200 MIL)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.067	0.088	1.70	2.25	
A1	0.002	0.011	0.05	0.30	
B	0.014	0.021	0.35	0.55	
C	0.006	0.011	0.15	0.30	
D	0.587	0.606	14.9	15.4	1
E	0.205	0.220	5.2	5.6	2
e	0.050 BSC		1.27 BSC		
H	0.296	0.326	7.5	8.3	
L	0.012	0.027	0.30	0.70	3
N	24		24		4
α	0°	10°	0°	10°	-

Rev. 0 12/93

NOTES:

1. Dimension "D" does not include mold flash, protrusions or gate burrs.
2. Dimension "E" does not include interlead flash or protrusions.
3. "L" is the length of terminal for soldering to a substrate.
4. "N" is the number of terminal positions.
5. Terminal numbers are shown for reference only.
6. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

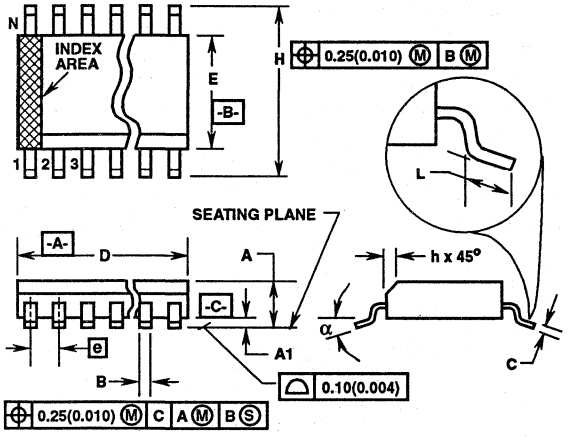
M28.3A

28 LEAD SMALL OUTLINE PLASTIC PACKAGE (300 MIL)

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.085	0.106	2.15	2.7	-
A1	0.002	0.011	0.05	0.30	-
B	0.014	0.021	0.35	0.55	-
C	0.004	0.009	0.10	0.25	-
D	0.737	0.755	18.7	19.2	1
E	0.296	0.311	7.50	7.90	2
e	0.05 BSC		1.27 BSC		-
H	0.390	0.421	9.90	10.70	-
L	0.012	0.027	0.30	0.70	3
N	28		28		4
α	0°	10°	0°	10°	-

Rev. 0 12/93

Small Outline (SOIC) Plastic Packages (Continued)



M28.3 (JEDEC MS-013-AE ISSUE C)
28 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

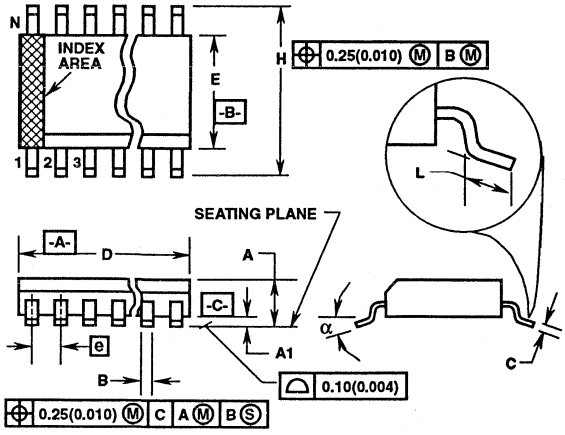
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.6969	0.7125	17.70	18.10	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.01	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Shrink Small Outline (SSOP) Plastic Packages



M28.209 (JEDEC MO-150-AH ISSUE A)
28 LEAD SHRINK SMALL OUTLINE PLASTIC PACKAGE

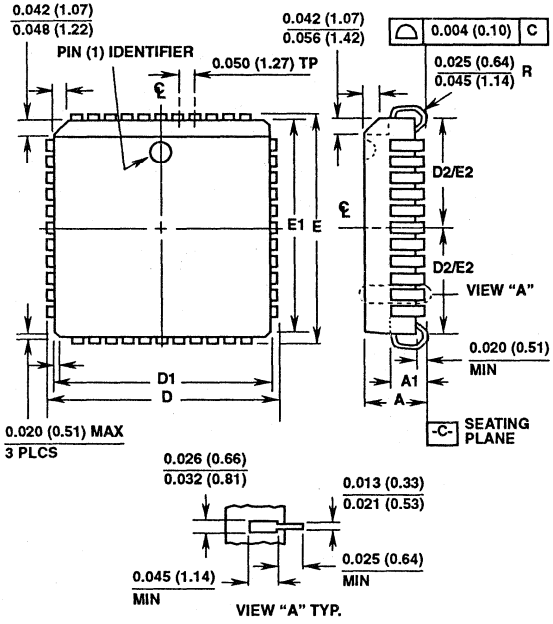
	INCHES		MILLIMETERS		
SYMBOL	MIN	MAX	MIN	MAX	NOTES
A	-	0.083	-	2.13	-
A1	0.002	0.009	0.05	0.25	-
B	0.009	0.014	0.22	0.38	9
C	0.004	0.007	0.09	0.20	-
D	0.390	0.413	9.90	10.50	3
E	0.197	0.220	5.00	5.60	4
e	0.026 BSC		0.65 BSC		-
H	0.292	0.322	7.40	8.20	-
L	0.025	0.040	0.63	1.03	6
N	28		28		7
α	0°	8°	0°	8°	-

Rev. 0 12/93

NOTES:

1. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.20mm (0.0078 inch) per side.
4. Dimension "E" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.20mm (0.0078 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width "B", as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.51mm (0.020 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

Plastic Leaded Chip Carrier (PLCC) Packages



NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

N20.35 (JEDEC MS-018 ISSUE A)
20 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.385	0.395	9.78	10.03	-
D1	0.350	0.356	8.89	9.04	3
D2	0.141	0.169	3.59	4.29	4, 5
E	0.385	0.395	9.78	10.03	-
E1	0.350	0.356	8.89	9.04	3
E2	0.141	0.169	3.59	4.29	4, 5
N	20		20		6

Rev. 0 12/93

N28.45 (JEDEC MS-018 ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

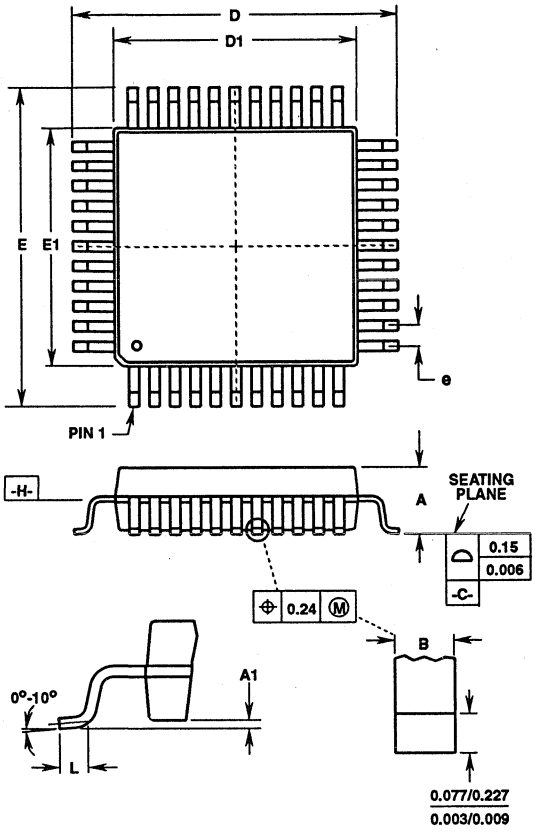
Rev. 0 12/93

N44.65 (JEDEC MS-018 ISSUE A)
44 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.685	0.695	17.40	17.65	-
D1	0.650	0.656	16.51	16.66	3
D2	0.291	0.319	7.40	8.10	4, 5
E	0.685	0.695	17.40	17.65	-
E1	0.650	0.656	16.51	16.66	3
E2	0.291	0.319	7.40	8.10	4, 5
N	44		44		6

Rev. 0 12/93

Metric Plastic Quad Flatpack Packages



Q32.A

32 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

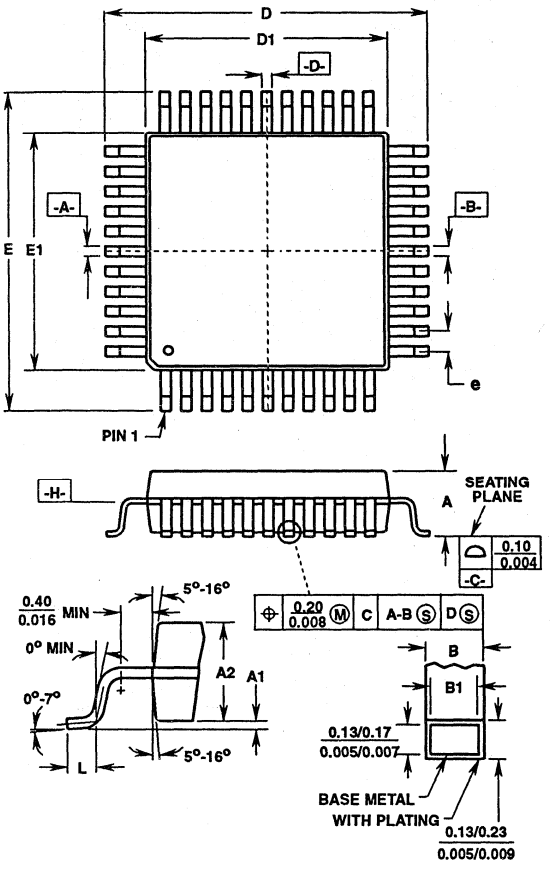
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.054	0.072	1.35	1.85	-
A1	0.000	0.011	0.00	0.30	-
B	0.008	0.017	0.20	0.45	5
D	0.347	0.362	8.80	9.20	2
D1	0.272	0.287	6.90	7.30	3, 4
E	0.347	0.362	8.80	9.20	2
E1	0.272	0.287	6.90	7.30	3, 4
L	0.012	0.027	0.30	0.70	-
N	32		32		6
e	0.032 BSC		0.80 BSC		-

Rev. 0 12/93

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensions D and E to be determined at seating plane -C-.
3. Dimensions D1 and E1 to be determined at datum plane -H-.
4. Dimensions D1 and E1 do not include mold protrusion.
5. Dimension B does not include dambar protrusion.
6. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (Continued)



Q44.A (JEDEC MO-108AA-2 ISSUE A)
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

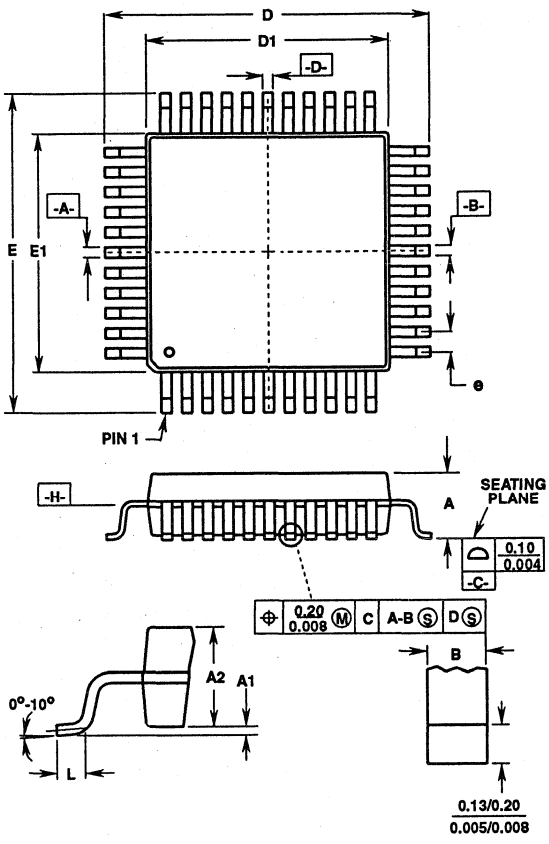
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.093	-	2.35	-
A1	0.000	0.010	0.00	0.25	-
A2	0.077	0.083	1.95	2.10	-
B	0.012	0.018	0.30	0.45	6
B1	0.012	0.016	0.30	0.40	-
D	0.510	0.530	12.95	13.45	3
D1	0.390	0.398	9.90	10.10	4, 5
E	0.510	0.530	12.95	13.45	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.026	0.037	0.65	0.95	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 0 12/93

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Metric Plastic Quad Flatpack Packages (Continued)



Q44.B

44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

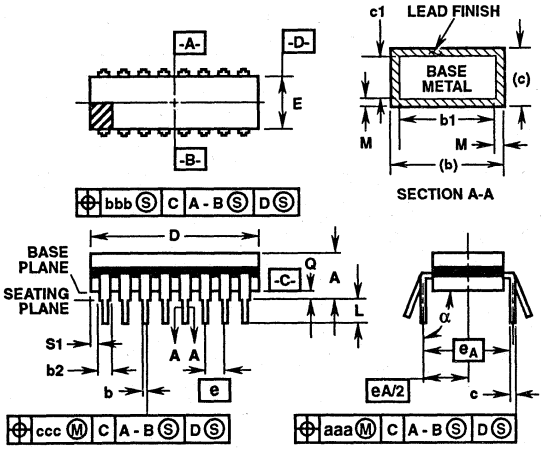
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.093	-	2.35	-
A1	0.000	0.004	0.00	0.10	-
A2	0.081	0.089	2.05	2.25	-
B	0.012	0.018	0.30	0.45	6
D	0.544	0.559	13.80	14.20	3
D1	0.390	0.398	9.90	10.10	4, 5
E	0.544	0.559	13.80	14.20	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.042	0.053	1.05	1.35	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 0 12/93

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension B does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. "N" is the number of terminal positions.

Dual-In-Line Frit-Seal Ceramic Packages



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: INCH

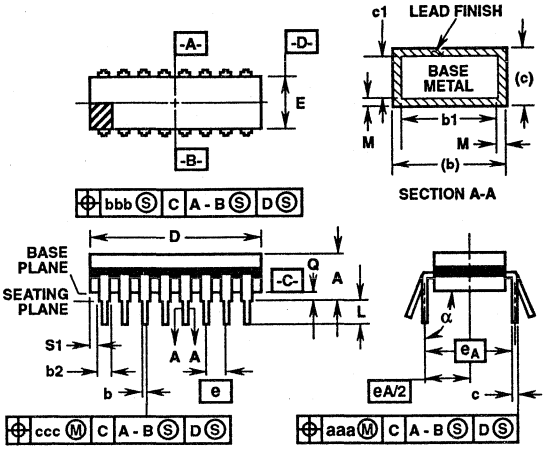
F14.3 MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)
14 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

Dual-In-Line Frit-Seal Ceramic Packages (Continued)



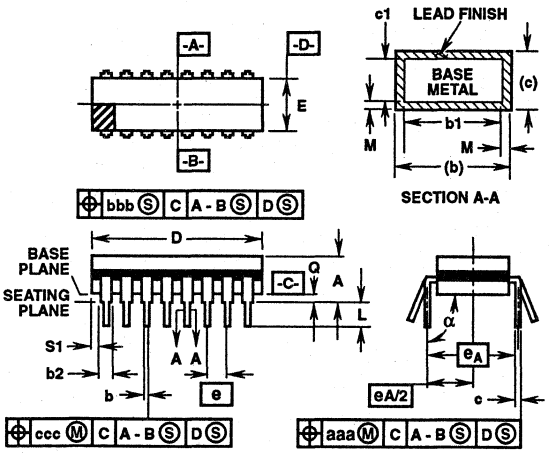
F18.3 MIL-STD-1835 GDIP1-T18 (D-6, CONFIGURATION A)
18 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.960	-	24.38	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	18		18		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: INCH

Dual-In-Line Frit-Seal Ceramic Packages (Continued)



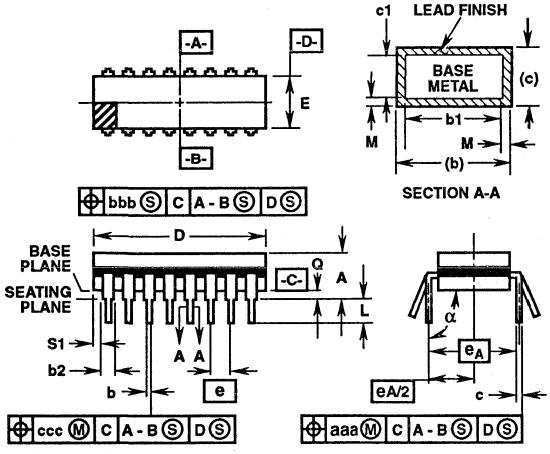
F20.3 MIL-STD-1835 GDIP1-T20 (D-8, CONFIGURATION A)
20 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.060	-	26.92	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	20		20		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: INCH

Dual-In-Line Frit-Seal Ceramic Packages (Continued)



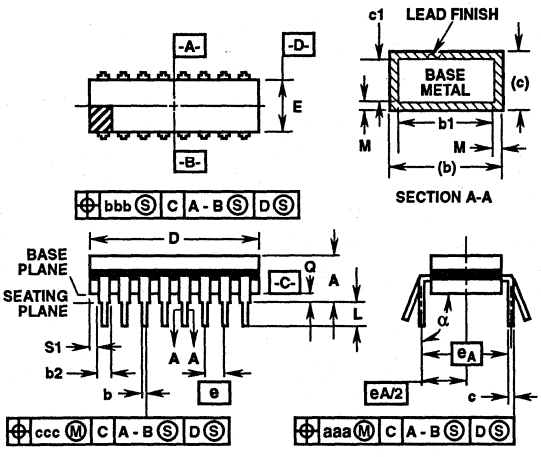
F24.3 MIL-STD-1835 GDIP3-T24 (D-9, CONFIGURATION A)
24 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.220	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.280	-	32.51	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	24		24		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: INCH

Dual-In-Line Frit-Seal Ceramic Packages (Continued)



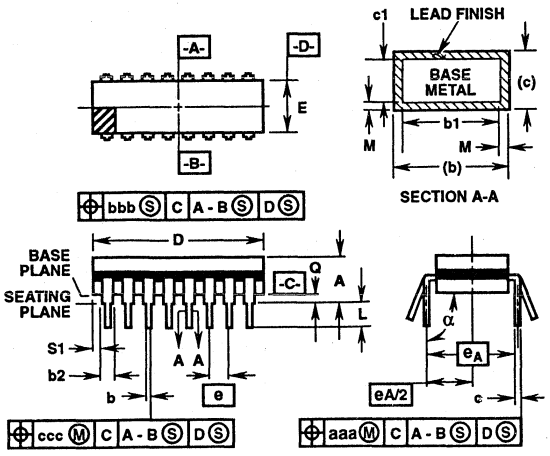
F24.6 MIL-STD-1835 GDIP1-T24 (D-3, CONFIGURATION A)
24 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.290	-	32.77	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.120	0.200	3.05	5.08	-
Q	0.015	0.075	0.38	1.91	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	24		24		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: INCH

Dual-In-Line Frit-Seal Ceramic Packages (Continued)



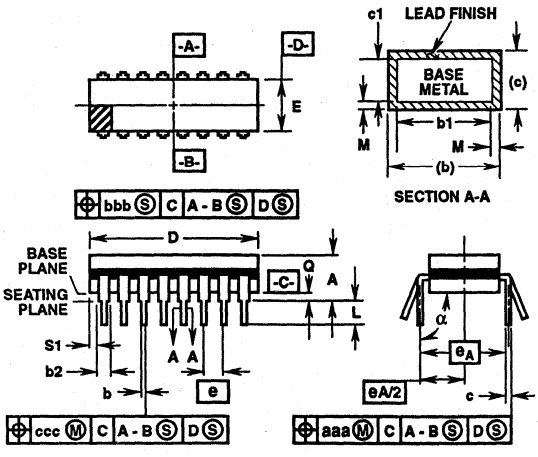
F28.6 MIL-STD-1835 GDIP1-T28 (D-10, CONFIGURATION A)
28 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	28		28		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: INCH

Dual-In-Line Frit-Seal Ceramic Packages (Continued)



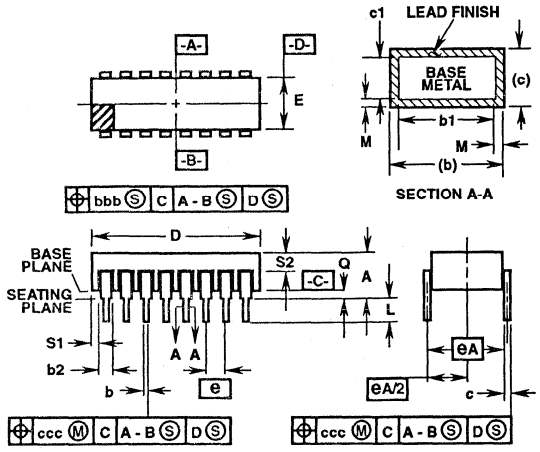
F40.6 MIL-STD-1835 GDIP1-T40 (D-5, CONFIGURATION A)
40 LEAD DUAL-IN-LINE FRIT-SEAL CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	5
E	0.510	0.620	12.95	15.75	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	-
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	40		40		8

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling Dimension: INCH

Metal Seal Dual-in-Line Ceramic Packages



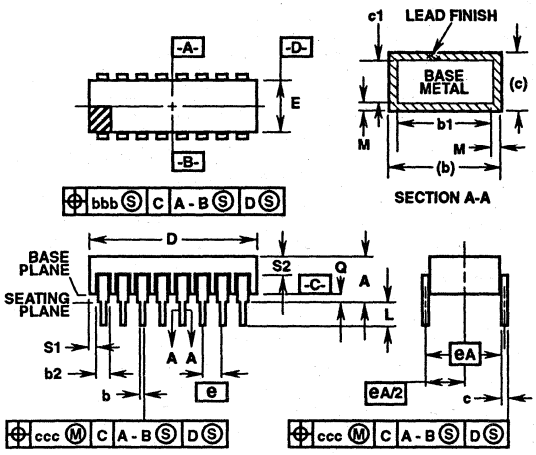
D28.6 MIL-STD-1835 CDIP2-T28 (D-10, CONFIGURATION C)
28 LEAD METAL SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.232	-	5.92	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	1.490	-	37.85	5
E	0.500	0.610	12.70	15.49	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	8
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	28		28		9

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
9. N is the maximum number of terminal positions.
10. Braze fillets shall be concave.
11. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
12. Controlling Dimension: INCH.

Metal Seal Dual-in-Line Ceramic Packages (Continued)



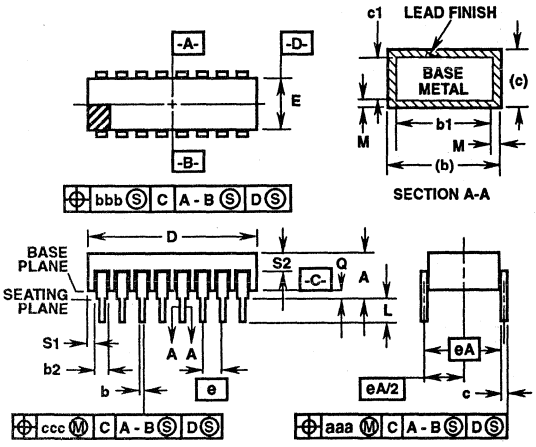
D40.6 MIL-STD-1835 CDIP2-T40 (D-5, CONFIGURATION C)
40 LEAD METAL SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.225	-	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	2.096	-	53.24	5
E	0.510	0.620	12.95	15.75	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.070	0.38	1.78	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	8
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	40		40		9

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
9. N is the maximum number of terminal positions.
10. Braze fillets shall be concave.
11. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
12. Controlling Dimension: INCH.

Metal Seal Dual-in-Line Ceramic Packages (Continued)



D42.6

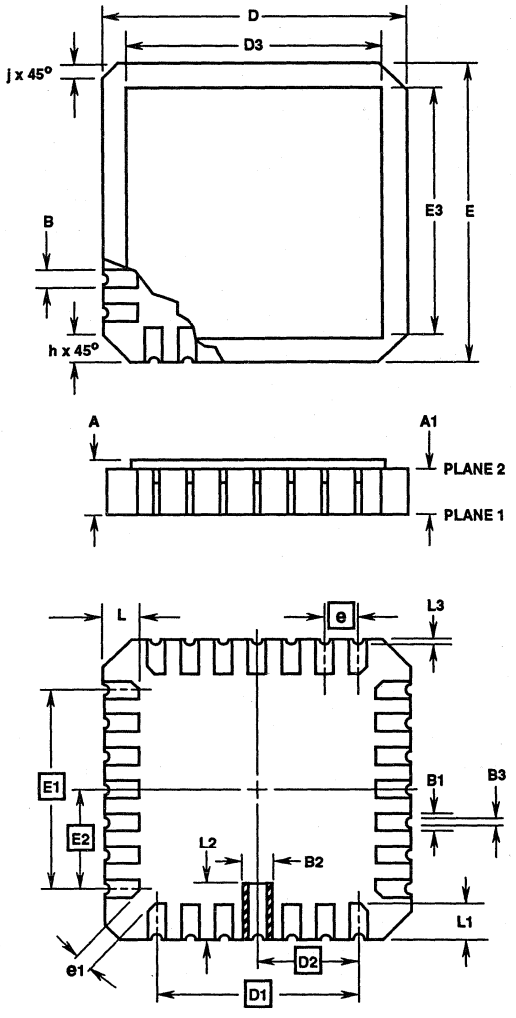
42 LEAD METAL SEAL DUAL-IN-LINE CERAMIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.142	0.225	3.60	5.72	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.022	0.36	0.56	3
b2	0.035	0.043	1.90	1.10	-
b3	-	-	-	-	4
c	0.009	0.015	0.23	0.38	2
c1	0.009	0.012	0.23	0.30	3
D	2.083	2.122	52.9	53.9	5
E	0.510	0.620	12.95	15.75	5
e	0.100 BSC		2.54 BSC		-
eA	0.600 BSC		15.24 BSC		-
eA/2	0.300 BSC		7.62 BSC		-
L	0.130	-	3.30	-	-
Q	0.039	-	1.00	-	6
S1	0.005	-	0.13	-	7
S2	0.005	-	0.13	-	8
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	42		42		9

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b1.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
9. N is the maximum number of terminal positions.
10. Braze fillets shall be concave.
11. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
12. Controlling dimension: INCH.

Metal Seal Leadless Ceramic Chip Carrier Packages



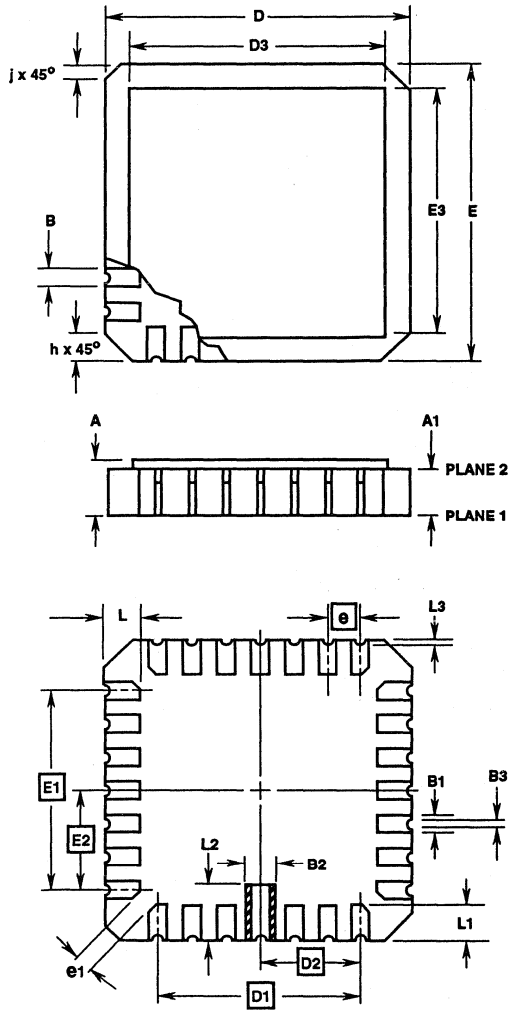
J20.A MIL-STD-1835 CQCC1-N20 (C-2)
20 PAD METAL SEAL LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	7
B	-	-	-	-	4
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	-	0.358	-	9.09	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	-	0.358	-	9.09	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.381mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals shall be ellectrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Maximum limits allows for 0.007 inch solder thickness on pads.

Metal Seal Leadless Ceramic Chip Carrier Packages (Continued)



J20.B

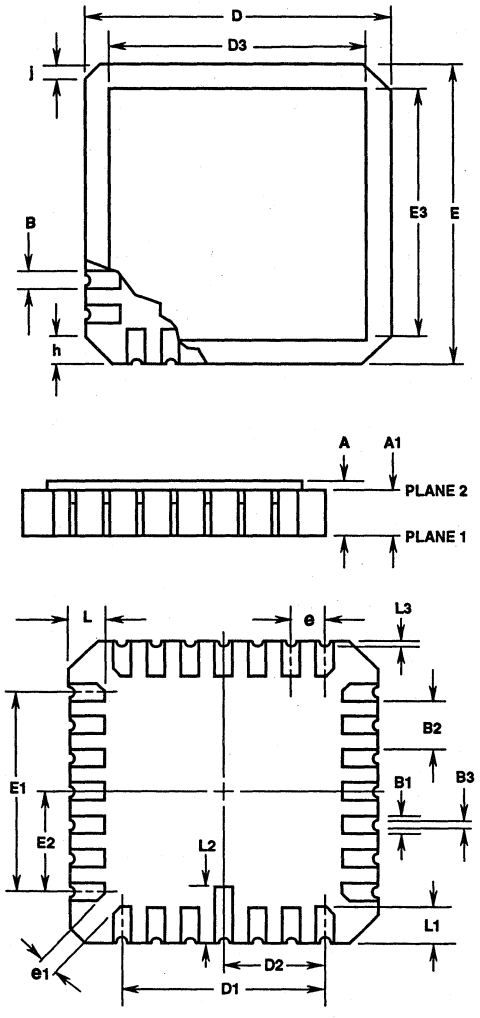
20 PAD METAL SEAL LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.070	0.097	1.78	2.46	6, 7
A1	0.054	0.077	1.37	1.96	7
B	-	-	-	-	-
B1	0.020	0.030	0.51	0.76	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.342	0.358	8.69	9.09	-
D1	0.200 BSC		5.08 BSC		-
D2	0.100 BSC		2.54 BSC		-
D3	0.325	0.335	8.26	8.51	2
E	0.342	0.358	8.69	9.09	-
E1	0.200 BSC		5.08 BSC		-
E2	0.100 BSC		2.54 BSC		-
E3	0.325	0.335	8.26	8.51	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.042	0.058	1.07	1.47	-
L1	0.042	0.058	1.07	1.47	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	5		5		3
NE	5		5		3
N	20		20		3

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.381mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals shall be electrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Maximum limits allows for 0.007 inch solder thickness on pads.

Metal Seal Leadless Ceramic Chip Carrier Packages (Continued)



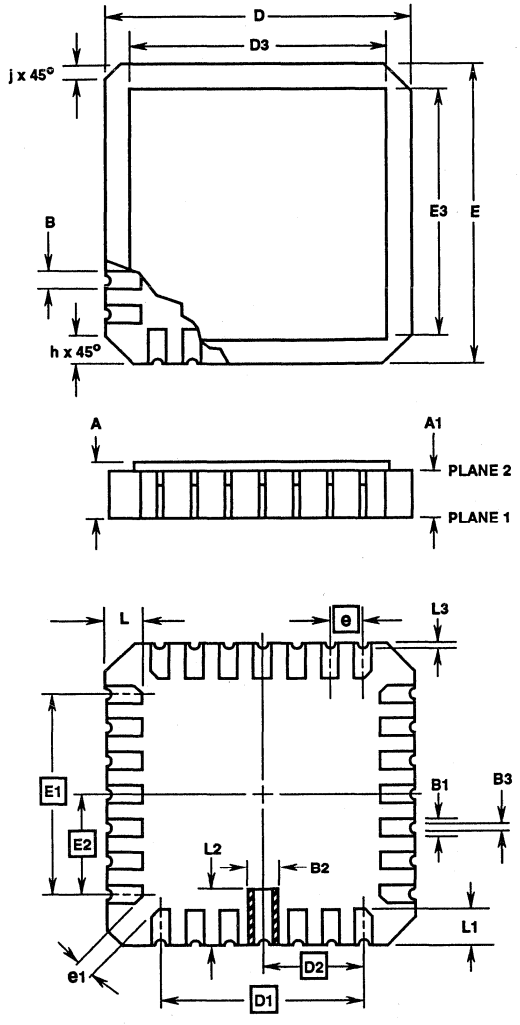
J28.A MIL-STD-1835 CQCC1-N28
28 PAD METAL SEAL LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.060	0.100	1.52	2.54	6, 7
A1	0.050	0.088	1.27	2.23	7
B	-	-	-	-	
B1	0.022	0.028	0.56	0.71	2, 4
B2	0.072 REF		1.83 REF		
B3	0.006	0.022	0.15	0.56	
D	0.442	0.460	11.23	11.68	
D1	0.300 BSC		7.62 BSC		
D2	0.150 BSC		3.81 BSC		
D3	-	0.460	-	11.68	2
E	0.442	0.460	11.23	11.68	
E1	0.300 BSC		7.62 BSC		
E2	0.150 BSC		3.81 BSC		
E3	-	0.460	-	11.68	2
e	0.050 BSC		1.27 BSC		
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	
L1	0.045	0.055	1.14	1.40	
L2	0.075	0.095	1.90	2.41	
L3	0.003	0.015	0.08	0.038	
ND	7		7		3
NE	7		7		3
N	28		28		3

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.381mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals shall be ellectrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Maximum limits allows for 0.007 inch solder thickness on pads.

Metal Seal Leadless Ceramic Chip Carrier Packages (Continued)



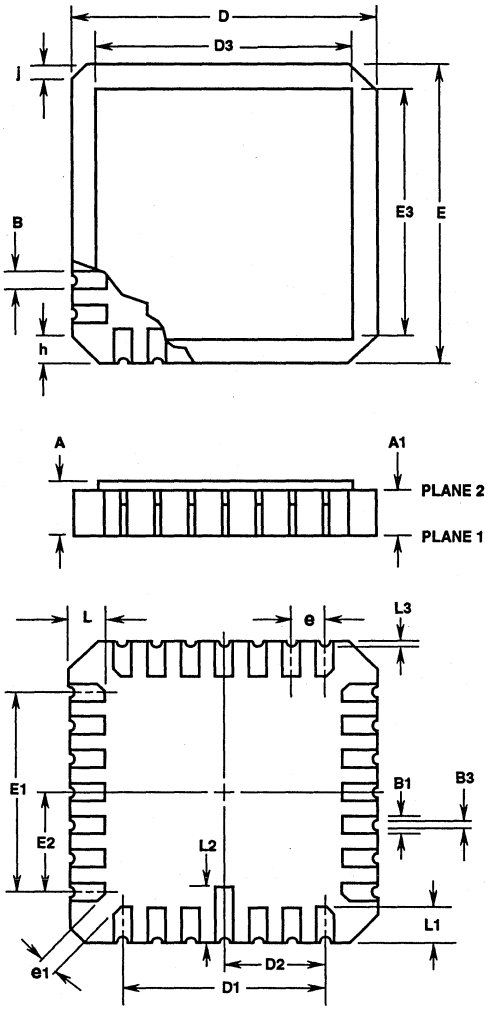
J44.A MIL-STD-1835 CQCC1-N44 (C-5)
44 PAD METAL SEAL LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.064	0.120	1.63	3.05	6, 7
A1	0.054	0.088	1.37	2.24	7
B	0.033	0.039	0.84	0.99	4
B1	0.022	0.028	0.561	0.71	2, 4
B2	0.072 REF		1.83 REF		-
B3	0.006	0.022	0.15	0.56	-
D	0.640	0.662	16.26	16.81	-
D1	0.500 BSC		12.70 BSC		-
D2	0.250 BSC		6.35 BSC		-
D3	-	0.662	-	16.81	2
E	0.640	0.662	16.26	16.81	-
E1	0.500 BSC		12.70 BSC		-
E2	0.250 BSC		6.35 BSC		-
E3	-	0.662	-	16.81	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.90	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	11		11		3
NE	11		11		3
N	44		44		3

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.381mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals shall be ellectrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Maximum limits allows for 0.007 inch solder thickness on pads.

Metal Seal Leadless Ceramic Chip Carrier Packages (Continued)



J44.B

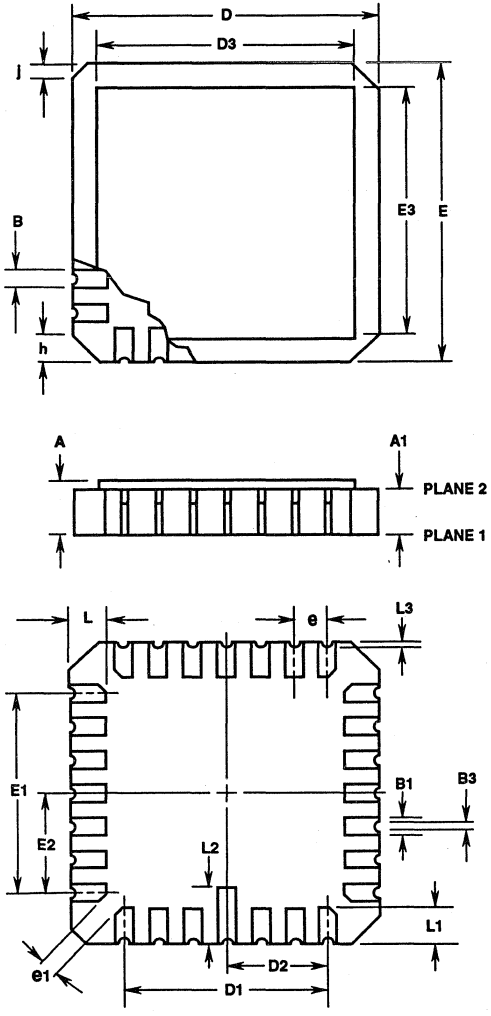
44 PAD METAL SEAL LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.067	0.087	1.70	2.20	6, 7
A1	0.058	0.072	1.47	1.83	7
B	-	-	-	-	-
B1	0.022	0.028	0.565	0.705	2, 4
B3	0.006	0.022	0.15	0.56	-
D	0.640	0.664	16.26	16.86	-
D1	0.500 BSC		12.70 BSC		-
D2	0.250 BSC		6.35 BSC		-
D3	0.484	0.50	12.30	12.70	2
E	0.640	0.664	16.26	16.86	-
E1	0.500 BSC		12.70 BSC		-
E2	0.250 BSC		6.35 BSC		-
E3	0.484	0.500	12.3	12.7	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
h	0.040 REF		1.02 REF		5
j	0.020 REF		0.51 REF		5
L	0.045	0.055	0.614	1.4	-
L1	0.045	0.055	0.614	1.4	-
L2	0.065	0.105	1.66	2.66	-
L3	0.003	0.015	0.08	0.38	-
ND	11		11		3
NE	11		11		3
N	44		44		3

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.381mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals shall be ellectrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Maximum limits allows for 0.007 inch solder thickness on pads.

Metal Seal Leadless Ceramic Chip Carrier Packages (Continued)



J68.A

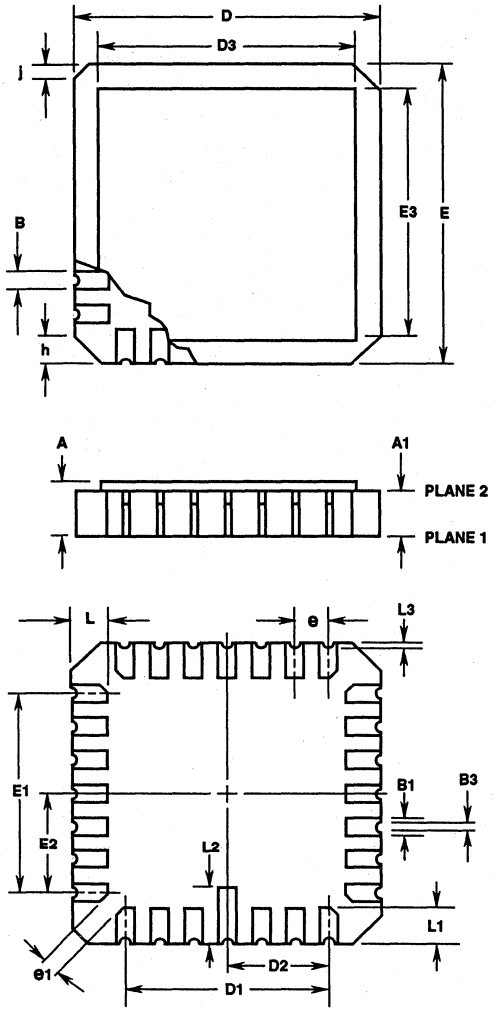
68 PAD METAL SEAL LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.067	0.087	1.70	2.20	6, 7
A1	0.058	0.072	1.47	1.83	7
B	-	-	-	-	-
B1	0.033	0.039	0.85	0.99	2, 4
B3	0.006	0.022	0.15	0.56	-
D	0.940	0.965	23.88	24.51	-
D1	0.800 BSC		20.32 BSC		-
D2	0.400 BSC		10.16 BSC		-
D3	0.616	0.632	15.65	16.05	2
E	0.940	0.965	23.88	24.51	-
E1	0.800 BSC		20.32 BSC		-
E2	0.400 BSC		10.16 BSC		-
E3	0.616	0.632	15.65	16.05	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
j	0.040 Ref		1.00 Ref		5
L	0.045	0.055	1.14	1.40	-
L1	0.045	0.055	1.14	1.40	-
L2	0.075	0.095	1.91	2.41	-
L3	0.003	0.015	0.08	0.38	-
ND	17		17		3
NE	17		17		3
N	68		68		3

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.381mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals shall be ellectrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Maximum limits allows for 0.007 inch solder thickness on pads.

Metal Seal Leadless Ceramic Chip Carrier Packages (Continued)



J68.B

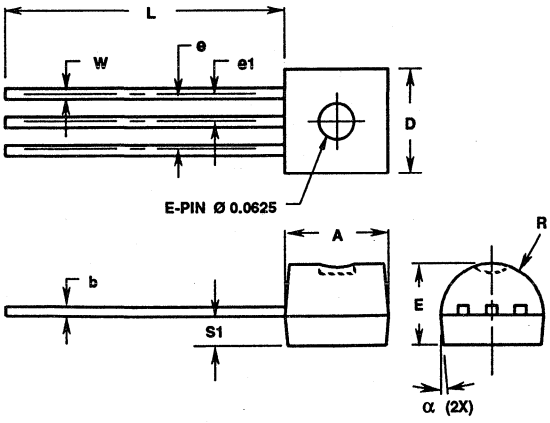
68 PAD METAL SEAL LEADLESS CERAMIC CHIP CARRIER

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.092	0.118	2.34	3.00	6, 7
A1	0.067	0.083	1.71	2.11	7
B	0.033	0.039	0.85	0.99	-
B1	0.033	0.039	0.085	0.99	2, 4
B3	0.006	0.022	0.15	0.56	-
D	0.940	0.960	23.88	24.38	-
D1	0.800 BSC		20.32 BSC		-
D2	0.400 BSC		10.16 BSC		-
D3	0.695	0.705	17.65	17.91	2
E	0.940	0.960	23.88	24.38	-
E1	0.800 BSC		20.32 BSC		-
E2	0.400 BSC		10.16 BSC		-
E3	0.695	0.705	17.65	17.91	2
e	0.050 BSC		1.27 BSC		-
e1	0.015	-	0.38	-	2
j	0.020 Ref		0.51 Ref		5
L	0.042	0.058	1.07	1.47	-
L1	0.042	0.058	1.07	1.47	-
L2	0.080	0.090	2.03	2.29	-
L3	0.003	0.015	0.08	0.38	-
ND	17		17		3
NE	17		17		3
N	68		68		3

NOTES:

1. Metallized castellations shall be connected to plane 1 terminals and extend toward plane 2 across at least two layers of ceramic or completely across all of the ceramic layers to make electrical connection with the optional plane 2 terminals.
2. Unless otherwise specified, a minimum clearance of 0.015 inch (0.381mm) shall be maintained between all metallized features (e.g., lid, castellations, terminals, thermal pads, etc.)
3. Symbol "N" is the maximum number of terminals. Symbols "ND" and "NE" are the number of terminals along the sides of length "D" and "E", respectively.
4. The required plane 1 terminals and optional plane 2 terminals shall be ellectrically connected.
5. The corner shape (square, notch, radius, etc.) may vary at the manufacturer's option, from that shown on the drawing.
6. Chip carriers shall be constructed of a minimum of two ceramic layers.
7. Maximum limits allows for 0.007 inch solder thickness on pads.

Single-In-Line Plastic Packages (SIP)



Z3.05

3 LEAD PLASTIC SINGLE-IN-LINE PACKAGE

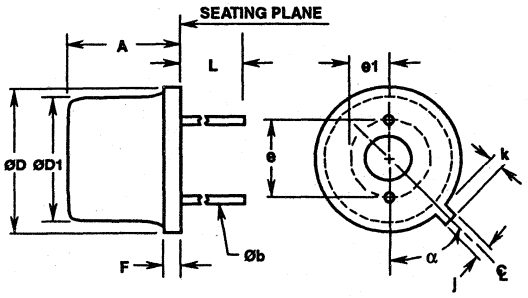
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.170	0.195	4.32	4.95
b	0.014	0.020	0.36	0.51
E	0.130	0.155	3.30	3.94
e	0.095	0.105	2.41	2.67
e1	0.045	0.055	1.14	1.40
L	0.500	0.610	12.70	15.49
R	0.085	0.095	2.16	2.41
S1	0.045	0.060	1.14	1.52
W	0.016	0.022	0.41	0.56
D	0.175	0.195	4.45	4.95
α	4°	6°	4°	6°

Rev. 0 12/93

NOTES:

1. Package outline exclusive of any mold flashes dimension.
2. Package outline exclusive of Burr dimension.

Metal Can Packages

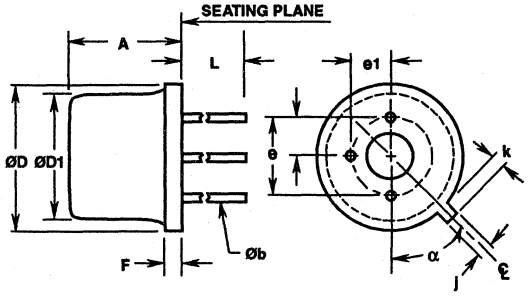


NOTES:

1. Measured from maximum diameter of the actual device.
2. Measured from tab centerline.
3. N is number of leads.

T2.A
2 LEAD METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.130	0.150	3.30	3.81	-
b	0.016	0.019	0.41	0.48	-
D	0.205	0.22	5.21	5.59	-
D1	0.180	0.190	4.57	4.83	-
F	0.010	0.025	0.25	0.64	-
k	0.033	0.046	0.84	1.17	1
j	0.033	0.045	0.84	1.14	-
L	0.500	0.560	12.70	14.22	-
e	0.100 BSC		2.54 BSC		-
e1	-		-		-
α	45		45		2
N	2		2		3



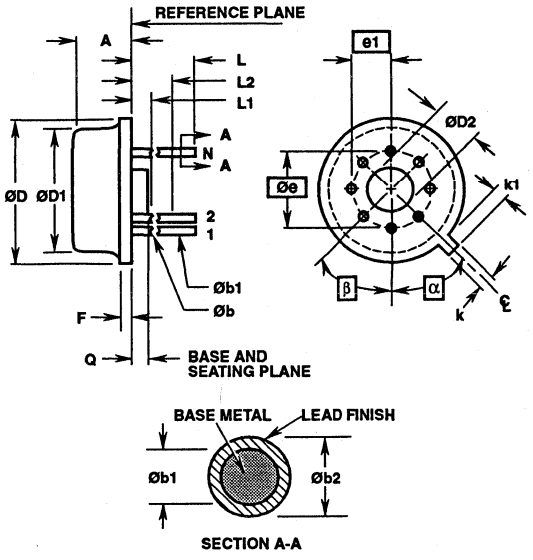
NOTES:

1. Measured from maximum diameter of the actual device.
2. Measured from tab centerline.
3. N is number of leads

T3.A
3 LEAD METAL CAN PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.130	0.150	3.30	3.81	-
b	0.016	0.019	0.41	0.48	-
D	0.205	0.220	5.21	5.59	-
D1	0.180	0.190	4.57	4.83	-
F	0.010	0.025	0.25	0.64	-
k	0.033	0.048	0.84	1.22	1
j	0.036	0.046	0.91	1.17	-
L	0.500	0.560	12.70	14.22	-
e	0.100 BSC		2.54 BSC		-
e1	0.050 BSC		1.27 BSC		-
α	45		45		2
N	3		3		3

Metal Can Packages (Continued)



T10.B MIL-STD-1835 MACY1-X10 (A2)
10 LEAD TO-100 METAL CAN

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.185	4.19	4.70	-
Øb	0.016	0.019	0.41	0.48	1
Øb1	0.016	0.021	0.41	0.53	1
Øb2	0.016	0.024	0.41	0.61	-
ØD	0.335	0.375	8.51	9.52	-
ØD1	0.305	0.335	7.75	8.51	-
ØD2	0.110	0.160	2.79	4.06	-
e	0.230 BSC		5.84 BSC		-
e1	0.115 BSC		2.92 BSC		-
F	-	0.040	-	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.750	12.70	19.05	1
L1	-	0.050	-	1.27	1
L2	0.250	-	6.35	-	1
Q	0.010	0.045	0.25	1.14	-
α	36° BSC		36° BSC		3
β	36° BSC		36° BSC		3
N	10		10		4

NOTES:

1. (All leads) Øb applies between L1 and L2. Øb1 applies between L2 and 0.500 from the reference plane. Diameter is uncontrolled in L1 and beyond 0.500 from the reference plane.
2. Measured from maximum diameter of the product.
3. α is the basic spacing from the centerline of the tab to terminal 1 and β is the basic spacing of each lead or lead position (N -1 places) from α, looking at the bottom of the package.
4. N is the maximum number of terminal positions.
5. Dimensioning and tolerancing per ANSI 414.5M - 1982.
6. Controlling dimension: INCH.

DATA ACQUISITION 18

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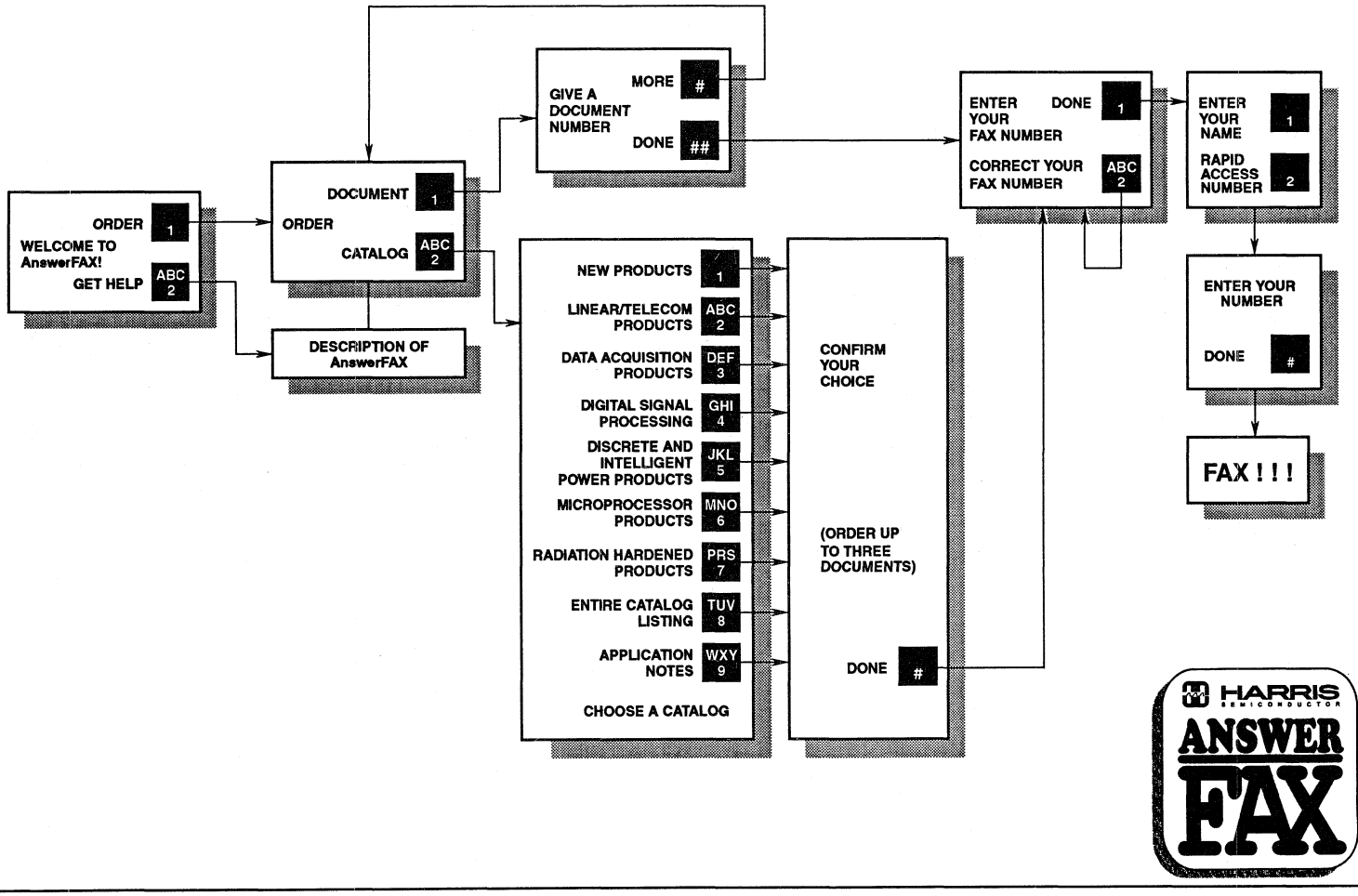

Harris AnswerFAX Data Book Request Form

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PUBLICATION NUMBER	DATA BOOK/DESCRIPTION
PSG201S	**PRODUCT SELECTION GUIDE** (1992: 320pp) Key product information on all Harris Semiconductor devices. Sectioned (Analog, Data Acquisition, Digital, Application Specific, Power, Hi-Rel & Rad-Hard, ASIC) for easy use and includes cross references and alphanumeric part number index.
DB500B	**LINEAR & TELECOM ICs** (1993: 1,312pp) Product specifications for: op amps, comparators, S/H amps, differential amps, arrays, special analog circuits, telecom ICs, and power processing circuits.
DB301.1	**DATA ACQUISITION** (1991: 1,104pp) Product specifications on A/D converters (display, integrating, successive approximation, flash); D/A converters, switches, multiplexers, and other products. NOTE: New and completely updated data acquisition databook available January '94.
DB306	**DATA ACQUISITION/NEW RELEASES** (1992: 144pp) Includes specifications on 22 products not contained in main book, plus an applications note. NOTE: New and completely updated data acquisition databook available January '94.
DB302A	**DIGITAL SIGNAL PROCESSING** (1993: 380pp) This new edition includes specifications on one- and two-dimensional filters, signal synthesizers, multipliers, special function devices (such as address sequencers, binary correlators, histogrammer). Includes sections on development tools, application notes and Quality/Reliability.
DB304	**INTELLIGENT POWER ICs** (1992: 512pp) Product specifications for low- and high-side switches, half bridges, AC-DC converters, full bridges, regulators & power supplies, protection circuits, and special function ICs. Includes application notes and Quality/Reliability sections.
DB450C	**TRANSIENT VOLTAGE SUPPRESSION DEVICES** (1994: 400pp) Product specifications of Harris varistors and surgectors. Also, general informational chapters such as: "Voltage Transients - An Overview," "Transient Suppression - Devices and Principles," "Suppression - Automotive Transients."
DB223.2	**POWER MOSFETs** (1992: 1,504pp) Product specifications on MOSFETs (N- and P-channel, logic level, military and radiation-hardened); IGBTs; Intelligent discretes; power drivers and switches; and ultra-fast rectifiers. Includes industry replacement guide and application notes.
DB220.1	**BIPOLAR POWER TRANSISTORS** (1992: 592pp) Technical information on over 750 power transistors for use in a wide range of consumer, industrial and military applications. Indexing and packaging included.
DB303	**MICROPROCESSOR PRODUCTS** (1992: 1,156pp) For commercial and military applications. Product specifications on CMOS microprocessors, peripherals, data communications, and memory ICs. Includes application notes and Quality/Reliability chapters.
Analog Military	**ANALOG MILITARY** (1989: 1,264pp) This databook describes Harris' military line of Linear, Data Acquisition, and Telecommunications circuits.
Digital Military	**DIGITAL MILITARY** (1989: 680pp) Harris CMOS digital ICs -- microprocessors, peripherals, data communications and memory -- are included in this databook.

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AnswerFAX Technical Support Application Note Listing

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9002	AN002	Principles of Data Acquisition and Conversion (20 pages)
9004	AN004	The IH5009 Analog Switch Series (9 pages)
9007	AN007	Using the 8048/8049 Log/Antilog Amplifier (6 pages)
9009	AN009	Pick Sample-Holds by Accuracy and Speed and Keep Hold Capacitors in Mind (7 pages)
9012	AN012	Switching Signals with Semiconductors (4 pages)
9013	AN013	Everything You Always Wanted to Know About the ICL8038 (4 pages)
9016	AN016	Selecting A/D Converters (7 pages)
9017	AN017	The Integrating A/D Converter (5 pages)
9018	AN018	Do's and Don'ts of Applying A/D Converters (4 pages)
9020	AN020	A Cookbook Approach to High Speed Data Acquisition and Microprocessor Interfacing (23 pages)
9023	AN023	Low Cost Digital Panel Meter Designs (5 pages)
9027	AN027	Power Supply Design Using the ICL8211 and 8212 (8 pages)
9028	AN028	Build an Auto-Ranging DMM with the ICL7103A/8052A A/D Converter Pair (6 pages)
9030	AN030	ICL7104: A Binary Output A/D Converter for Microprocessors (16 pages)
9032	AN032	Understanding the Auto-Zero and Common Mode Performance of the ICL7106/7107/7109 Family (8 pages)
9040	AN040	Using the ICL8013 Four Quadrant Analog Multiplier (6 pages)
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9054	AN054	Display Driver Family Combines Convenience of Use with Microprocessor Interfaceability (18 pages)
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9115	AN115	Digital Filter (DF) Family Overview (6 pages)
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9517	AN517	Applications of Monolithic Sample and Hold Amplifier (5 pages)
9519	AN519	Operational Amplifier Noise Prediction (4 pages)

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99206	AN9206	Correlating on Extended Data Lengths (2 pages)
99207	AN9207	DSP Temperature Considerations (2 pages)
99208	AN9208	High Frequency Power Converters (10 pages)

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99210	AN9210	A New PSpice Subcircuit for the Power MOSFET Featuring Global Temperature Options (12 pages)
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99328	AN9328	Using the HI1166 Evaluation Board (9 pages)
99329	AN9329	Using the HI1176/HI1171 Evaluation Board (5 pages)
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660001	MM0001	HFA-0001 Spice Operational Amplifier Macro-Model (4 pages)
660002	MM0002	HFA-0002 Spice Operational Amplifier Macro-Model (4 pages)
660005	MM0005	HFA-0005 Spice Operational Amplifier Marco-Model (4 pages)
662500	MM2500	HA2500/02 Spice Operational Amplifier Macro-Model (5 pages)
662510	MM2510	HA-2510/12 Spice Operational Amplifier Macro-Model (4 pages)
662520	MM2520	HA-2520/22 Spice Operational Amplifier Macro-Model (4 pages)
662539	MM2539	HA-2539 Spice Operational Amplifier Macro-Model (4 pages)
662540	MM2540	HA-2540 Spice Operational Amplifier Macro-Model (4 pages)

AnswerFAX Technical Support Application Note Listing

AnswerFAX DOCUMENT NUMBER	PART NUMBER	DESCRIPTION
662541	MM2541	HA-2541 Spice Operational Amplifier Macro-Model (5 pages)
662542	MM2542	HA-2542 Spice Operational Amplifier Macro-Model (5 pages)
662544	MM2544	HA-2544 Spice Operational Amplifier Macro-Model (5 pages)
662548	MM2548	HA-2548 Spice Operational Amplifier Macro-Model (5 pages)
662600	MM2600	HA-2600/02 Spice Operational Amplifier Macro-Model (5 pages)
662620	MM2620	HA-2620/22 Spice Operational Amplifier Macro-Model (5 pages)
662839	MM2839	HA-2839 Spice Operational Amplifier Macro-Model (4 pages)
662840	MM2840	HA-2840 Spice Operational Amplifier Macro-Model (4 pages)
662841	MM2841	HA-2841 Spice Operational Amplifier Macro-Model (4 pages)
662842	MM2842	HA-2842 Spice Operational Amplifier Macro-Model (4 pages)
662850	MM2850	HA-2850 Spice Operational Amplifier Macro-Model (4 pages)
665002	MM5002	HA-5002 Spice Buffer Amplifier Macro-Model (4 pages)
665004	MM5004	HA-5004 Spice Current Feedback Amplifier Macro-Model (4 pages)

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665020	MM5020	HA-5020 Spice Current Feedback Operational Amplifier Macro-Model (4 pages)
665033	MM5033	HA-5033 Spice Buffer Amplifier Macro-Model (4 pages)
665101	MM5101	HA-5101 Spice Operational Amplifier Macro-Model (5 pages)
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665112	MM5112	HA-5112 Spice Operational Amplifier Macro-Model (5 pages)
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665147	MM5147	HA-5147 Spice Operational Amplifier Macro-Model (4 pages)
665190	MM5190	HA-5190 Spice Operational Amplifier Macro-Model (4 pages)
665221	MM5221	HA-5221/22 Spice Operational Amplifier Macro-Model (4 pages)
797338	MM PWRDEV	Harris Power MOSFET and MCT Spice Model Library (16 pages)

DATA ACQUISITION 19

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Digital
- CMOS Microprocessors and Peripherals
- CMOS Microcontrollers
- CMOS Logic

Rad-Hard Products
- Microprocessors and Peripherals
- Memories
- Analog ICs
- Digital ICs
- Discrete Power
  - Bipolar
  - MOSFET
- ASICs
- ESA SCC 9000 and Class S Screening

Military/Aerospace Programs
- Strategic and Space Programs
- Military ASIC Programs

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